SLG7RN45708

GreenPAK ™

Level Shifter

General Description

Renesas SLG7RN45708 is a low power and small form device. The SoC is housed in a 1.6mm x 1.6mm STQFN package which is optimal for using with small devices.

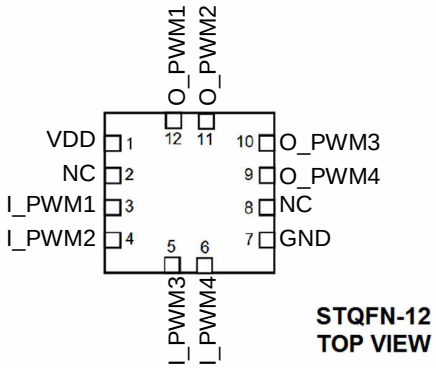
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 12 Package

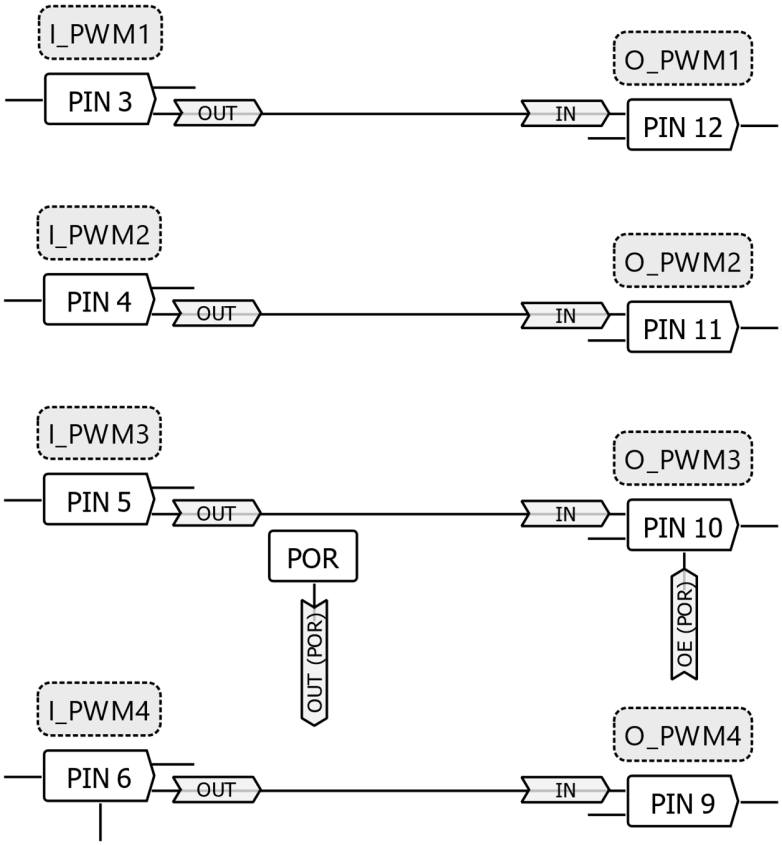
Output Summary

4 Outputs - Push Pull 2X

Pin Configuration



Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	I_PWM1	Digital Input	Low Voltage Digital Input	floating
4	I_PWM2	Digital Input	Low Voltage Digital Input	floating
5	I_PWM3	Digital Input	Low Voltage Digital Input	floating
6	I_PWM4	Digital Input	Low Voltage Digital Input	floating
7	GND	GND	Ground	--
8	NC	--	Keep Floating or Connect to GND	--
9	O_PWM4	Digital Output	Push Pull 2X	floating
10	O_PWM3	Digital Output	Push Pull 2X	floating
11	O_PWM2	Digital Output	Push Pull 2X	floating
12	O_PWM1	Digital Output	Push Pull 2X	floating

Ordering Information

Part Number	Package Type
SLG7RN45708V	V=STQFN-12
SLG7RN45708VTR	STQFN-12 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	Push-Pull 2x	--	17	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1000	--	V
Moisture Sensitivity Level		1		

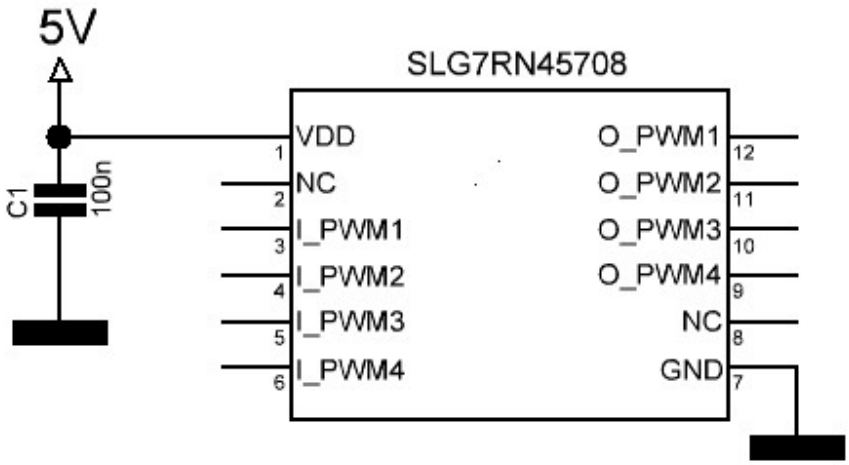
Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	5	5.5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	PINs3,4,5,6 are LOW	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 110°C	--	--	44	mA
V_{IH}	HIGH-Level Input Voltage	Low-Level Logic Input at VDD=1.8V	0.980	--	VDD	V
		Low-Level Logic Input at VDD=3.3V	1.130	--	VDD	V
		Low-Level Logic Input at VDD=5.0V	1.230	--	VDD	V
V_{IL}	LOW-Level Input Voltage	Low-Level Logic Input at VDD=1.8V	0	--	0.520	V
		Low-Level Logic Input at VDD=3.3V	0	--	0.690	V
		Low-Level Logic Input at VDD=5.0V	0	--	0.780	V

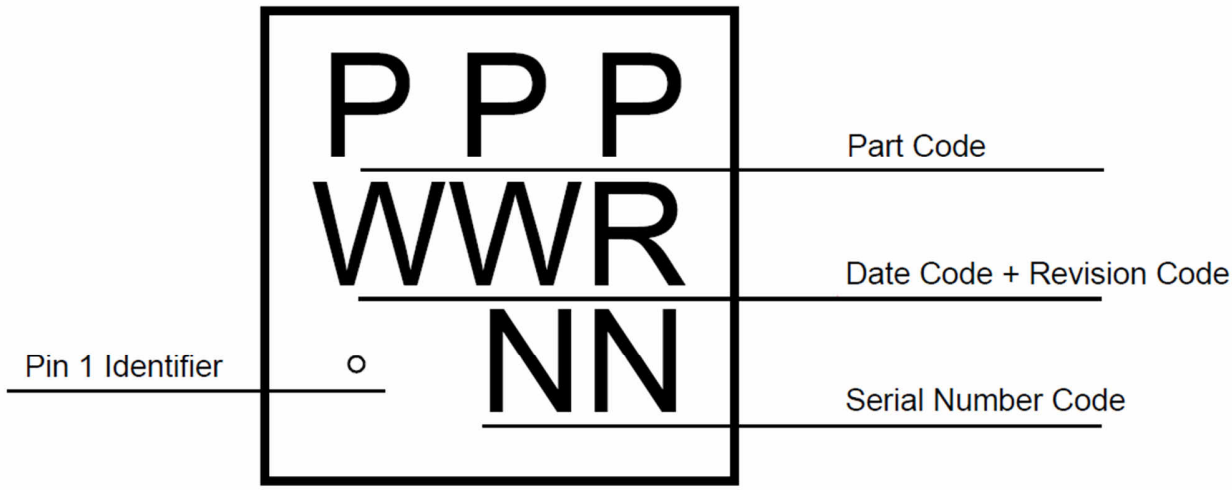
V_{OH}	HIGH-Level Output Voltage	Push-Pull 2X, Open Drain PMOS 2X, I_{OH}=100µA, at VDD=1.8V	1.700	1.800	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH}=3mA, at VDD=3.3V	2.850	3.190	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH}=5mA, at VDD=5.0V	4.320	4.860	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 2X, I_{OL}=100µA, at VDD=1.8V	--	0.010	0.020	V
		Push-Pull 2X, I_{OL}=3mA, at VDD=3.3V	--	0.090	0.130	V
		Push-Pull 2X, I_{OL}=5mA, at VDD=5.0V	--	0.120	0.160	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 2X, Open Drain PMOS 2X, V_{OH}=VDD-0.2V, at VDD=1.8V	2.100	2.680	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH}=2.4V, at VDD=3.3V	11.460	19.610	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH}=2.4V, at VDD=5.0V	41.886	55.990	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 2X, V_{OL}=0.15V, at VDD=1.8V	1.520	2.660	--	mA
		Push-Pull 2X, V_{OL}=0.4V, at VDD=3.3V	8.130	12.360	--	mA
		Push-Pull 2X, V_{OL}=0.4V, at VDD=5.0V	11.590	19.460	--	mA
T_{SU}	Startup Time	From VDD rising past 1.35 V	--	0.31	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10, 11 and 12 to another.
3. Guaranteed by Design.

Typical Application Circuit



Package Top Marking

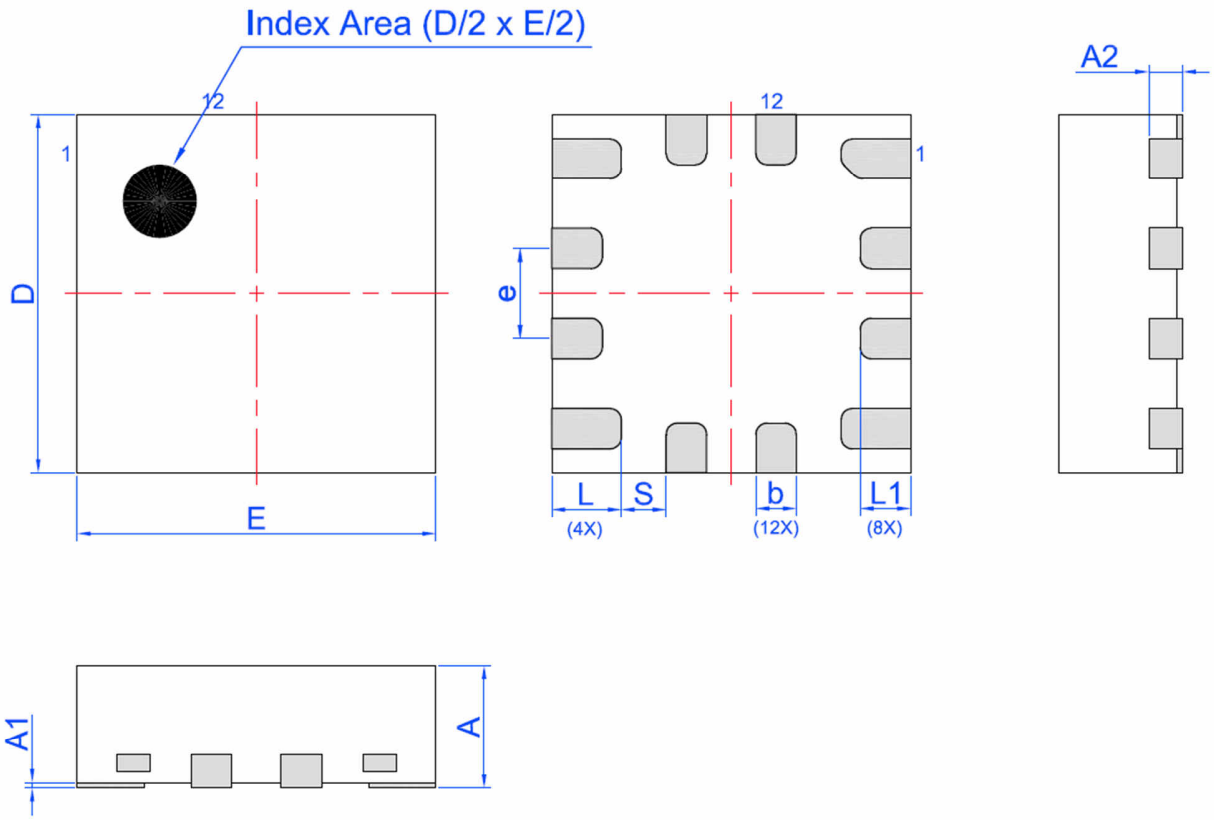


Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.10	001	L	0x67022BC5			04/14/2022

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

12 Lead STQFN FCA Package 1.6 x 1.6 mm



Unit: mm

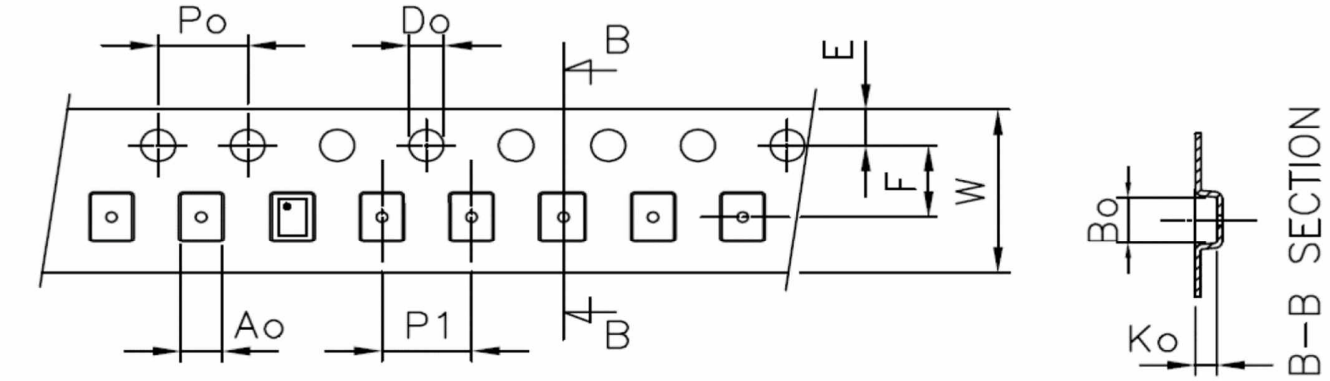
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 12L FCA 0.4P Green	12	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

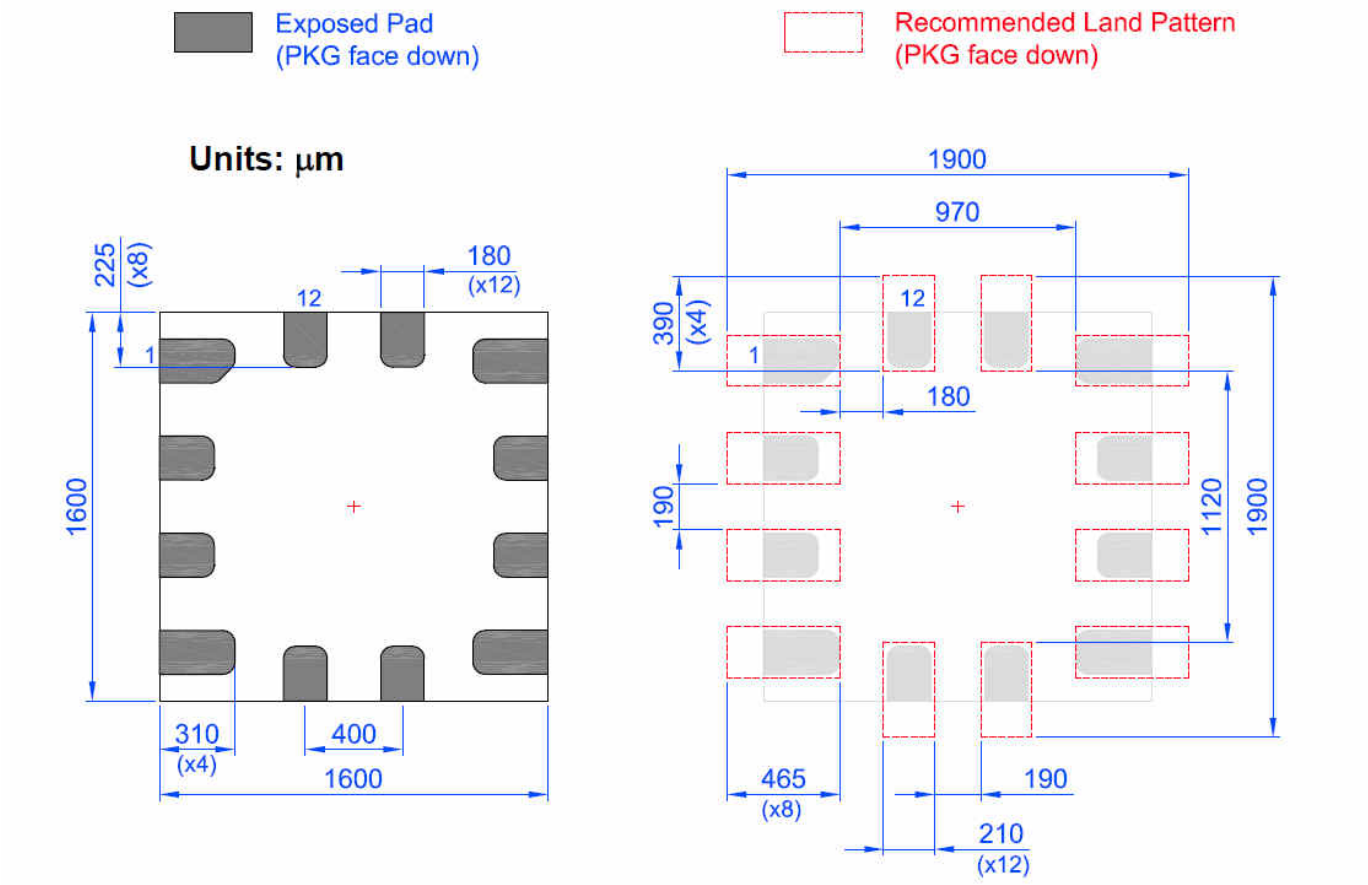
Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L FCA 0.4P Green	1.80±0.05	1.80±0.05	±0.7	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.408 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern



Datasheet Revision History

Date	Version	Change
04/14/2022	0.10	New design for SLG46120 chip

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.