General Description

Renesas SLG7RN46352 is a low power and small form device. The SoC is housed in a 3mm x 3mm STQFN package which is optimal for using with small devices.

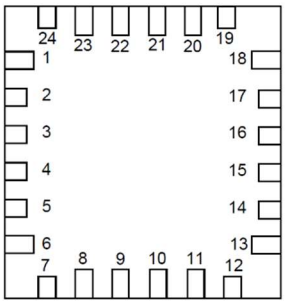
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 24 Package

Output Summary

1 Output - Push Pull 1X

Pin Configuration

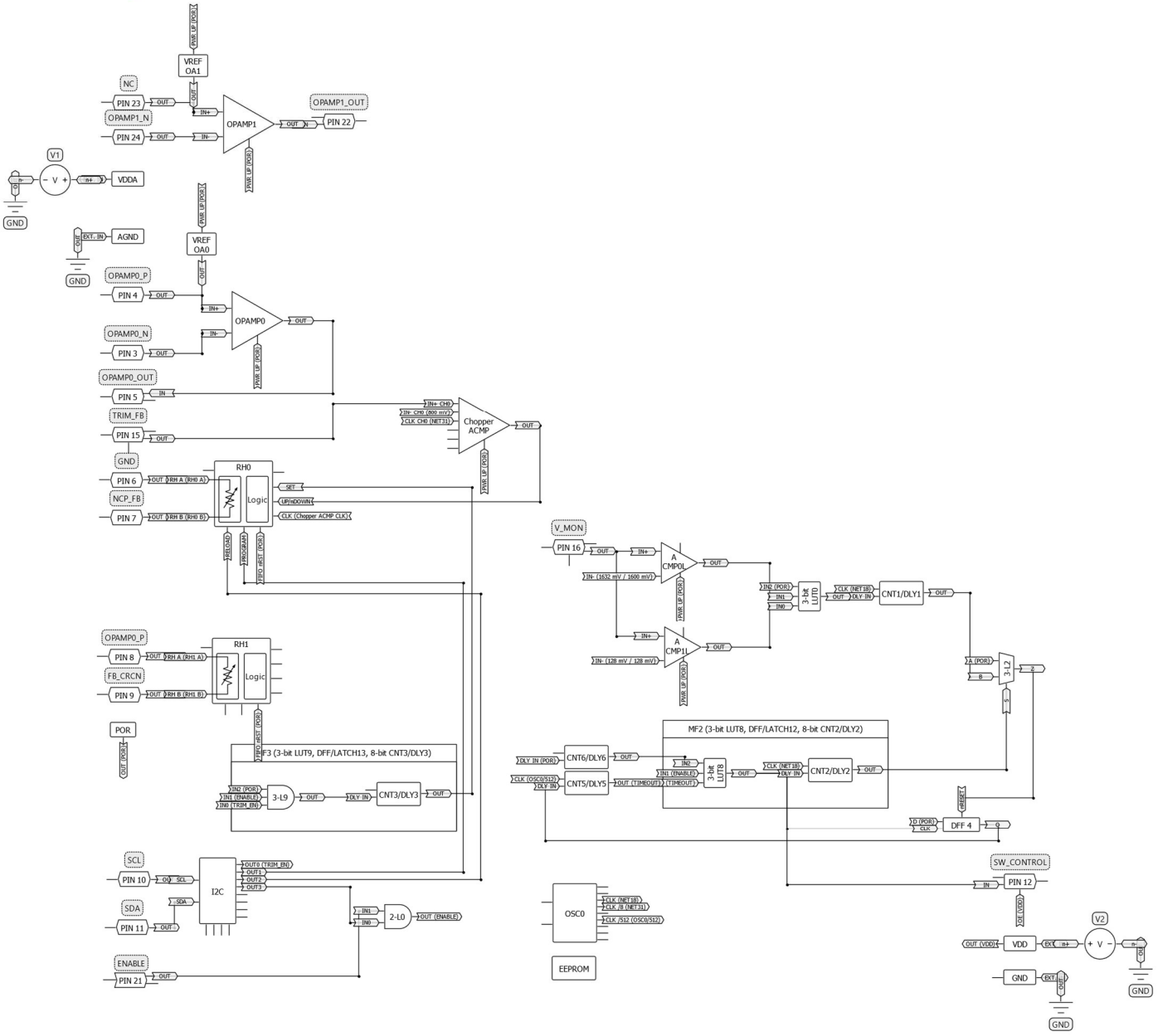


(Top View)
STQFN-24

Pin name

Pin #	Pin name	Pin #	Pin name
1	VDDA	13	VDD
2	AGND	14	GND
3	OPAMP0_N	15	TRIM_FB
4	OPAMP0_P	16	V_MON
5	OPAMP0_OUT	17	NC
6	GND	18	NC
7	NCP_FB	19	NC
8	OPAMP0_P	20	NC
9	FB_CRCN	21	ENABLE
10	SCL	22	OPAMP1_OUT
11	SDA	23	NC
12	SW_CONTROL	24	OPAMP1_N

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDDA	Analog Power Supply	Analog Power Supply	--
2	AGND	AGND	Ground	--
3	OPAMP0_N	Analog Input/Output	Analog Input/Output	floating
4	OPAMP0_P	Analog Input/Output	Analog Input/Output	floating
5	OPAMP0_OUT	Analog Input/Output	Analog Input/Output	floating
6	GND	Analog Input/Output	Analog Input/Output	floating
7	NCP_FB	Analog Input/Output	Analog Input/Output	floating
8	OPAMP0_P	Analog Input/Output	Analog Input/Output	floating
9	FB_CRCN	Analog Input/Output	Analog Input/Output	floating
10	SCL	Digital Input	Low Voltage Digital Input	floating
11	SDA	Digital Input	Low Voltage Digital Input	floating
12	SW_CONTROL	Digital Output	Push Pull 1X	floating
13	VDD	PWR	Supply Voltage	--
14	GND	GND	Ground	--
15	TRIM_FB	Analog Input/Output	Analog Input/Output	floating
16	V_MON	Analog Input/Output	Analog Input/Output	floating
17	NC	--	Keep Floating or Connect to GND	--
18	NC	--	Keep Floating or Connect to GND	--
19	NC	--	Keep Floating or Connect to GND	--
20	NC	--	Keep Floating or Connect to GND	--
21	ENABLE	Digital Input	Digital Input with Schmitt trigger	floating
22	OPAMP1_OUT	Analog Input/Output	Analog Input/Output	floating
23	NC	Analog Input/Output	Analog Input/Output	floating
24	OPAMP1_N	Analog Input/Output	Analog Input/Output	floating

Ordering Information

Part Number	Package Type
SLG7RN46352V	24-pin STQFN
SLG7RN46352V	24-pin STQFN - Tape and Reel (5k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
V_{DD} to GND, V_{DDA} to AGND (Note 1)		-0.3	7	V
Maximum Slew Rate of V_{DDA}		--	2	V/µs
Voltage at Input Pin		GND-0.3	VDD+0.3	V
Current at Input Pin		-1.0	1.0	mA
Maximum Average or DC Current through V_{DDA} or AGND Pin (Per chip side)	T_J=85°C	--	110	mA
	T_J=110°C	--	50	mA
Maximum Average or DC Current through V_{DD} or GND Pin (Per chip side)	T_J=85°C	--	100	mA
	T_J=110°C	--	50	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		
Note 1: V_{DDA} must be equal to V_{DD}				

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.4	3.3	5.5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at V_{DD}		0.1	--	--	µF
C_{IN}	Input Capacitance	PINs 10, 11	--	2.9	--	pF
C_{IN}	Input Capacitance	PIN 12	--	3.6	--	pF
C_{IN}	Input Capacitance	PINs 15, 16	--	3.8	--	pF
C_{IN}	Input Capacitance	PINs 17, 18, 19	--	10.2	--	pF
C_{IN}	Input Capacitance	PIN 20	--	27.8	--	pF
C_{IN}	Input Capacitance	PIN 21	--	5.7	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs. PINs 10, 11 are HIGH, PIN 21 is LOW	--	290	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}+0.3	V
V_{IH}	HIGH-Level Input Voltage	Logic Input with Schmitt Trigger	0.8xVDD	--	VDD+0.3	V
		Low-Level Logic Input (Note 1)	1.25	--	VDD+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input with Schmitt Trigger	GND-0.3	--	0.2xVDD	V
		Low-Level Logic Input (Note 1)	GND-0.3	--	0.5	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I_{OH}=1mA at V_{DD}=2.5V (Note 1)	2.387	--	--	V
		Push-Pull 1X, I_{OH}=3mA at V_{DD}=3.3V (Note 1)	3.037	--	--	V
		Push-Pull 1X, I_{OH}=5mA at V_{DD}=5.0V (Note 1)	4.687	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=1mA, at V_{DD}=2.5V (Note 1)	--	--	0.082	V

		Push-Pull 1X, I_{OL}=3mA, at V_{DD}=3.3V (Note 1)	--	--	0.202	V
		Push-Pull 1X, I_{OL}=5mA, at V_{DD}=5.0V (Note 1)	--	--	0.260	V
I_{OH}	HIGH-Level Output Current (Note 2)	Push-Pull 1X, V_{OH}=V_{DD}-0.2V at V_{DD}=2.5V (Note 1)	1.72	--	--	mA
		Push-Pull 1X, V_{OH}=2.4V at V_{DD}=3.3V (Note 1)	8.31	--	--	mA
		Push-Pull 1X, V_{OH}=2.4V at V_{DD}=5.0V (Note 1)	24.00	--	--	mA
I_{OL}	LOW-Level Output Current (Note 2)	Push-Pull 1X, V_{OL}=0.15V, at V_{DD}=2.5V (Note 1)	1.74	--	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at V_{DD}=3.3V (Note 1)	5.48	--	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at V_{DD}=5.0V (Note 1)	7.27	--	--	mA
T_{DLY1}	Delay1 Time	At temperature 25°C	38.6	39.8	41.7	ms
		At temperature -40 +85°C	38.6	39.8	44.2	ms
T_{DLY2}	Delay2 Time	At temperature 25°C	61.1	62.7	65.0	ms
		At temperature -40 +85°C	61.0	62.7	68.9	ms
T_{DLY3}	Delay3 Time	At temperature 25°C	3	4	7	µs
		At temperature -40 +85°C	3	4	9	µs
T_{DLY5}	Delay5 Time	At temperature 25°C	7.82	8.12	8.38	s
		At temperature -40 +85°C	7.80	8.12	8.88	s
T_{DLY6}	Delay6 Time	At temperature 25°C	61	63	66	µs
		At temperature -40 +85°C	61	63	69	µs
V_{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature 25°C	1617	--	1642	mV
		Low to High transition, at temperature -40 +85°C	1606	--	1646	mV
		High to Low transition, at temperature 25°C	1585	--	1610	mV
		High to Low transition, at temperature -40 +85°C	1574	--	1613	mV
V_{ACMP1}	Analog Comparator1 Threshold Voltage	Low to High transition, at temperature 25°C	118	--	135	mV
		Low to High transition, at temperature -40 +85°C	117	--	136	mV
		High to Low transition, at temperature 25°C	118	--	135	mV
		High to Low transition, at temperature -40 +85°C	117	--	136	mV
Chopper ACMP Channel 0		Low to High transition, at temperature 25°C	788	--	808	mV
		Low to High transition, at temperature -40 +85°C	783	--	807	mV
		High to Low transition, at temperature 25°C	788	--	808	mV
		High to Low transition, at temperature -40 +85°C	783	--	807	mV
V_{HYST}	Analog Comparator Hysteresis Voltage	ACMP 0 at temperature 25°C	25	32	33	mV
		ACMP 0 at temperature -40 +85°C	25	32	33	mV

T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	1.9	2.7	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.63	--	2.04	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.96	--	1.54	V
Note 1 No hysteresis. Note 2 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

Operational Amplifier0,1 Electrical Characteristics, V_{DDA}=2.4V to 5.5V, V_{CM}=V_{DDA}/2, V_{OUT}≈V_{DDA}/2, R_L=100kΩ to V_{DDA}/2, C_L=50pF, T=25°C

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	Guaranteed by PSRR Test	2.4	--	5.5	V
GBW	Gain Bandwidth Product	R_{LOAD}=10kΩ, C_{LOAD}=20pF, G=+1V/V BW=2.048MHz	--	2569	--	kHz
V_{OFFSET}	Input Offset Voltage	BW=2MHz	--	47	500	µV
V_{OFFSET}	Input Offset Voltage	BW=2MHz, T=-40°C to +85°C	--	47	1030	µV
V_{CMR}	Input Common-Mode Voltage Range	T=-40°C to +85°C	-0.2	--	V_{DD}+0.2	V
CMRR	Common-Mode Rejection Ratio	All Op Amps, GND+0.8V<VCM<VDD-0.8V, T=-40°C to +85°C	73.5	102	--	dB
CMRR	Common-Mode Rejection Ratio		69.7	101	--	dB
PSRR	Power Supply Rejection Ratio	V_{CM}=V_{DD}/2, T=-40°C to +85°C	80	101	--	dB
PSRR	Power Supply Rejection Ratio	V_{CM}=GND, T=-40°C to +85°C	83	102	--	dB
I_B	Input Bias Current	T=25°C	--	1.9	±9.0	pA
I_B	Input Bias Current	T=+85°C	--	1.9	±258.0	pA
I_{OFFSET}	Input Offset Current	T=25°C	--	--	3.2	pA
I_{OFFSET}	Input Offset Current	T=+85°C	--		210	pA
R_{CM}	Common-Mode Input Resistance		--	$3*10^{12}$	--	Ω
R_{DIFF}	Differential Input Resistance		--	10^{13}	--	Ω
A_{OL}	DC Open Loop Gain	R_{LOAD}=1MΩ, GND+0.1V < V_{OUT} < V_{DD}-0.1V, T=-40°C to +85°C	103.3	125.0	--	dB
A_{OL}	DC Open Loop Gain	R_{LOAD} = 50kΩ, GND+0.5V < V_{OUT} < V_{DD}-0.5V T=-40°C to +85°C	103.4	125.0	--	dB
SR	Slew Rate	R_{LOAD}=50kΩ, C_{LOAD}=85pF BW=2.048MHz, T=-40°C to +85°C	--	1.85	--	V/µs
Note 1 AGND = GND, unless otherwise noted. Note 2 Equivalent offset voltage of the amplifier after user's trim using digital rheostat. Gain of the amplifier is G=200 and the zero output voltage level Vzero=VDD/2. Note 3 Op amps analog supporting blocks are always turned on.						

100K Digital Rheostat EC at VA=VDD, VB=GND, T=-40°C to +85°C, VDD=2.4V to 5.5V Unless Otherwise Noted

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DR}	Rheostat Pin Voltage Range	Voltage between any (A or B) pins and AGND	AGND	--	VDDA	V
R_{DR}	Digital Rheostat Resistance	Full resistance with all switches open (Note 1)	94.426	101.582	113.741	kΩ
R_{DR_MIN}	Minimal Rheostat Resistance	Code=0x00	43.679	--	84.779	Ω
Number of taps					1024	
Calculated resistance RH0	Rs* Resistance (Initial data)	Code=800	--	79.39	--	kΩ
Calculated resistance RH1	Rs* Resistance (Initial data)	Code=1023	--	101.52	--	kΩ
R_S	Step Resistance	V_{DD}=(2.4V; 3.3V; 5.5V) V_{DDA}=(1V; -1V) T=(-40°C; 25°C; 85°C)	--	99.236	--	Ω
I_{DR_MAX}	Max current through Rheostat	T=25°C	--	--	2	mA
Note 1 User can calculate actual Digital Rheostat value using calibration data from NVM. Note 2 Includes internal timing. External circuit should be counted separately.						

I²C Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
F_{SCL}	Clock Frequency, SCL		--	--	400	kHz
t_{LOW}	Clock Pulse Width Low		1300	--	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)		--	--	50	ns
t_{AA}	Clock Low to Data Out Valid		--	--	900	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	--	ns
t_{HD_STA}	Start Hold Time		600	--	--	ns
t_{SU_STA}	Start Set-up Time		600	--	--	ns
t_{HD_DAT}	Data Hold Time		185	--	--	ns
t_{SU_DAT}	Data Set-up Time		335	--	--	ns
t_R	Inputs Rise Time		--	--	300	ns
t_F	Inputs Fall Time		--	--	300	ns
t_{SU_STD}	Stop Set-up Time		600	--	--	ns
t_{DH}	Data Out Hold Time		50	--	--	ns

Chip address

HEX	BIN	DEC
0x38	0111000	56

I2C Description

1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<1019:1016>. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 1 shows this basic command structure.

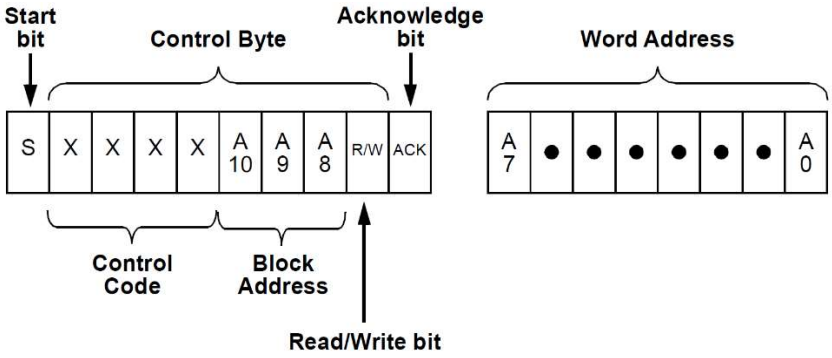


Figure1. I2C Basic Command Structure

2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

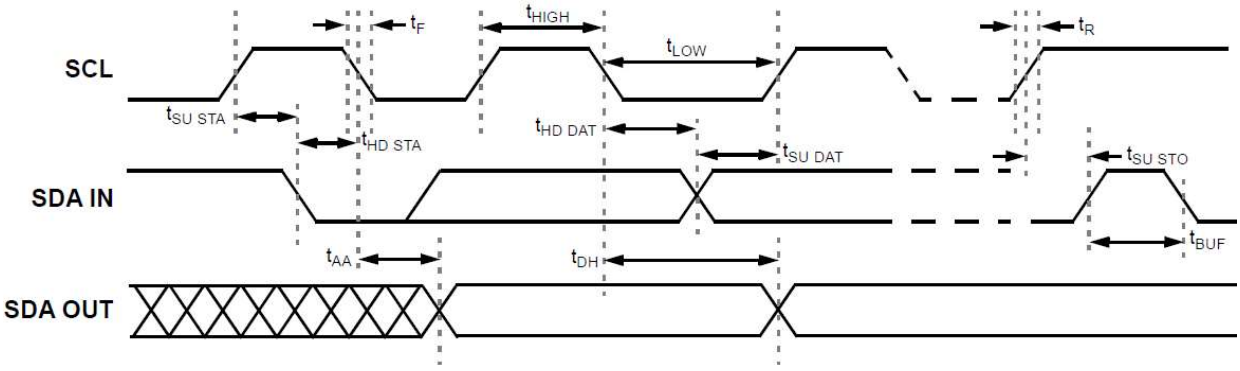


Figure2. I2C Serial General Timing

3. I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to “0”), are placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledge bit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7RN46352V to the correct data byte to be written. After the SLG7RN46352V sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG7RN46352V again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7RN46352V generates the Acknowledge bit.

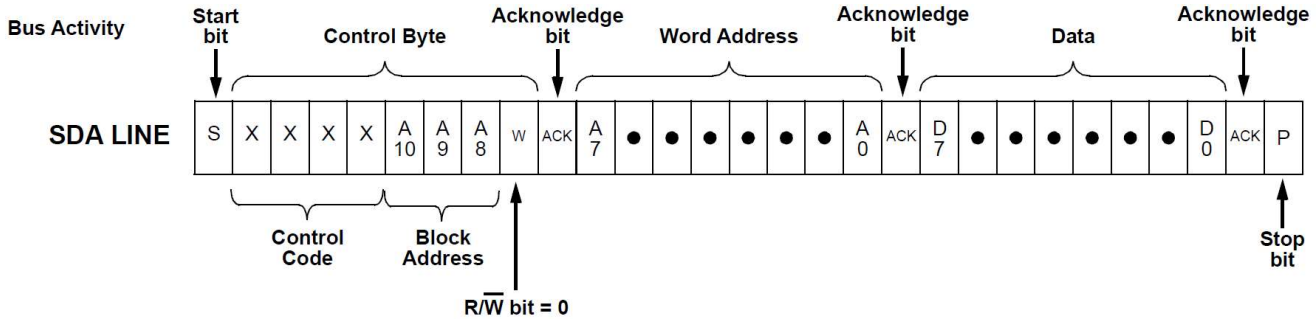


Figure3. I2C Write Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG7RN46352V issues an Acknowledge bit, followed by the requested eight data bits.

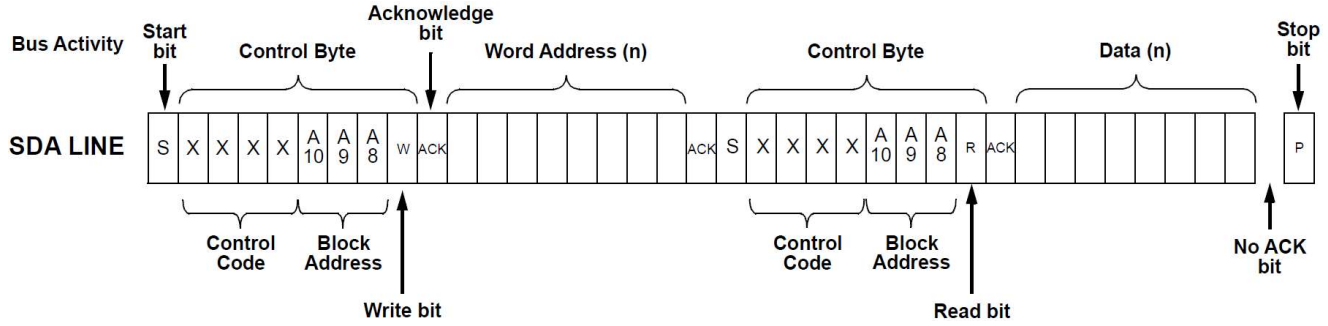


Figure4. I2C Random Read Command

4. Chip reconfiguration

SLG7RN46352V has an ISP capability. This means that the chip internal blocks configuration may be changed on the fly or even re-programmed via I2C. If there is a need for temporary change of the chip configuration (it will be reset to the programmed configuration after the chip is reset or power on again) one should use Registers (A10, A9, A8 = “000”). To reprogram a configuration via I2C NVM should be accessed with A10, A9, A8 = “010”. Please keep in mind that random byte write procedure is not supported, this may lead to incorrect chip configuration. Only page write procedure is supported.

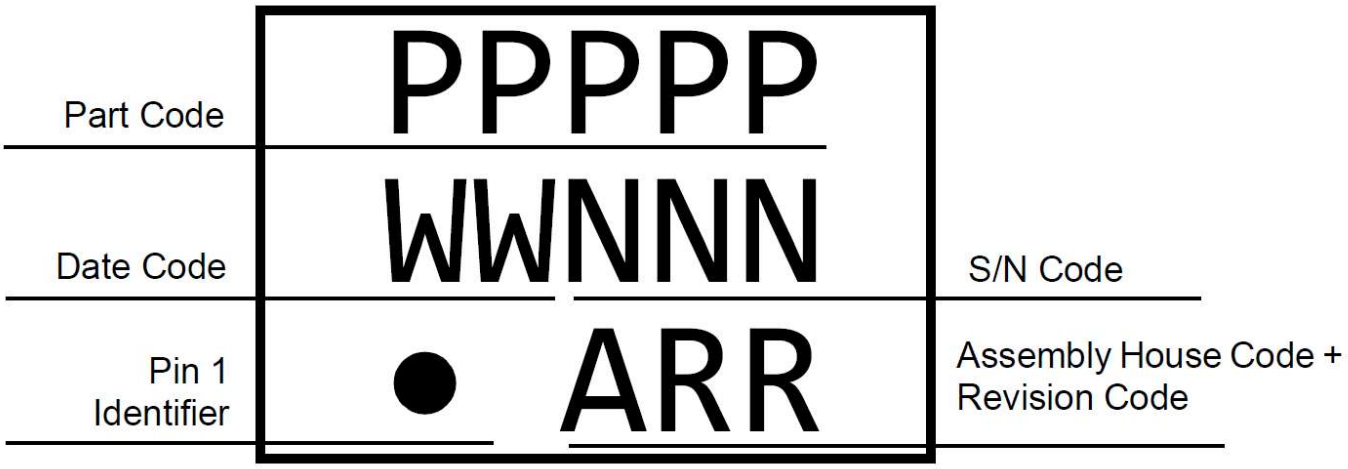
5. I2C register control data

Address Byte	Register Bit	Block	Function
0x7C	reg<992>	Virtual Input <0>	TRIM_EN. Default is 0.
	reg<993>	Virtual Input <1>	PROGRAM for RH0. Default is 0.
	reg<994>	Virtual Input <2>	RELOAD for RH0. Default is 0.
	reg<995>	Virtual Input <3>	ENABLE. Default is 1.

6. I2C Commands:

1. [start] [0x38] [w] [0x7C] [xxxxxxx(OUT0)] [stop] // set TRIM_EN
2. [start] [0x38] [w] [0x7C] [xxxxxx(OUT1)x] [stop] // set PROGRAM for RH0
3. [start] [0x38] [w] [0x7C] [xxxxx(OUT2)xx] [stop] // set RELOAD for RH0
4. [start] [0x38] [w] [0x7C] [xxxx(OUT3)xxx] [stop] // set ENABLE
5. [start] [0x38] [w] [0x7C] [start] [0x08] [R] [xxxx(OUT3)(OUT2)(OUT1)(OUT0)] [stop] // read state status OUT0-OUT3

Package Top Marking



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.12	002	U	0xA24CC898			04/14/2023

Lock coverage for this part is indicated by √, from one of the following options:

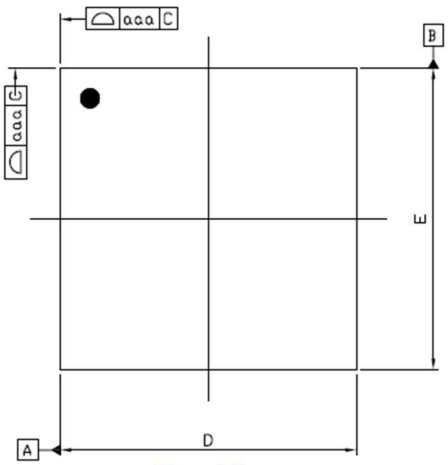
√	Unlocked
	Partly lock read
	Partly lock write
	Partly lock read and write
	Partly lock read and lock write
	Lock read and partly lock write
	Read lock
	Write lock
	Lock read and write

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

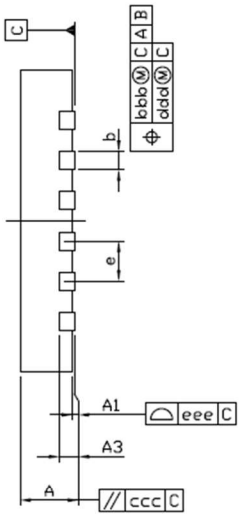
Package Outlines

STQFN 24L 3 MM X 3 MM X 0.55 MM 0.4P GREEN PACKAGE

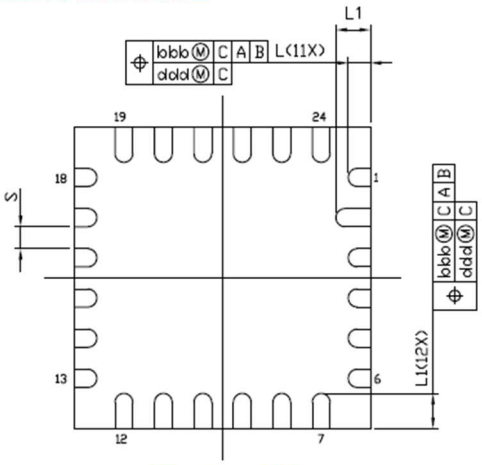
IC Net Weight: 0.0116 g



Top View



Side View



Bottom View

PKG CODE	UQFN					
SYMBOLS	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.10	0.15	0.20	0.004	0.006	0.008
b	0.13	0.18	0.23	0.005	0.007	0.009
D	2.95	3.00	3.05	0.116	0.118	0.120
E	2.95	3.00	3.05	0.116	0.118	0.120
e	0.40 BSC			0.016 BSC		
L	0.175	0.225	0.275	0.007	0.009	0.011
L1	0.30	0.35	0.40	0.012	0.014	0.016
S	0.22 REF.			0.009 REF.		
aaa	0.07			0.003		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

"A1" MAX LEAD COPLANARITY 0.05mm
STANDARD TOLERANCE : ±0.05

PAD SIZE	LEAD FINISH		JEDEC CODE
	Pure Tin	PPF	
	V	X	N/A

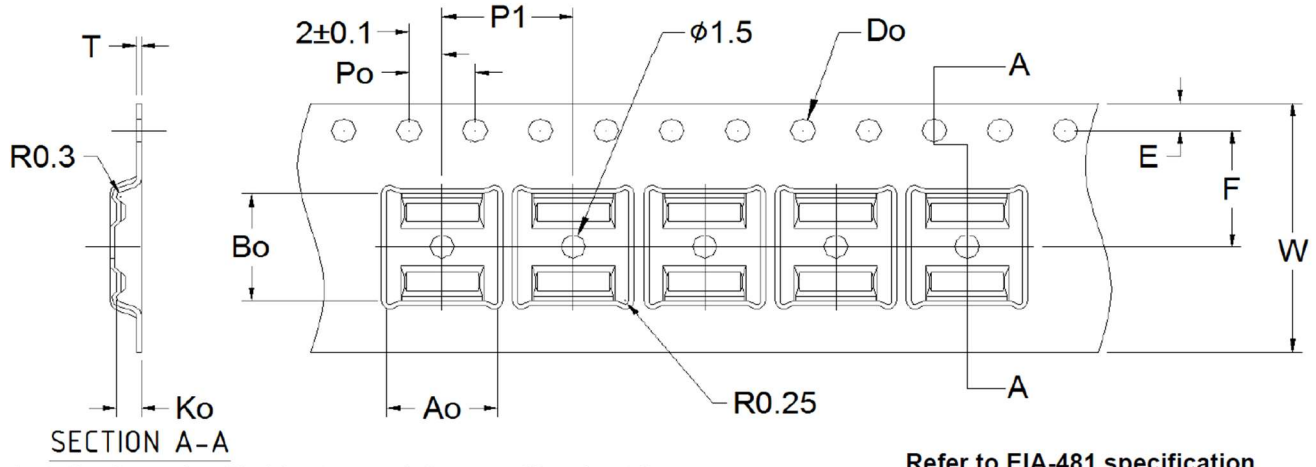
NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 24L 3mmx3mm 0.4P FC Green	24	3 x 3 x 0.55	5000	10000	330 / 100	42	336	42	336	12	8

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 24L 3mmx3mm 0.4P FC Green	3.3	3.3	0.8	4	8	1.55	1.75	5.5	12



Note: Orientation in carrier: Pin1 is at upper left corner (Quadrant1).

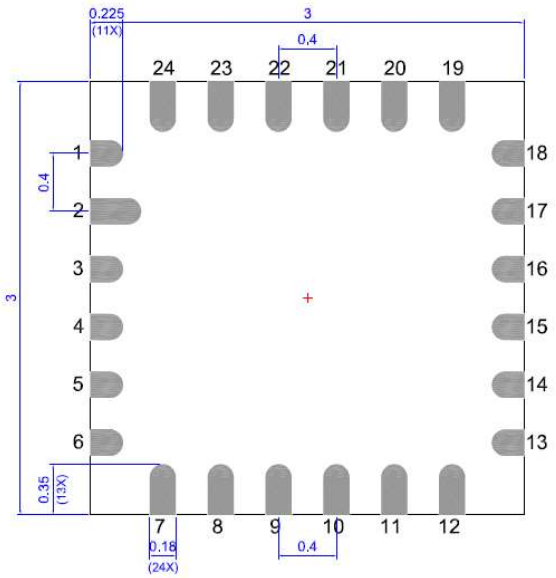
Refer to EIA-481 specification

Recommended Reflow Soldering Profile

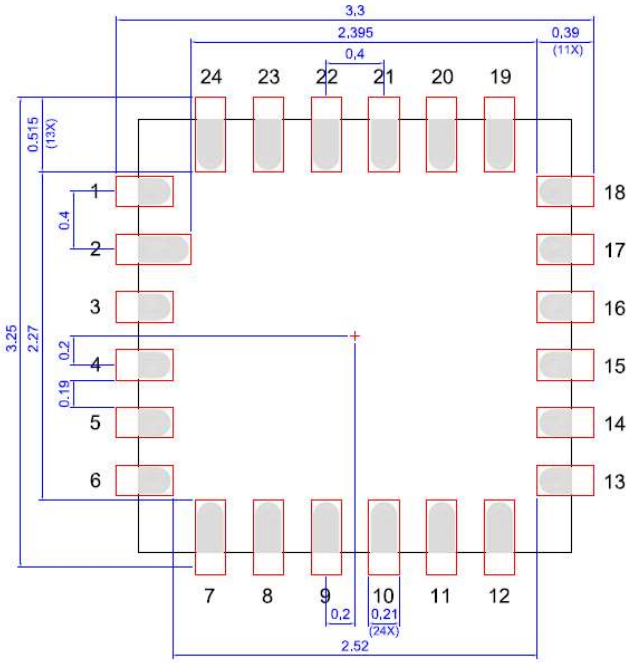
Please see IPC/JEDEC J-STD-020: for relevant soldering information. More information can be found at www.jedec.org.

Layout Guidelines

Expose Pad
(Package face down)



Recommended Landing Pattern
(Package face down)



Datasheet Revision History

Date	Version	Change
03/06/2023	0.10	New design for SLG47004V chip
03/28/2023	0.11	Updated datasheet revision table
04/14/2023	0.12	Design was updated by customer

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.