SLG7RN46360

GreenPAK ™

Standard reset circuit for JTAG I/F

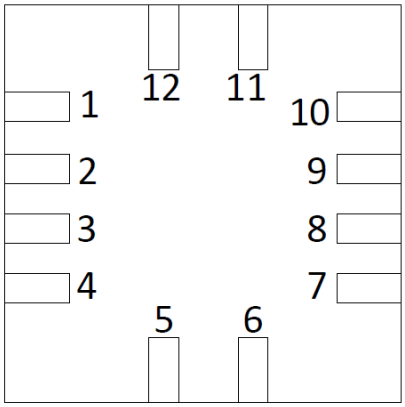
General Description

Renesas SLG7RN46360 is a low power and small form device. The SoC is housed in a 1.6mm x 1.6mm STQFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 12 Package

Pin Configuration



STQFN-12
(Top View)

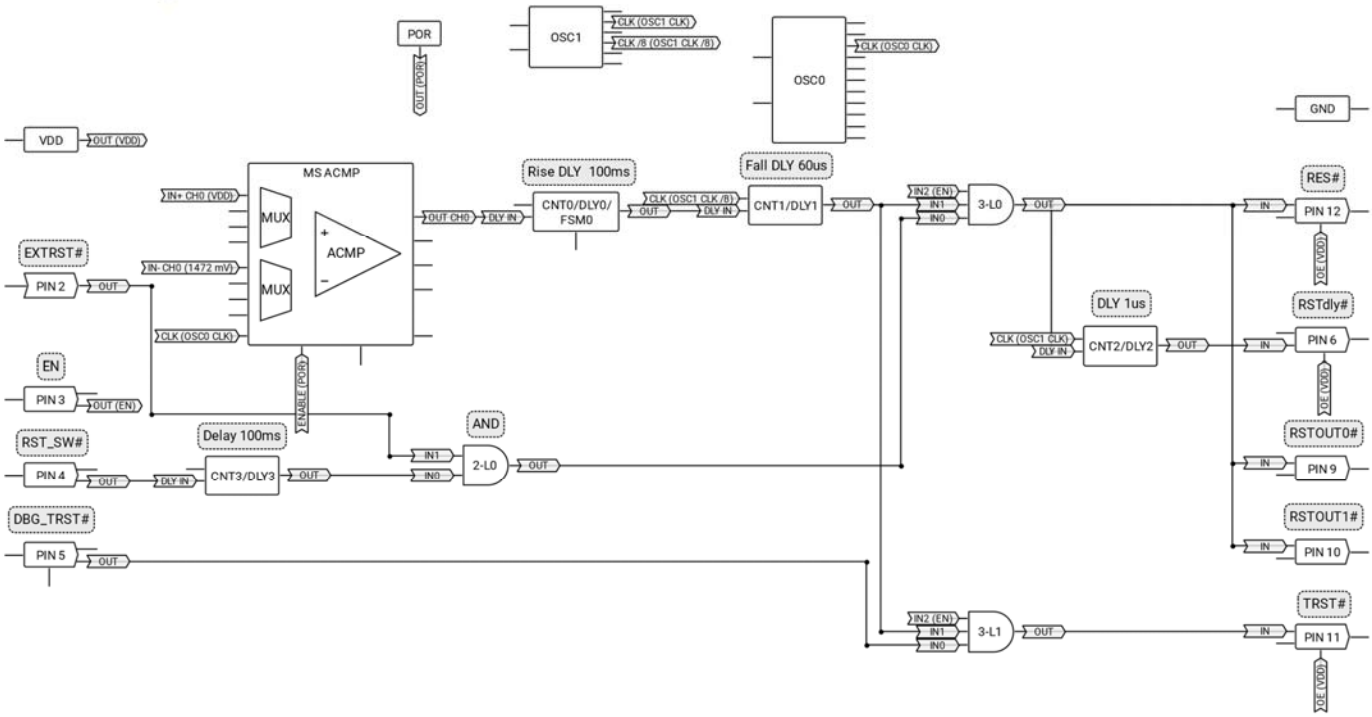
Output Summary

3 Outputs - 3-State Output 1X
2 Outputs - Open Drain NMOS 1X

Pin Name

Pin #	Pin name	Pin #	Pin name
1	VDD	7	GND
2	EXTRST#	8	NC
3	EN	9	RSTOUT0#
4	RST_SW#	10	RSTOUT1#
5	DBG_TRST#	11	TRST#
6	RSTdly#	12	RES#

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	EXTRST#	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
3	EN	Digital Input	Digital Input without Schmitt trigger	floating
4	RST_SW#	Digital Input	Digital Input without Schmitt trigger	floating
5	DBG_TRST#	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
6	RSTdly#	Digital Output	3-State Output 1X	1MΩ pulldown
7	GND	GND	Ground	--
8	NC	--	Keep Floating or Connect to GND	--
9	RSTOUT0#	Digital Output	Open Drain NMOS 1X	floating
10	RSTOUT1#	Digital Output	Open Drain NMOS 1X	floating
11	TRST#	Digital Output	3-State Output 1X	1MΩ pulldown
12	RES#	Digital Output	3-State Output 1X	1MΩ pulldown

Ordering Information

Part Number	Package Type
SLG7RN46360V	12-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
V_{HIGH} to GND		-0.3	7	V
Voltage at Input Pin		GND-0.5V	V_{DD}+0.5V	V
Maximum Average or DC Current (Through V_{DD} or GND pin)		--	90	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	OD 1x	--	11	
Current at Input Pin		-1.0	1.0	mA
Input leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

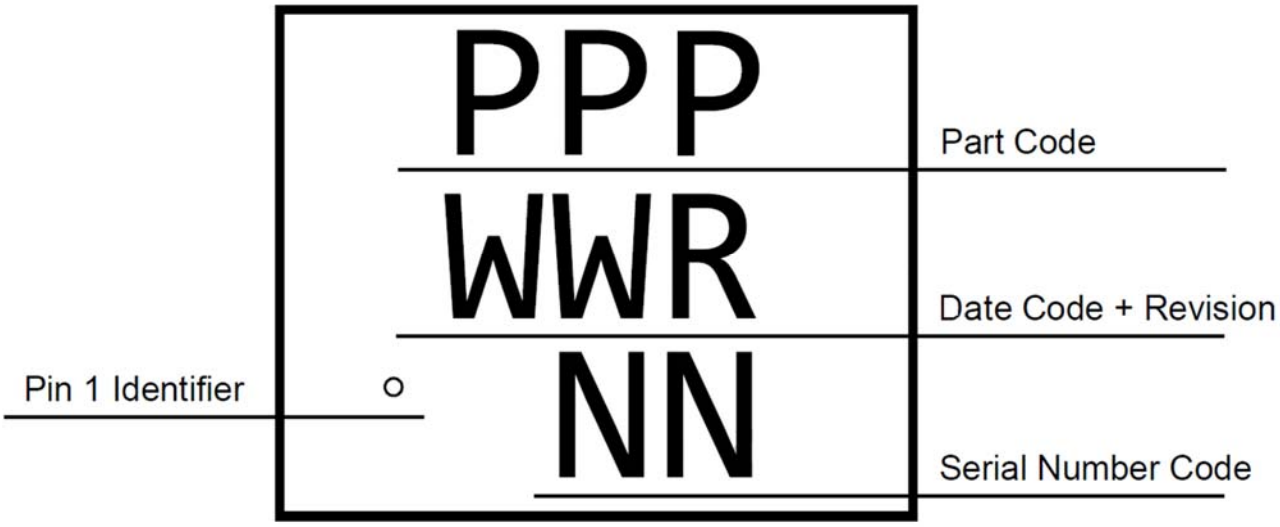
Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		0.1	--	--	µF
C_{IN}	Input Capacitance		--	2.5	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs. PINs 2,3,4,5 are LOW. (after DLY0 time)	--	40	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3	V
V_{IH}	HIGH-Level Input Voltage	Logic Input (Note 1)	0.7xVDD	--	VDD+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input (Note 1)	GND-0.3	--	0.3xVDD	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I_{OH}=3mA at VDD=3.3V	2.68	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V	--	--	0.227	V
		Open Drain NMOS 1X, I_{OL}=3mA, at VDD=3.3V	--	--	0.089	V
I_{OH}	HIGH-Level Output Current	Push-Pull 1X, V_{OH}=2.4V at VDD=3.3V	5.125	--	--	mA
I_{OL}	LOW-Level Output Current (Note 2)	Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V	4.622	--	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=3.3V	11.438	--	--	mA
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 2, 5, 6, 11, 12	--	1	--	MΩ
T_{DLY0}	Delay time	At temperature 25°C	97.57	100.34	103.60	ms
		At temperature -40 +85°C (Note 3)	96.74	100.34	109.89	ms
T_{DLY1}	Delay time	At temperature 25°C	59	60	63	µs
		At temperature -40 +85°C (Note 3)	59	60	65	µs
T_{DLY2}	Delay time	At temperature 25°C	0.9	1.0	1.4	µs
		At temperature -40 +85°C (Note 3)	0.9	1.0	1.5	µs

T_{DLY3}	Delay time	At temperature 25°C	97.57	100.34	103.60	ms
		At temperature -40 +85°C (Note 3)	96.74	100.34	109.89	ms
V_{ACMP}	MS ACMP Channel0 Threshold Voltage	Low to High transition, at temperature 25°C	2924	--	2963	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	2910	--	2970	mV
		High to Low transition, at temperature 25°C	2925	--	2963	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	2909	--	2971	mV
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.85	3.42	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.55	1.86	2.17	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.06	1.34	1.62	V

Note 1 No hysteresis.
Note 2 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 3 Guaranteed by Design.

Package Top Marking



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.20	008	U	0xC9D5A51E	1EZ	C	09/03/2024

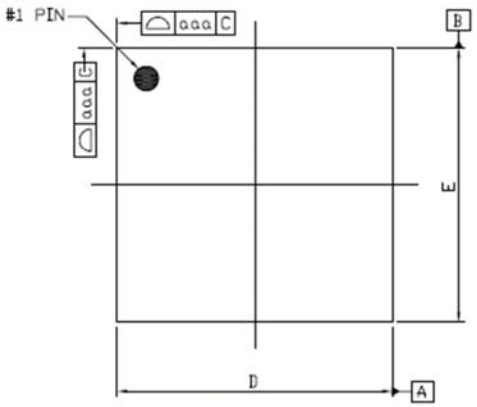
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

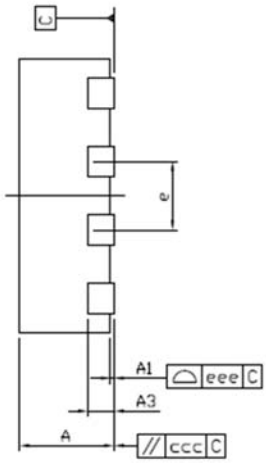
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Outlines

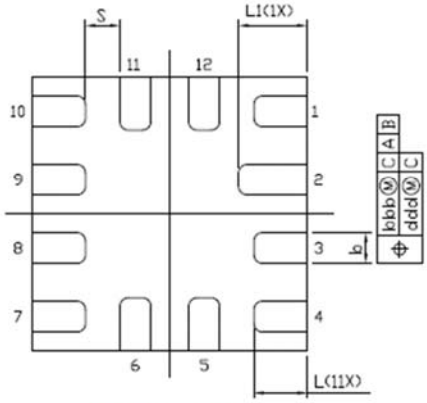
JEDEC MO-220IC Net Weight: 0.0035 g



Top View



Side View



Bottom View

Controlling dimensions: mm

Symbol	MILLIMETER			INCH		
	Min	Nom.	Max	Min	Nom.	Max
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.10	0.15	0.20	0.004	0.006	0.008
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.55	1.60	1.65	0.061	0.063	0.065
e	0.40 BSC			0.016 BSC		
L	0.26	0.31	0.36	0.010	0.012	0.014
L1	0.35	0.40	0.45	0.014	0.016	0.018
b	0.13	0.18	0.23	0.005	0.007	0.009
S	0.200 REF			0.008 REF		
aaa	0.07			0.003		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

"A1" max lead coplanarity 0.05 mm
Standard tolerance: ±0.05

Notes:

1. All dimensions are in millimeters.

2. Dimension "b" applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension "b" should not be measured in that radius area.

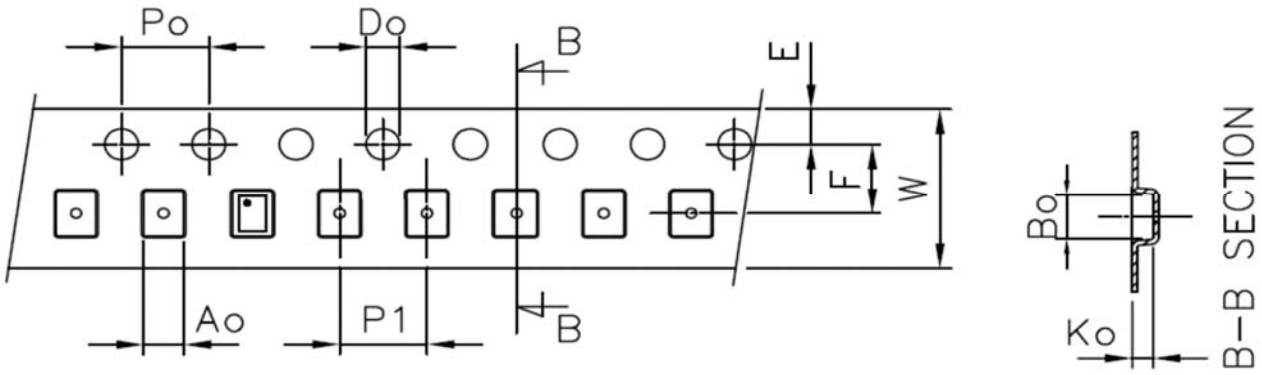
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 12L 1.6mm x 1.6mm x 0.55mm 0.4P FC Green	12	1.6x1.6x0.55	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L 1.6mm x 1.6mm x 0.55mm 0.4P FC Green	1.9	2.3	0.76	4	4	1.5	1.75	3.5	8

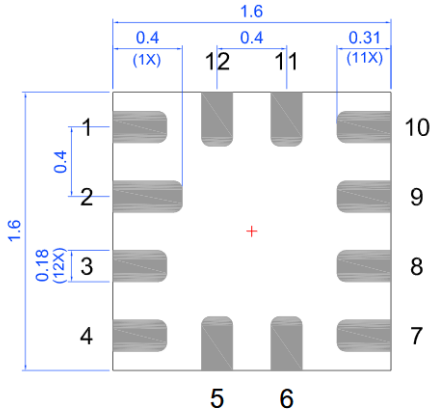


Recommended Reflow Soldering Profile

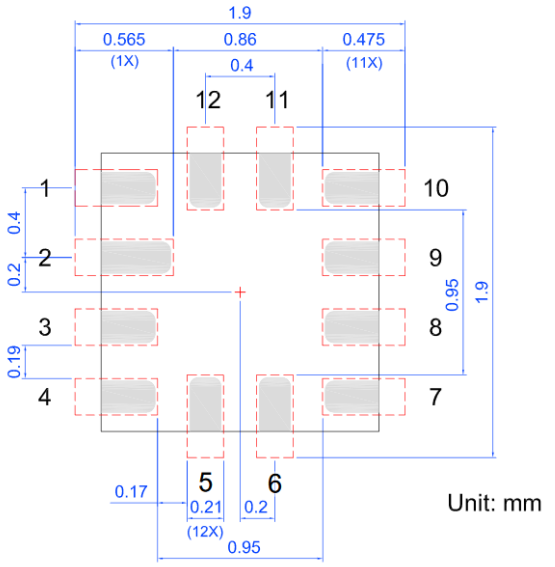
Please see IPC/JEDEC J-STD-020. More information can be found at www.jedec.org.

Layout Guidelines

Expose Pad
(Package face down)



Recommended Landing Pattern
(Package face down)



Datasheet Revision History

Date	Version	Change
03/07/2023	0.10	New design
10/13/2023	0.11	Updated Device Revision Table
10/25/2023	0.12	Added PIN2 and 2-L0 LUT, set PIN12 output mode to 1x push pull
10/30/2023	0.13	Updated Device Revision Table
01/23/2024	0.14	The PIN11 and PIN12 output mode were updated to 1x 3-State
03/14/2024	0.15	Design updated by customer
04/23/2024	0.16	Design updated by customer
05/15/2024	0.17	Design updated by customer
08/12/2024	0.18	Design updated by customer
08/20/2024	0.19	Design updated by customer
09/03/2024	0.20	Updated DRS Table

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