SLG7XL44677

GreenPAK™

Carrier Card Reset Logic

General Description

SLG7XL44677 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

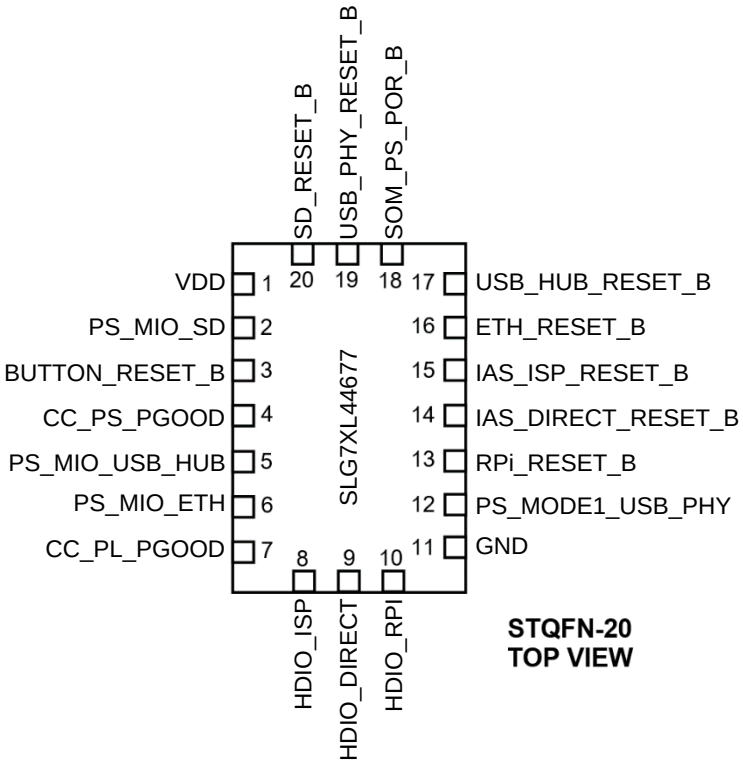
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

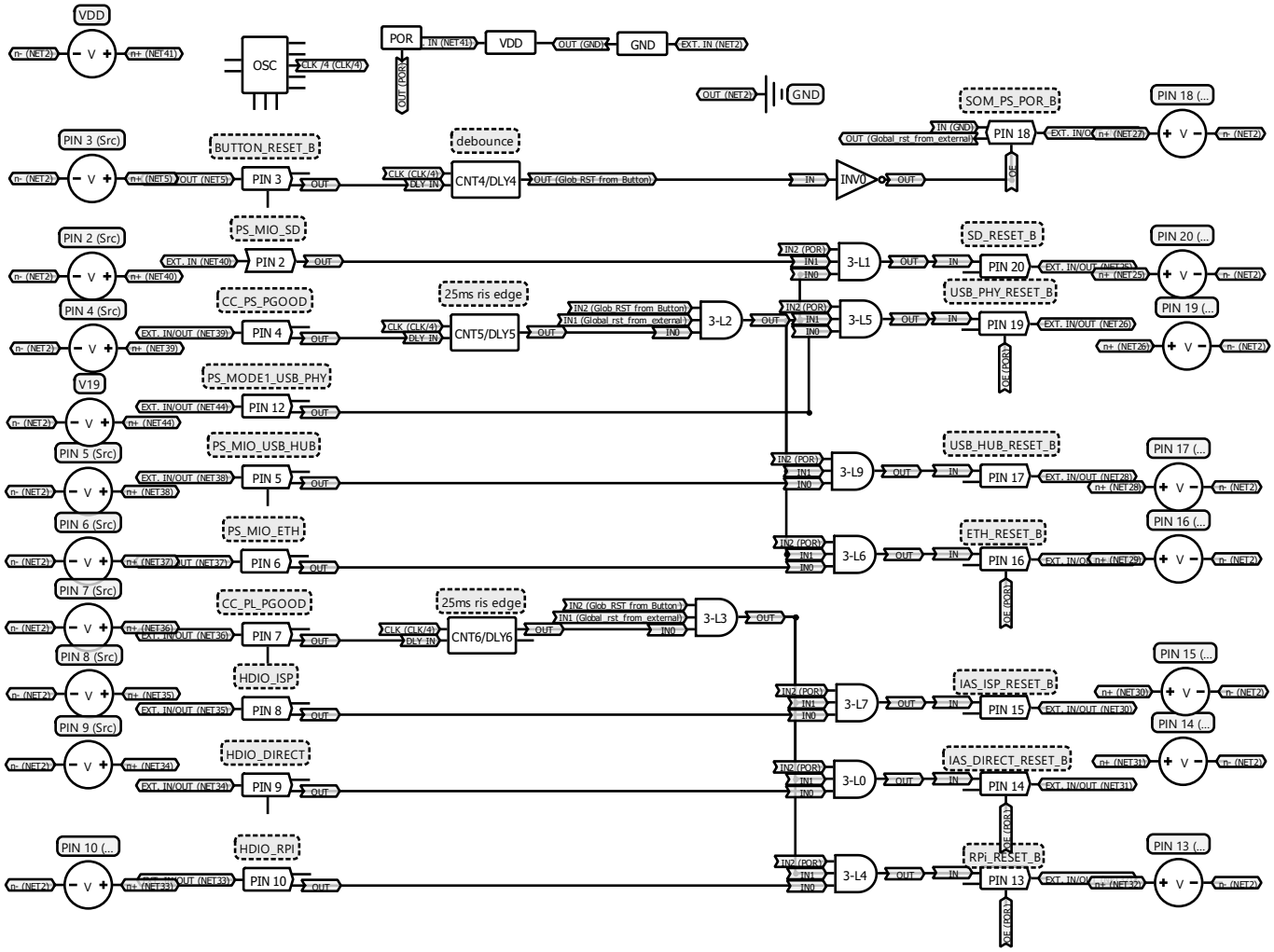
Output Summary

8 Outputs - Open Drain NMOS 1X

Pin Configuration



Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	PS_MIO_SD	Digital Input	Low Voltage Digital Input	1MΩ pulldown
3	BUTTON_RESET_B	Digital Input	Digital Input without Schmitt trigger	10kΩ pullup
4	CC_PS_PGOOD	Digital Input	Digital Input without Schmitt trigger	100kΩ pullup
5	PS_MIO_USB_HUB	Digital Input	Low Voltage Digital Input	1MΩ pulldown
6	PS_MIO_ETH	Digital Input	Low Voltage Digital Input	1MΩ pulldown
7	CC_PL_PGOOD	Digital Input	Digital Input without Schmitt trigger	100kΩ pullup
8	HDIO_ISP	Digital Input	Low Voltage Digital Input	1MΩ pulldown
9	HDIO_DIRECT	Digital Input	Low Voltage Digital Input	1MΩ pulldown
10	HDIO_RPI	Digital Input	Low Voltage Digital Input	1MΩ pulldown
11	GND	GND	Ground	--
12	PS_MODE1_USB_PHY	Digital Input	Low Voltage Digital Input	floating
13	RPi_RESET_B	Digital Output	Open Drain NMOS 1X	floating
14	IAS_DIRECT_RESET_B	Digital Output	Open Drain NMOS 1X	floating
15	IAS_ISP_RESET_B	Digital Output	Open Drain NMOS 1X	floating
16	ETH_RESET_B	Digital Output	Open Drain NMOS 1X	floating
17	USB_HUB_RESET_B	Digital Output	Open Drain NMOS 1X	floating
18	SOM_PS_POR_B	Bi-directional	Low Voltage Digital Input / Open Drain NMOS 1X	floating
19	USB_PHY_RESET_B	Digital Output	Open Drain NMOS 1X	floating
20	SD_RESET_B	Digital Output	Open Drain NMOS 1X	floating

Ordering Information

Part Number	Package Type
SLG7XL44677V	V=STQFN-20
SLG7XL44677VTR	VTR=STQFN-20 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	OD 1x	--	8	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

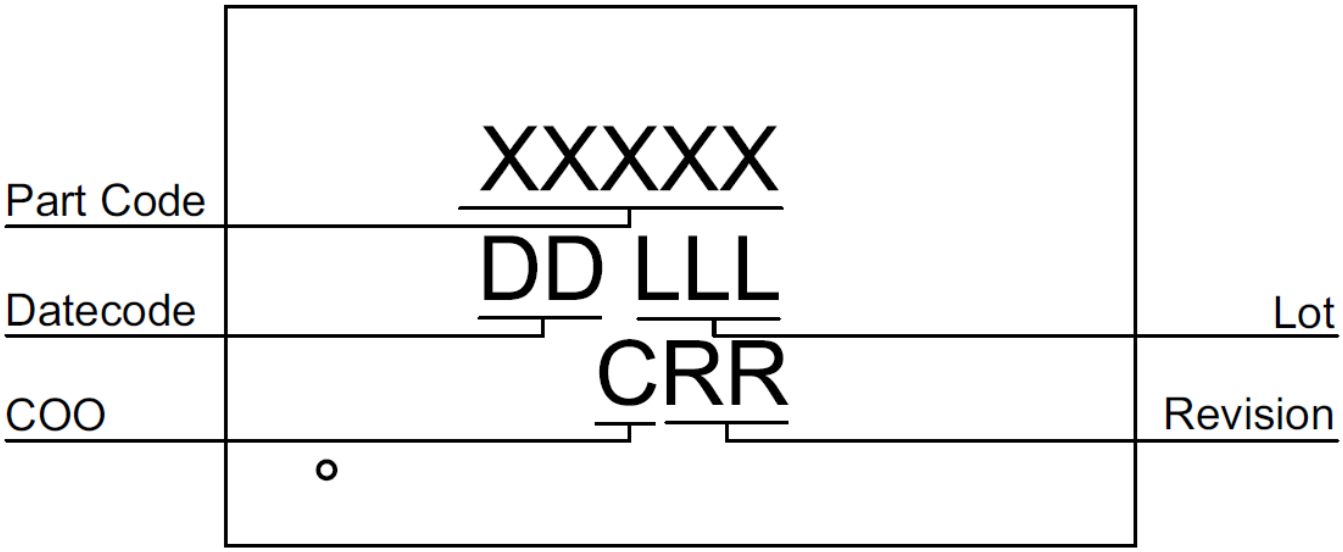
Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5	5.5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	84	mA
		T_J = 110°C	--	--	40	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input at VDD=5.0V	2.64	--	--	V
		Low-Level Logic Input at VDD=5.0V	1.23	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input at VDD=5.0V	--	--	1.84	V
		Low-Level Logic Input at VDD=5.0V	--	--	0.78	V
V_{OL}	LOW-Level Output Voltage	Open Drain NMOS 1X, I_{OL}=5mA, at VDD=5.0V	--	0.102	0.18	V
I_{OL}	LOW-Level Output Current (Note 1)	Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=5.0V	10.82	17.38	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PIN 3	7	10	13	kΩ
		Pull up on PINs 4, 7	70	100	130	kΩ
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 2, 5, 6, 8, 9, 10	700	1000	1300	kΩ
T_{DLY4}	Delay4 Time	At temperature 25°C	39.98	41.20	42.50	ms
		At temperature -40 +85°C (Note 3)	36.27	41.20	50.68	ms
T_{DLY5}	Delay5 Time	At temperature 25°C	24.26	25.04	25.87	ms
		At temperature -40 +85°C (Note 3)	22.01	25.04	30.85	ms
T_{DLY6}	Delay6 Time	At temperature 25°C	24.26	25.04	25.87	ms
		At temperature -40 +85°C (Note 3)	22.01	25.04	30.85	ms
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.3	--	ms

PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.18	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.73	0.914	1.103	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 14, 15, 16, 17, 18, 19 and 20 to another.
3. Guaranteed by Design.

Package Top Marking



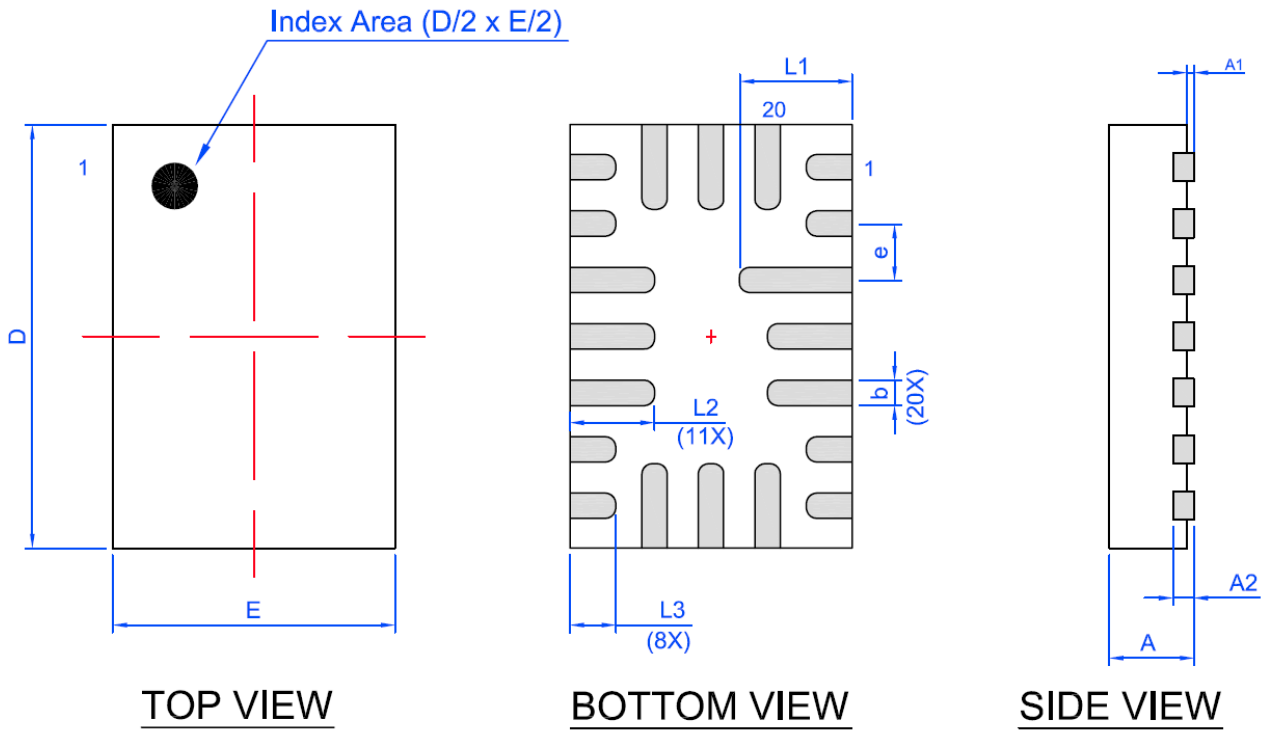
XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	002	L	0x48C9F90A	44677	AA	01/22/2021

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P COL Package
JEDEC MO-220, Variation WECE



Unit: mm

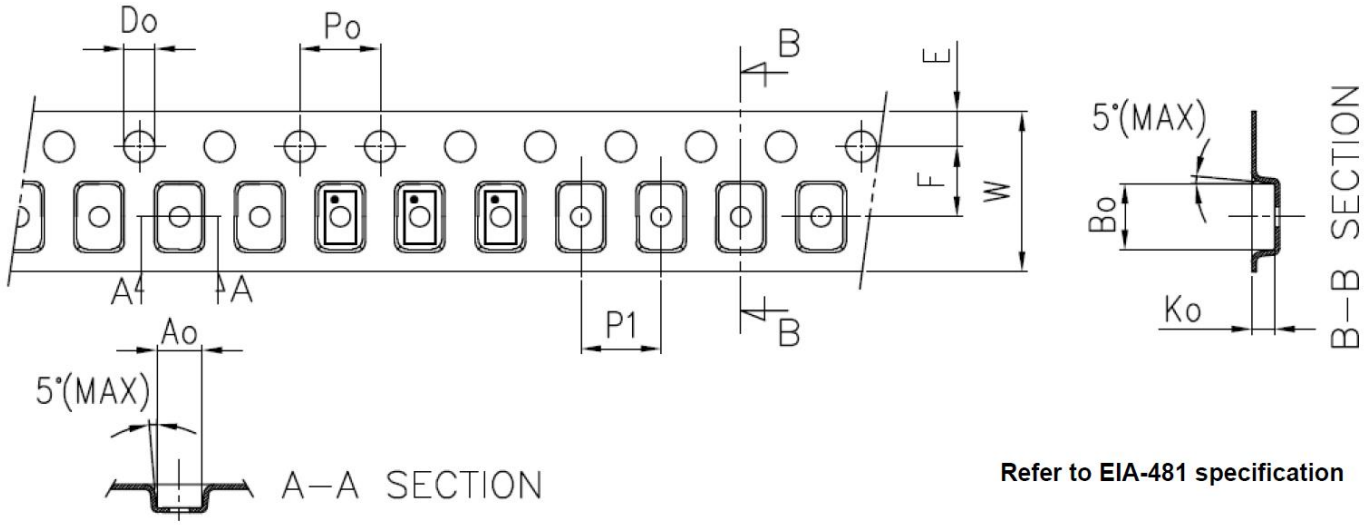
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

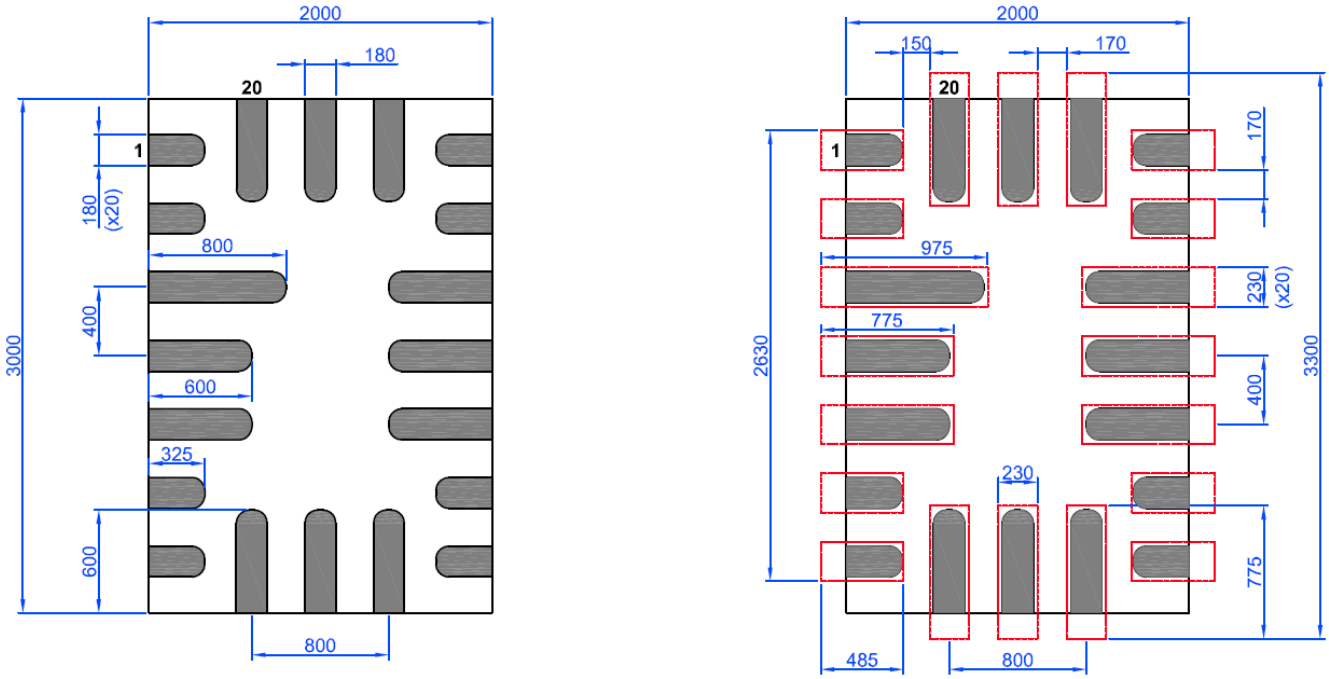
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern

Exposed Pad
(Top View)

Recommended Land Pattern
(Top View)

Units: µm



Datasheet Revision History

Date	Version	Change
01/07/2021	0.10	New design for SLG46721 chip
01/07/2021	0.11	Pins renamed
01/20/2021	0.12	Updated Lock Status
01/22/2021	0.13	Updated Device Revision Table
01/22/2021	1.00	Production Release

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