

TP65H070G4PS

650V SuperGaN® GaN FET in PQFN (source tab)

Description

The TP65H070G4PS 650V, 72mΩ Gallium Nitride (GaN) FET is a normally-off device. It combines state-of-the-art high voltage GaN HEMT and low voltage silicon MOSFET technologies—offering superior reliability and performance.

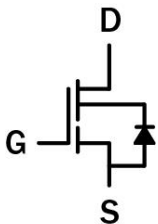
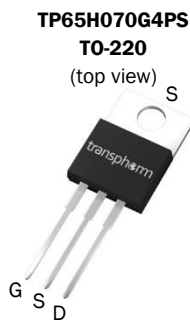
The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge

Related Literature

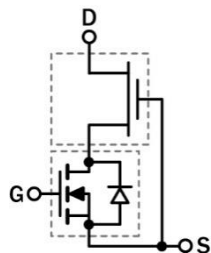
- [Recommended External Circuitry for GaN FETs](#)
- [Printed Circuit Board Layout and Probing](#)
- [Paralleling GaN FETs](#)
- [Low cost driver solution](#)

Ordering Information

Part Number	Package	Package Configuration
TP65H070G4PS	3 lead T0-220	Source



Cascode Schematic Symbol



Cascode Device Structure

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
 - Wide gate safety margin
 - Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Benefits

- Achieves increased efficiency in both hard- and soft-switched circuits
 - Increased power density
 - Reduced system size and weight
 - Overall lower system cost
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor
- Computing
- Consumer



Key Specifications

V_{DSS} (V)	650
$V_{DSS(TR)}$ (V)	800
$R_{DS(on)eff}$ (mΩ) max*	85
Q_{oss} (nC) typ	78
Q_G (nC) typ	9

* Dynamic on-resistance; see Figures 18 and 19

Absolute Maximum Ratings ($T_c=25\text{ }^\circ\text{C}$ unless otherwise stated.)

Symbol	Parameter	Limit Value	Unit	
V_{DSS}	Drain to source voltage ($T_J = -55\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$)	650	V	
$V_{DSS(TR)}$	Transient drain to source voltage ^(a)	800		
V_{GSS}	Gate to source voltage	± 20		
P_D	Maximum power dissipation @ $T_c=25\text{ }^\circ\text{C}$	96	W	
I_D	Continuous drain current @ $T_c=25\text{ }^\circ\text{C}$ ^(b)	29	A	
	Continuous drain current @ $T_c=100\text{ }^\circ\text{C}$ ^(b)	18.4	A	
I_{DM}	Pulsed drain current (pulse width: $10\mu\text{s}$)	120	A	
T_c	Operating temperature	Case	-55 to +150	$^\circ\text{C}$
T_J		Junction	-55 to +150	$^\circ\text{C}$
T_s	Storage temperature	-55 to +150	$^\circ\text{C}$	
T_{SOLD}	Soldering peak temperature ^(c)	260	$^\circ\text{C}$	

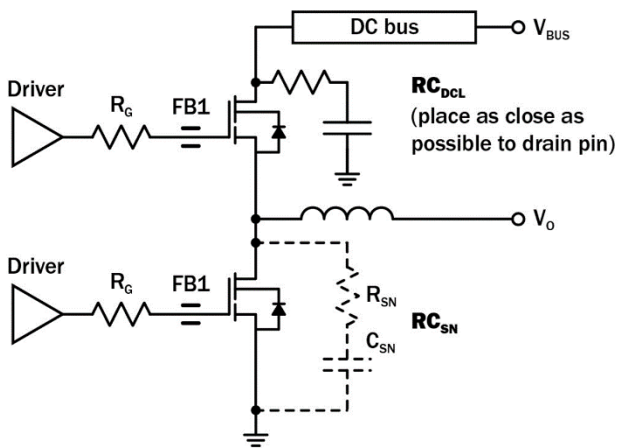
Notes:

- a. In off-state, spike duration < $30\mu\text{s}$, non-repetitive
- b. For increased stability at high current operation, see Circuit Implementation on page 3
- c. For 10 sec., 1.6mm from the case

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Junction-to-case	1	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient	62	$^\circ\text{C}/\text{W}$

Circuit Implementation



Simplified Half-bridge Schematic (See also on Figure 13)

For additional gate driver options/configurations, please see Application Note [Recommended External Circuitry for GaN FETs](#)

Layout Recommendations

Gate Loop:

- Gate Driver: SiLab Si823x/Si827x
- Keep gate loop compact

Power loop: (For reference see page 13)

- Minimize power loop path inductance
- Minimize switching node coupling with high and low power plane
- Add DC bus snubber to reduce to voltage ringing
- Add Switching node snubber for high current operation

Recommended gate drive: (0V, 12V) with $R_G = 50\Omega$

Gate Ferrite Bead (FB1)	Required DC Link RC Snubber (RC_{DCL}) ^(d)	Recommended Switching Node RC Snubber (RC_{SN}) ^(e)
200 – 300 Ω at 100MHz	10nF + 5 Ω	Not necessary ^(e)

Notes:

d. RC_{DCL} should be placed as close as possible to the drain pin

e. RC_{SN} (68pF + 15 Ω) is needed only if R_G is smaller than recommendations

Electrical Parameter (T_J=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
V _{(BL)DSS}	Drain-source voltage	650	—	—	V	V _{GS} =0V, I _D =1mA
V _{GS(th)}	Gate threshold voltage	3.3	4	4.8	V	V _{DS} =V _{GS} , I _D =0.7mA
R _{DS(on)eff}	Drain-source on-resistance ^(f)	—	72	85	mΩ	V _{GS} =10V, I _D =18A, T _J =25 °C
		—	148	—		V _{GS} =10V, I _D =18A, T _J =150 °C
I _{DSS}	Drain-to-source leakage current	—	1.2	12	μA	V _{DS} =650V, V _{GS} =0V, T _J =25 °C
		—	8	—		V _{DS} =650V, V _{GS} =0V, T _J =150 °C
I _{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V _{GS} =20V
	Gate-to-source reverse leakage current	—	—	-100		V _{GS} =-20V
C _{ISS}	Input capacitance	—	638	—	pF	V _{GS} =0V, V _{DS} =400V, f=1MHz
C _{OSS}	Output capacitance	—	72	—		
C _{RSS}	Reverse transfer capacitance	—	2	—		
C _{O(er)}	Output capacitance, energy related ^(g)	—	105	—	pF	V _{GS} =0V, V _{DS} =0V to 400V
C _{O(tr)}	Output capacitance, time related ^(h)	—	194	—		
Q _G	Total gate charge	—	9	—	nC	V _{DS} =400V, V _{GS} =0V to 10V, I _D =18A
Q _{GS}	Gate-source charge	—	3.7	—		
Q _{GD}	Gate-drain charge	—	2.4	—		
Q _{OSS}	Output charge	—	80	—	nC	V _{GS} =0V, V _{DS} =0V to 400V
t _{D(on)}	Turn-on delay	—	43.4	—	ns	V _{DS} =400V, V _{GS} =0V to 12V, I _D =18A, R _G =50Ω
t _R	Rise time	—	6.2	—		
t _{D(off)}	Turn-off delay	—	56	—		
t _F	Fall time	—	7.2	—		

Notes:

f. Dynamic on-resistance; see Figures 19 and 20 for test circuit and conditions

g. Equivalent capacitance to give same stored energy as V_{DS} rises from 0V to 400V

h. Equivalent capacitance to give same charging time as V_{DS} rises from 0V to 400V

Electrical Parameters ($T_J=25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	18	A	$V_{GS}=0V$, $T_C=100^\circ\text{C}$, $\leq 25\%$ duty cycle
V_{SD}	Reverse voltage ⁽ⁱ⁾	—	2.4	—	V	$V_{GS}=0V$, $I_S=18A$
		—	1.7	—		$V_{GS}=0V$, $I_S=9A$
t_{RR}	Reverse recovery time	—	80	—	ns	$I_S=18A$, $V_{DD}=400V$, $di/dt=1000A/ms$
Q_{RR}	Reverse recovery charge ^(j)	—	0	—	nC	

Notes:

i. Includes dynamic $R_{DS(on)}$ effect

j. Excludes Q_{oss}

Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)

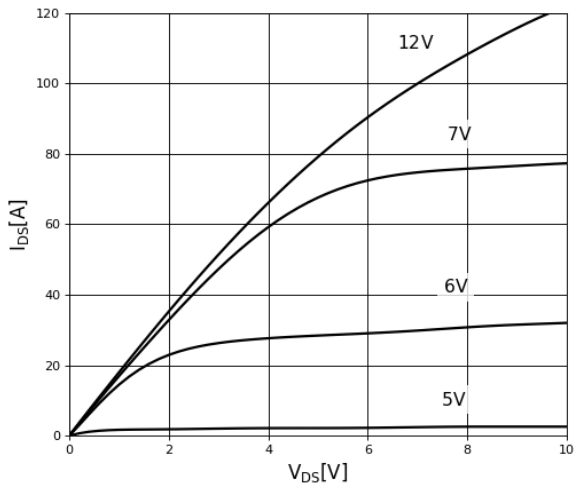


Figure 1. Typical Output Characteristics $T_J=25^\circ\text{C}$
Parameter: V_{GS}

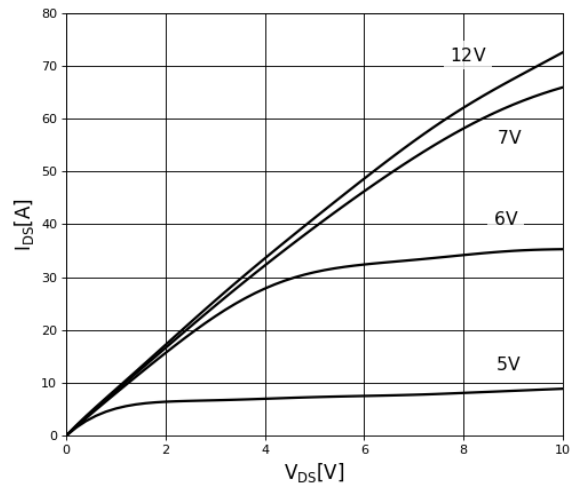


Figure 2. Typical Output Characteristics $T_J=150^\circ\text{C}$
Parameter: V_{GS}

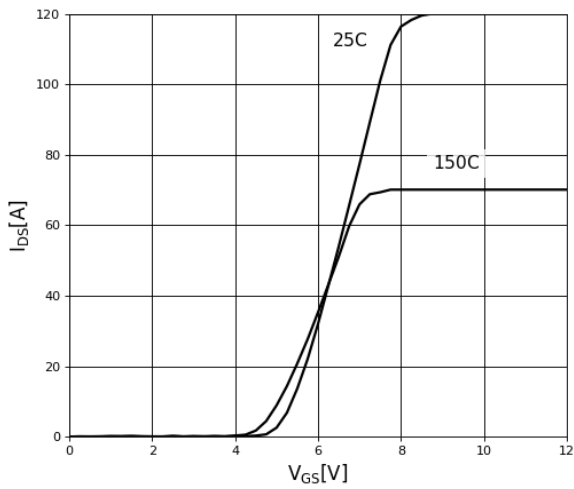


Figure 3. Typical Transfer Characteristics
 $V_{DS}=10\text{V}$, parameter: T_J

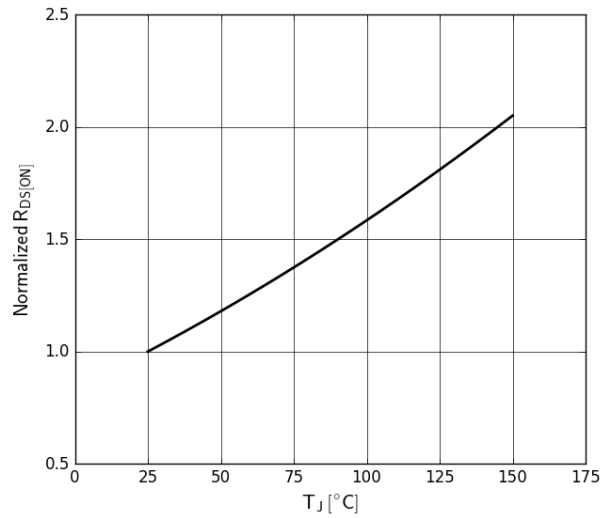


Figure 4. Normalized On-resistance
 $I_D=18\text{A}$, $V_{GS}=10\text{V}$

Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)

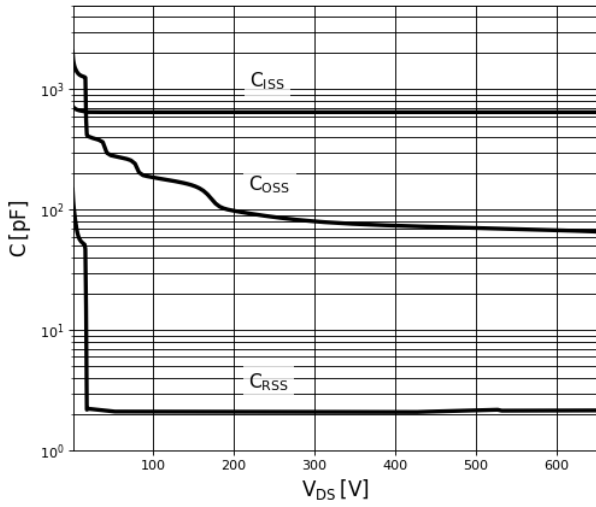


Figure 5. Typical Capacitance
 $V_{GS}=0V, f=1MHz$

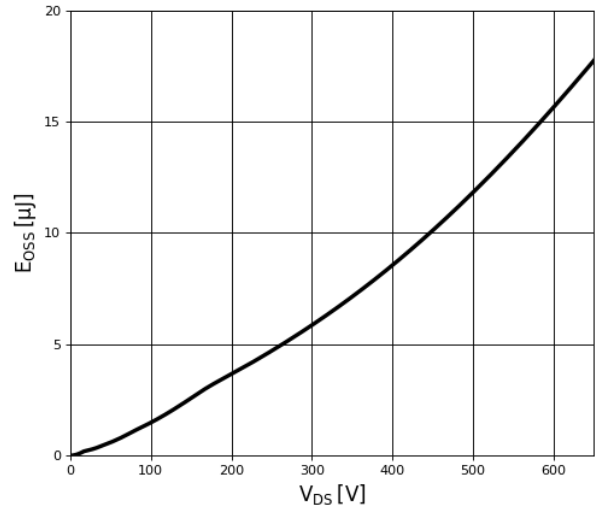


Figure 6. Typical C_{oss} Stored Energy

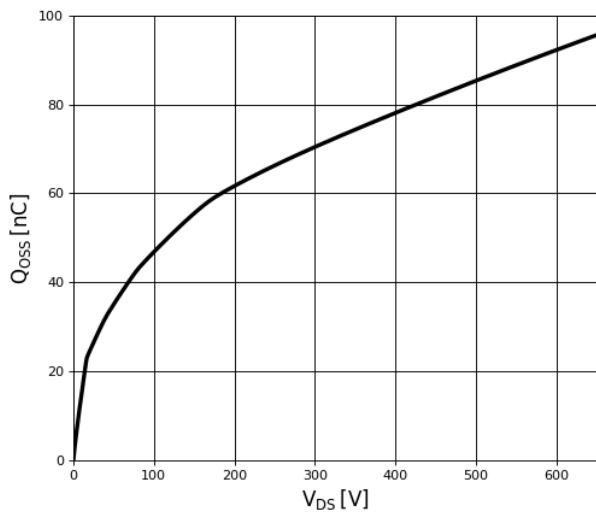


Figure 7. Typical Q_{oss}

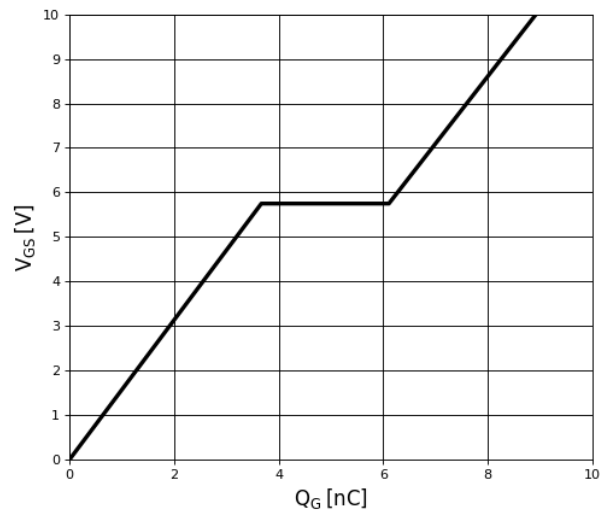


Figure 8. Typical Gate Charge
 $I_{DS}=18A, V_{DS}=400V$

Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)

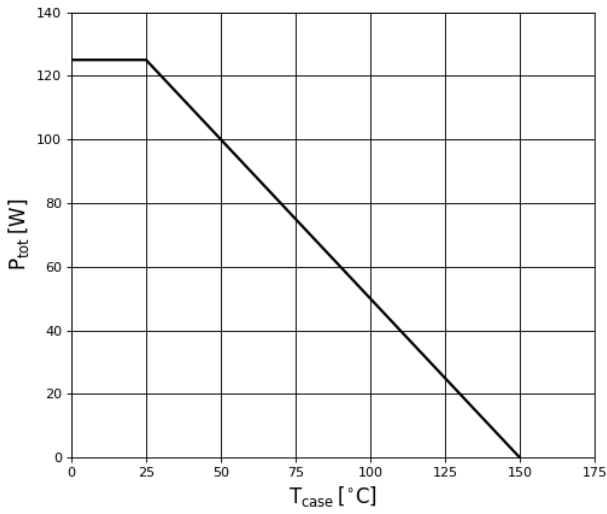


Figure 9. Power Dissipation

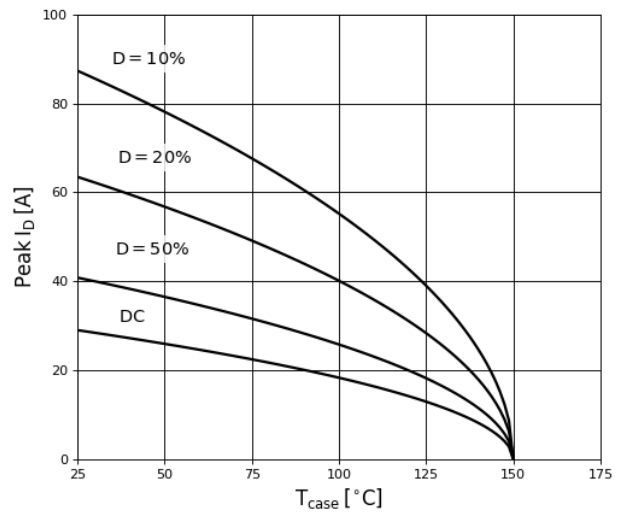


Figure 10. Current Derating

Pulse width $\leq 10\mu\text{s}$, $V_{GS} \geq 10\text{V}$

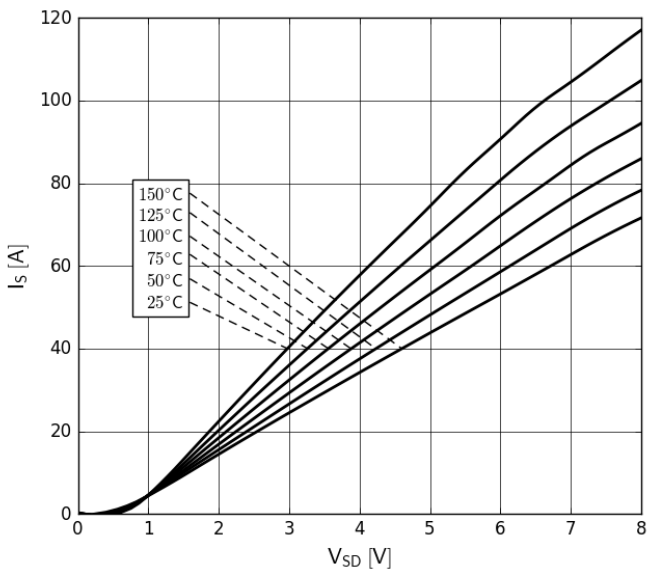


Figure 11. Forward Characteristics of Rev. Diode

$I_S=f(V_{SD})$, parameter: T_J

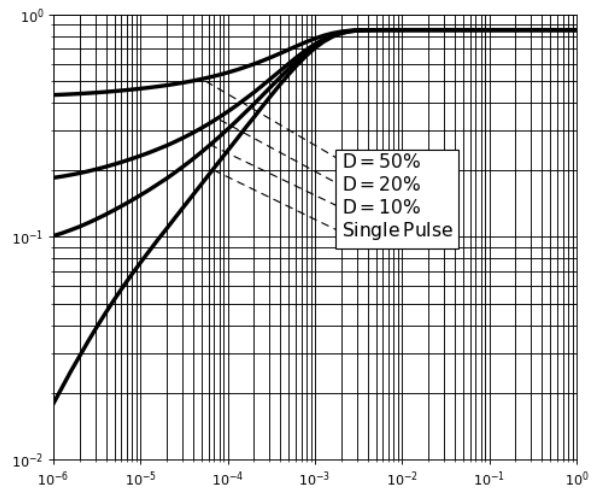


Figure 12. Transient Thermal Resistance

Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)

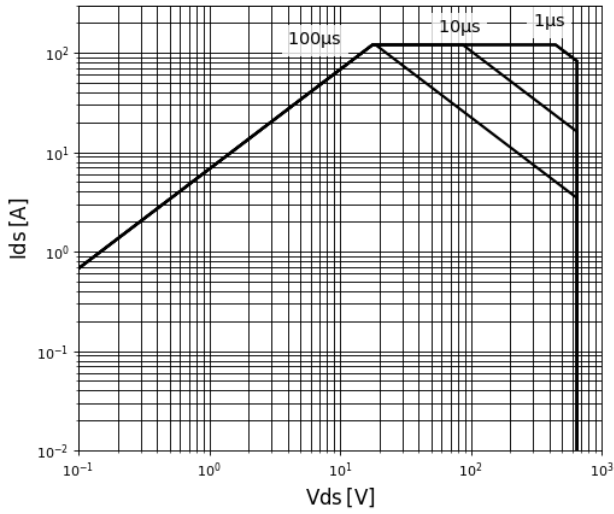


Figure 13. Safe Operating Area $T_c=25^\circ\text{C}$

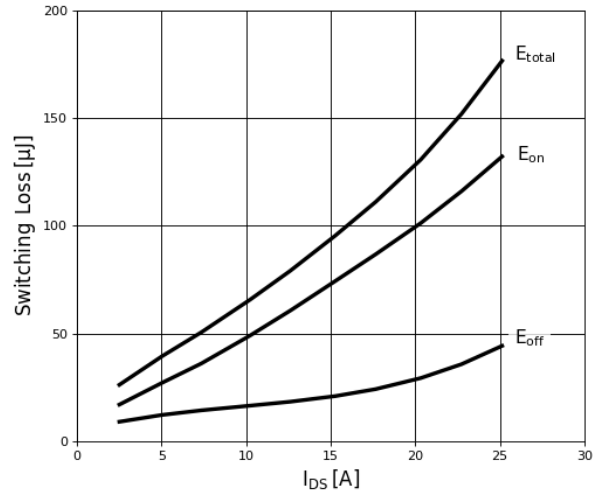


Figure 14. Inductive Switching Loss $T_c=25^\circ\text{C}$
 $R_g=50\Omega$, $V_{DS}=400\text{V}$

Test Circuits and Waveforms

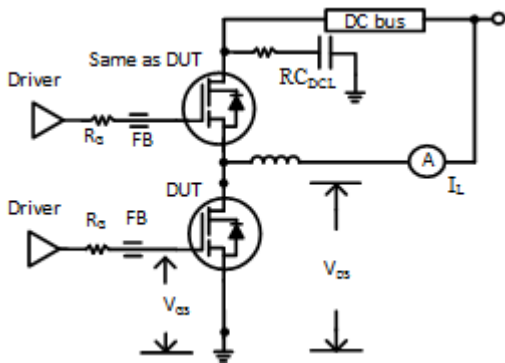


Figure 15. Switching Time Test Circuit

(see circuit implementation on page 3 for methods to ensure clean switching)

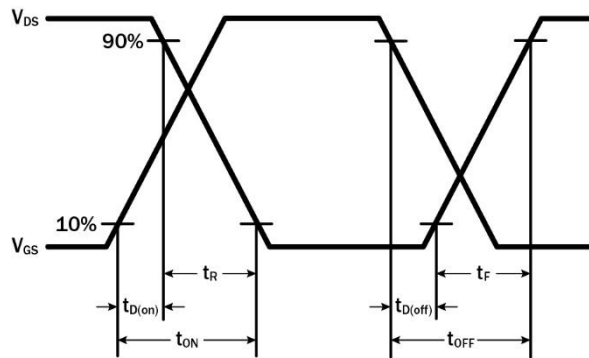


Figure 16. Switching Time Waveform

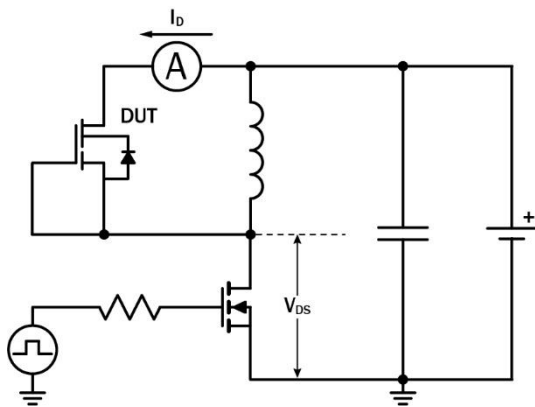


Figure 17. Diode Characteristics Test Circuit

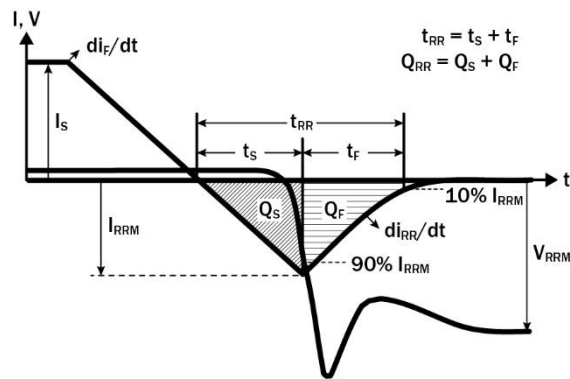


Figure 18. Diode Recovery Waveform

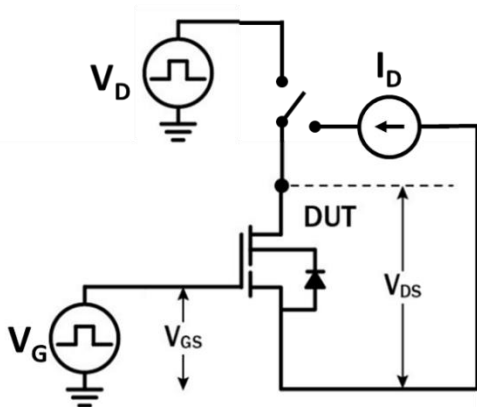


Figure 19. Dynamic $R_{DS(on)eff}$ Test Circuit

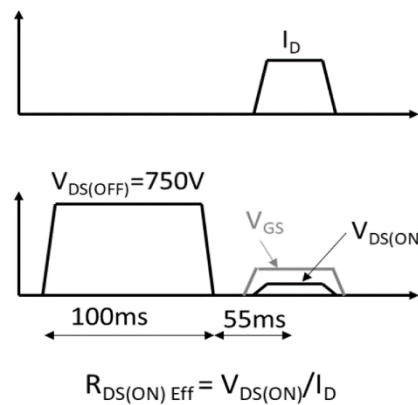


Figure 20. Dynamic $R_{DS(on)eff}$ Waveform

Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Renesas GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Renesas GaN Devices:

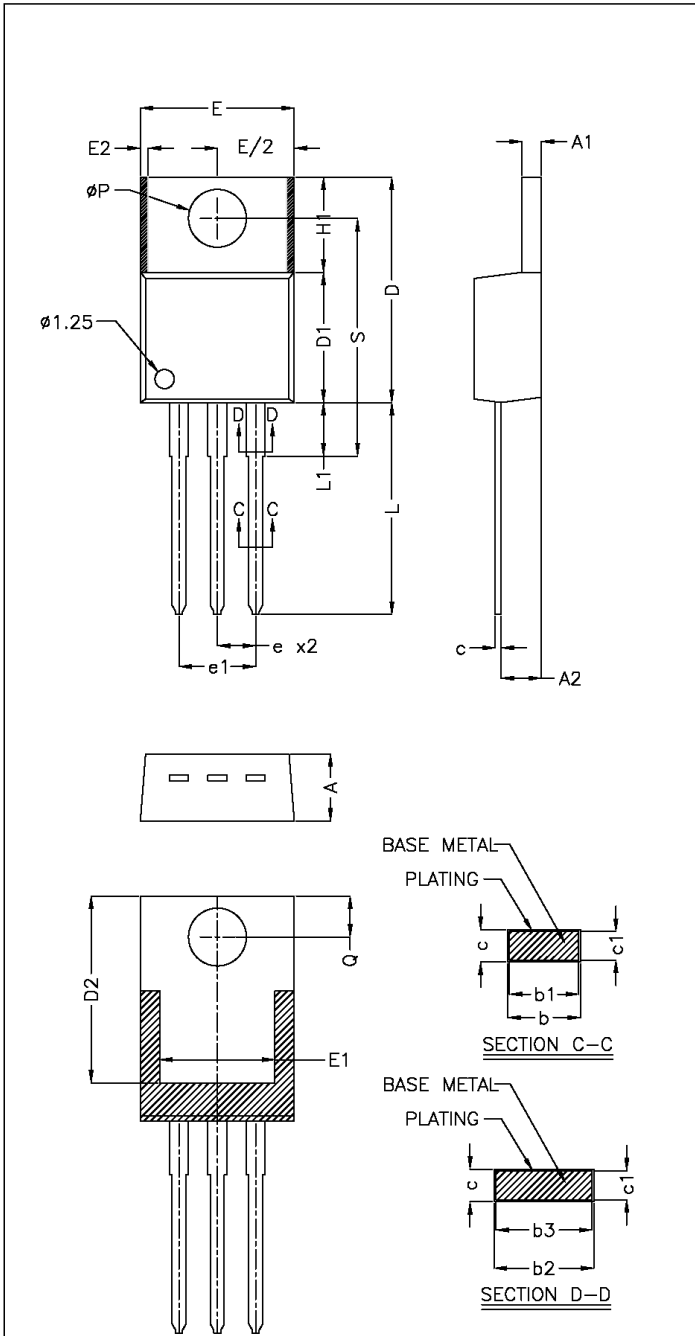
DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See Printed Circuit Board Layout and Probing	

GaN Design Resources

The complete technical library of GaN design tools can be found at [Renesasusa.com/design](https://www.renesas.com/design):

- Reference designs
- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

8x8 PQFN Package



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.29	4.45	4.73	0.169	0.175	0.186
A1	1.09	1.31	1.40	0.043	0.052	0.055
A2	2.48	2.64	2.93	0.098	0.104	0.115
b	0.77	0.86	1.02	0.031	0.034	0.040
b1	0.70	—	0.86	0.027	—	0.034
b2	1.23	1.33	1.43	0.048	0.052	0.057
b3	1.20	—	1.37	0.047	—	0.054
c	0.35	0.40	0.47	0.014	0.016	0.019
c1	0.35	—	0.43	0.014	—	0.017
D	14.78	14.95	15.75	0.581	0.589	0.620
D1	8.38	—	9.01	0.330	—	0.355
D2	12.19	—	12.88	0.480	—	0.507
E	9.96	10.25	10.36	0.392	0.404	0.408
E1	6.86	—	8.89	0.271	—	0.350
E2	—	—	0.76	—	—	0.030
e	2.54 BSC			0.100 BSC		
e1	5.08 BSC			0.200 BSC		
H1	6.10	6.37	6.60	0.241	0.251	0.260
L	12.70	13.84	14.27	0.500	0.545	0.562
L1	3.40	3.55	3.90	0.133	0.140	0.154
øP	3.72	3.80	3.88	0.146	0.150	0.153
Q	2.60	2.80	3.00	0.102	0.110	0.119
S	15.42	15.80	16.51	0.607	0.622	0.650

Notes:

1. Dimensions D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extreme of the plastic body.
2. Dimensions E2 and H1 define a zone where stamping and singulation irregularities are allowed.
3. Outline conforms to JEDEC TO-220AB.

TO-220AB			
transphorm			
SCALE	1:1	SHEET	1/1
DRAWING NO.	200014		VER.
			3

Mechanical