

TP65H150BG4JSG

650V SuperGaN® GaN FET in PQFN (source tab)

Description

The TP65H150BG4JSG 650V, 150mΩ Gallium Nitride (GaN) FET is a normally-off device using Renesas's Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

Related Literature

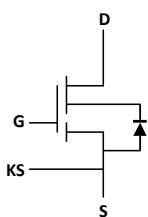
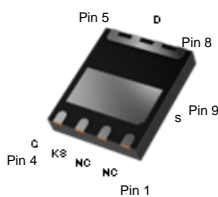
- [Printed Circuit Board Layout and Probing](#)
- [Recommendations for Vapor Phase Reflow](#)
- [Recommended External Circuitry for GaN FETs](#)
- [PQFN Tape and Reel Information](#)

Product Series and Ordering Information

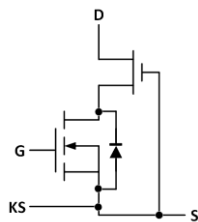
Part Number	Package	Package Configuration
TP65H150BG4JSG-TR	5x6 PQFN	Source

* "-TR" suffix refers to tape and reel. Refer to AN0012 for details.

TP65H150BG4JSG PQFN (bottom view)



Cascode Schematic Symbol



Cascode Device Structure

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
 - Wide gate safety margin
 - Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Benefits

- Achieves increased efficiency in both hard- and soft-switched circuits
 - Increased power density
 - Reduced system size and weight
 - Overall lower system cost
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting



Key Specifications

V_{DS} (V) min	650
$V_{DSS(TR)}$ (V) max	800
$R_{DS(on)}$ (mΩ) max*	180
Q_{oss} (nC) typ	35
Q_G (nC) typ	8.8

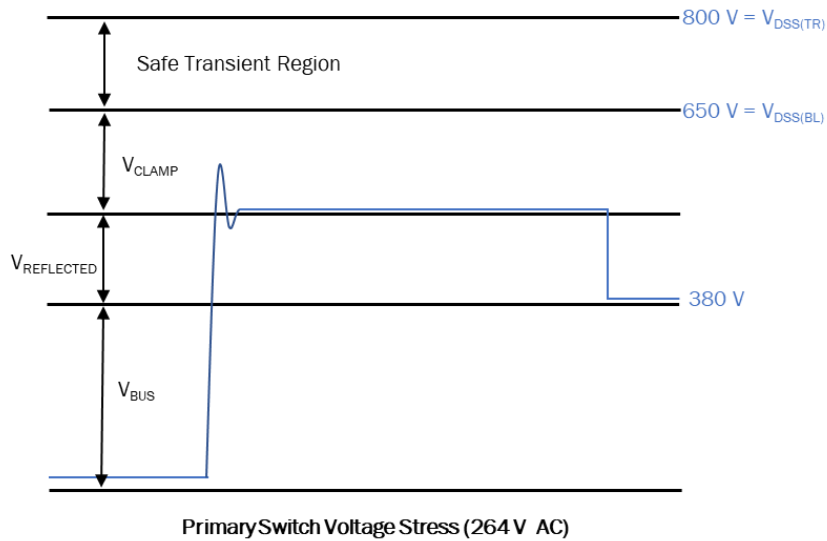
* Dynamic $R_{DS(on)}$; see Figures 18 and 19

Absolute Maximum Ratings ($T_c=25\text{ }^\circ\text{C}$ unless otherwise stated.)

Symbol	Parameter	Limit Value	Unit	
V_{DSS}	Drain to source voltage ($T_J = -55\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$)	650	V	
$V_{DSS(TR)}$	Transient drain to source voltage ^(a)	800		
V_{GSS}	Gate to source voltage	± 10		
P_D	Maximum power dissipation @ $T_c=25\text{ }^\circ\text{C}$	83	W	
I_D	Continuous drain current @ $T_c=25\text{ }^\circ\text{C}$ ^(b)	16	A	
	Continuous drain current @ $T_c=100\text{ }^\circ\text{C}$ ^(b)	10	A	
I_{DM}	Pulsed drain current (pulse width: $10\mu\text{s}$)	55	A	
T_c	Operating temperature	Case	-55 to $+150$	$^\circ\text{C}$
T_J		Junction	-55 to $+150$	$^\circ\text{C}$
T_s	Storage temperature	-55 to $+150$	$^\circ\text{C}$	
T_{SOLD}	Reflow soldering temperature ^(c)	260	$^\circ\text{C}$	

Notes:

- a. In off-state, spike duration < $30\mu\text{s}$, non-repetitive.
- b. For increased stability at high current operation, see Circuit Implementation on page 3
- c. Reflow MSL3



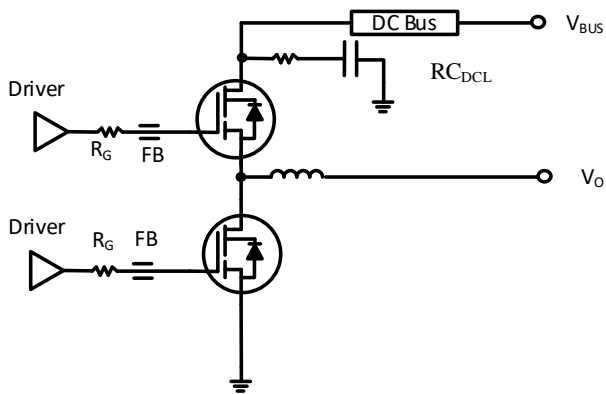
Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Junction-to-case	1.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient ^(d)	50	$^\circ\text{C}/\text{W}$

Notes:

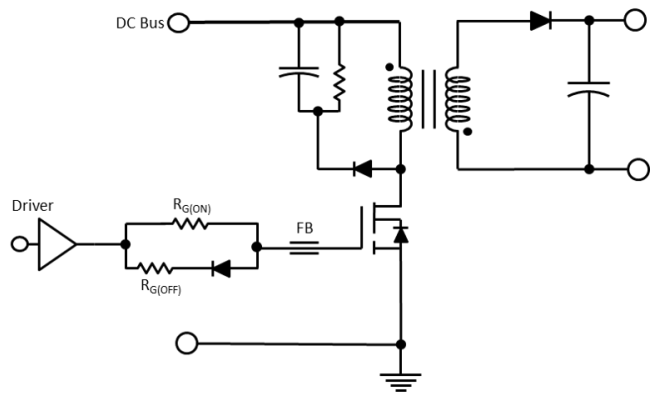
- d. Device on one layer epoxy PCB for source connection (vertical and without air stream cooling, with 6cm^2 copper area and $70\mu\text{m}$ thickness)

Circuit Implementation



Simplified Half-bridge Schematic

Recommended gate drive: (0V, 6V) with $R_{G(tot)} = 65 \Omega^e$



Simplified Single Ended Schematic

Recommended gate drive:

Gate drive: (0V, 6V): $R_{G(ON)} = 65$ to 150Ω ; $R_{G(OFF)} = 0$ to 10Ω

Gate drive*: (-6V, 6V): $R_{G(ON)} = 65$ to 100Ω ; $R_{G(OFF)} = 0$ to 20Ω

*Drop-in with discrete e-mode gate drive that level shifts any standard silicon MOSFET controller with integrated driver (i.e. NCP1342)

Gate Ferrite Bead (FB)	Required DC Link RC Snubber (RC_{DCL}) ^f
330 Ω @ 100MHz	10nF + 3.3 Ω

Notes:

e. For bridge topologies only. R_G could be much smaller in single ended topologies.

f. RC_{DCL} should be placed as close as possible to the drain pin.

Electrical Parameters ($T_J=25\text{ }^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{DSS(BL)}$	Maximum drain-source voltage	650	—	—	V	$V_{GS}=0V$
$V_{GS(th)}$	Gate threshold voltage	2	2.4	2.8	V	$V_{DS}=V_{GS}, I_D=0.5mA$
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	—	-5.8	—	mV/ $^\circ\text{C}$	
$R_{DS(on)eff}$	Drain-source on-resistance ^(g)	—	150	180	m Ω	$V_{GS}=6V, I_D=10A, T_J=25\text{ }^\circ\text{C}$
		—	307	—		$V_{GS}=6V, I_D=10A, T_J=150\text{ }^\circ\text{C}$
I_{DSS}	Drain-to-source leakage current	—	2.5	25	μA	$V_{DS}=650V, V_{GS}=0V, T_J=25\text{ }^\circ\text{C}$
		—	10	—		$V_{DS}=650V, V_{GS}=0V, T_J=150\text{ }^\circ\text{C}$
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	$V_{GS}=10V$
	Gate-to-source reverse leakage current	—	—	-100		$V_{GS}=-10V$
C_{ISS}	Input capacitance	—	400	—	pF	$V_{GS}=0V, V_{DS}=400V, f=1MHz$
C_{OSS}	Output capacitance	—	37	—		
C_{RSS}	Reverse transfer capacitance	—	1.2	—		
$C_{O(er)}$	Output capacitance, energy related ^(h)	—	50	—	pF	$V_{GS}=0V, V_{DS}=0V$ to 400V
$C_{O(tr)}$	Output capacitance, time related ⁽ⁱ⁾	—	88	—		
Q_G	Total gate charge	—	4.9	—	nC	$V_{DS}=400V, V_{GS}=0V$ to 10V, $I_D=10A$
Q_{GS}	Gate-source charge	—	1.6	—		
Q_{GD}	Gate-drain charge	—	0.8	—		
Q_{OSS}	Output charge	—	35	—	nC	$V_{GS}=0V, V_{DS}=0V$ to 400V
$t_{D(on)}$	Turn-on delay	—	24	—	ns	$V_{DS}=400V, V_{GS}=0V$ to 6V, $I_D=10A, R_G=65\Omega, Z_{FB}=330\Omega$ at 100MHz (See Figure 14)
t_R	Rise time	—	3.2	—		
$t_{D(off)}$	Turn-off delay	—	22	—		
t_F	Fall time	—	4	—		

Notes:

- g. Dynamic $R_{DS(on)}$, 100% tested; see Figures 18 and 19 for conditions
- h. Equivalent capacitance to give same stored energy from 0V to 400V
- i. Equivalent capacitance to give same charging time from 0V to 400V

Electrical Parameters ($T_J=25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	8.3	A	$V_{GS}=0V$, $T_C=100^\circ\text{C}$, $\leq 20\%$ duty cycle
V_{SD}	Reverse voltage ^(j)	—	1.7	—	V	$V_{GS}=0V$, $I_S=8.5A$
		—	1.2	—		$V_{GS}=0V$, $I_S=4.5A$
t_{RR}	Reverse recovery time	—	28.3	—	ns	$I_S=10A$, $V_{DD}=400V$, $di/dt=1000A/ms$
Q_{RR}	Reverse recovery charge ^(k)	—	0	—	nC	

Notes:

j. Includes dynamic $R_{DS(on)}$ effect

k. Excludes Q_{oss}

Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)

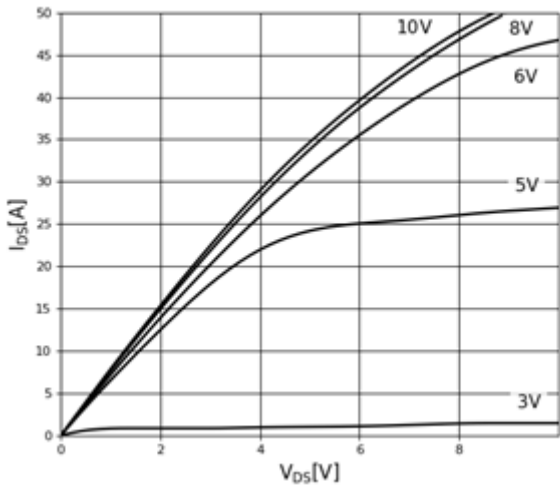


Figure 1. Typical Output Characteristics $T_J=25^\circ\text{C}$
Parameter: V_{GS}

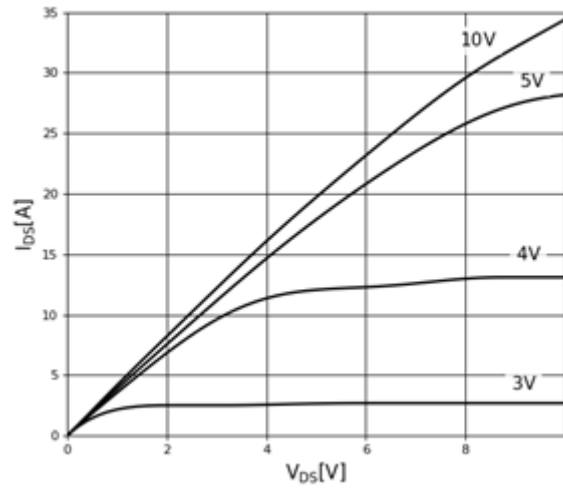


Figure 2. Typical Output Characteristics $T_J=150^\circ\text{C}$
Parameter: V_{GS}

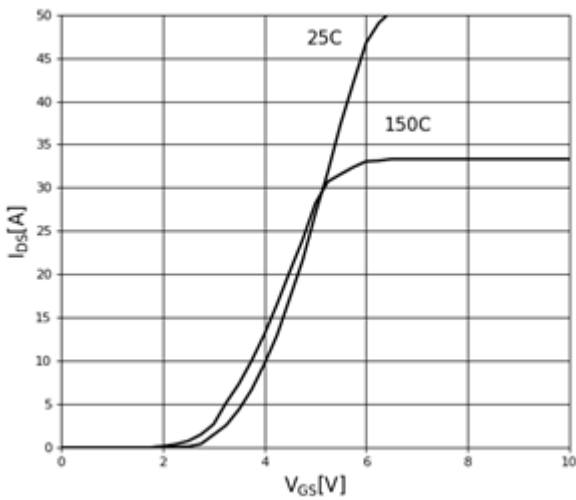


Figure 3. Typical Transfer Characteristics
 $V_{DS}=10\text{V}$, parameter: T_J

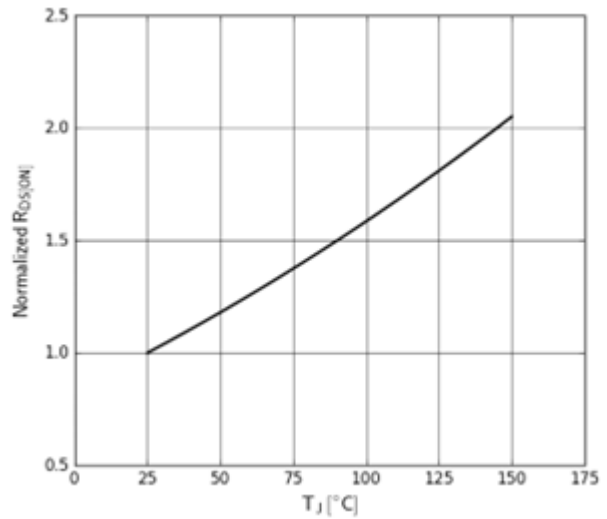


Figure 4. Normalized On-resistance
 $I_D=10\text{A}$, $V_{GS}=6\text{V}$

Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)

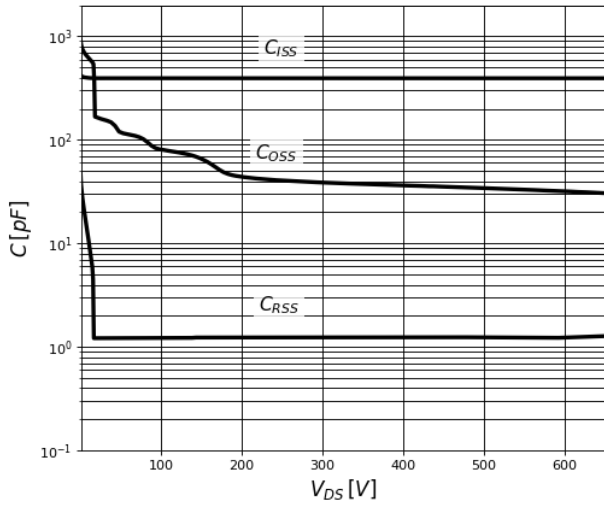


Figure 5. Typical Capacitance
 $V_{GS}=0V, f=1MHz$

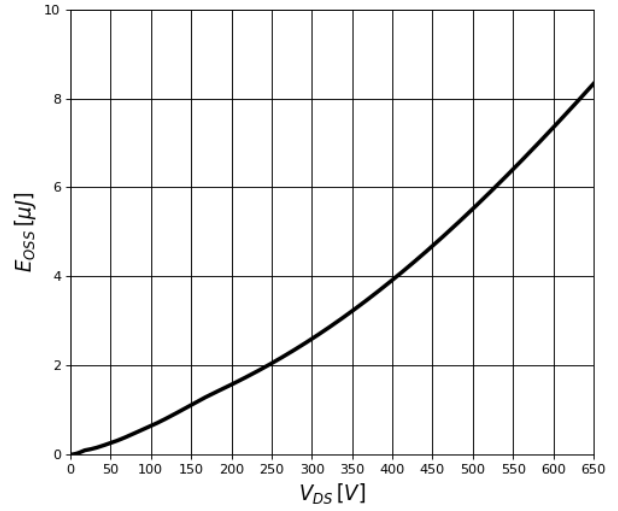


Figure 6. Typical C_{oss} Stored Energy

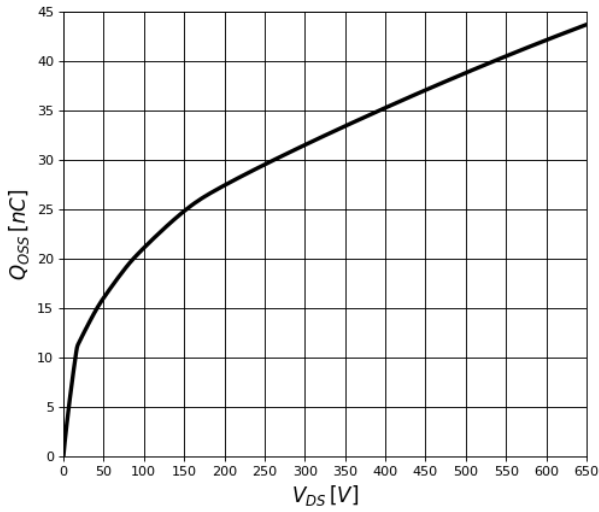


Figure 7. Typical Q_{oss}

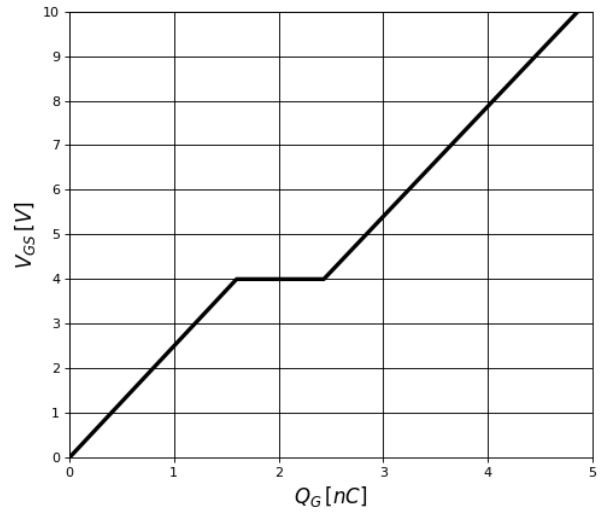


Figure 8. Typical Gate Charge
 $I_{DS}=10A, V_{DS}=400V$

Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)

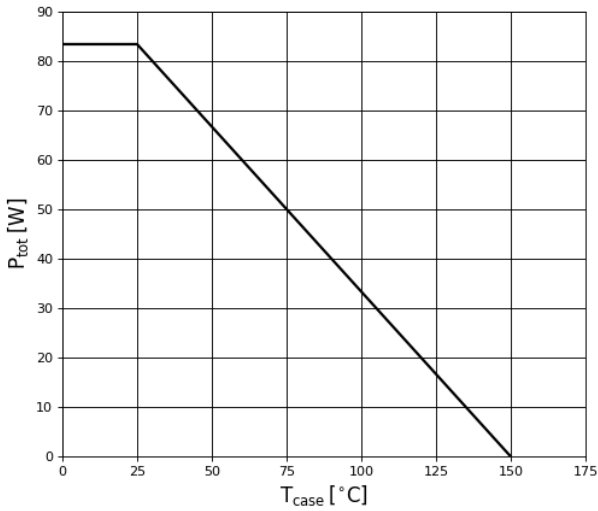


Figure 9. Power Dissipation

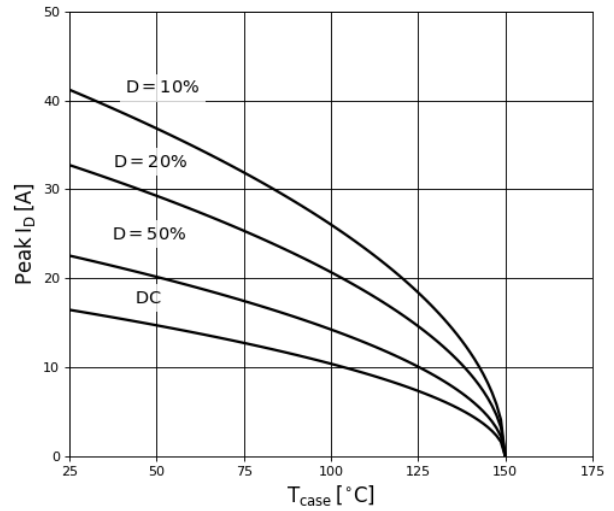


Figure 10. Current Derating

Pulse width $\leq 10\mu\text{s}$, $V_{\text{GS}} \geq 10\text{V}$

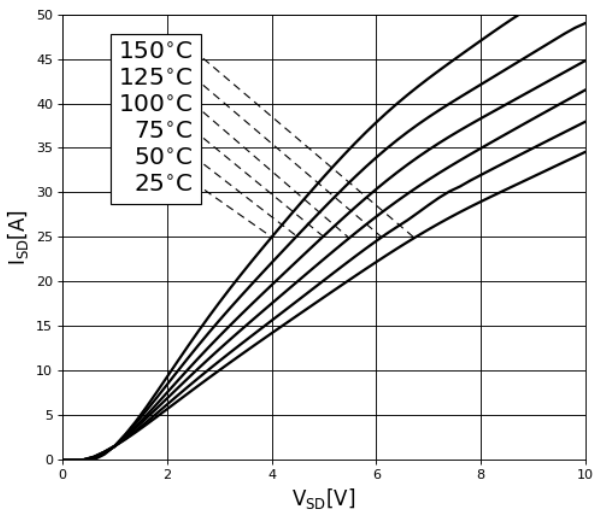


Figure 11. Forward Characteristics of Rev. Diode

$I_s=f(V_{\text{SD}})$, parameter: T_J

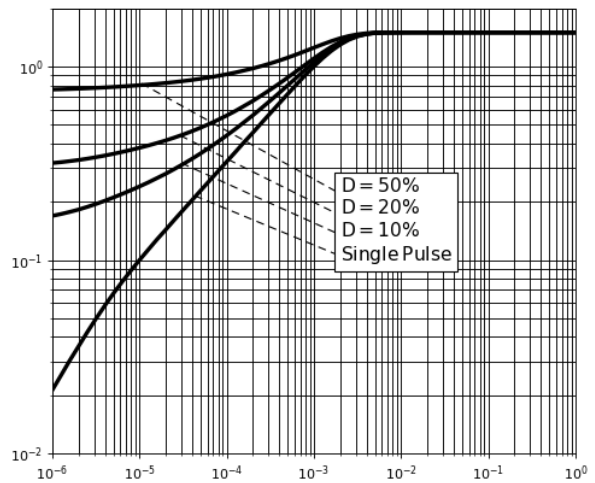


Figure 12. Transient Thermal Resistance

Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)

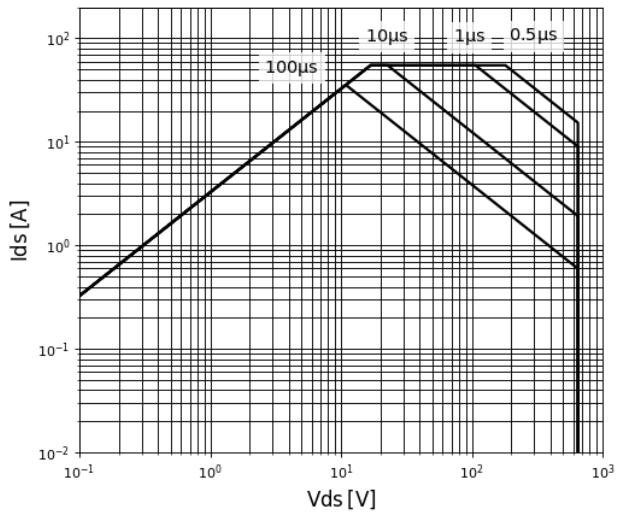


Figure 13. Safe Operating Area $T_c=25^\circ\text{C}$

Test Circuits and Waveforms

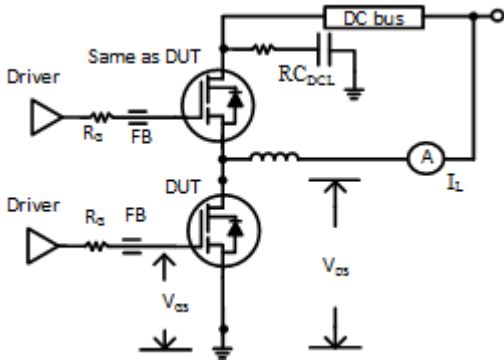


Figure 14. Switching Time Test Circuit

(see circuit implementation on page 3 for methods to ensure clean switching)

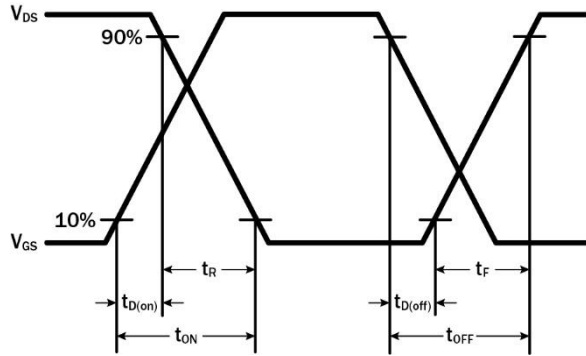


Figure 15. Switching Time Waveform

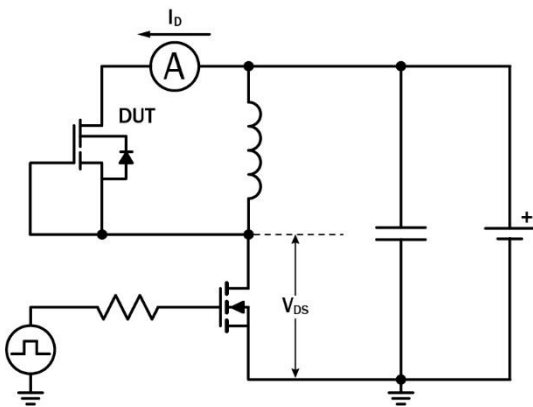


Figure 16. Diode Characteristics Test Circuit

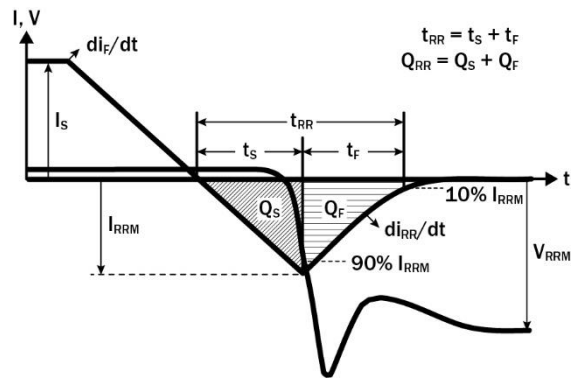


Figure 17. Diode Recovery Waveform

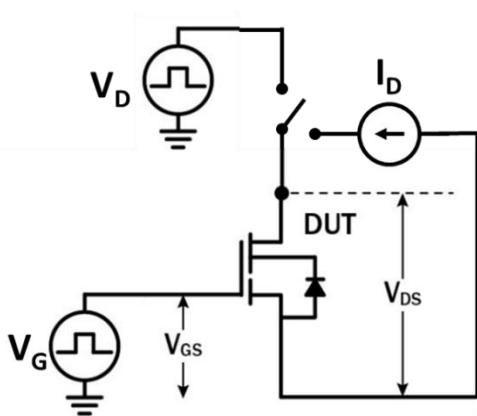


Figure 18. Dynamic $R_{DS(on)eff}$ Test Circuit

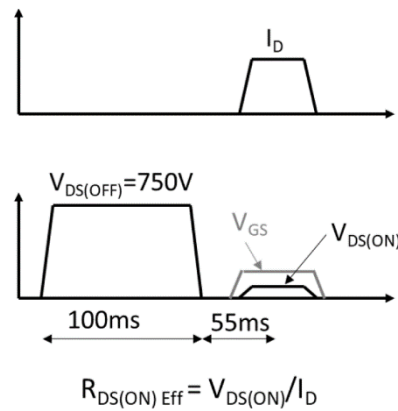


Figure 19. Dynamic $R_{DS(on)eff}$ Waveform

Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Renesas GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Renesas GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See Printed Circuit Board Layout and Probing	

GaN Design Resources

The complete technical library of GaN design tools can be found at [Renesasusa.com/design](https://www.renesas.com/design):

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

8x8 PQFN Package

Mechanical

