TW2828

HD/SD DVR Video Port Expander

FN8291
Rev. 1.00
March 27, 2013

TW2828 is a display and recording MUX chip with HD SPOT capability designed to work with popular H.264 CODEC on the market today. TW2828 provides a clean and cost effective MUX solution to the multi-channel PC HD DVR marketplace. On the embedded DVR market, using TW2828 in conjunction with a host SOC can deliver the most cost effective solution on the market.

Digital Input Ports

- Four byte interleaved BT.656 ports each supporting up to 4 SD (108 MHz) and 4 960H (144 MHz) signals for a total of 16 SD video input signals
- Five frame interleaved BT.1120 ports, each supporting up to 148.5 MHz for a total of 20 HD signals. One port (PB5) is shared with GPIO port
- Four frame interleaved BT.656 ports (shared with the lower half of the BT.1120 port), supporting up to 16 SD (or 960H) signals in frame/field interleaved format
- Supports input resizing, cutting and cropping
- Supports channel cascading

Display Controller

- Supports popular sizes such as: 1920x1080i50, i60, 1920x1080p50 or p60,720p50 and p60
- Max pixel clock: 148.5MHz
- Capable of displaying up to 36 SD Channels by using byte interleaved inputs and frame interleaved inputs
- Motion Box (MD) on all live channels
- Selectable Weave/2D de-interlacing method for video quality enhancement
- Up/down scaler for arbitrary windows size
- OSD display layer for title and channel ID
- Single Box Display for highlighting and Mouse/Cursor Overlay
- BT.1120 or digital RGB output interface
- Analog VGA output (shared with SPOT output)

Digital Output Port

- One BT. 1120 port to the backend chip
- Digital RGB output (shared with BT.1120 port)
- SPOT digital output (BT.656) through record (shared) pins with all the channels

SPOT and Record Interface

- Two SPOT port with Integrated DAC
- 1/4/9/16 format for each SD (or 960H) and HD channels
- Supports anti-rolling display
- Similar recording functions like TW2880

Motion Detection

- 16 SD/WD1 (960H) mode size 16x12
- 720p HD mode 40x36
- 1080i HD mode 60x27
- 1080p HD mode 60x54

DDR2 Interface

- Supports 16-bit DDR2 memories running up to 333MHz
- Supports DRAM density from 512Mb to 1Gb

Host Interface

- 8-bit parallel host interface or I^2C slave interface (shared pin)
- Four I^2C slave addresses on two separate pins for cascaded operation
- IRQs

Package

- 18mmx18mm 409 LFBGA

Ordering Information

PART NUMBER	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
TW2828-BA2-CR (Note 1)	TW2828 BA2-CR	409 Ball LFBGA	V409.18X18

NOTE:

1. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

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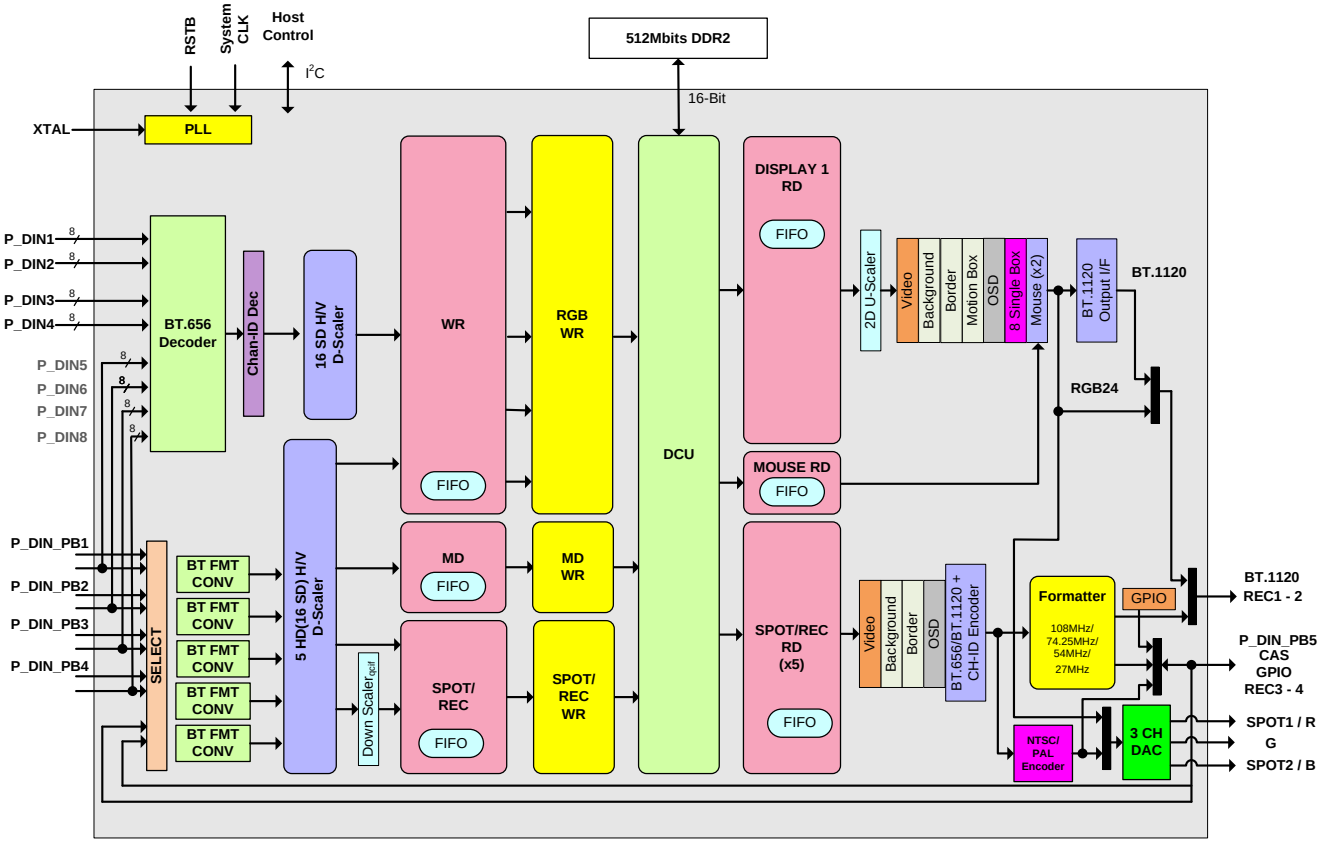
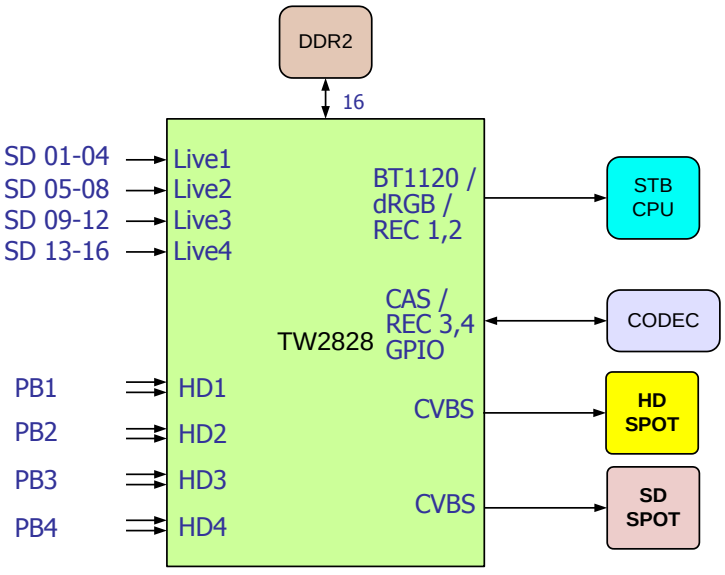
System Diagram





16SD + 4HD + 2SPOT Example

Pin Descriptions

(230 signal pins + 24 Analog VCC/GND + 149 VCC/GND + 6 NC = 409 balls)

TABLE 1. PIN DESCRIPTION OF DIGITAL VIDEO INPUT INTERFACE 1

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
L5	P_CKVIN1	I	Clock input for Digital Video Port 1
L4	P_DIN1_0	I	Port1 Video input bit 0
K3	P_DIN1_1	I	Port1 Video input bit 1
J2	P_DIN1_2	I	Port1 Video input bit 2
J1	P_DIN1_3	I	Port1 Video input bit 3
K2	P_DIN1_4	I	Port1 Video input bit 4
M4	P_DIN1_5	I	Port1 Video input bit 5
L3	P_DIN1_6	I	Port1 Video input bit 6
K1	P_DIN1_7	I	Port1 Video input bit 7
L2	P_CKVIN2	I	Clock input for Digital Video Port 2
M5	P_DIN2_0	I	Port2 Video input bit 0
M3	P_DIN2_1	I	Port2 Video input bit 1
N4	P_DIN2_2	I	Port2 Video input bit 2
M2	P_DIN2_3	I	Port2 Video input bit 3
N5	P_DIN2_4	I	Port2 Video input bit 4
M1	P_DIN2_5	I	Port2 Video input bit 5
N2	P_DIN2_6	I	Port2 Video input bit 6
N1	P_DIN2_7	I	Port2 Video input bit 7
P5	P_CKVIN3	I	Clock input for Digital Video Port 3
P3	P_DIN3_0	I	Port3 Video input bit 0

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
P4	P_DIN3_1	I	Port3 Video input bit 1
P1	P_DIN3_2	I	Port3 Video input bit 2
P2	P_DIN3_3	I	Port3 Video input bit 3
R3	P_DIN3_4	I	Port3 Video input bit 4
R4	P_DIN3_5	I	Port3 Video input bit 5
R2	P_DIN3_6	I	Port3 Video input bit 6
R5	P_DIN3_7	I	Port3 Video input bit 7
R1	P_CKVIN4	I	Clock input for Digital Video Port 4
T3	P_DIN4_0	I	Port4 Video input bit 0
T4	P_DIN4_1	I	Port4 Video input bit 1
U2	P_DIN4_2	I	Port4 Video input bit 2
U1	P_DIN4_3	I	Port4 Video input bit 3
V1	P_DIN4_4	I	Port4 Video input bit 4
U3	P_DIN4_5	I	Port4 Video input bit 5
V2	P_DIN4_6	I	Port4 Video input bit 6
T5	P_DIN4_7	I	Port4 Video input bit 7
U5	P_DIN_PB4_0	I	PB4 port bit 0
W1	P_DIN_PB4_1	I	PB4 port bit 1
V3	P_DIN_PB4_2	I	PB4 port bit 2
U6	P_DIN_PB4_3	I	PB4 port bit 3
W2	P_DIN_PB4_4	I	PB4 port bit 4
W3	P_DIN_PB4_5	I	PB4 port bit 5

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
V5	P_DIN_PB4_6	I	PB4 port bit 6
Y2	P_DIN_PB4_7	I	PB4 port bit 7
U7	P_CK27PB4	I	Clock input for PB port 4
V6	P_DIN_PB4_8	I	PB4 port bit 8 / Port5 Video input bit 0
W4	P_DIN_PB4_9	I	PB4 port bit 9 / Port5 Video input bit 1
W5	P_DIN_PB4_10	I	PB4 port bit 10 / Port5 Video input bit 2
AA2	P_DIN_PB4_11	I	PB4 port bit 11 / Port5 Video input bit 3
V7	P_DIN_PB4_12	I	PB4 port bit 12 / Port5 Video input bit 4
Y4	P_DIN_PB4_13	I	PB4 port bit 13 / Port5 Video input bit 5
U8	P_DIN_PB4_14	I	PB4 port bit 14 / Port5 Video input bit 6
W6	P_DIN_PB4_15	I	PB4 port bit 15 / Port5 Video input bit 7

TABLE 2. PIN DESCRIPTION OF DIGITAL VIDEO INPUT INTERFACE 2

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
AA3	P_DIN_PB1_0	I	PB1 port bit 0
Y5	P_DIN_PB1_1	I	PB1 port bit 1
AA4	P_DIN_PB1_2	I	PB1 port bit 2
W7	P_DIN_PB1_3	I	PB1 port bit 3
AA5	P_DIN_PB1_4	I	PB1 port bit 4
AA6	P_DIN_PB1_5	I	PB1 port bit 5
Y7	P_DIN_PB1_6	I	PB1 port bit 6
W8	P_DIN_PB1_7	I	PB1 port bit 7
V9	P_CK27PB1	I	Clock input for PB port 1

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
Y8	P_DIN_PB1_8	I	PB1 port bit 8 / Port6 Video input bit 0
W9	P_DIN_PB1_9	I	PB1 port bit 9 / Port6 Video input bit 1
U9	P_DIN_PB1_10	I	PB1 port bit 10 / Port6 Video input bit 2
AA8	P_DIN_PB1_11	I	PB1 port bit 11 / Port6 Video input bit 3
Y9	P_DIN_PB1_12	I	PB1 port bit 12 / Port6 Video input bit 4
V10	P_DIN_PB1_13	I	PB1 port bit 13 / Port6 Video input bit 5
AA9	P_DIN_PB1_14	I	PB1 port bit 14 / Port6 Video input bit 6
W10	P_DIN_PB1_15	I	PB1 port bit 15 / Port6 Video input bit 7
U10	P_DIN_PB2_0	I	PB2 port bit 0
AA10	P_DIN_PB2_1	I	PB2 port bit 1
U11	P_DIN_PB2_2	I	PB2 port bit 2
V11	P_DIN_PB2_3	I	PB2 port bit 3
W11	P_DIN_PB2_4	I	PB2 port bit 4
Y11	P_DIN_PB2_5	I	PB2 port bit 5
W12	P_DIN_PB2_6	I	PB2 port bit 6
V12	P_DIN_PB2_7	I	PB2 port bit 7
Y12	P_CK27PB2	I	Clock input for PB port 2
U12	P_DIN_PB2_8	I	PB2 port bit 8 / Port7 Video input bit 0
AA12	P_DIN_PB2_9	I	PB2 port bit 9 / Port7 Video input bit 1
AA13	P_DIN_PB2_10	I	PB2 port bit 10 / Port7 Video input bit 2
Y13	P_DIN_PB2_11	I	PB2 port bit 11 / Port7 Video input bit 3
W13	P_DIN_PB2_12	I	PB2 port bit 12 / Port7 Video input bit 4

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
AA14	P_DIN_PB2_13	I	PB2 port bit 13 / Port7 Video input bit 5
W14	P_DIN_PB2_14	I	PB2 port bit 14 / Port7 Video input bit 6
Y15	P_DIN_PB2_15	I	PB2 port bit 15 / Port7 Video input bit 7
U13	P_DIN_PB3_0	I	PB3 port bit 0
AA16	P_DIN_PB3_1	I	PB3 port bit 1
W15	P_DIN_PB3_2	I	PB3 port bit 2
V14	P_DIN_PB3_3	I	PB3 port bit 3
Y16	P_DIN_PB3_4	I	PB3 port bit 4
AA17	P_DIN_PB3_5	I	PB3 port bit 5
U14	P_DIN_PB3_6	I	PB3 port bit 6
V15	P_DIN_PB3_7	I	PB3 port bit 7
W16	P_CK27PB3	I	Clock input for PB port 3
U15	P_DIN_PB3_8	I	PB3 port bit 8 / Port8 Video input bit 0
AA18	P_DIN_PB3_9	I	PB3 port bit 9 / Port8 Video input bit 1
Y17	P_DIN_PB3_10	I	PB3 port bit 10 / Por8 Video input bit 2
Y18	P_DIN_PB3_11	I	PB3 port bit 11 / Port8 Video input bit 3
V16	P_DIN_PB3_12	I	PB3 port bit 12 / Port8 Video input bit 4
W18	P_DIN_PB3_13	I	PB3 port bit 13 / Port8 Video input bit 5
Y19	P_DIN_PB3_14	I	PB3 port bit 14 / Port8 Video input bit 6
V17	P_DIN_PB3_15	I	PB3 port bit 15 / Port8 Video input bit 7

TABLE 3. PIN DESCRIPTION OF XTAL INPUT INTERFACE

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
A21	P_XTAL_IN	I	Crystal Input
A20	P_XTAL_OUT	O	Crystal Output

TABLE 4. PIN DESCRIPTION OF RECORD PORT INTERFACE

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
A13	P_REC_DATA_0	O	REC Port 1 bit 0 / Display Y0 / Display G0
E11	P_REC_DATA_1	O	REC Port 1 bit 1 / Display Y1 / Display G1
D10	P_REC_DATA_2	O	REC Port 1 bit 2 / Display Y2 / Display G2
C11	P_REC_DATA_3	O	REC Port 1 bit 3 / Display Y3 / Display G3
B12	P_REC_DATA_4	O	REC Port 1 bit 4 / Display Y4 / Display G4
C10	P_REC_DATA_5	O	REC Port 1 bit 5 / Display Y5 / Display G5
D9	P_REC_DATA_6	O	REC Port 1 bit 6 / Display Y6 / Display G6
E10	P_REC_DATA_7	O	REC Port 1 bit 7 / Display Y7 / Display G7
A11	P_REC_CLK_LP	O	Clock output for REC port 1(positive phase) / BT.1120 display clock
A10	P_REC_CLK_LN	O	Clock output for REC port 1(negative phase)
E9	P_REC_DATA_8	O	REC Port 2 bit 0 / Display C0 / Display R0
B10	P_REC_DATA_9	O	REC Port 2 bit 1 / Display C1 / Display R1
C9	P_REC_DATA_10	O	REC Port 2 bit 2 / Display C2 / Display R2
B9	P_REC_DATA_11	O	REC Port 2 bit 3 / Display C3 / Display R3
A9	P_REC_DATA_12	O	REC Port 2 bit 4 / Display C4 / Display R4
D8	P_REC_DATA_13	O	REC Port 2 bit 5 / Display C5 / Display R5
C8	P_REC_DATA_14	O	REC Port 2 bit 6 / Display C6 / Display R6
B8	P_REC_DATA_15	O	REC Port 2 bit 7 / Display C7 / Display R7

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
A7	P_REC_CLK_HP	O	Clock output for record port2(positive phase) /Display HSync for VGA
A6	P_REC_CLK_HN	O	Clock output for record port2(negative phase) /Display VSync for VGA

TABLE 5. PIN DESCRIPTION OF GPIO INTERFACE

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
E3	P_GPIO_0	B	REC Port 3 bit 0 / PB5 bit 0 / GPIO0 / Display B0 / Cascade Y0
H5	P_GPIO_1	B	REC Port 3 bit 1 / PB5 bit 1 / GPIO1 / Display B1 / Cascade Y1
D2	P_GPIO_2	B	REC Port 3 bit 2 / PB5 bit 2 / GPIO2 / Display B2 / Cascade Y2
F3	P_GPIO_3	B	REC Port 3 bit 3 / PB5 bit 3 / GPIO3 / Display B3 / Cascade Y3
C1	P_GPIO_4	B	REC Port 3 bit 4 / PB5 bit 4 / GPIO4 / Display B4 / Cascade Y4
H4	P_GPIO_5	B	REC Port 3 bit 5 / PB5 bit 5 / GPIO5 / Display B5 / Cascade Y5
E2	P_GPIO_6	B	REC Port 3 bit 6 / PB5 bit 6 / GPIO6 / Display B6 / Cascade Y6
J5	P_GPIO_7	B	REC Port 3 bit 7 / PB5 bit 7 / GPIO7 / Display B7 / Cascade Y7
E1	P_GCLK1P	B	Clock output for REC port 3, positive phase
F1	P_GCLK1N	B	Clock output for REC port 3, negative phase
G3	P_GPIO_8	B	REC Port 4 bit 0 / PB5 bit 8 / GPIO8 / Display DE / Cascade C0
J4	P_GPIO_9	B	REC Port 4 bit 1 / PB5 bit 9 / GPIO9 / Display CLK / Cascade C1
H3	P_GPIO_10	B	REC Port 4 bit 2 / PB5 bit 10 / GPIO10 / Display HS / Cascade C2
K5	P_GPIO_11	B	REC Port 4 bit 3 / PB5 bit 11 / GPIO11 / Display VS / Cascade C3
G2	P_GPIO_12	B	REC Port 4 bit 4 / PB5 bit 12 / GPIO12 / Cascade C4
J3	P_GPIO_13	B	REC Port 4 bit 5 / PB5 bit 13 / GPIO13 / Cascade C5
K4	P_GPIO_14	B	REC Port 4 bit 6 / PB5 bit 14 / GPIO14 / Cascade C6
G1	P_GPIO_15	B	REC Port 4 bit 7 / PB5 bit 15 / GPIO15 / Cascade C7

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
H2	P_GCLK2P	O	Clock output for REC port 4, positive phase
H1	P_GCLK2N	O	Clock output for REC port 4, negative phase

TABLE 6. PIN DESCRIPTION OF MISC. INTERFACE

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
E7	P_EXT_CLKO	O	Output clock to Video decoder chip.
B6	P_TEST_ENA1	I	Set to one to enable test mode, normal operation tie to ground
D7	P_TEST_ENA2	I	Set to one to enable test mode, normal operation tie to ground
A5	P_RSTB	I	Chip reset when it is LOW
C6	P_I2C_SID1	I	Select alternate I²C address pin bit 1
B4	P_I2C_SID2	I	Select alternate I²C address pin bit 2
C5	P_HSPB	I	I²C Interface when this bit is HIGH, 8bits parallel interface when this bit is LOW.

TABLE 7. PIN DESCRIPTION OF HOST PORT INTERFACE

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
E15	P_IRQ_OUT	O	Interrupt to the host
D14	P_HCSB	I	Chip select in parallel interface/I²C Clock in serial interface
C17	P_HWRB	I	Host write in parallel interface
C16	P_HRDB	I	Host read in parallel interface
E14	P_HADDR_0	I	Host address bit 0
B18	P_HADDR_1	I	Host address bit 1
A19	P_HADDR_2	I	Host address bit 2
B17	P_HADDR_3	I	Host address bit 3
E13	P_HADDR_4	I	Host address bit 4

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
C15	P_HADDR_5	I	Host address bit 5
D13	P_HADDR_6	I	Host address bit 6
A18	P_HADDR_7	I	Host address bit 7
B16	P_HADDR_8	I	Host address bit 8
D12	P_HADDR_9	I	Host address bit 9
A17	P_HADDR_10	I	Host address bit 10
B15	P_HADDR_11	I	Host address bit 11
C13	P_HDAT_0	B	Host data bit 0
A16	P_HDAT_1	B	Host data bit 1
B14	P_HDAT_2	B	Host data bit 2
E12	P_HDAT_3	B	Host data bit 3
D11	P_HDAT_4	B	Host data bit 4
C12	P_HDAT_5	B	Host data bit 5
B13	P_HDAT_6	B	Host data bit 6
A14	P_HDAT_7	B	Host data bit 7/I²C Data in serial interface (open drian)

TABLE 8. PIN DESCRIPTION OF SPOT PORT INTERFACE

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
F5	P_SPOT2_CVBS / P_VGA_B	O	SPOT2 Analog composite TV signal / Analog Blue signal for VGA
D4	P_SPOT1_CVBS / P_VGA_R	O	SPOT1 Analog composite TV signal / Analog Red signal for VGA
D5	P_VGA_G	O	Analog Green signal for VGA
A2	P_SPOT_COMP	O	Compensation pin for AHVDD. This pin should be connected through a 0.01µF ceramic capacitor and parallel with a 10µF tantalum capacitor to AHVDD externally.
D3	P_SPOT_RSET	I/O	A resistor connecting this pin to AHVSS will determine full scale output current.
F4	P_SPOT_VREF	I	1.183V Reference voltage input pin. Also connect with a 0.1 uF ceramic capacitor to AHVSS pin.

TABLE 9. PIN DESCRIPTION OF DRAM INTERFACE

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
U21	DDRA_ADDR0	O	DRAM address bit 0
R19	DDRA_ADDR1	O	DRAM address bit 1
P18	DDRA_ADDR2	O	DRAM address bit 2
T20	DDRA_ADDR3	O	DRAM address bit 3
T21	DDRA_ADDR4	O	DRAM address bit 4
R20	DDRA_ADDR5	O	DRAM address bit 5
P19	DDRA_ADDR6	O	DRAM address bit 6
R21	DDRA_ADDR7	O	DRAM address bit 7
N18	DDRA_ADDR8	O	DRAM address bit 8
P20	DDRA_ADDR9	O	DRAM address bit 9
N19	DDRA_ADDR10	O	DRAM address bit 10
M18	DDRA_ADDR11	O	DRAM address bit 11
P21	DDRA_ADDR12	O	DRAM address bit 12

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
W21	DDRA_CLK	O	DRAM clock
V21	DDRA_CLKN	O	DRAM clockn
P17	DDRA_BA0	O	DRAM bank address 0
R17	DDRA_BA1	O	DRAM bank address 1
T19	DDRA_BA2	O	DRAM bank address 2
T18	DDRA_RASN	O	DRAM control RASN
V19	DDRA_CASN	O	DRAM control CASN
W20	DDRA_WEN	O	DRAM control WEN
V18	DDRA_CKE	O	DRAM control CKE
W19	DDRA_ODT	O	DRAM control ODT
N20	DDRA_DQ0	B	DRAM data bit 0
N21	DDRA_DQ1	B	DRAM data bit 1
M20	DDRA_DQ2	B	DRAM data bit 2
M21	DDRA_DQ3	B	DRAM data bit 3
K21	DDRA_DQS0	B	DRAM DQS bit 0
K20	DDRA_DQSN0	B	DRAM DQSN bit 0
L21	DDRA_DM0	B	DRAM DM bit 0
J21	DDRA_DQ4	B	DRAM data bit 4
J20	DDRA_DQ5	B	DRAM data bit 5
H21	DDRA_DQ6	B	DRAM data bit 6
H20	DDRA_DQ7	B	DRAM data bit 7
J18	DDRA_FWI	I	DRAM FWI
K17	DDRA_FWO	O	DRAM FWO
G21	DDRA_DQ8	B	DRAM data bit 8
G20	DDRA_DQ9	B	DRAM data bit 9

PIN(S) NO.	SYMBOL	ATTRIBUTE	DESCRIPTION
F20	DDRA_DQ10	B	DRAM data bit 10
F21	DDRA_DQ11	B	DRAM data bit 11
D21	DDRA_DQS1	B	DRAM DQS bit 1
D20	DDRA_DQSN1	B	DRAM DQSN bit 1
E21	DDRA_DM1	B	DRAM DM bit 1
C21	DDRA_DQ12	B	DRAM data bit 12
C20	DDRA_DQ13	B	DRAM data bit 13
B21	DDRA_DQ14	B	DRAM data bit 14
B20	DDRA_DQ15	B	DRAM data bit 15

TABLE 10. PIN DESCRIPTION OF POWER AND GROUND

SYMBOL	PIN(S) NO.	VOLTAGE	DESCRIPTION
DVDI	F8, F14, H8, H9, H10, H11, H12, H13, K8, L10, L11, L12, M8, N6, P9, P11, P13, T6, T8, T10, T12, T14	1.0 Volts	Power of the core logic
DVDE	A4, A8, A12, A15, AA7, AA11, AA15, AA20, B1, B19, D1, E4, E8, E17, F10, F12, L6, T1, U4, W17, Y1	3.3 Volts	Power of the external I/O
DVDSS	A1, AA1, AA19, B5, B7, B11, C14, D6, F2, F9, F11, F13, F15, G4, G18, H6, J8, J9, J10, J11, J12, K6, K9, K10, K11, K12, L1, L8, L9, M6, M9, M10, M11, M12, N3, N8, N9, N10, N11, N12, P8, P10, P12, R6, R18, T2, T7, T9, T11, T13, T15, U16, V4, V8, V13, Y6, Y10, Y14	-	Digital Ground
VDDPSSTL	G16, G19, K19, L18, L19, M19, N16, U18, V20	1.8 Volts	1.8V for SSTL
VSSPSSTL	E20, H14, H18, J13, J16, K13, K14, L13, L20, M13, M14, N13, P14, P16, U17, U20	-	Ground for SSTL
VDDSSTL	H16, H17, J14, L14, L16, M16, N14, R16, T16	1.0 Volts	1.0V for DDR2 PHY
VSSSSTL	Y21, Y20, T17, N17, L17, K18, K16, F19, U19	-	Ground for SSTL
VREFSSTL	M17, J17, F18	0.9 Volts	Reference Voltage for DDR2
VSSRSSTL	J19, G17	-	Ground for Reference Voltage
AHVDDR	B3	3.3 Volts	Analog power of DAC for SPOT1 or R
AHVSSR	C3	-	Analog ground of DAC for SPOT1 or R
AHVDDB	E6	3.3 Volts	Analog power of DAC for SPOT2 or B
AHVSSB	E5	-	Analog ground of DAC for SPOT2 or B
AHVDDG	A3	3.3 Volts	Analog power of DAC for G
AHVSSG	C4	-	Analog ground of DAC for G
AHVDD	C2	3.3V	Analog power of Band gap
AHVSS	B2	-	Analog ground of Band gap
DHVDD	F6	3.3V	Digital IO power of DAC

SYMBOL	PIN(S) NO.	VOLTAGE	DESCRIPTION
DHVSS	F7	-	Digital IO ground of DAC
DVDD	G6	1.0V	Digital internal power of DAC
DVSS	J6	-	Digital ground of DAC
MPLL_AVSS	F17	-	Analog ground of the MCK PLL
MPLL_DVSS	E19	-	Digital ground of the MCK PLL
MPLL_AVDD	E16	1.0 Volts	Analog power of the MCK PLL
MPLL_DVDD	E18	1.0 Volts	Digital power of the MCK PLL
VPLL_AVSS	D18	-	Analog ground of the VCK PLL
VPLL_DVSS	D19	-	Digital ground of the VCK PLL
VPLL_AVDD	D16	1.0 Volts	Analog power of the VCK PLL
VPLL_DVDD	D17	1.0 Volts	Digital power of the VCK PLL
SPLL_AVSS	F16	-	Analog ground of the SCK PLL
SPLL_DVSS	C19	-	Digital ground of the SCK PLL
SPLL_AVDD	C18	1.0 Volts	Analog power of the SCK PLL
SPLL_DVDD	D15	1.0 Volts	Digital power of the SCK PLL
NC	AA21, C7, G5, H19, P6, Y3	-	No Connect

TABLE 11. DIFFERENT FUNCTIONS OF THE TW2828

	Configuration 1	Configuration 2	Configuration 3	Configuration 4
P_rec_data[7]	Display BT.1120 Y[7]	Display Green Data[7]	Display BT.1120 Y[7]	REC1 data[7]
P_rec_data[6]	Display BT.1120 Y[6]	Display Green Data[6]	Display BT.1120 Y[6]	REC1 data[6]
P_rec_data[5]	Display BT.1120 Y[5]	Display Green Data[5]	Display BT.1120 Y[5]	REC1 data[5]
P_rec_data[4]	Display BT.1120 Y[4]	Display Green Data[4]	Display BT.1120 Y[4]	REC1 data[4]
P_rec_data[3]	Display BT.1120 Y[3]	Display Green Data[3]	Display BT.1120 Y[3]	REC1 data[3]
P_rec_data[2]	Display BT.1120 Y[2]	Display Green Data[2]	Display BT.1120 Y[2]	REC1 data[2]
P_rec_data[1]	Display BT.1120 Y[1]	Display Green Data[1]	Display BT.1120 Y[1]	REC1 data[1]
P_rec_data[0]	Display BT.1120 Y[0]	Display Green Data[0]	Display BT.1120 Y[0]	REC1 data[0]
P_rec_clk1_lp	Display BT.1120 Clock		Display BT.1120 Clock	REC1 Clock Positive
P_rec_clk1_ln				REC1 Clock Negative
P_rec_data[15]	Display BT.1120 C[7]	Display Red Data[7]	Display BT.1120 C[7]	REC2 data[7]
P_rec_data[14]	Display BT.1120 C[6]	Display Red Data[6]	Display BT.1120 C[6]	REC2 data[6]
P_rec_data[13]	Display BT.1120 C[5]	Display Red Data[5]	Display BT.1120 C[5]	REC2 data[5]
P_rec_data[12]	Display BT.1120 C[4]	Display Red Data[4]	Display BT.1120 C[4]	REC2 data[4]
P_rec_data[11]	Display BT.1120 C[3]	Display Red Data[3]	Display BT.1120 C[3]	REC2 data[3]
P_rec_data[10]	Display BT.1120 C[2]	Display Red Data[2]	Display BT.1120 C[2]	REC2 data[2]
P_rec_data[9]	Display BT.1120 C[1]	Display Red Data[1]	Display BT.1120 C[1]	REC2 data[1]
P_rec_data[8]	Display BT.1120 C[0]	Display Red Data[0]	Display BT.1120 C[0]	REC2 data[0]
P_rec_clk2_lp	**Display Hsync**			REC2 Clock Positive
P_rec_clk2_ln	**Display Vsync**			REC2 Clock Negative
Setting	0x201[2] = 0 0x21F[7] = 0	0x201[2] = 1 0x21F[7] = 0	0x201[2] = 0 0x21F[7] = 0	0x21F[7] = 1
P_GPIO[7]	Cascade BT.1120 Y[7]	Display Blue Data[7]	GPIO[7]	REC3 data[7]
P_GPIO[6]	Cascade BT.1120 Y[6]	Display Blue Data[6]	GPIO[6]	REC3 data[6]
P_GPIO[5]	Cascade BT.1120 Y[5]	Display Blue Data[5]	GPIO[5]	REC3 data[5]
P_GPIO[4]	Cascade BT.1120 Y[4]	Display Blue Data[4]	GPIO[4]	REC3 data[4]
P_GPIO[3]	Cascade BT.1120 Y[3]	Display Blue Data[3]	GPIO[3]	REC3 data[3]
P_GPIO[2]	Cascade BT.1120 Y[2]	Display Blue Data[2]	GPIO[2]	REC3 data[2]
P_GPIO[1]	Cascade BT.1120 Y[1]	Display Blue Data[1]	GPIO[1]	REC3 data[1]
P_GPIO[0]	Cascade BT.1120 Y[0]	Display Blue Data[0]	GPIO[0]	REC3 data[0]
P_GCLK1p	Cascade BT.1120 Clock Input			REC3 Clock Positive
P_GCLK1n				REC3 Clock Negative
P_GPIO[15]	Cascade BT.1120 C[7]		GPIO[15]	REC4 data[7]
P_GPIO[14]	Cascade BT.1120 C[6]		GPIO[14]	REC4 data[6]
P_GPIO[13]	Cascade BT.1120 C[5]		GPIO[13]	REC4 data[5]
P_GPIO[12]	Cascade BT.1120 C[4]		GPIO[12]	REC4 data[4]
P_GPIO[11]	Cascade BT.1120 C[3]	Display Vsync	GPIO[11]	REC4 data[3]
P_GPIO[10]	Cascade BT.1120 C[2]	Display Hsync	GPIO[10]	REC4 data[2]
P_GPIO[9]	Cascade BT.1120 C[1]	Display Pixel Clock	GPIO[9]	REC4 data[1]
P_GPIO[8]	Cascade BT.1120 C[0]	Display DE	GPIO[8]	REC4 data[0]
P_GCLK2p				REC4 Clock Positive
P_GCLK2n				REC4 Clock Negative
Setting	0x21F[6:5] = 0; 0x24C[7:0] = 0; 0x24D[7:0] = 0	0x21F[6:5] = 0; 0x24C[7:0] = FF; 0x24D[7:0] = FF	0x21F[6:5] = 0; 0x24C[7:0] = FF; 0x24D[7:0] = FF	0x21F[6:5] = 3; 0x24C[7:0] = FF; 0x24D[7:0] = FF

Pin Configurations

TW2828 Pin Assignment(Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	DVDSS	P_SPOT_COMP	AHVDDG	DVDE	P_RSTB	P_REC_CLK_HN	P_REC_CLK_HP	DVDE	P_REC_DATA_12	P_REC_CLK_LN	P_REC_CLK_LP	DVDE	P_REC_DATA_0	P_HDAT_7	DVDE	P_HDAT_1	P_HADDR_10	P_HADDR_7	P_HADDR_2	P_XTAL_OUT	P_XTAL_IN	A
B	DVDE	AHVSS	AHVDDR	P_I2C_SID2	DVDSS	P_TEST_ENA1	DVDSS	P_REC_DATA_15	P_REC_DATA_11	P_REC_DATA_9	DVDSS	P_REC_DATA_4	P_HDAT_6	P_HDAT_2	P_HADDR_11	P_HADDR_8	P_HADDR_3	P_HADDR_1	DVDE	DDRA_DQ15	DDRA_DQ14	B
C	P_GPIO_4	AHVDD	AHVSSR	AHVSSG	P_HSPB	P_I2C_SID1	NC	P_REC_DATA_14	P_REC_DATA_10	P_REC_DATA_5	P_REC_DATA_3	P_HDAT_5	P_HDAT_0	DVDSS	P_HADDR_5	P_HRDB	P_HWRB	SPLL_AVDD	SPLL_DVSS	DDRA_DQ13	DDRA_DQ12	C
D	DVDE	P_GPIO_2	P_SPOT_RSET	P_SPOT1_CVBS	P_VGA_G	DVDSS	P_TEST_ENA2	P_REC_DATA_13	P_REC_DATA_6	P_REC_DATA_2	P_HDAT_4	P_HADDR_9	P_HADDR_6	P_HCSB	SPLL_DVDD	VPLL_AVDD	VPLL_DVDD	VPLL_AVSS	VPLL_DVSS	DDRA_DQSN1	DDRA_DQS1	D
E	P_GCLK1P	P_GPIO_6	P_GPIO_0	DVDE	AHVSSB	AHVDDB	P_EXT_CLKO	DVDE	P_REC_DATA_8	P_REC_DATA_7	P_REC_DATA_1	P_HDAT_3	P_HADDR_4	P_HADDR_0	P_IRQ_OUT	MPLL_AVDD	DVDE	MPLL_DVDD	MPLL_DVSS	VSSPSSTL	DDRA_DM1	E
F	P_GCLK1N	DVDSS	P_GPIO_3	P_SPOT_VREF	P_SPOT2_CVBS	DHVDD	DHVSS	DVDI	DVDSS	DVDE	DVDSS	DVDE	DVDSS	DVDI	DVDSS	SPLL_AVSS	MPLL_AVSS	VREFSSTL	VSSSSTL	DDRA_DQ10	DDRA_DQ11	F
G	P_GPIO_15	P_GPIO_12	P_GPIO_8	DVDSS	NC	DVDD										VDDPSSTL	VSSRSSTL	DVDSS	VDDPSSTL	DDRA_DQ9	DDRA_DQ8	G
H	P_GCLK2N	P_GCLK2P	P_GPIO_10	P_GPIO_5	P_GPIO_1	DVDSS		DVDI	DVDI	DVDI	DVDI	DVDI	DVDI	VSSPSSTL		VDDSSTL	VDDSSTL	VSSPSSTL	NC	DDRA_DQ7	DDRA_DQ6	H
J	P_DIN1_3	P_DIN1_2	P_GPIO_13	P_GPIO_9	P_GPIO_7	DVSS		DVDSS	DVDSS	DVDSS	DVDSS	DVDSS	VSSPSSTL	VDDSSTL		VSSPSSTL	VREFSSTL	DDRA_FWI	VSSRSSTL	DDRA_DQ5	DDRA_DQ4	J
K	P_DIN1_7	P_DIN1_4	P_DIN1_1	P_GPIO_14	P_GPIO_11	DVDSS		DVDI	DVDSS	DVDSS	DVDSS	DVDSS	VSSPSSTL	VSSPSSTL		VSSSSTL	DDRA_FWO	VSSSSTL	VDDPSSTL	DDRA_DQSN0	DDRA_DQS0	K
L	DVDSS	P_CKVIN2	P_DIN1_6	P_DIN1_0	P_CKVIN1	DVDE		DVDSS	DVDSS	DVDI	DVDI	DVDI	VSSPSSTL	VDDSSTL		VDDSSTL	VSSSSTL	VDDPSSTL	VDDPSSTL	VSSPSSTL	DDRA_DM0	L
M	P_DIN2_5	P_DIN2_3	P_DIN2_1	P_DIN1_5	P_DIN2_0	DVDSS		DVDI	DVDSS	DVDSS	DVDSS	DVDSS	VSSPSSTL	VSSPSSTL		VDDSSTL	VREFSSTL	DDRA_ADDR11	VDDPSSTL	DDRA_DQ2	DDRA_DQ3	M
N	P_DIN2_7	P_DIN2_6	DVDSS	P_DIN2_2	P_DIN2_4	DVDI		DVDSS	DVDSS	DVDSS	DVDSS	DVDSS	VSSPSSTL	VDDSSTL		VDDPSSTL	VSSSSTL	DDRA_ADDR8	DDRA_ADDR10	DDRA_DQ0	DDRA_DQ1	N
P	P_DIN3_2	P_DIN3_3	P_DIN3_0	P_DIN3_1	P_CKVIN3	NC		DVDSS	DVDI	DVDSS	DVDI	DVDSS	DVDI	VSSPSSTL		VSSPSSTL	DDRA_BA0	DDRA_ADDR2	DDRA_ADDR6	DDRA_ADDR9	DDRA_ADDR12	P
R	P_CKVIN4	P_DIN3_6	P_DIN3_4	P_DIN3_5	P_DIN3_7	DVDSS										VDDSSTL	DDRA_BA1	DVDSS	DDRA_ADDR1	DDRA_ADDR5	DDRA_ADDR7	R
T	DVDE	DVDSS	P_DIN4_0	P_DIN4_1	P_DIN4_7	DVDI	DVDSS	DVDI	DVDSS	DVDI	DVDSS	DVDI	DVDSS	DVDI	DVDSS	VDDSSTL	VSSSSTL	DDRA_RASN	DDRA_BA2	DDRA_ADDR3	DDRA_ADDR4	T
U	P_DIN4_3	P_DIN4_2	P_DIN4_5	DVDE	P_DIN_PB4_0	P_DIN_PB4_3	P_CK27PB4	P_DIN_PB4_14	P_DIN_PB1_10	P_DIN_PB2_0	P_DIN_PB2_2	P_DIN_PB2_8	P_DIN_PB3_0	P_DIN_PB3_6	P_DIN_PB3_8	DVDSS	VSSPSSTL	VDDPSSTL	VSSSSTL	VSSPSSTL	DDRA_ADDR0	U
V	P_DIN4_4	P_DIN4_6	P_DIN_PB4_2	DVDSS	P_DIN_PB4_6	P_DIN_PB4_8	P_DIN_PB4_12	DVDSS	P_CK27PB1	P_DIN_PB1_13	P_DIN_PB2_3	P_DIN_PB2_7	DVDSS	P_DIN_PB3_3	P_DIN_PB3_7	P_DIN_PB3_12	P_DIN_PB3_15	DDRA_CKE	DDRA_CASN	VDDPSSTL	DDRA_CLKN	V
W	P_DIN_PB4_1	P_DIN_PB4_4	P_DIN_PB4_5	P_DIN_PB4_9	P_DIN_PB4_10	P_DIN_PB4_15	P_DIN_PB1_3	P_DIN_PB1_7	P_DIN_PB1_9	P_DIN_PB1_15	P_DIN_PB2_4	P_DIN_PB2_6	P_DIN_PB2_12	P_DIN_PB2_14	P_DIN_PB3_2	P_CK27PB3	DVDE	P_DIN_PB3_13	DDRA_ODT	DDRA_WEN	DDRA_CLK	W
Y	DVDE	P_DIN_PB4_7	NC	P_DIN_PB4_13	P_DIN_PB1_1	DVDSS	P_DIN_PB1_6	P_DIN_PB1_8	P_DIN_PB1_12	DVDSS	P_DIN_PB2_5	P_CK27PB2	P_DIN_PB2_11	DVDSS	P_DIN_PB2_15	P_DIN_PB3_4	P_DIN_PB3_10	P_DIN_PB3_11	P_DIN_PB3_14	VSSSSTL	VSSSSTL	Y
AA	DVDSS	P_DIN_PB4_11	P_DIN_PB1_0	P_DIN_PB1_2	P_DIN_PB1_4	P_DIN_PB1_5	DVDE	P_DIN_PB1_11	P_DIN_PB1_14	P_DIN_PB2_1	DVDE	P_DIN_PB2_9	P_DIN_PB2_10	P_DIN_PB2_13	DVDE	P_DIN_PB3_1	P_DIN_PB3_5	P_DIN_PB3_9	DVDSS	DVDE	NC	AA

FIGURE 1. MAP OF ALL THE TW2828 SIGNAL POSITIONS

AC/DC Electrical Parameters

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage
- AHVDD ..... +4.0V
- DHVDD ..... +4.0V
- DVDD ..... +1.2V
- PLL_AVDD ..... +1.2V
- PLL_DVDD ..... +1.2V
- VDDPSSTL ..... +2.0V
- VREFSSTL ..... +1.2V
- VDDSSTL ..... +1.2V
- DVDI ..... +1.2V
- DVDE ..... +4.0V

Voltage on any Digital Signal Pin
(See the note below) ..... -0.3V to DVDE+0.3V

Votage on OSC Related
Analog Pin.....-0.3V to AHVDD+0.3V

Thermal Information

Thermal Resistance θ_{JA} (°C/W)
409 Ball LFBGA (Note 1)..... 18.1

Storage Temperature Range ..... -55°C to +125°C

Junction Temperature Range ..... -40°C to +125°C

Pb-free Reflow Profile ..... see link below

http://www.intersil.com/pbfree/Pb-FreeReflow.asp

NOTE:
1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

TABLE 12. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DAC Analog Power	AHVDD	3.0	3.3	3.6	V
DAC Digital Power	DHVDD	3.0	3.3	3.6	V
DAC Core Power	DVDD	0.9	1.0	1.1	V
PLL Analog Power	PLL_AVDD	0.9	1.0	1.1	V
PLL Digital Power	PLL_DVDD	0.9	1.0	1.1	V
SSTL Pad Power	VDDPSSTL	1.6	1.8	1.9	V
SSTL Reference Power	VREFSSTL	0.49* VDDPSSTL	0.9	0.51* VDDPSSTL	V
SSTL Core Power	VDDSSTL	0.9	1.0	1.1	V
Digital Core 1.0V	DVDI	0.9	1.0	1.1	V
Digital I/O 3.3V	DVDE	3.0	3.3	3.6	V
Ambient Operating Temperature	T_A	0	25	70	°C

Supply Current and Power Dissipation

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
PLL Supply Current (1.0V nom)	I_{DDP}		8.36		mA
DAC Supply Current (3.3V nom)	I_{DDD}		69.3		mA
SSTL Pad Current (1.8V nom)	I_{DDH}		227.7		mA
SSTL Core Current (1.0V nom)	I_{DDH}		237.6		mA
Digital Internal Supply Current (1.0V nom)	I_{DDI}		278.3		mA
Digital I/O Supply Current (3.3V nom)	I_{DDO}		73.7		mA
Total Power Dissipation	Pd		1.41		W

DC Characteristics

PARAMETER	SYMBOL	MIN (NOTE 2)	TYP	MAX (NOTE 2)	UNITS
DIGITAL INPUTS					
Input High Voltage (TTL)	V_{IH}	2.0		V_{DDE} + 0.3	V
Input Low Voltage (TTL)	V_{IL}	−0.3		0.8	V
Input Leakage Current (@V_I = 3.3V or 0V)	I_L			± 4	µA
DIGITAL OUTPUTS					
Output High Voltage	V_{OH}	V_{DDE} −0.2		V_{DDE}	V
Output Low Voltage	V_{OL}	0		0.2	V

NOTES:

2. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Analog Performance Parameter

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
DAC CHARACTERISTIC					
Differential Non-Linearity	D_{NL}		±1		LSB
Output Impedance	Z_o		50		kΩ
DAC-to-DAC Matching			3		%
Signal-to-Noise and Distortion Ratio	SNDR		40		dB

NOTES:

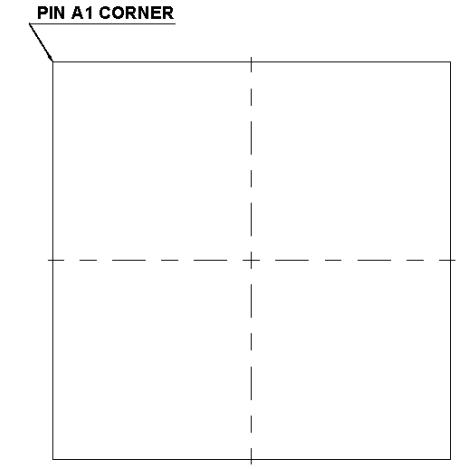
1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Package Outline Drawing

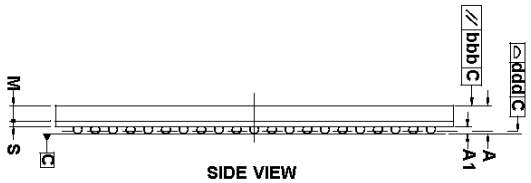
V409.18x18

409 LOW PROFILE FINE PITCH PLASTIC BALL GRID ARRAY PACKAGE (LFBGA)

Rev 0, 3/12

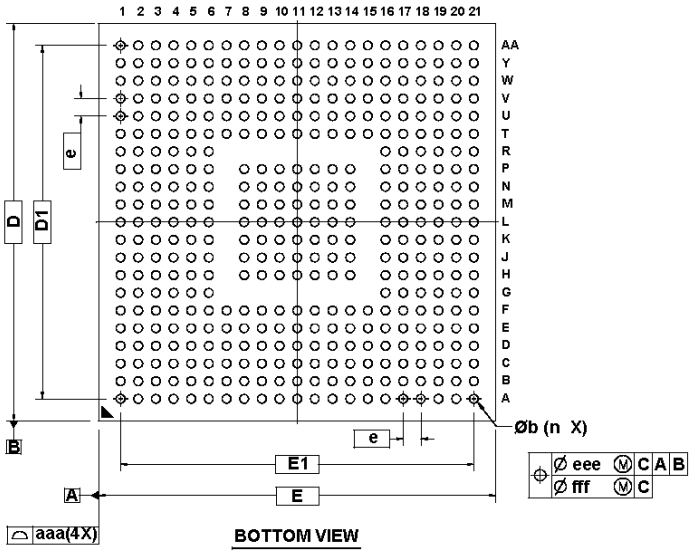


TOP VIEW



SIDE VIEW

		SYMBOL	COMMON DIMENSIONS
Package			LFBGA
Body Size	X	E	18.00
	Y	D	18.00
Ball Pitch			0.800
Total Thickness		A	1.400 MAX
Mold Thickness		M	0.700 Ref.
Substrate Thickness		S	0.260 Ref.
Ball Diameter			0.400
Stand Off		A1	0.270 ~ 0.370
Ball Width		b	0.380 ~ 0.480
Package Edge Tolerance		aaa	0.150
Mold Flatness		bbb	0.200
Coplanarity		ddd	0.120
Ball Offset (Package)		eee	0.150
Ball Offset (Ball)		fff	0.080
Ball Count		n	409
Edge Ball Center to Center	X	E1	16.00
	Y	D1	16.00



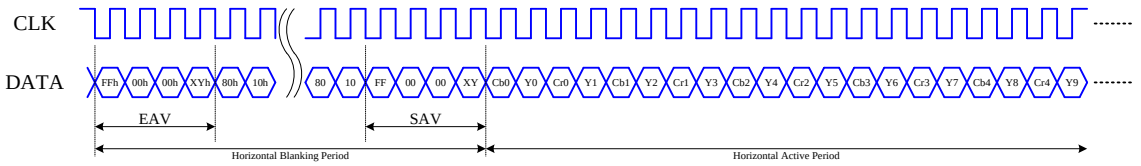
BOTTOM VIEW

Digital Video Input (Type 1)

Digital Video Input

The TW2828 has 4 independent digital video input ports which can receive byte-interleaved video stream in ITU-R BT.656 format. This byte-interleaved BT.656 bit stream can run at 27, 54,108 MHz for D1 channel or 36, 72, 144 MHz for WD1 channel. Altogether TW2828 can support up to 16 byte interleaved channels. There are also 4 shared byte interleaved inputs (shared with type 2 inputs). When used in this configuration, each input is running at x2 frequency to lower the input frequency. The type 2 input port is reduced to 8 bit mode only in this configuration. All these inputs can be paired with many Intersil front end decoders to get the desired input. One thing needs to pay attention to is if the decoders output are running at high frequencies, they better use the clock provided by TW2828 as the their input clock source. This is for better clock / data synchronization.

After the digital data is decoded by the built-in BT.656 decoder, the image will be fed into a down scalar to adjust the final image to the desired sizes. The down scaler also generates corresponding vertical and horizontal timing signals and sends those to the write buffer.

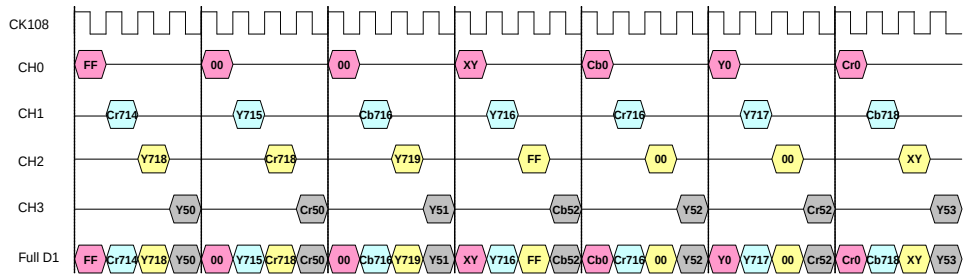


TIMING DIAGRAM OF BT.656 FORMAT FOR DIGITAL VIDEO INPUT

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE			
FIELD	VERTICAL	HORIZONTAL	F	V	H	FIRST	SECOND	THIRD	FOURTH
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1
		SAV			0				0xEC
EVEN	Active	EAV	1	0	1				0xDA
		SAV			0				0xC7
ODD	Blank	EAV	0	1	1				0xB6
		SAV			0				0xAB
ODD	Active	EAV	0	0	1				0x9D
		SAV			0				0x80

BT.656 SAV AND EAV CODE SEQUENCE

Byte-interleaved Format



FOUR D1 VIDEO INPUT MULTIPLEXED INTO 1 VIDEO STREAM

The above diagram depicts how a high speed byte-interleaved video sequence looks like. In this case we are transmitting 4 D1 channel running at 108 MHz. This input sequence will go to a de-mux module and split into four normal BT.656 sequence for later consumption.

Down Scaler for Live Inputs

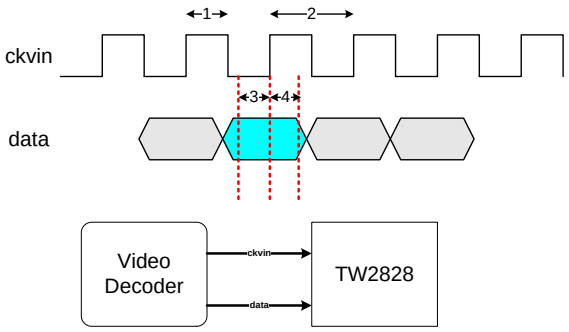
For each live channel, two sixteen-bit registers control the final video stream size. One is for horizontal ratio and the other one is for vertical ratio. Take window 1 for example, 0x301 and 0x300 is the horizontal down scale ratio register and 0x321 and 0x320 are the vertical down scale register. The formula is:

Ratio = 65535 * target size / source size.

From this formula we can see if the When down scaler is set to 65535 (0xFFFF), the down scaler is disabled.

There are five down scaler for play back ports. Detail description is in separated chapter.

AC Timing for Live and PB Input



FOR D1 SYSTEM

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Clock Half Period	1		4.62(108) 9.26 (54), 18.52 (27)		ns
Input Clock Period	2		9.25(108) 18.51 (54), 37.03 (27)		ns
Input Data Setup Time	3	3			ns
Input Data Hold Time	4	1.5			ns

FOR WD1 SYSTEM:

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Clock Half Period	1		3.47(144) 6.94 (72), 13.88 (36)		ns
Input Clock Period	2		6.94(144) 13.88 (72), 27.26 (36)		ns
Input Data Setup Time	3	2.5			ns
Input Data Hold Time	4	1.5			ns

Register Table

Page 3 is for live channel and play back channel

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x300	R/W	0xFF	HSCL_X1[7:0]
0x301	R/W	0x7F	HSCL_X1[15:8]
0x302	R/W	0xFF	HSCL_X2[7:0]
0x303	R/W	0x7F	HSCL_X2[15:8]
0x304	R/W	0xFF	HSCL_X3[7:0]
0x305	R/W	0x7F	HSCL_X3[15:8]
0x306	R/W	0xFF	HSCL_X4[7:0]
0x307	R/W	0x7F	HSCL_X4[15:8]
0x308	R/W	0xFF	HSCL_X5[7:0]
0x309	R/W	0x7F	HSCL_X5[15:8]
0x30A	R/W	0xFF	HSCL_X6[7:0]
0x30B	R/W	0x7F	HSCL_X6[15:8]
0x30C	R/W	0xFF	HSCL_X7[7:0]
0x30D	R/W	0x7F	HSCL_X7[15:8]
0x30E	R/W	0xFF	HSCL_X8[7:0]
0x30F	R/W	0x7F	HSCL_X8[15:8]
0x310	R/W	0xFF	HSCL_X9[7:0]
0x311	R/W	0x7F	HSCL_X9[15:8]
0x312	R/W	0xFF	HSCL_X10[7:0]
0x313	R/W	0x7F	HSCL_X10[15:8]
0x314	R/W	0xFF	HSCL_X11[7:0]
0x315	R/W	0x7F	HSCL_X11[15:8]
0x316	R/W	0xFF	HSCL_X12[7:0]
0x317	R/W	0x7F	HSCL_X12[15:8]
0x318	R/W	0xFF	HSCL_X13[7:0]
0x319	R/W	0x7F	HSCL_X13[15:8]
0x31A	R/W	0xFF	HSCL_X14[7:0]
0x31B	R/W	0x7F	HSCL_X14[15:8]
0x31C	R/W	0xFF	HSCL_X15[7:0]
0x31D	R/W	0x7F	HSCL_X15[15:8]
0x31E	R/W	0xFF	HSCL_X16[7:0]
0x31F	R/W	0x7F	HSCL_X16[15:8]
0x320	R/W	0xFF	VSCL_X1[7:0]
0x321	R/W	0x7F	VSCL_X1[15:8]

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x322	R/W	0xFF	VSCL_X2[7:0]
0x323	R/W	0x7F	VSCL_X2[15:8]
0x324	R/W	0xFF	VSCL_X3[7:0]
0x325	R/W	0x7F	VSCL_X3[15:8]
0x326	R/W	0xFF	VSCL_X4[7:0]
0x327	R/W	0x7F	VSCL_X4[15:8]
0x328	R/W	0xFF	VSCL_X5[7:0]
0x329	R/W	0x7F	VSCL_X5[15:8]
0x32A	R/W	0xFF	VSCL_X6[7:0]
0x32B	R/W	0x7F	VSCL_X6[15:8]
0x32C	R/W	0xFF	VSCL_X7[7:0]
0x32D	R/W	0x7F	VSCL_X7[15:8]
0x32E	R/W	0xFF	VSCL_X8[7:0]
0x32F	R/W	0x7F	VSCL_X8[15:8]
0x330	R/W	0xFF	VSCL_X9[7:0]
0x331	R/W	0x7F	VSCL_X9[15:8]
0x332	R/W	0xFF	VSCL_X10[7:0]
0x333	R/W	0x7F	VSCL_X10[15:8]
0x334	R/W	0xFF	VSCL_X11[7:0]
0x335	R/W	0x7F	VSCL_X11[15:8]
0x336	R/W	0xFF	VSCL_X12[7:0]
0x337	R/W	0x7F	VSCL_X12[15:8]
0x338	R/W	0xFF	VSCL_X13[7:0]
0x339	R/W	0x7F	VSCL_X13[15:8]
0x33A	R/W	0xFF	VSCL_X14[7:0]
0x33B	R/W	0x7F	VSCL_X14[15:8]
0x33C	R/W	0xFF	VSCL_X15[7:0]
0x33D	R/W	0x7F	VSCL_X15[15:8]
0x33E	R/W	0xFF	VSCL_X16[7:0]
0x33F	R/W	0x7F	VSCL_X16[15:8]
0x340	R/W	0x00	[7:6]: VSCL_MD_X4 [5:4]: VSCL_MD_X3 [3:2]: VSCL_MD_X2 [1:0]: VSCL_MD_X1
0x341	R/W	0x00	[7:6]: VSCL_MD_X8 [5:4]: VSCL_MD_X7 [3:2]: VSCL_MD_X6 [1:0]: VSCL_MD_X5
0x342	R/W	0x00	[7:6]: VSCL_MD_X12 [5:4]: VSCL_MD_X11 [3:2]: VSCL_MD_X10 [1:0]: VSCL_MD_X9
0x343	R/W	0x00	[7:6]: VSCL_MD_X16 [5:4]: VSCL_MD_X15 [3:2]: VSCL_MD_X14 [1:0]: VSCL_MD_X13
0x344	R/W	0x00	[7:6]: VSCL_MD_Y4 [5:4]: VSCL_MD_Y3 [3:2]: VSCL_MD_Y2 [1:0]: VSCL_MD_Y1
0x345	R/W	0x00	[7:6]: VSCL_MD_Y8 [5:4]: VSCL_MD_Y7 [3:2]: VSCL_MD_Y6 [1:0]: VSCL_MD_Y5

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x346	R/W	0x00	[7:6]: VSCL_MD_Y12 [5:4]: VSCL_MD_Y11 [3:2]: VSCL_MD_Y10 [1:0]: VSCL_MD_Y9
0x347	R/W	0x00	[7:6]: VSCL_MD_Y16 [5:4]: VSCL_MD_Y15 [3:2]: VSCL_MD_Y14 [1:0]: VSCL_MD_Y13
0x348	R/W	0x00	[7:6]: HLPF_MD_X4 [5:4]: HLPF_MD_X3 [3:2]: HLPF_MD_X2 [1:0]: HLPF_MD_X1
0x349	R/W	0x00	[7:6]: HLPF_MD_X8 [5:4]: HLPF_MD_X7 [3:2]: HLPF_MD_X6 [1:0]: HLPF_MD_X5
0x34A	R/W	0x00	[7:6]: HLPF_MD_X12 [5:4]: HLPF_MD_X11 [3:2]: HLPF_MD_X10 [1:0]: HLPF_MD_X9
0x34B	R/W	0x00	[7:6]: HLPF_MD_X16 [5:4]: HLPF_MD_X15 [3:2]: HLPF_MD_X14 [1:0]: HLPF_MD_X13
0x34C	R/W	0x00	[7:6]: HLPF_MD_Y4 [5:4]: HLPF_MD_Y3 [3:2]: HLPF_MD_Y2 [1:0]: HLPF_MD_Y1
0x34D	R/W	0x00	[7:6]: HLPF_MD_Y8 [5:4]: HLPF_MD_Y7 [3:2]: HLPF_MD_Y6 [1:0]: HLPF_MD_Y5
0x34E	R/W	0x00	[7:6]: HLPF_MD_Y12 [5:4]: HLPF_MD_Y11 [3:2]: HLPF_MD_Y10 [1:0]: HLPF_MD_Y9
0x34F	R/W	0x00	[7:6]: HLPF_MD_Y16 [5:4]: HLPF_MD_Y15 [3:2]: HLPF_MD_Y14 [1:0]: HLPF_MD_Y13
0x350	R/W	0xF0	[7:4] HSCL_QUAD[3:0] [3:2]: CIF down scaler horizontal ratio[1:0] [0]: PAL_DLY_X
0x351	R/W	0xF0	[7:4] HSCL_QUAD[7:4] [3:2]: CIF down scaler horizontal ratio[3:2] [0]: PAL_DLY_Y
0x352	R/W	0xF0	[7:4] HSCL_QUAD[11:8] [3:0]: ODD_SKEW
0x353	R/W	0x70	[7:4] HSCL_QUAD[15:12] [3:0]: EVEN_SKEW

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x354	R/W	0x00	[7]: MAN_VSCL_LPFY8 [6]: MAN_VSCL_LPFY7 [5]: MAN_VSCL_LPFY6 [4]: MAN_VSCL_LPFY5 [3]: MAN_VSCL_LPFY4 [2]: MAN_VSCL_LPFY3 [1]: MAN_VSCL_LPFY2 [0]: MAN_VSCL_LPFY1
0x355	R/W	0x00	[7]: MAN_VSCL_LPFY16 [6]: MAN_VSCL_LPFY15 [5]: MAN_VSCL_LPFY14 [4]: MAN_VSCL_LPFY13 [3]: MAN_VSCL_LPFY12 [2]: MAN_VSCL_LPFY11 [1]: MAN_VSCL_LPFY10 [0]: MAN_VSCL_LPFY9
0x356	R/W	0x00	[7:3]: CIF down scaler horizontal ratio[9:4] [1]: IN16_MODE_PB5 [0]: TST_VSCL_VAV
0x357	R/W	0x00	[7]: TOGGLE_FLD4 [6]: TOGGLE_FLD3 [5]: TOGGLE_FLD2 [4]: TOGGLE_FLD1 [3]: TST_FLDLY_Y [2]: TST_FLDLY_X [1]: TST_VSCL_Y [0]: TST_VSCL_X
0x358	R/W	0xF0	VTAR_PB1[7:0]
0x359	R/W	0x00	[6:4] VTAR_PB2[10:8] [2:0] VTAR_PB1[10:8]
0x35A	R/W	0xF0	VTAR_PB2[7:0]
0x35B	R/W	0xF0	VTAR_PB3[7:0]
0x35C	R/W	0x00	[6:4]: VTAR_PB4[10:8] [2:0]: VTAR_PB3[10:8]
0x35D	R/W	0xF0	VTAR_PB4[7:0]
0x35E	R/W	0xF0	VSOR_PB1[7:0]
0x35F	R/W	0x00	[6:4]: VSOR_PB2[10:8] [2:0]: VSOR_PB1[10:8]
0x360	R/W	0xF0	VSOR_PB2[7:0]
0x361	R/W	0xF0	VSOR_PB3[7:0]
0x362	R/W	0x00	[6:4]: VSOR_PB4[10:8] [2:0]: VSOR_PB3[10:8]
0x363	R/W	0xF0	VSOR_PB4[7:0]
0x364	R/W	0xD0	HTAR_PB1[7:0]
0x365	R/W	0x22	[6:4]: HTAR_PB2[10:8] [2:0]: HTAR_PB1[10:8]
0x366	R/W	0xD0	HTAR_PB2[7:0]
0x367	R/W	0xD0	HTAR_PB3[7:0]
0x368	R/W	0x22	[6:4]: HTAR_PB4[10:8] [2:0]: HTAR_PB3[10:8]
0x369	R/W	0xD0	HTAR_PB4[7:0]
0x36A	R/W	0xD0	HSOR_PB1[7:0]
0x36B	R/W	0x22	[6:4]: HSOR_PB2[10:8] [2:0]: HSOR_PB1[10:8]
0x36C	R/W	0xD0	HSOR_PB2[7:0]
0x36D	R/W	0xD0	HSOR_PB3[7:0]

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x36E	R/W	0x22	[6:4]: HSOR_PB4[10:8] [2:0]: HSOR_PB3[10:8]
0x36F	R/W	0xD0	HSOR_PB4[7:0]
0x370	R/W	0x00	[7]: QUAD_AUTO_SCL_PB4 [6]: QUAD_AUTO_SCL_PB3 [5]: QUAD_AUTO_SCL_PB2 [4]: QUAD_AUTO_SCL_PB1 [3]: BYPASS_PB4 [2]: BYPASS_PB3 [1]: BYPASS_PB2 [0]: BYPASS_PB1
0x371	R/W	0x20	[7]: OUTPUT_SELECT [6]: SYNC_SEL [5]: YC_SWITCH (all PB ports) [4]: SYNC656_SEL [3]: IN16_MODE_PB4 [2]: IN16_MODE_PB3 [1]: IN16_MODE_PB2 [0]: IN16_MODE_PB1
0x372 (Shadow)	R/W	0x00	[7:5]: SEL_PB_CH[2:0] [4]: YC_SWITCH5 (PB5) [3]: YC_SWITCH4 (PB4) [2]: YC_SWITCH3 (PB3) [1]: YC_SWITCH2 (PB2) [0]: YC_SWITCH1 (PB1)
0x373 (Shadow)	R/W	0x00	[7]: TSEL [4]: IN_PB_TEST5 [3]: IN_PB_TEST4 [2]: IN_PB_TEST3 [1]: IN_PB_TEST2 [0]: IN_PB_TEST1
0x372	RO	0x07	CHID_RD_BUS_PB1[39:32]
0x373	RO	0x00	CHID_RD_BUS_PB1[31:24]
0x374	RO	0x07	CHID_RD_BUS_PB1[23:16]
0x375	R/W	0x00	HDELAY_X1
0x376	R/W	0x00	HDELAY_X2
0x377	R/W	0x00	HDELAY_X3
0x378	R/W	0x00	HDELAY_X4
0x379	R/W	0x00	HDELAY_X5
0x37A	R/W	0x00	HDELAY_X6
0x37B	R/W	0x00	HDELAY_X7
0x37C	R/W	0x00	HDELAY_X8
0x37D	R/W	0x00	HDELAY_X9
0x37E	R/W	0x00	HDELAY_X10
0x37F	R/W	0x00	HDELAY_X11
0x380	R/W	0x00	HDELAY_X12
0x381	R/W	0x00	HDELAY_X13
0x382	R/W	0x00	HDELAY_X14
0x383	R/W	0x00	HDELAY_X15
0x384	R/W	0x00	HDELAY_X16
0x385	R/W	0x00	HDELAY_Y2 [3:0], HDELAY_Y1[3:0]
0x386	R/W	0x00	HDELAY_Y4 [3:0], HDELAY_Y3[3:0]
0x387	R/W	0x00	HDELAY_Y6 [3:0], HDELAY_Y5[3:0]
0x388	R/W	0x00	HDELAY_Y8 [3:0], HDELAY_Y7[3:0]
0x389	R/W	0x00	HDELAY_Y10 [3:0], HDELAY_Y9[3:0]

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x38A	R/W	0x00	HDELAY_Y12 [3:0], HDELAY_Y11[3:0]
0x38B	R/W	0x00	HDELAY_Y14 [3:0], HDELAY_Y13[3:0]
0x38C	R/W	0x00	HDELAY_Y16 [3:0], HDELAY_Y15[3:0]
0x38D	R/W	0x00	VDELAY_Y2 [3:0], VDELAY_Y1[3:0]
0x38E	R/W	0x00	VDELAY_Y4 [3:0], VDELAY_Y3[3:0]
0x38F	R/W	0x00	VDELAY_Y6 [3:0], VDELAY_Y5[3:0]
0x390	R/W	0x00	VDELAY_Y8 [3:0], VDELAY_Y7[3:0]
0x391	R/W	0x00	VDELAY_Y10 [3:0], VDELAY_Y9[3:0]
0x392	R/W	0x00	VDELAY_Y12 [3:0], VDELAY_Y11[3:0]
0x393	R/W	0x00	VDELAY_Y14 [3:0], VDELAY_Y13[3:0]
0x394	R/W	0x00	VDELAY_Y16 [3:0], VDELAY_Y15[3:0]
0x395	R/W	0x00	VDELAY_X1
0x396	R/W	0x00	VDELAY_X2
0x397	R/W	0x00	VDELAY_X3
0x398	R/W	0x00	VDELAY_X4
0x399	R/W	0x00	VDELAY_X5
0x39A	R/W	0x00	VDELAY_X6
0x39B	R/W	0x00	VDELAY_X7
0x39C	R/W	0x00	VDELAY_X8
0x39D	R/W	0x00	VDELAY_X9
0x39E	R/W	0x00	VDELAY_X10
0x39F	R/W	0x00	VDELAY_X11
0x3A0	R/W	0x00	VDELAY_X12
0x3A1	R/W	0x00	VDELAY_X13
0x3A2	R/W	0x00	VDELAY_X14
0x3A3	R/W	0x00	VDELAY_X15
0x3A4	R/W	0x00	VDELAY_X16
0x3A5	R/W	0x00	HDELAY_PB5
0x3A6	R/W	0x00	VDELAY_PB5
0x3A7	R/W	0x00	HSOR_PB5L
0x3A8	R/W	0x00	HSCL_PB5L
0x3A9	R/W	0x00	[6:4]:HSCL_PB5H[10:8] [2:0]:HSOR_PB5H[10:8]
0x3AA	R/W	0x00	VSOR_PB5L[7:0]
0x3AB	R/W	0x00	VSCL_PB5L[[7:0]
0x3AC	R/W	0x00	[7]:VBI_DLY5 [6:4] : VSCL_PB5H[10:8] [3]: Reserved [2:0]:VSOR_PB5H[10:8]
0x3AD	R/W	0x00	[7]: BYPASS_PB5 [6]: FLD_SEL_EN_PB5 [5]: FLD_MODE_PB5 [4]: FLD_MODE_PB5_EN [3]: FRAME_IL_PB5 [2]: FRAME_IL_PB5_EN [1:0]: PB_MAN_NOVID5[1:0]
0x3AE	R/W	0x00	[7:4]: VBI_SIZE_PB5[3:0] [3]: VBI_E_EN_PB5 [2]: VBI_O_EN_PB5 [1]: TOGGLE_FLD5 [0]: VS_DIS5

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x3AF	R/W	0x00	[7:4]: CHID_RD_SEL_PB5[3:0] [3]: [VBI_RIC_ON_PB5 [2]: VBI_AUTO_DET_PB5 [1]: VBI_D_EN_PB5 [0]: VBI_A_EN_PB5
0x3B0	R/W	0x00	[7]: NO_SYNC_CHECK [6]: NON_STANDARD_CHECK [5]: NO_VIDEO_CHECK [4:0] VBI_VOS_PB5
0x3B1	R/W	0x00	[7:5]: VBI_PIXEL_WIDTH_PB5 [4:0]: VBI_FOS_PB5
0x3B2	R/W	0x00	VBI_HOS_PB5
0x3B3	R/W	0x00	VBI_MID_VAL_PB5
0x3B4	R/W	0x00	Reserved
0x3B5	R/W	0x00	[7:0]: HDELAY_PB1
0x3B6	R/W	0x00	[7:0]: VDELAY_PB1
0x3B7	R/W	0x00	[7:0]: HDELAY_PB2
0x3B8	R/W	0x00	[7:0]: VDELAY_PB2
0x3B9	R/W	0x00	[7:0]: HDELAY_PB3
0x3BA	R/W	0x00	[7:0]: VDELAY_PB3
0x3BB	R/W	0x00	[7:0]: HDELAY_PB4
0x3BC	R/W	0x00	[7:0]: VDELAY_PB4
0x3BD	R/W	0x00	[7:6]: MAN_NOVID4 [5:4]: MAN_NOVID3 [3:2]: MAN_NOVID2 [1:0]: MAN_NOVID1
0x3BE	R/W	0x00	[7:6]:MAN_NOVID8 [5:4]: MAN_NOVID7 [3:2]: MAN_NOVID6 [1:0]: MAN_NOVID5
0x3BF	R/W	0x00	[7:6]:MAN_NOVID12 [5:4]: MAN_NOVID11 [3:2]: MAN_NOVID10 [1:0]: MAN_NOVID9
0x3C0	R/W	0x00	[7:6]:MAN_NOVID16 [5:4]: MAN_NOVID15 [3:2]: MAN_NOVID14 [1:0]: MAN_NOVID13
0x3C1	R/W	0x00	[7:6]:MAN_NONSTD4 [5:4]: MAN_NONSTD3 [3:2]: MAN_NONSTD2 [1:0]: MAN_NONSTD1
0x3C2	R/W	0x00	[7:6]:MAN_NONSTD8 [5:4]: MAN_NONSTD7 [3:2]: MAN_NONSTD6 [1:0]: MAN_NONSTD5
0x3C3	R/W	0x00	[7:6]:MAN_NONSTD12 [5:4]: MAN_NONSTD11 [3:2]: MAN_NONSTD10 [1:0]: MAN_NONSTD9
0x3C4	R/W	0x00	[7:6]:MAN_NONSTD16 [5:4]: MAN_NONSTD15 [3:2]: MAN_NONSTD14 [1:0]: MAN_NONSTD13

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x3C5	R/W	0x00	[7]: Reserved [6]: STILL_PAT [5]: PALNT [4]: IN_TEST [3]: Reserved [2]: CHID_BIT [1]: NO_CHID [0]: SYNC_CHID
0x3C6	R/W	0x00	[7:2]: CIF down scaler horizontal ratio[15:10] [1]: SEL960 [0]: SYS_60
0x3C7	RO	0x00	CHID_RD_BUS_PB1[15:8]
0x3C8	RO	0x00	CHID_RD_BUS_PB1[7:0]
0x3C9	RO	0x00	CHID_RD_BUS_PB2[39:32]
0x3CA	RO	0x00	CHID_RD_BUS_PB2[31:24]
0x3CC	RO	0x00	Read: CHID_RD_BUS_PB2[23:16] Write: [6:4]: VID_FMT2 [2:0]: VID_FMT1
0x3CD	RO	0x00	Read: CHID_RD_BUS_PB2[15:8] Write: [6:4]: VID_FMT4 [2:0]: VID_FMT3
0x3CE	RO	0x00	Read: CHID_RD_BUS_PB2[7:0] Write: [6]: PURE_L [5]: PURE_P [4:0]: DYNAMIC[4:0]
0x3CF	RO	0x00	CHID_RD_BUS_PB3[39:32]
0x3D0	RO	0x00	CHID_RD_BUS_PB3[31:24]
0x3D1	RO	0x00	CHID_RD_BUS_PB3[23:16]
0x3D2	R/W	0x10	[7:4]: VIN_SEL2 [3:0]: VIN_SEL1
0x3D3	R/W	0x32	[7:4]: VIN_SEL4 [3:0]: VIN_SEL3
0x3D4	R/W	0x54	[7:4]: VIN_SEL6 [3:0]: VIN_SEL5
0x3D5	R/W	0x76	[7:4]: VIN_SEL8 [3:0]: VIN_SEL7
0x3D6	R/W	0x98	[7:4]: VIN_SEL10 [3:0]: VIN_SEL9
0x3D7	R/W	0xBA	[7:4]: VIN_SEL12 [3:0]: VIN_SEL11
0x3D8	R/W	0xDC	[7:4]: VIN_SEL14 [3:0]: VIN_SEL13
0x3D9	R/W	0xFE	[7:4]: VIN_SEL16 [3:0]: VIN_SEL15
0x3DA	R/W	0x01	[7]: VIN_SEL_XY [0]: V_OFST_X
0x3DB	R/W	0x00	[7:0]: Reserved
0x3DC	R/W	0x08	[7:5]: VID_FMT for PB5 [4]: DIR2 [3]: DIR1 [2:1]: FRAME_RATE [0]: IN_PB_TEST
0x3DD	RW	0x00	PIXEL_SHIFT

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x3DE	R/W	0x0F	[7:4]: CHID_RD_SEL_PB1 [3]: VBI_RIC_ON_PB1 [2]: VBI_AUTO_DET_PB1 [1]: VBI_D_EN_PB1 [0]: VBI_A_EN_PB1
0x3DF	R/W	0x00	[7]: NO_SYNC_CHECK [6]: NON_STANDARD_CHECK [5]: NO_VIDEO_CHECK [4:0]: VBI_VOS_PB1
0x3E0	R/W	0x80	[7:5]: VBI_PIXEL_WIDTH_PB1 [4:0]: VBI_FOS_PB1
0x3E1	R/W	0x00	VBI_HOS_PB1
0x3E2	R/W	0x1F	VBI_MID_VAL_PB1
0x3E3	R/W	0x0F	[7:4]: CHID_RD_SEL_PB2 [3]: VBI_RIC_ON_PB2 [2]: VBI_AUTO_DET_PB2 [1]: VBI_D_EN_PB2 [0]: VBI_A_EN_PB2
0x3E4	R/W	0x00	[7]: NO_SYNC_CHECK [6]: NON_STANDARD_CHECK [4]: NO_VIDEO_CHECK [4:0]: VBI_VOS_PB2
0x3E5	R/W	0x80	[7:5]: VBI_PIXEL_WIDTH_PB2 [4:0]: VBI_FOS_PB2
0x3E6	R/W	0x00	VBI_HOS_PB2
0x3E7	R/W	0x1F	VBI_MID_VAL_PB2
0x3E8	R/W	0x0F	[7:4]CHID_RD_SEL_PB3 [3]: VBI_RIC_ON_PB3 [2]: VBI_AUTO_DET_PB3 [1]: VBI_D_EN_PB3 [0]: VBI_A_EN_PB3
0x3E9	R/W	0x00	[7]: NO_SYNC_CHECK [6]: NON_STANDARD_CHECK [5]: NO_VIDEO_CHECK [4:0]: VBI_VOS_PB3
0x3EA	R/W	0x80	[7:5]: VBI_PIXEL_WIDTH_PB3 [4:0]: VBI_FOS_PB3
0x3EB	R/W	0x00	VBI_HOS_PB3
0x3EC	R/W	0x1F	VBI_MID_VAL_PB3
0x3ED	R/W	0x0F	[7:4]: CHID_RD_SEL_PB4 [3]: VBI_RIC_ON_PB4 [2]: VBI_AUTO_DET_PB4 [1]: VBI_D_EN_PB4 [0]: VBI_A_EN_PB4
0x3EE	R/W	0x00	[7]: NO_SYNC_CHECK [6]: NON_STANDARD_CHECK [5]: NO_VIDEO_CHECK [4:0] VBI_VOS_PB4
0x3EF	R/W	0x80	[7:5]: VBI_PIXEL_WIDTH_PB4 [4:0]: VBI_FOS_PB4
0x3F0	R/W	0x00	VBI_HOS_PB4
0x3F1	R/W	0x00	VBI_MID_VAL_PB4

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x3F2	R/W	0x00	[7]: FRAME_IL_PB4_EN [6]: FRAME_IL_PB3_EN [5]: FRAME_IL_PB2_EN [4]: FRAME_IL_PB1_EN [3]: FRAME_IL_PB4 [2]: FRAME_IL_PB3 [1]: FRAME_IL_PB2 [0]: FRAME_IL_PB1
0x3F3	R/W	0x00	[7]: FLD_MODE_PB4_EN [6]: FLD_MODE_PB3_EN [5]: FLD_MODE_PB2_EN [4]: FLD_MODE_PB1_EN [3]: FLD_MODE_PB4 [2]: FLD_MODE_PB3 [1]: FLD_MODE_PB2 [0]: FLD_MODE_PB1
0x3F4	R/W	0xFF	[7]: VBI_E_EN_PB4 [6]: VBI_E_EN_PB3 [5]: VBI_E_EN_PB2 [4]: VBI_E_EN_PB1 [3]: VBI_O_EN_PB4 [2]: VBI_O_EN_PB3 [1]: VBI_O_EN_PB2 [0]: VBI_O_EN_PB1
0x3F5	RO	0x00	CHID_RD_BUS_PB3[15:8]
0x3F6	RO	0x00	CHID_RD_BUS_PB3[7:0]
0x3F7	RO	0x00	CHID_RD_BUS_PB4[39:32]
0x3F8	RO	0x00	CHID_RD_BUS_PB4[31:24]
0x3F9	RO	0x00	CHID_RD_BUS_PB4[23:16]
0x3FA	RO	0x00	CHID_RD_BUS_PB4[15:8]
0x3FB	RO	0x00	CHID_RD_BUS_PB4[7:0]
0x3F8 (Shadow)	R/W	0x2F	HD_UP_LIM[7:0]
0x3F9 (Shadow)	R/W	0x02	[2:0]: HD_UP_LIM[10:8]
0x3FA (Shadow)	R/W	0x09	HD_DOWN_LIM[7:0]
0x3FB (Shadow)	R/W	0x02	[2:0]: HD_DOWN_LIM[10:8]
0x3F8 (Shadow)	R/W	0x0F	SD_PIXEL_WIDTH[7:0]
0x3F9 (Shadow)	R/W	0x00	SD_PIXEL_WIDTH[11:8]
0x3FA (Shadow)	R/W	0x04	SD_LINE_CNT[7:0]
0x3FB (Shadow)	R/W	0x0F	SD_LINE_WIDTH[7:0]
0x3FC	R/W	0x00	[7]: VBI_DLY4 [6]: VBI_DLY3 [5]: VBI_DLY2 [4]: VBI_DLY1 [3]: FLD_SEL_EN_PB4 [2]: FLD_SEL_EN_PB3 [1]: FLD_SEL_EN_PB2 [0]: FLD_SEL_EN_PB1

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x3FD	R/W	0xEE	[7:4]: VBI_SIZE_PB2 [3:0]: VBI_SIZE_PB1
0x3FE	R/W	0xEE	[7:4]: VBI_SIZE_PB4 [3:0]: VBI_SIZE_PB3
0x3FF	R/W	0x00	[7]: selm [6:5]: Reserved [4]: DIG_CODE [3]: VS_DIS_PB4 [2]: VS_DIS_PB3 [1]: VS_DIS_PB2 [0]: VS_DIS_PB1

Registers

Here are register descriptions for live channel down scaler. Registers related to PB down scaler will be described in separated chapter.

LIVE VIDEO CHANNEL 1 HORIZONTAL SCALER LOW BYTE REGISTER – 0X300

BIT	R/W	DEFAULT	DESCRIPTION
7:0	R/W	0xFF	HSCL_X1[7:0] Horizontal scaler factor. Maximum is 0xFFFF. The number is smaller; the down scaler factor is bigger.

LIVE VIDEO CHANNEL 1 HORIZONTAL SCALER HIGH BYTE REGISTER – 0X301

BIT	R/W	DEFAULT	DESCRIPTION
7:0	R/W	0x7F	HSCL_X1[15:8] Horizontal scaler factor. Maximum is 0xFFFF. The number is smaller; the down scaler factor is bigger.

Register 0x302 to 0x31F are for channel 2 to 16 which are similar to 0x300 and 0x301.

LIVE VIDEO CHANNEL 1 VERTICAL SCALER LOW BYTE REGISTER – 0X320

Bit	R/W	Default	Description
7:0	R/W	0xFF	VSCL_X1[7:0] Vertical scaler factor. Maximum is 0xFFFF. The number is smaller; the down scaler factor is bigger.

LIVE VIDEO CHANNEL 1 VERTICAL SCALER HIGH BYTE REGISTER – 0X321

Bit	R/W	Default	Description
7:0	R/W	0xFF	VSCL_X1[15:8] Vertical scaler factor. Maximum is 0xFFFF. The number is smaller; the down scaler factor is bigger.

Register 0x322 to 0x33F are for channel 2 to 16 which are similar to 0x320 and 0x321.

LIVE VIDEO VERTICAL SCALE MODE REGISTER – 0X340

Bit	R/W	Default	Description
7:0	R/W	0x00	**VSCL_MD_X:** Vertical scale mode [7:6]: VSCL_MD_X4 [5:4]: VSCL_MD_X3 [3:2]: VSCL_MD_X2 [1:0]: VSCL_MD_X1

Register 0x341 to 0x343 are for other channels in display down scaler. Register 0x344 to 0x347 are for record down scaler.

LIVE VIDEO HORIZONTAL SCALE MODE REGISTER – 0X348

Bit	R/W	Default	Description
7:0	R/W	0x00	**HLPF_MD_X** [7:6]: HLPF_MD_X4 [5:4]: HLPF_MD_X3 [3:2]: HLPF_MD_X2 [1:0]: HLPF_MD_X1

Register 0x349 to 0x34B are for other channels in display down scaler. Register 0x34C to 0x34F are for record down scaler.

LIVE VIDEO PAL DELAY MODE REGISTER – 0X350

Bit	R/W	Default	Description
7:4	R/W	0xF	**HSCL_QUAD[3:0] Horizontal Scale Factor for REC Quad mode**
3:2	R/W	0x0	**HSCL_CIF[1:0]:** CIF down scaler horizontal ratio[1:0]
1	R	0x0	**Reserved**
0	R/W	0x00	**PAL_DLY_X**

LIVE VIDEO PAL DELAY MODE REGISTER – 0X351

Bit	R/W	Default	Description
7:4	R/W	0xF	**HSCL_QUAD[7:4] Horizontal Scale Factor for REC Quad mode**
3:2	R/W	0x0	**HSCL_CIF[3:2]:** CIF down scaler horizontal ratio[3:2]
1	R	0x0	**Reserved**
0	R/W	0x00	**PAL_DLY_Y**

LIVE VIDEO ODD FIELD SKEW REGISTER – 0X352

Bit	R/W	Default	Description
7:4	R/W	0xF	**HSCL_QUAD[11:8] Horizontal Scale Factor for REC Quad mode**
3:0	R/W	0x00	**ODD_SKEW**

LIVE VIDEO EVEN FIELD SKEW REGISTER – 0X353

Bit	R/W	Default	Description
7:4	R/W	0x7	HSCL_QUAD[15:12] Horizontal Scale Factor for REC Quad mode
3:0	R/W	0x00	EVEN_SKEW

LIVE VIDEO VERTICAL SCALER LPF REGISTER – 0X354

Bit	R/W	Default	Description
7:0	R/W	0x00	MAN_VSCL_LPFY [7]: MAN_VSCL_LPFY8 [6]: MAN_VSCL_LPFY7 [5]: MAN_VSCL_LPFY6 [4]: MAN_VSCL_LPFY5 [3]: MAN_VSCL_LPFY4 [2]: MAN_VSCL_LPFY3 [1]: MAN_VSCL_LPFY2 [0]: MAN_VSCL_LPFY1

Register 0x355 is for channel 9 to 16

LIVE VIDEO VERTICAL SCALE VAV TEST REGISTER – 0X356

Bit	R/W	Default	Description
7:2	R/W	0x00	HSCL_CIF[9:4]: CIF down scaler horizontal ratio[9:4]
1	R/W	0x00	IN16_MODE_PB5: 1 = set PB5 to 16bit operation
0	R/W	0x00	TST_VSCL_VAV

LIVE VIDEO CHANNEL 1 HORIZONTAL PIXEL ADJUSTMENT REGISTER – 0X375

Bit	R/W	Default	Description
7:0	R/W	0x00	HDELAY_X1[7:0]: Number of pixels times two. This is for display video.

Register 0x376 to 0x384 are for channel 2 to 16.

LIVE VIDEO CHANNEL 1,2 HORIZONTAL PIXEL ADJUSTMENT REGISTER – 0X385

Bit	R/W	Default	Description
7:4	RW	0x0	HDELAY_Y2[3:0]: Number of pixels times four. This is for record video.
3:0	RW	0x0	HDELAY_Y1[3:0]: Number of pixels times four. This is for record video.

Register 0x386 to 0x38A are for channel 3 to 16.

LIVE VIDEO CHANNEL 1,2 VERTICAL PIXEL ADJUSTMENT REGISTER – 0X38B

Bit	R/W	Default	Description
7:4	RW	0x0	VDELAY_Y2[3:0]: Number of lines times four. This is for record video.
3:0	RW	0x0	VDELAY_Y1[3:0]: Number of lines times four. This is for record video.

Register 0x38C to 0x394 are for channel 3 to 16.

LIVE VIDEO CHANNEL 1 VERTICAL PIXEL ADJUSTMENT REGISTER – 0X395

Bit	R/W	Default	Description
7:0	R/W	0x00	VDELAY_X1[7:0]: Number of lines times two. This is for display video.

Register 0x396 to 0x3A4 are for channel 2 to 16.

PB5 HORIZONTAL PIXEL ADJUSTMENT REGISTER – 0X3A5

Bit	R/W	Default	Description
7:0	RW	0x00	**HDELAY_PB5[7:0]:** Number of pixels times four. This is for PB.

PB5 VERTICAL PIXEL ADJUSTMENT REGISTER – 0X3A6

Bit	R/W	Default	Description
7:0	RW	0x00	**VDELAY_PB5[7:0]:** Number of lines times two. This is for PB.

PB5 HORIZONTAL SCALER SOURCE LSB REGISTER – 0X3A7

Bit	R/W	Default	Description
7:0	RW	0x00	**HSOR_PB5[7:0]** PB5 down scalar horizontal source size. **Unit is one pixel**.

PB5 HORIZONTAL SCALER TARGET LSB REGISTER – 0X3A8

Bit	R/W	Default	Description
7:0	RW	0x00	**HTAR_PB5[7:0]** PB5 down scalar horizontal target size. **Unit is one pixel**.

PB5 HORIZONTAL SCALER MSB REGISTER – 0X3A9

Bit	R/W	Default	Description
7	R	0	**Reserved**
6:4	RW	0	**HTAR_PB5[10:8]**: PB5 down scalar horizontal target size
3	R	0	**Reserved**
2:0	RW	0	**HSOR_PB5[10:8]**: PB5 down scalar horizontal source size

PB5 VERTICAL SCALER SOURCE LSB REGISTER – 0X3AA

Bit	R/W	Default	Description
7:0	RW	0x00	**VSOR_PB5[7:0]** PB5 down scalar vertical source size. **Unit is one line**. In interlaced Mode, this register should set to half of the vertical lines of one frame.

PB5 VERTICAL SCALER TARGET LSB REGISTER – 0X3AB

Bit	R/W	Default	Description
7:0	RW	0x00	VTAR_PB5[7:0] PB5 down scalar vertical target size. Unit is one line. In interlaced Mode, this register should set to half of the vertical lines of one frame.

PB5 VERTICAL SCALER MSB REGISTER – 0X3AC

Bit	R/W	Default	Description
7	RW	0	VBI_DLY5
6:4	RW	0	VTAR_PB5[10:8]: PB5 down scalar vertical target size
3	R	0	Reserved
2:0	RW	0	VSOR_PB5[10:8]: PB5 down scalar vertical source size

PB5 FORMAT CONTROL REGISTER 1 – 0X3AD

Bit	R/W	Default	Description
7	RW	0	BYPASS_PB5
6	RW	0	FLD_SEL_EN_PB5
5	RW	0	FLD_MODE_PB5
4	RW	0	FLD_MODE_PB5_EN
3	RW	0	FRAME_IL_PB5
2	RW	0	FRAME_IL_PB5_EN
1:0	RW	0	PB_MAN_NOVID5

PB5 FORMAT CONTROL REGISTER 2 – 0X3AE

Bit	R/W	Default	Description
7:4	RW	0	VBI_SIZE_PB5[3:0]
3	RW	0	VBI_E_EN_PB5
2	RW	0	VBI_O_EN_PB5
1	RW	0	TOGGLE_FLD5
0	RW	0	VS_DIS5

PB5 FORMAT CONTROL REGISTER 2 – 0X3AF

Bit	R/W	Default	Description
7:4	R	0	CHID_RD_SEL_PB5[3:0]
3	RW	0	VBI_RIC_ON_PB5
2	RW	0	VBI_AUTO_DET_PB5
1	RW	0	VBI_D_EN_PB5
0	RW	0	VBI_A_EN_PB5

PB CHANNEL ID DEC PB5 VOS – 0X3B0

Bit	R/W	Default	Description
7	R/W	0	**HD5 NO_SYNC_CHECK control** 0 HD5 no sync check enable 1 HD5 no sync check disable **NON_STD_STATUS (read only)** 0 = standard 1 = non standard
6	R/W	0	**SD5 NON_STANDARD_CHECK control** 0 SD5 non standard check enable 1 SD5 non standard check disable
5	R/W	0	**HD5 NO_VIDEO_CHECK control** 0 HD5 no video check enable 1 HD5 no video check disable
4:0	RW	0x0	**VBI_VOS_PB5** Line number of vertical offset for channel id in First field in unit of one.

PB CHANNEL ID DEC PB5 FOS – 0X3B1

Bit	R/W	Default	Description
7:5	RW	0x4	**VBI_PIXEL_WIDTH_PB5** Define half width of analog CHID sample rate.
4:0	RW	0x0	**VBI_FOS_PB5** Line number of vertical offset for channel id in second field in unit of one

PB CHANNEL ID DEC PB5 HOS – 0X3B2

Bit	R/W	Default	Description
7:0	RW	0x0	**VBI_HOS_PB5:** Pixel horizontal offset for channel.

PB CHANNEL ID DEC PB5 MID_VAL – 0X3B3

Bit	R/W	Default	Description
7:0	RW	0x1f	**VBI_MID_VAL_PB5** Middle value of VIS_HIGH_VAL and VIS_LOW_VAL in CHID encoder.

LIVE VIDEO CHANNEL 1~4 NO VIDEO REGISTER – 0X3BD

Bit	R/W	Default	Description
7:6	RW	0	**MAN_NOVID4**: definition same as MAN_NOVID1
5:4	RW	0	**MAN_NOVID3**: definition same as MAN_NOVID1
3:2	RW	0	**MAN_NOVID2**: definition same as MAN_NOVID1
1:0	RW	0	**MAN_NOVID1**: no video status override enable If bit 1 is set to 0, no video status is automatically detected by hardware (default). If bit 1 is set to 1, no video status is manually set by bit 0. To fully utilize this feature, user needs to enable TW2864/TW2865 MPP_MODE[5] bit 1: 1= enable no video status override bit 0: 1: no video, 0: has video

Register 0x3BE to 0x3C0 are for channel 5 to 16.

LIVE VIDEO CHANNEL 1~4 NON STANDARD REGISTER – 0X3C1

Bit	R/W	Default	Description
7:6	RW	0	**MAN_NONSTD4**: definition same as MAN_NONSTD1
5:4	RW	0	**MAN_NONSTD3**: definition same as MAN_NONSTD1
3:2	RW	0	**MAN_NONSTD2**: definition same as MAN_NONSTD1
1:0	RW	0	**MAN_NONSTD1**: non-standard video status override If bit 1 is set to 0, non-standard status is automatically detected by hardware (default). If bit 1 is set to one, non-standard status is manually set by bit 0. Bit 1: 1= enable non-standard video status override Bit 0: 1: non-standard video 0: standard video

Register 0x3C2 to 0x3C4 are for channel 5 to 16.

LIVE VIDEO CHANNEL CONTROL REGISTER – 0X3C5

Bit	R/W	Default	Description
7	R	0	**Reserved**
6	RW	0	**STILL_PAT** 0: moving pattern 1: still pattern
5	RW	0	**PALNT:** Only used for test pattern 0: NTSC pattern 1: PAL pattern
4	RW	0	**IN_TEST** 1 = Test pattern enable
3	RW	0	**Reserved**
2	RW	0	**CHID_BIT** 0: channel ID is 1 bit 1: channel ID is 2 bit
1	RW	0	**NO_CHID** 0: has channel ID in video data 1: no channel ID in video data

Bit	R/W	Default	Description
0	RW	0	**SYNC_CHID:** Channel ID location 0: in horizontal blank data last 2 bit 1: In timing reference data protection bit

LIVE VIDEO CHANNEL SYSTEM SELECT REGISTER – 0X3C6

Bit	R/W	Default	Description
7:2	R	0	**HSCL_CIF**[15:10]: CIF down scaler horizontal ratio[15:10]
1	R	0	**SEL960** 0: Select SD format 1: Select 960 format
0	RW	0	**SYS_60** 0: 50Hz, PAL 1: 60Hz, NTSC

TEST PATTERN VIDEO FORMAT SELECT REGISTER – 0X3CC

Bit	R/W	Default	Description
7	R	0	**Reserved**
6:4	R/W	0	**VID_FMT2:** Definition same as VID_FMT5
3	R	0	**Reserved**
2:0	RW	0	**VID_FMT1:** Definition same as VID_FMT5

TEST PATTERN VIDEO FORMAT SELECT REGISTER – 0X3CD

Bit	R/W	Default	Description
7	R	0	**Reserved**
6:4	R/W	0	**VID_FMT4:** Definition same as VID_FMT5
3	R	0	**Reserved**
2:0	RW	0	**VID_FMT3:** Definition same as VID_FMT5

TEST PATTERN VIDEO FORMAT SELECT REGISTER – 0X3CE

Bit	R/W	Default	Description
7	R	0	**Reserved**
6	R/W	0	**PURE_L:** Pure color for live test pattern
5	R/W	0	**PURE_P:** Pure color for PB test pattern
4:0	RW	0	**DYNAMIC[4:0]:** 1= change test pattern gen to FMI format

LIVE/RECORD CHANNEL SELECT REGISTER – 0X3D2

Bit	R/W	Default	Description
7:4	RW	1	VIN_SEL2 Input channel select for channel 2 for display or record. When VIN_SEL_XY is "0", this register is for display, when VIN_SEL_XY is "1", this register is for record.
3:0	RW	0	VIN_SEL1 Input channel select for channel 1.

Register 0x3D3 to 0x3D9 are for channel 3 to 16.

LIVE/RECORD SET SELECT REGISTER – 0X3DA

Bit	R/W	Default	Description
7	RW	0	VIN_SEL_XY This bit is used for select VIN_SEL X or Y. VIN_SEL share address for display and record. When VIN_SEL_XY is 0, VIN_SEL can be read/write for display. When VIN_SEL_XY is 1, VIN_SEL can be read/write for record.
6:1	R	0	Reserved
0	RW	1	V_OFST_X Vertical scale offset select

Digital Video Input (Type 2)

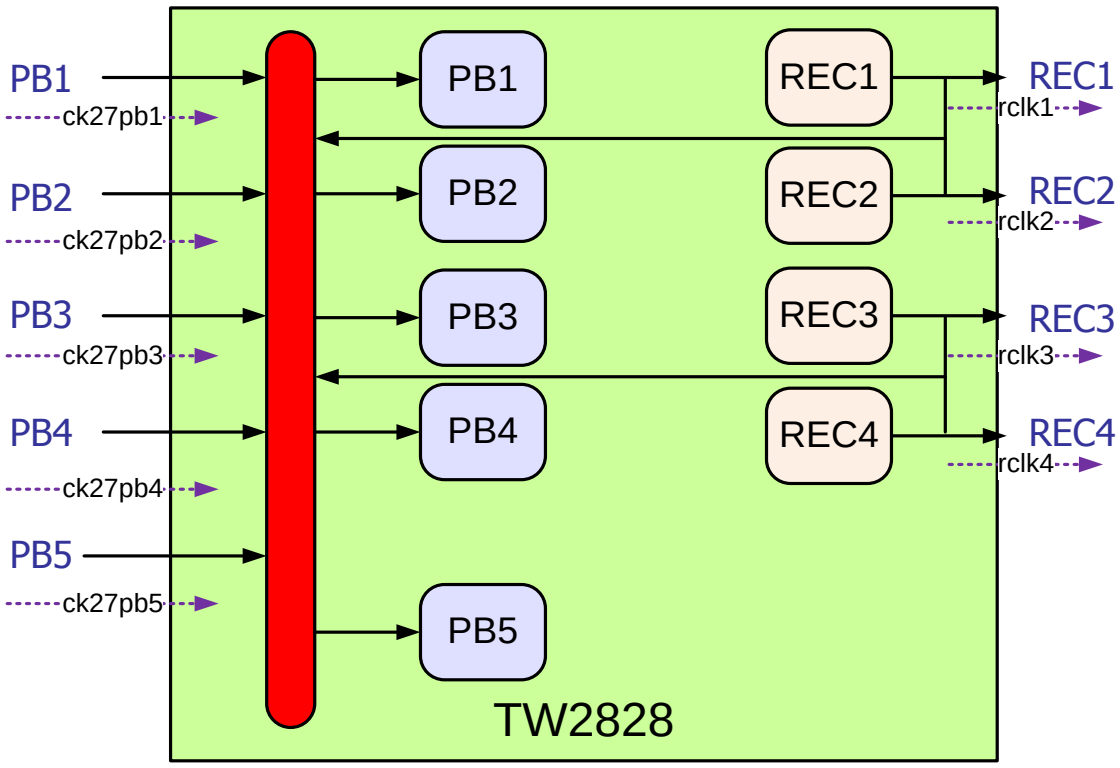
Introduction

TW2828 is equipped with 5 digital input port that can accept frame interleaved format. Type 2 input ports can be configured to support 8 bit BT.656 format or 16 bit BT.1120 format. The maximum number of the 8 bit port is four. The maximum number of 16 bit port is five. If channel ID is used, each input port can support up to 16 channels (auto mode). The maximum horizontal resolution is 1920 for each port. Data rate can be up to 148.5MHz. Each input port can support both interlace or progressive video. Five high quality down scalers applied to each port.

Features

- Five channel HD input support ITU-R BT.1120 up to 148.5 MHz
- Four channel SD input support ITU-R BT.656 up to 108 MHz
- Four channel WD1 input support ITU-R BT.656 up to 144MHz
- Channel ID detection in forms of analog and digital
- Cost efficient programmable down scalar with good quality
- Using same clock for input formatter and down scalar make the system flexible for different applications

Input Port Architecture



TYPE 2 port routing example

BT.656 MODE ARCHITECTURE

When using type 2 port to receive BT.656 stream, each port can handle one to four channels with different data rate (27/54/108 MHz or 36/72/144Mhz). Because each type 2 port has its own clock input which is controlled by the user so the frame rate of each receiving channel can be very flexible. For example, if a four-channels data stream is sent using frame interleaved format at 54 MHz, the frame rate will become 15 fps that makes this stream a non-real time stream. On the other hand if the data rate is 108 MHz then this channel combination is real time. TW2828 supports both real-time mode and non real-time stream but final display frame rate will be the smallest rate.

Three data formats are supported: Frame interleaved, Field interleaved and Field switching mode. The data and sync position diagram can be seen in recording section. For best viewing result don't mix video stream with different speed into the different input port. This will cause tearing or studder in the final display.

If the incoming stream has more than one channel this receiving mode is called auto mode. The video channels will be broken apart and stored into different places in the DDR2 SDRAM according to the channel ID. The maximum number of channels supported is 16. If each stream has only one channel and this is called normal mode receiving and maximum number of channels is four.

After each video data frame is received, the data will go through a down scaler to reshape and reposition the window in the final display. The size from the same port has to stay the same. The resizing circuitry make the composition of the final display very flexible. The down scaler can be by-pass to preserve video quality.

Play Back Architecture in 16-bit Mode

In BT.1120 HD input mode, the method and setting are similar to 8 bit mode except the input data format. In BT.1120 mode, one 8 bit port is for Y-data and the other port is for Cb-Cr data. Both data stream should have SAV and EAV flag and signature. The supported data formats are 74.25 MHz (1080i60 and 720p60), 148.5 MHz (1080p60) and 37.125 MHz (720p30).

FUNCTIONS

Input Formatter

Input formatter supports SD BT.656 in NTSC, PAL or non-standard video format. In HD BT.1120, it supports 1920x1080i. It generates Y, Cb and Cr data bus to down scalar. HSYNC, VSYNC and VALID signals generate accordingly. In BT.1120 mode, the input formatter can be set either take Y data or take Cb/Cr data and output Y or Cb/Cr will be generated respectively. Two input formatter's outputs go to one down scalar.

HDELAY and VDELAY can be configured to get portion of one frame for display.

Down Scalar

There are five down scalar for five play back ports. Down scale ratio register is different from live channels. Source width and height must be set correctly. And target width and height will be set to desired size.

Channel ID Decoder

TW2828 Channel ID Decoder is using same protocol of TW2828 Channel ID encoder. For the detail definition and description of Channel ID, please take a look at Channel ID Encoder Unit.

There are twelve words (lines) of channel ID: one word of Auto Channel ID, two words of Detection Channel ID, three words of User Channel ID and 6 words (192 bits) Motion Detection Channel ID. They can be represented in terms of digital and analog formats. One of them or both can be existed in BT.656 video bit stream. Usually, they appear in horizontal active area of vertical blanking period. Channel ID encoder may also possible program them to vertical active area. But in this design, it only allows it in the first two top lines of active video area to ensure proper display video image. Any Channel ID information program outside of top two lines of active video area in both fields will be ignored in both Channel ID encoder and decoder. Analog Channel ID follows after digital channel ID if digital channel ID exists.

There are two modes to decoding channel ID: Auto detection and Non-auto detection. Digital channel ID can be detected fully automatic. However, decoding analog channel ID even in Auto mode requires extra host configuration.

Decoded twelve words of channel ID data and corresponding valid signals are readable by host.

Bypass Down Scalar

Each channel has its configuration bit BYPASS_PB to bypass down scalar. Input formatter's output directly goes to rgb_interface for display.

Display Part of Video Frame

Incoming video frame can be display partially by configuring HDELAY and VDELAY. Down scalar still can be applied.

Register Descriptions

TOGGLE FIELD SIGNAL ENABLE REGISTER – 0X357

Bit	R/W	Default	Description
7:4	RW	0	TOGGLE_FLD4 - TOGGLE_FLD1 These bits are used for progressive play back capture mode. In progressive mode, field signal is always 0. If this bit is set to high, hardware will generate toggled field signal for channel ID decoder. It is toggled after 3 line of the beginning of vertical blank. 1: toggle field signal for channel ID decoder 0: use original field signal
3	RW	0	TST_FLDLY_Y
2	RW	0	TST_FLDLY_X
1	RW	0	TST_VSCL_Y
0	RW	0	TST_VSCL_X

PB1 VERTICAL TARGET SIZE LSB REGISTER – 0X358

Bit	R/W	Default	Description
7:0	RW	0xf0	VTAR_PB1[7:0] PB1 down scalar vertical target size. **Unit is one line**. In interlaced mode, this register should set to half of the vertical lines of one frame.

PB1 AND PB2 VERTICAL TARGET SIZE MSB REGISTER – 0X359

Bit	R/W	Default	Description
6:4	RW	0x0	VTAR_PB2[10:8] PB2 down scalar vertical target size. **Unit is one line**. In interlaced mode, this register is set to half of the vertical lines of one frame.
2:0	RW	0x0	VTAR_PB1[10:8] PB1 down scalar vertical target size. **Unit is one line**. In interlaced mode, this register is set to half of the vertical lines of one frame.

PB2 VERTICAL TARGET SIZE LSB REGISTER – 0X35A

Bit	R/W	Default	Description
7:0	RW	0xf0	VTAR_PB2[7:0] PB2 down scalar vertical target size. **Unit is one line**. In interlaced mode, this register is set to half of the vertical lines of one frame.

Register 0x35B to 0x35D are for PB channel 3 and 4.

PB1 VERTICAL SOURCE SIZE LSB REGISTER – 0X35E

Bit	R/W	Default	Description
7:0	RW	0xf0	VSOR_PB1[7:0] PB1 down scalar vertical source size. **Unit is one line**. In interlaced mode, this register is set to half of the vertical lines of one frame.

PB1 AND PB2 VERTICAL SOURCE SIZE MSB REGISTER – 0X35F

Bit	R/W	Default	Description
6:4	RW	0x00	VSOR_PB2[10:8] PB2 down scalar vertical source size. **Unit is one line**. In interlaced mode, this register is set to half of the vertical lines of one frame.
2:0	RW	0x0	VSOR_PB1[10:8] PB1 down scalar vertical source size. **Unit is one line**. In interlaced mode, this register is set to half of the vertical lines of one frame.

PB2 VERTICAL SOURCE SIZE LSB REGISTER – 0X360

Bit	R/W	Default	Description
7:0	RW	0xf0	VSOR_PB2[7:0] PB2 down scalar vertical source size. **Unit is one line**. In interlaced mode, this register is set to half of the vertical lines of one frame.

Register 0x361 to 0x363 are for PB channel 3 and 4.

PB1 HORIZONTAL SCALER TARGET LSB REGISTER – 0X364

Bit	R/W	Default	Description
7:0	RW	0xd0	HTAR_PB1[7:0] PB1 down scalar horizontal target size. **Unit is one pixel**.

PB1 AND PB2 HORIZONTAL TARGET SIZE MSB REGISTER – 0X365

Bit	R/W	Default	Description
6:4	RW	0x2	HTAR_PB2[10:8] PB2 down scalar horizontal target size. **Unit is one pixel**.
2:0	RW	0x2	HTAR_PB1[10:8] PB1 down scalar horizontal target size. **Unit is one pixel**.

PB2 HORIZONTAL SCALER TARGET LSB REGISTER – 0X366

Bit	R/W	Default	Description
7:0	RW	0xd0	HTAR_PB2[7:0] PB2 down scalar horizontal target size. **Unit is one pixel**.

Register 0x367 to 0x369 is for channel 3 and 4.

PB1 HORIZONTAL SCALER SOURCE LSB REGISTER – 0X36A

Bit	R/W	Default	Description
7:0	RW	0xd0	HSOR_PB1[7:0] PB1 down scalar horizontal source size. **Unit is one pixel**.

PB1 AND PB2 HORIZONTAL SOURCE SIZE MSB REGISTER – 0X36B

Bit	R/W	Default	Description
6:4	RW	0x2	**HSOR_PB2[10:8]** PB2 down scalar horizontal source size. **Unit is one pixel.**
2:0	RW	0x2	**HSOR_PB1[10:8]** PB1 down scalar horizontal source size. **Unit is one pixel.**

PB2 HORIZONTAL SCALER SOURCE LSB REGISTER – 0X36C

Bit	R/W	Default	Description
7:0	RW	0xd0	**HSOR_PB2[7:0]** PB2 down scalar horizontal source size. **Unit is one pixel.**

Register 0x36D to 0x36F is for channel 3 and 4.

PB Auto Downscale and Bypass Register – 0x370

Bit	R/W	Default	Description
7:4	RW	0	**QUAD_AUTO_SCL_PB4 - QUAD_AUTO_SCL_PB1** Down scale ratio can be changed in multi-mode for each play back port 1: enable, D1 and Quad is 2:1 in down scale ratio 0: disable, down scale ratio keep same
3:0	RW	0x1	**BYPASS_PB4 - BYPASS_PB1** Bypass down scalar. Video data from in_fmt_27 directly go to rgb_interface for display. 1: enable 0: disable

PB MISC CONTROL REGISTER – 0X371

Bit	R/W	Default	Description
7	RW	0x0	**Output Select: 1 = Select 0x372, 0x373 alternate read**
6	RW	0x0	**SYNC_SEL:** When this bit is set to high, use external H/V/F sync. 1: use external sync 0: use embedded sync
5	RW	0x1	**YC_SWITCH:** 0 = high byte is Y, Control all PB ports
4	RW	0	**SYNC656_SEL** 1 = Play back port sync from state machine 0 = Play back port sync from byte compare
3	RW	0	**IN16_MODE_PB4:** Play back port 4 data is 16bit or 8bit 1: 16bit 0: 8bit

Bit	R/W	Default	Description
2	RW	0	**IN16_MODE_PB3:** Play back port 3 data is 16bit or 8bit 1: 16bit 0: 8bit
1	RW	0	**IN16_MODE_PB2:** Play back port 2 data is 16bit or 8bit 1: 16bit 0: 8bit
0	RW	0	**IN16_MODE_PB1:** Play back port 1 data is 16bit or 8bit 1: 16bit 0: 8bit

PB YC COMPONENT SWITCH REGISTER – 0X372

Bit	R/W	Default	Description
7:5	RW	0x0	**SEL_PB_CH[2:0]** Select PB channels for SD or HD to define start/end sync position of active video data through 0x3. 0 : To set start/end sync position for HD channel 1 1 : To set start/end sync position for HD channel 2 2 : To set start/end sync position for HD channel 3 3 : To set start/end sync position for HD channel 4 4 : To set start/end sync position for HD channel 5 5 : To set Pixel Width for SD channels 6 : To set Line Count for SD channels 7 : To set Line Width for SD channels If 3FF [7] = 1, the read data of 0x3FC - 0x3FF is CHID of PB4.
5	RW	0x0	**YC_SWITCH5:** Set this bit to 1 will enable PB port 5 Y/C input switch. This is a physical switch including the embedded signals and channels ID. This switch is used in 16 bit mode only.
4	RW	0x0	**YC_SWITCH4:** Set this bit to 1 will enable PB port 4 Y/C input switch. This is a physical switch including the embedded signals and channels ID. This switch is used in 16 bit mode only.
3	RW	0x1	**YC_SWITCH3:** Set this bit to 1 will enable PB port 3 Y/C input switch. This is a physical switch including the embedded signals and channels ID. This switch is used in 16 bit mode only.
1	RW	0x0	**YC_SWITCH2:** Set this bit to 1 will enable PB port 2 Y/C input switch. This is a physical switch including the embedded signals and channels ID. This switch is used in 16 bit mode only.
0	RW	0x0	**YC_SWITCH1:** Set this bit to 1 will enable PB port 1 Y/C input switch. This is a physical switch including the embedded signals and channels ID. This switch is used in 16 bit mode only.

The read part of this register and the next one are controlled by 0x371[7].

PB TEST INPUT CONTROL REGISTER – 0X373

Bit	R/W	Default	Description
7	RW	0x0	**TSEL: 1 =** Select 0XCC, 0XCD, 0XCE read output as PB2 CHID
6	RW	0x0	**Reserved**
5	RW	0x0	**IN_PB_TEST5:** Set this bit to 1 will enable PB port 5 test mode where the input is coming from a pattern generator. This can be in 8 bit mode or 16 bit mode. Only normal mode pattern are supplied.
4	RW	0x0	**IN_PB_TEST4:** Set this bit to 1 will enable PB port 4 test mode where the input is coming from a pattern generator. This can be in 8 bit mode or 16 bit mode. Only normal mode pattern are supplied.
3	RW	0x1	**IN_PB_TEST3:** Set this bit to 1 will enable PB port 3 test mode where the input is coming from a pattern generator. This can be in 8 bit mode or 16 bit mode. Only normal mode pattern are supplied.
1	RW	0x0	**IN_PB_TEST2:** Set this bit to 1 will enable PB port 2 test mode where the input is coming from a pattern generator. This can be in 8 bit mode or 16 bit mode. Only normal mode pattern are supplied.
0	RW	0x0	**IN_PB_TEST1:** Set this bit to 1 will enable PB port 1 test mode where the input is coming from a pattern generator. This can be in 8 bit mode or 16 bit mode. Only normal mode pattern are supplied.

PB CHANNEL ID DEC READ BUS PB1 BYTE 1– 0X372

Bit	R/W	Default	Description
7:0	R	0x7	**CHID_RD_BUS_PB1[39:32]** Read CHID_rd_bus_pb1[39:32]. Depend on CHID_RD_SEL_PB1(REG OX3DE), it read one of six CHID word: 0: auto CHID [7] digital_chid_valid_pb1, 1: D CHID valid, 0: A CHID valid [6] auto_valid_pb1, 1: auto_CHID valid, 0 not valid [5:0] auto_chid_pb1[37:32] 1: detection CHID1 [7] digital_chid_valid_pb1, 1: D CHID valid, 0: A CHID valid [4] det1_valid_pb1, 1: det1_CHID valid, 0 not valid [3:0] det1_chid_pb1[35:32] 2: detection CHID2 [7] digital_chid_valid_pb1, 1: D CHID valid, 0: A CHID valid [4] det2_valid_pb1, 1: det2_CHID valid, 0 not valid [3:0] det2_chid_pb1[35:32] 3: Motion detection CHID1 [7] digital_chid_valid_pb1, 1: D CHID valid, 0: A CHID valid [4] det3_valid_pb1, 1: det2_CHID valid, 0 not valid [3:0] de3_chid_pb1[35:32] 4: Motion detection CHID1 [7] digital_chid_valid_pb1, 1: D CHID valid, 0: A CHID valid [4] det4_valid_pb1, 1: det4_CHID valid, 0 not valid [3:0] det4_chid_pb1[35:32] 5: Motion detection CHID1 [7] digital_chid_valid_pb1, 1: D. CHID valid, 0: A. CHID valid [4] det5_valid_pb1, 1: det5_CHID valid, 0 not valid [3:0] det5_chid_pb1[35:32]

Bit	R/W	Default	Description
			6: Motion detection CHID1 [7] digital_chid_valid_pb1, 1: D CHID valid, 0: A CHID valid [4] det6_valid_pb1, 1: det6_CHID valid, 0 not valid [3:0] det6_chid_pb1[35:32] 7: Motion detection CHID1 [7] digital_chid_valid_pb1, 1: D CHID valid, 0: A CHID valid [4] det7_valid_pb1, 1: det7_CHID valid, 0 not valid [3:0] det7_chid_pb1[35:32] 8: Motion detection CHID1 [7] digital_chid_valid_pb1, 1: D CHID valid, 0: A CHID valid [4] det8_valid_pb1, 1: det8_CHID valid, 0 not valid [3:0] det8_chid_pb1[35:32] 9: user CHID1 [7] digital_chid_valid_pb1, 1: D CHID valid, 0: A CHID valid [4] usr1_valid_pb1, 1: usr1_CHID valid, 0 not valid [3:0] usr1_chid_pb1[35:32] a: user CHID2 [7] digital_chid_valid_pb1, 1: D CHID valid, 0: A CHID valid [4] usr2_valid_pb1, 1: usr2_CHID valid, 0 not valid [3:0] usr2_chid_pb1[35:32] b: user CHID3 [7] digital_chid_valid_pb1, 1: D CHID valid, 0: A CHID valid [4] usr3_valid_pb1, 1: usr3_CHID valid, 0 not valid [3:0] usr3_chid_pb1[35:32]

To get most up-to-date channel ID on four PB ports, write any value to 0x372 to trigger a self update process.

PB CHANNEL ID DEC READ BUS PB1 BYTE 2 – 0X373

Bit	R/W	Default	Description
7:0	R	0x0	CHID_RD_BUS_PB1[31:24] Read CHID_rd_bus_pb1[31:24]. Depend on CHID_RD_SEL_PB1(REG 0X3DE), it read one of six CHID word: 0: auto CHID [7:0] auto_chid_pb1[31:24] 1: detection CHID1 [7:0] det1_chid_pb1[31:24] 2: detection CHID2 [7:0] det2_chid_pb1[31:24] 3: Motion detection CHID1 [7:0] det3_chid_pb1[31:24] 4: Motion detection CHID1 [7:0] det4_chid_pb1[31:24] 5: Motion detection CHID1 [7:0] det5_chid_pb1[31:24] 6: Motion detection CHID1 [7:0] det6_chid_pb1[31:24] 7: Motion detection CHID1 [7:0] det7_chid_pb1[31:24] 8: Motion detection CHID1 [7:0] det8_chid_pb1[31:24]

Bit	R/W	Default	Description
			9: user CHID1 [7:0] usr1_chid_pb1[31:24] a: user CHID2 [7:0] usr2_chid_pb1[31:24] b: user CHID3 [7:0] usr3_chid_pb1[31:24]

PB CHANNEL ID DEC READ BUS PB1 BYTE 3 – 0X374

Bit	R/W	Default	Description
7:0	R	0x7	CHID_RD_BUS_PB1[23:16] Read CHID_rd_bus_pb1[23:16]. Depend on CHID_RD_SEL_PB1(REG 0X3DE), it read one of six CHID word: 0: auto CHID [7:0] auto_chid_pb1[23:16] 1: detection CHID1 [7:0] det1_chid_pb1[23:16] 2: detection CHID2 [7:0] det2_chid_pb1[23:16] 3: Motion detection CHID1 [7:0] det3_chid_pb1[23:16] 4: Motion detection CHID1 [7:0] det4_chid_pb1[23:16] 5: Motion detection CHID1 [7:0] det5_chid_pb1[23:16] 6: Motion detection CHID1 [7:0] det6_chid_pb1[23:16] 7: Motion detection CHID1 [7:0] det7_chid_pb1[23:16] 8: Motion detection CHID1 [7:0] det8_chid_pb1[23:16] 9: user CHID1 [7:0] usr1_chid_pb1[23:16] a: user CHID2 [7:0] usr2_chid_pb1[23:16] b: user CHID3 [7:0] usr3_chid_pb1[23:16]

HORIZONTAL DELAY FOR PLAYBACK PORT 1 REGISTER – 0X3B5

Bit	R/W	Default	Description
7:0	RW	0x0	HDELAY_PB1 Horizontal Delay (Cut off left side) of horizontal active picture in unit of two pixels.

VERTICAL DELAY FOR PLAYBACK PORT 1 REGISTER – 0X3B6

Bit	R/W	Default	Description
7:0	RW	0x0	VDELAY_PB1 Horizontal Delay (Cut off top portion) of vertical active picture in unit of one line.

Register 0x3B7 to 0x3BC are for PB port 2 to 4

PB CHANNEL ID DEC READ BUS PB1 BYTE 4 – 0X3C7

Bit	R/W	Default	Description
7:0	R	0x7	CHID_RD_BUS_PB1[15:8] Read CHID_rd_bus_pb1[15:8]. Depend on CHID_RD_SEL_PB1(REG 0X3DE), it read one of six CHID word: 0: auto CHID [7:0] auto_chid_pb1[15:8] 1: detection CHID1 [7:0] det1_chid_pb1[15:8] 2: detection CHID2 [7:0] det2_chid_pb1[15:8] 3: Motion detection CHID1 [7:0] det3_chid_pb1[15:8] 4: Motion detection CHID1 [7:0] det4_chid_pb1[15:8] 5: Motion detection CHID1 [7:0] det5_chid_pb1[15:8] 6: Motion detection CHID1 [7:0] det6_chid_pb1[15:8] 7: Motion detection CHID1 [7:0] det7_chid_pb1[15:8] 8: Motion detection CHID1 [7:0] det8_chid_pb1[15:8] 9: user CHID1 [7:0] usr1_chid_pb1[15:8] a: user CHID2 [7:0] usr2_chid_pb1[15:8] b: user CHID3 [7:0] usr3_chid_pb1[15:8]

PB CHANNEL ID DEC READ BUS PB1 BYTE 5 – 0X3C8

Bit	R/W	Default	Description
7:0	RO	0x7	CHID_RD_BUS_PB1[7:0] Read CHID_rd_bus_pb1[7:0]. Depend on CHID_RD_SEL_PB1(REG 0X3DE), it read one of six CHID word: 0: auto CHID [7:0] auto_chid_pb1[7:0] 1: detection CHID1 [7:0] det1_chid_pb1[7:0] 2: detection CHID2 [7:0] det2_chid_pb1[7:0] 3: Motion detection CHID1 [7:0] det3_chid_pb1[7:0] 4: Motion detection CHID1 [7:0] det4_chid_pb1[7:0]

Bit	R/W	Default	Description
			5: Motion detection CHID1 [7:0] det5_chid_pb1[7:0] 6: Motion detection CHID1 [7:0] det6_chid_pb1[7:0] 7: Motion detection CHID1 [7:0] det7_chid_pb1[7:0] 8: Motion detection CHID1 [7:0] det8_chid_pb1[7:0] 9: user CHID1 [7:0] usr1_chid_pb1[7:0] a: user CHID2 [7:0] usr2_chid_pb1[7:0] b: user CHID3 [7:0] usr3_chid_pb1[7:0]

Register 0x3C9 to 0x3D1 are for PB port 2 to 4

PB IN_PB_TEST REGISTER – 0X3DC

Bit	R/W	Default	Description
7:5	RW	0x0	**VID_FMT[2:0]:** HD test sequence generator format selection 101 = 720p30 100 = 720p60 011 = 1080i50 010 = 1080i60 001 = 1080i50 000 = 1080i60 Default:1080i60
4	RW	0x0	**DIR2:** PB test pattern generator BT1120_gen2 color bar shift direction. 1: shift to left 0: shift to right
3	RW	0x1	**DIR1:** PB test pattern generator BT1120_gen1 color bar shift direction. 1: shift to left 0: shift to right
2:1	RW	0x0	**Frame Rate** PB test pattern generator color bar shift frame rate for both BT1120_gen1 and BT1120_gen2 0: change every 16 frame 1: change every 32 frame Others: change every 64 frame
0	RW	0x0	**IN_PB_TEST:** PB test pattern generator color bar for PB in BT.1120 1: enable PB HD color bar generator 0: disable. PB use data from port.

PB IN_PB_TEST PATTERN GENERATOR COLOR BAR SHIFT VOLUME – 0X3DD

Bit	R/W	Default	Description
7:0	RW	0x0	**PIXEL_SHIFT** HD Color bar shift volume in unit of pixel

PB CHANNEL ID DEC PB1 CTRL – 0X3DE

Bit	R/W	Default	Description
7:4	RW	0x0	**CHID_RD_SEL_PB1** Host selects one of 11 CHID words to read. b: User CHID3 a: User CHID2 9: User CHID1 8: Motion detection CHID6 7: Motion detection CHID5 6: Motion detection CHID4 5: Motion detection CHID3 4: Motion detection CHID2 3: Motion detection CHID1 2: Detection CHID2 1: Detection CHID1 0: Auto CHID
3	RW	0x1	**VBI_RIC_ON_PB1** Enable run in clock detection. It should be same as CHID encoder configured. 1: enable 0: disable
2	RW	0x1	**VBI_AUTO_DET_PB1** Automatic detect channel ID for digital channel ID vertical offset and analog channel ID run in clock frequency. 1: enable 0: disable
1	RW	0x1	**VBI_D_EN_PB1:** Enable digital CHID. It should be same as CHID encoder 1: enable 0: disable
0	RW	0x1	**VBI_A_EN_PB1:** Enable analog CHID. It should be same as CHID encoder, if both enable then use analog CHID. 1: enable 0: disable

PB CHANNEL ID DEC PB1 VOS – 0X3DF

Bit	R/W	Default	Description
7	R/W	0	**HD1 NO_SYNC_CHECK control** 0 HD1 no sync check enable 1 HD1 no sync check disable **NON_STD_STATUS (read only)** 0 = standard

Bit	R/W	Default	Description
			1 = non standard
6	R/W	0	**SD1 NON_STANDARD_CHECK control** 0 SD1 non standard check enable 1 SD1 non standard check disable
5	R/W	0	**HD1 NO_VIDEO_CHECK control** 0 HD1 no video check enable 1 HD1 no video check disable
4:0	RW	0x0	**VBI_VOS_PB1** Line number of vertical offset for channel id in First field in unit of one.

PB CHANNEL ID DEC PB1 FOS – 0X3E0

Bit	R/W	Default	Description
7:5	RW	0x4	**VBI_PIXEL_WIDTH_PB1** Define half width of analog CHID sample rate.
4:0	RW	0x0	**VBI_FOS_PB1** Line number of vertical offset for channel id in second field in unit of one

PB CHANNEL ID DEC PB1 HOS – 0X3E1

Bit	R/W	Default	Description
7:0	RW	0x0	**VBI_HOS_PB1:** Pixel horizontal offset for channel.

PB CHANNEL ID DEC PB1 MID_VAL – 0X3E2

Bit	R/W	Default	Description
7:0	RW	0x1f	**VBI_MID_VAL_PB1** Middle value of VIS_HIGH_VAL and VIS_LOW_VAL in CHID encoder.

PB CHANNEL ID DEC PB2 VAL – 0X3E3

Bit	R/W	Default	Description
7:4	RW	0x0	**CHID_RD_SEL_PB2**
3	RW	0x1	**VBI_RIC_ON_PB2**
2	RW	0x1	**VBI_AUTO_DET_PB2**
1	RW	0x1	**VBI_D_EN_PB2**
0	RW	0x1	**VBI_A_EN_PB2**

PB CHANNEL ID DEC PB2 VOS – 0X3E4

Bit	R/W	Default	Description
7	RW	0	HD2 NO_SYNC_CHECK control 0 HD2 no sync check enable 1 HD2 no sync check disable NON_STD_STATUS (read only) 0 = standard 1 = non standard
6	RW	0	SD2 NON_STANDARD_CHECK control 0 SD2 non standard check enable 1 SD2 non standard check disable
5	RW	0	HD2 NO_VIDEO_CHECK control 0 HD2 no video check enable 1 HD2 no video check disable
4:0	RW	0x0	VBI_VOS_PB2 Line number of vertical offset for channel id in First field in unit of one.

PB CHANNEL ID DEC PB2 VOS – 0X3E5

Bit	R/W	Default	Description
7:5	RW	0	VBI_PIXEL_WIDTH_PB2
4:0	RW	0x80	VBI_FOS_PB2

PB CHANNEL ID DEC PB2 HOS – 0X3E6

Bit	R/W	Default	Description
7:0	RW	0x0	VBI_HOS_PB2

PB CHANNEL ID DEC PB2 MID_VAL – 0X3E7

Bit	R/W	Default	Description
7:0	RW	0x1f	VBI_MID_VAL_PB2 Middle value of VIS_HIGH_VAL and VIS_LOW_VAL in CHID encoder.

PB CHANNEL ID DEC PB3 VAL – 0X3E8

Bit	R/W	Default	Description
7:4	RW	0	CHID_RD_SEL_PB3
3	RW	1	VBI_RIC_ON_PB3
2	RW	1	VBI_AUTO_DET_PB3
1	RW	1	VBI_D_EN_PB3
0	RW	1	VBI_A_EN_PB3

PB CHANNEL ID DEC PB3 VOS – 0X3E9

Bit	R/W	Default	Description
7	RW	0	HD3 NO_SYNC_CHECK control 0 HD3 no sync check enable 1 HD3 no sync check disable NON_STD_STATUS (read only) 0 = standard 1 = non standard
6	RW	0	SD3 NON_STANDARD_CHECK control 0 SD3 non standard check enable 1 SD3 non standard check disable
5	RW	0	HD3 NO_VIDEO_CHECK control 0 HD3 no video check enable 1 HD3 no video check disable
4:0	RW	0x0	VBI_VOS_PB3 Line number of vertical offset for channel id in First field in unit of one.

PB CHANNEL ID DEC PB3 VOS – 0X3EA

Bit	R/W	Default	Description
7:5	RW	0	VBI_PIXEL_WIDTH_PB3
4:0	RW	0x0	VBI_FOS_PB3

PB CHANNEL ID DEC PB3 HOS – 0X3EB

Bit	R/W	Default	Description
7:0	RW	0x01	VBI_HOS_PB3: Pixel horizontal offset for channel.

PB CHANNEL ID DEC PB3 MID_VAL – 0X3EC

Bit	R/W	Default	Description
7:0	RW	0x01	VBI_MID_VAL_PB3[7:0] Middle value of VIS_HIGH_VAL and VIS_LOW_VAL in CHID encoder.

PB CHANNEL ID DEC PB4 VAL – 0X3ED

Bit	R/W	Default	Description
7:4	RW	0	CHID_RD_SEL_PB4[3:0]
3	RW	1	VBI_RIC_ON_PB4
2	RW	1	VBI_AUTO_DET_PB4
1	RW	1	VBI_D_EN_PB4
0	RW	1	VBI_A_EN_PB4

PB CHANNEL ID DEC PB4 VOS – 0X3EE

Bit	R/W	Default	Description
7	RW	0	**HD4 NO_SYNC_CHECK control** 0 HD4 no sync check enable 1 HD4 no sync check disable **NON_STD_STATUS (read only)** 0 = standard 1 = non standard
6	RW	0	**SD4 NON_STANDARD_CHECK control** 0 SD4 non standard check enable 1 SD4 non standard check disable
5	RW	0	**HD4 NO_VIDEO_CHECK control** 0 HD4 no video check enable 1 HD4 no video check disable
4:0	RW	0x0	**VBI_VOS_PB4** Line number of vertical offset for channel id in First field in unit of one.

PB CHANNEL ID DEC PB4 VOS – 0X3EF

Bit	R/W	Default	Description
7:5	RW	0x4	**VBI_PIXEL_WIDTH_PB4**
4:0	RW	0x0	**VBI_FOS_PB4**

PB CHANNEL ID DEC PB4 HOS – 0X3F0

Bit	R/W	Default	Description
7:0	RW	0x01	**VBI_HOS_PB4:** Pixel horizontal offset for channel.

PB CHANNEL ID DEC PB4 MID_VAL – 0X3F1

Bit	R/W	Default	Description
7:0	RW	0x01	**VBI_MID_VAL_PB4** Middle value of VIS_HIGH_VAL and VIS_LOW_VAL in CHID encoder.

PB FRAME/FIELD CONTROL REGISTER – 0X3F2

Bit	R/W	Default	Description
7:4	RW	0	**FRAME_IL_PB4_EN – FRAME_IL_PB1_EN:** Force the receiving mode of PB4 – PB1 to follow the value of bit [3:0]. 1: enable 0: disable

Bit	R/W	Default	Description
3:0	RW	0	**FRAME_IL_PB4 - FRAME_IL_PB1:** Host define the stream is frame interleaved or field interleaved. 1: field interleaved mode (auto), interlaced mode (normal) 0: frame interleaved mode (auto), progressive mode (normal)

PB FIELD MODE REGISTER – 0X3F3

Bit	R/W	Default	Description
7:4	RW	0	**FLD_MODE_PB4_EN - FLD_MODE_PB1_EN:** Manual set field mode 1: enable, get field mode from **FLD_MODE_PB4-1** 0: disable, get field mode from channel ID
3:0	RW	0	**FLD_MODE_PB4 - FLD_MODE_PB1:** Field mode in manual mode for port 4-1 1: even field when fld is 0 0: even field when fld is 1

PB DIGITAL CHANNEL ID ENABLE REGISTER – 0X3F4

Bit	R/W	Default	Description
7:4	RW	0xf	**VBI_E_EN_PB4 - VBI_E_EN_PB1:** Digital CHID even field enable 1: enable 0: disable
3:0	RW	0xf	**VBI_O_EN_PB4 - VBI_O_EN_PB1:** Digital CHID odd field enable 1: enable 0: disable

PB3 CHID READ BUS REGISTER 2 – 0X3F5

Bit	R/W	Default	Description
7:0	R	0x0	**CHID_RD_BUS_PB3[15:8]**

PB3 CHID READ BUS REGISTER 1 – 0X3F6

Bit	R/W	Default	Description
7:0	R	0x0	**CHID_RD_BUS_PB3 [7:0]**

PB3 CHID READ BUS REGISTER 5 – 0X3F7

Bit	R/W	Default	Description
7:0	R	0x0	**CHID_RD_BUS_PB4 [39:32]**

NON-STANDARD VIDEO UPPER LIMIT – HD REGISTER – 0X3F8

Bit	R/W	Default	Description
7:0	R/W	0x2F	**HD_UP_LIM[7:0] :** HD line counter upper limit LSB

NON-STANDARD VIDEO UPPER LIMIT – HD REGISTER – 0X3F9

Bit	R/W	Default	Description
7:3			**Reserve**
2:0	R/W	0x2	**HD_ UP_LIM[10:8] :** HD line counter upper limit MSB

NON-STANDARD VIDEO LOWER LIMIT – HD REGISTER – 0X3FA

Bit	R/W	Default	Description
7:0	R/W	0x09	**HD_DOWN_LIM[7:0] :** HD line counter lower limit LSB

NON-STANDARD VIDEO LOWER LIMIT – HD REGISTER – 0X3FB

Bit	R/W	Default	Description
7:3			**Reserve**
2:0	R/W	0x02	**HD_DOWN_LIM[10:8] :** HD line counter lower limit MSB

When 372 [7:5] = 0, HD channel 1 setting.

When 372 [7:5] = 1, HD channel 2 setting.

When 372 [7:5] = 2, HD channel 3 setting.

When 372 [7:5] = 3, HD channel 4 setting.

When 372 [7:5] = 4, HD channel 5 setting.

NON-STANDARD VIDEO PIXEL WIDTH – SD REGISTER – 0X3F8

Bit	R/W	Default	Description
7:0	R/W	0x0F	**SD_PIXEL_WIDTH[7:0] :** SD pixel width for non standard status LSB

NON-STANDARD VIDEO PIXEL WIDTH – SD REGISTER – 0X3F9

Bit	R/W	Default	Description
7:4			**Reserve**
3:0	R/W	0	**SD_PIXEL_WIDTH [11:8] :** SD pixel width for non standard status MSB

When 372 [7:5] = 5, SD_PIXEL_WIDTH setting.

NON-STANDARD VIDEO NON STANDARD LINE COUNTER – SD REGISTER – 0X3F8

Bit	R/W	Default	Description
7:0	R/W	0x04	**SD_LINE_CNT[7:0] :** Line count value for non standard

When 372 [7:5] = 6, SD_LINE_CNT setting.

NON-STANDARD VIDEO LINE WIDTH – SD REGISTER – 0X3F8

Bit	R/W	Default	Description
7:0	R/W	0x0F	**SD_LINE_WIDTH[7:0] :** SD line width for non standard status

When 372 [7:5] = 7, SD_LINE_WIDTH setting.

When 3FF [7] = 1, the read data of 0x3FC - 0x3FF is CHID of PB4.

PB CHID DECODER CONTROL REGISTER – 0X3FC

Bit	R/W	Default	Description
7:4	RW	0	**VBI_DLY4 - VBI_DLY1:** 1 = New field signal delay one line. It is used for digital channel ID in first active line.
3:0	RW	0	**FLD_SEL_EN_PB4 - FLD_SEL_EN_PB1:** Field signal source selection 1: from embedded field signature. 0: from channel ID

When 3C6 [1] = 1, the read data of 0x3FC and 0x3FD is non-standard video signal of live channels.

ANALOG CHANNEL ID LINE NUMBER REGISTER 1 – 0X3FD

Bit	R/W	Default	Description
7:4	RW	0xE	**VBI_SIZE_PB2** Analog channel ID line number for PB port 2
3:0	RW	0xE	**VBI_SIZE_PB1** Analog channel ID line number for PB port 1

ANALOG CHANNEL ID LINE NUMBER REGISTER 2 – 0X3FE

Bit	R/W	Default	Description
7:4	RW	0xE	**VBI_SIZE_PB4:** Analog channel ID line number for PB port 4
3:0	RW	0xE	**VBI_SIZE_PB3:** Analog channel ID line number for PB port 3

MISC. CONTROL REGISTER – 0X3FF

Bit	R/W	Default	Description
7	RW	0	**selm:** This bit selects the read output of 0x3f8 – 0x3fb 1: Output of PB port channel ID 0: Output of 0x3f8 – ox3fb.
6:5	RW	0	**Reserved**
4	RW	0	**DIG_CODE:** This bit selects digital channel ID start code 1: 0x80_9F_80_90 0: 0x00_9F_00_90

Bit	R/W	Default	Description
3:0	RW	0	**VS_DIS4 – VS_DIS1:** New field signal disabled in even field for progressive mode 1: disable even field new field signal 0: don't disable even field new field signal

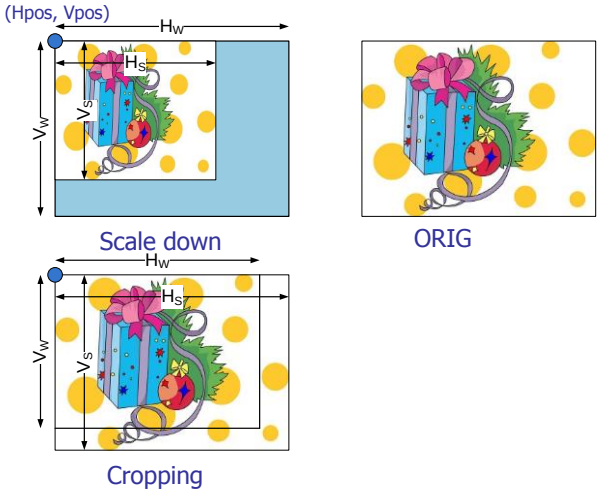
Video Write Buffer (RGBW)

Introduction

TW2828 has incorporated 36 write buffers to support 16 live video channels and 20 playback channels. Each channel has its own registers for users to adjust window width, height, starting positions and orientations. Each live channel can support up to D1 size while for playback channel the resolution can go up to HD (1920x1080). One thing to remember is in this HD configuration, only two windows are available. All write requests from the buffers will be summed up and prioritized in the mux unit and later sent to DDR2 SDRAM controller. Each channel need to be programmed to write to different locations in DDR2 SDRAM.

Window Control

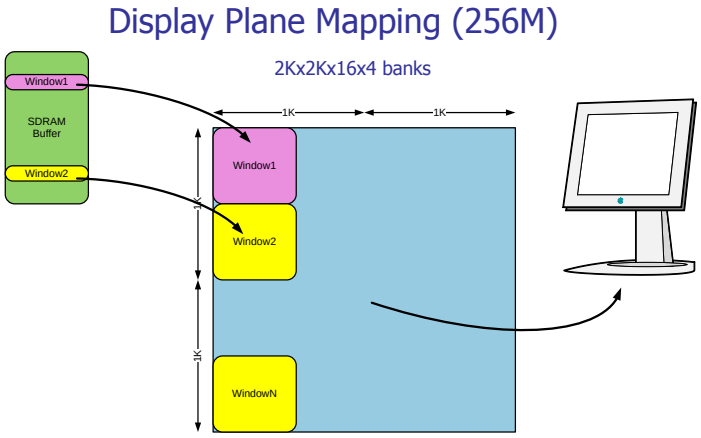
Each window in the display path has its own set of control. It can be enabled and disable. The height, width and the starting position of the window is adjustable. User can mirror the image horizontally or vertically to compensate the position of the camera. Cropping is also supported if the display window size is smaller than the incoming signal. One thing to be remembered is windows cannot be overlapped otherwise artifact will appear in the display area.



Display Map Control

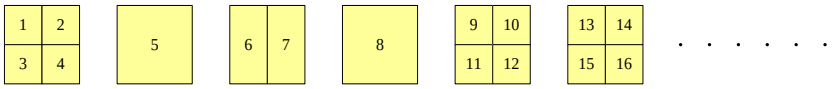
When updating video information, all channels are writing into the same bank of display memory. When display controller read data, it will read out the data sequentially. The bank control of the reading and writing controller is handled by Frame Rate Control Module (FRSC) and is discussed in detailed in later sections.

TW2828 has a different display map control when 2D de-interlacing is deployed.



Play Back Channels

Play back channels can support several modes, such as interlaced or progressive. And also for one play back port, different formats can be support in different frames, such as D1, half D1, CIF and Quad. And also different channels being in one port is possible. Data rate in play back channel can be 27/36MHz, 54/72MHz or 108/144MHz. In BT1120 case, clock can be 74.25MHz. Here is an example for one play back port.



Play back write control unit can write different channels to different location in DDR2 SDRAM. User can set size and location register for different channels. There are total 20 groups of register for play back channels. These registers share address with live channels. Channel number and format information is given by play back channel ID decoder unit.

If play back port has only one channel and data rate is 27/36MHz, it can be set to normal write buffer mode. In normal mode, channel number is not used.

In summary, play back write control unit can support two mode: auto mode and normal mode. In auto mode, channel data will be written to different location according to channel number. In normal mode, channel data will be written to one location according to port number.

Register Table

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x600	R/W	0	rgb_wr_ctrl0 [3]: freeze0 [2]: wr_en0 [1]: hinv0 [0]: vinv0
0x601	R/W	0	rgb_wr_ctrl1 [3]: freeze1 [2]: wr_en1 [1]: hinv1 [0]: vinv1
0x602	R/W	0	rgb_wr_ctrl2 [3]: freeze2 [2]: wr_en2 [1]: hinv2 [0]: vinv2
0x603	R/W	0	rgb_wr_ctrl3 [3]: freeze3 [2]: wr_en3 [1]: hinv3 [0]: vinv3
0x604	R/W	0	rgb_wr_ctrl4 [3]: freeze4 [2]: wr_en4 [1]: hinv4 [0]: vinv4
0x605	R/W	0	rgb_wr_ctrl5 [3]: freeze5 [2]: wr_en5 [1]: hinv5 [0]: vinv5
0x606	R/W	0	rgb_wr_ctrl6 [3]: freeze6 [2]: wr_en6 [1]: hinv6 [0]: vinv6
0x607	R/W	0	rgb_wr_ctrl7 [3]: freeze7 [2]: wr_en7 [1]: hinv7 [0]: vinv7
0x608	R/W	0	rgb_wr_ctrl8 [3]: freeze8 [2]: wr_en8 [1]: hinv8 [0]: vinv8
0x609	R/W	0	rgb_wr_ctrl9 [3]: freeze9 [2]: wr_en9 [1]: hinv9 [0]: vinv9
0x60A	R/W	0	rgb_wr_ctrl10 [3]: freeze10 [2]: wr_en10 [1]: hinv10 [0]: vinv10

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x60B	R/W	0	rgb_wr_ctrl11 [3]: freeze11 [2]: wr_en11 [1]: hinv11 [0]: vinv11
0x60C	R/W	0	rgb_wr_ctrl12 [3]: freeze12 [2]: wr_en12 [1]: hinv12 [0]: vinv12
0x60D	R/W	0	rgb_wr_ctrl13 [3]: freeze13 [2]: wr_en13 [1]: hinv13 [0]: vinv13
0x60E	R/W	0	rgb_wr_ctrl14 [3]: freeze14 [2]: wr_en14 [1]: hinv14 [0]: vinv14
0x60F	R/W	0	rgb_wr_ctrl15 [3]: freeze15 [2]: wr_en15 [1]: hinv15 [0]: vinv15
0x610	R/W	0	rgb_wr_ctrl16: PB1 [7]: No valid video present, read only [6]: FSEL_0 [5:4]: fmt_sel_0 [3]: freeze16 [2]: wr_en16 [1]: hinv16 [0]: vinv16
0x611	R/W	0	rgb_wr_ctrl17: PB2 [7]: No valid video present, read only [6]: FSEL_1 [5:4]: fmt_sel_1 [3]: freeze17 [2]: wr_en17 [1]: hinv17 [0]: vinv17
0x612	R/W	0	rgb_wr_ctrl18: PB3 [7]: No valid video present, read only [6]: FSEL_2 [5:4]: fmt_sel_2 [3]: freeze18 [2]: wr_en18 [1]: hinv18 [0]: vinv18
0x613	R/W	0	rgb_wr_ctrl19: PB4 [7]: No valid video present, read only [6]: FSEL_3 [5:4]: fmt_sel_3 [3]: freeze19 [2]: wr_en19 [1]: hinv19 [0]: vinv19

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x614	R/W	0	rgb_vpos0_live[7:0] / rgb_vpos0_pb[7:0]
0x615	R/W	0	rgb_vpos0_live[11:8] / rgb_vpos0_pb[11:8]
0x616	R/W	0	rgb_vpos1_live[7:0] / rgb_vpos1_pb[7:0]
0x617	R/W	0	rgb_vpos1_live[11:8] / rgb_vpos1_pb[11:8]
0x618	R/W	0	rgb_vpos2_live[7:0] / rgb_vpos2_pb[7:0]
0x619	R/W	0	rgb_vpos2_live[11:8] / rgb_vpos2_pb[11:8]
0x61A	R/W	0	rgb_vpos3_live[7:0] / rgb_vpos3_pb[7:0]
0x61B	R/W	0	rgb_vpos3_live[11:8] / rgb_vpos3_pb[11:8]
0x61C	R/W	0	rgb_vpos4_live[7:0] / rgb_vpos4_pb[7:0]
0x61D	R/W	0	rgb_vpos4_live[11:8] / rgb_vpos4_pb[11:8]
0x61E	R/W	0	rgb_vpos5_live[7:0] / rgb_vpos5_pb[7:0]
0x61F	R/W	0	rgb_vpos5_live[11:8] / rgb_vpos5_pb[11:8]
0x620	R/W	0	rgb_vpos6_live[7:0] / rgb_vpos6_pb[7:0]
0x621	R/W	0	rgb_vpos6_live[11:8] / rgb_vpos6_pb[11:8]
0x622	R/W	0	rgb_vpos7_live[7:0] / rgb_vpos7_pb[7:0]
0x623	R/W	0	rgb_vpos7_live[11:8] / rgb_vpos7_pb[11:8]
0x624	R/W	0	rgb_vpos8_live[7:0] / rgb_vpos8_pb[7:0]
0x625	R/W	0	rgb_vpos8_live[11:8] / rgb_vpos8_pb[11:8]
0x626	R/W	0	rgb_vpos9_live[7:0] / rgb_vpos9_pb[7:0]
0x627	R/W	0	rgb_vpos9_live[11:8] / rgb_vpos9_pb[11:8]
0x628	R/W	0	rgb_vpos10_live[7:0] / rgb_vpos10_pb[7:0]
0x629	R/W	0	rgb_vpos10_live[11:8] / rgb_vpos10_pb[11:8]
0x62A	R/W	0	rgb_vpos11_live[7:0] / rgb_vpos11_pb[7:0]
0x62B	R/W	0	rgb_vpos11_live[11:8] / rgb_vpos11_pb[11:8]
0x62C	R/W	0	rgb_vpos12_live[7:0] / rgb_vpos12_pb[7:0]
0x62D	R/W	0	rgb_vpos12_live[11:8] / rgb_vpos12_pb[11:8]
0x62E	R/W	0	rgb_vpos13_live[7:0] / rgb_vpos13_pb[7:0]
0x62F	R/W	0	rgb_vpos13_live[11:8] / rgb_vpos13_pb[11:8]
0x630	R/W	0	rgb_vpos14_live[7:0] / rgb_vpos14_pb[7:0]
0x631	R/W	0	rgb_vpos14_live[11:8] / rgb_vpos14_pb[11:8]
0x632	R/W	0	rgb_vpos15_live[7:0] / rgb_vpos15_pb[7:0]
0x633	R/W	0	rgb_vpos15_live[11:8] / rgb_vpos15_pb[11:8]
0x634	R/W	0	rgb_vpos16_pb[7:0]
0x635	R/W	0	rgb_vpos16_pb[11:8]
0x636	R/W	0	rgb_vpos17_pb[7:0]
0x637	R/W	0	rgb_vpos17_pb[11:8]
0x638	R/W	0	rgb_vpos18_pb[7:0]
0x639	R/W	0	rgb_vpos18_pb[11:8]
0x63A	R/W	0	rgb_vpos19_pb[7:0]
0x63B	R/W	0	rgb_vpos19_pb[11:8]
0x63C	R/W	0	rgb_vsize0_live[7:0] / rgb_vsize0_pb[7:0]
0x63D	R/W	0	rgb_vsize0_live[10:8] / rgb_vsize0_pb[10:8]
0x63E	R/W	0	rgb_vsize1_live[7:0] / rgb_vsize1_pb[7:0]
0x63F	R/W	0	rgb_vsize1_live[10:8] / rgb_vsize1_pb[10:8]
0x640	R/W	0	rgb_vsize2_live[7:0] / rgb_vsize2_pb[7:0]
0x641	R/W	0	rgb_vsize2_live[10:8] / rgb_vsize2_pb[10:8]
0x642	R/W	0	rgb_vsize3_live[7:0] / rgb_vsize3_pb[7:0]
0x643	R/W	0	rgb_vsize3_live[10:8] / rgb_vsize3_pb[10:8]
0x644	R/W	0	rgb_vsize4_live[7:0] / rgb_vsize4_pb[7:0]
0x645	R/W	0	rgb_vsize4_live[10:8] / rgb_vsize4_pb[10:8]
0x646	R/W	0	rgb_vsize5_live[7:0] / rgb_vsize5_pb[7:0]
0x647	R/W	0	rgb_vsize5_live[10:8] / rgb_vsize5_pb[10:8]
0x648	R/W	0	rgb_vsize6_live[7:0] / rgb_vsize6_pb[7:0]
0x649	R/W	0	rgb_vsize6_live[10:8] / rgb_vsize6_pb[10:8]

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x64A	R/W	0	rgb_vsize7_live[7:0] / rgb_vsize7_pb[7:0]
0x64B	R/W	0	rgb_vsize7_live[10:8] / rgb_vsize7_pb[10:8]
0x64C	R/W	0	rgb_vsize8_live[7:0] / rgb_vsize8_pb[7:0]
0x64D	R/W	0	rgb_vsize8_live[10:8] / rgb_vsize8_pb[10:8]
0x64E	R/W	0	rgb_vsize9_live[7:0] / rgb_vsize9_pb[7:0]
0x64F	R/W	0	rgb_vsize9_live[10:8] / rgb_vsize9_pb[10:8]
0x650	R/W	0	rgb_vsize10_live[7:0] / rgb_vsize10_pb[7:0]
0x651	R/W	0	rgb_vsize10_live[10:8] / rgb_vsize10_pb[10:8]
0x652	R/W	0	rgb_vsize11_live[7:0] / rgb_vsize11_pb[7:0]
0x653	R/W	0	rgb_vsize11_live[10:8] / rgb_vsize11_pb[10:8]
0x654	R/W	0	rgb_vsize12_live[7:0] / rgb_vsize12_pb[7:0]
0x655	R/W	0	rgb_vsize12_live[10:8] / rgb_vsize12_pb[10:8]
0x656	R/W	0	rgb_vsize13_live[7:0] / rgb_vsize13_pb[7:0]
0x657	R/W	0	rgb_vsize13_live[10:8] / rgb_vsize13_pb[10:8]
0x658	R/W	0	rgb_vsize14_live[7:0] / rgb_vsize14_pb[7:0]
0x659	R/W	0	rgb_vsize14_live[10:8] / rgb_vsize14_pb[10:8]
0x65A	R/W	0	rgb_vsize15_live[7:0] / rgb_vsize15_pb[7:0]
0x65B	R/W	0	rgb_vsize15_live[10:8] / rgb_vsize15_pb[10:8]
0x65C	R/W	0	rgb_vsize16_pb[7:0]
0x65D	R/W	0	rgb_vsize16_pb[10:8]
0x65E	R/W	0	rgb_vsize17_pb[7:0]
0x65F	R/W	0	rgb_vsize17_pb[10:8]
0x660	R/W	0	rgb_vsize18_pb[7:0]
0x661	R/W	0	rgb_vsize18_pb[10:8]
0x662	R/W	0	rgb_vsize19_pb[7:0]
0x663	R/W	0	rgb_vsize19_pb[10:8]
0x664	R/W	0	rgb_hpos0_live[7:0] / rgb_hpos0_pb[7:0]
0x665	R/W	0	rgb_hpos0_live[9:8] / rgb_hpos0_pb[9:8]
0x666	R/W	0	rgb_hpos1_live[7:0] / rgb_hpos1_pb[7:0]
0x667	R/W	0	rgb_hpos1_live[9:8] / rgb_hpos1_pb[9:8]
0x668	R/W	0	rgb_hpos2_live[7:0] / rgb_hpos2_pb[7:0]
0x669	R/W	0	rgb_hpos2_live[9:8] / rgb_hpos2_pb[9:8]
0x66A	R/W	0	rgb_hpos3_live[7:0] / rgb_hpos3_pb[7:0]
0x66B	R/W	0	rgb_hpos3_live[9:8] / rgb_hpos3_pb[9:8]
0x66C	R/W	0	rgb_hpos4_live[7:0] / rgb_hpos4_pb[7:0]
0x66D	R/W	0	rgb_hpos4_live[9:8] / rgb_hpos4_pb[9:8]
0x66E	R/W	0	rgb_hpos5_live[7:0] / rgb_hpos5_pb[7:0]
0x66F	R/W	0	rgb_hpos5_live[9:8] / rgb_hpos5_pb[9:8]
0x670	R/W	0	rgb_hpos6_live[7:0] / rgb_hpos6_pb[7:0]
0x671	R/W	0	rgb_hpos6_live[9:8] / rgb_hpos6_pb[9:8]
0x672	R/W	0	rgb_hpos7_live[7:0] / rgb_hpos7_pb[7:0]
0x673	R/W	0	rgb_hpos7_live[9:8] / rgb_hpos7_pb[9:8]
0x674	R/W	0	rgb_hpos8_live[7:0] / rgb_hpos8_pb[7:0]
0x675	R/W	0	rgb_hpos8_live[9:8] / rgb_hpos8_pb[9:8]
0x676	R/W	0	rgb_hpos9_live[7:0] / rgb_hpos9_pb[7:0]
0x677	R/W	0	rgb_hpos9_live[9:8] / rgb_hpos9_pb[9:8]
0x678	R/W	0	rgb_hpos10_live[7:0] / rgb_hpos10_pb[7:0]
0x679	R/W	0	rgb_hpos10_live[9:8] / rgb_hpos10_pb[9:8]
0x67A	R/W	0	rgb_hpos11_live[7:0] / rgb_hpos11_pb[7:0]
0x67B	R/W	0	rgb_hpos11_live[9:8] / rgb_hpos11_pb[9:8]
0x67C	R/W	0	rgb_hpos12_live[7:0] / rgb_hpos12_pb[7:0]
0x67D	R/W	0	rgb_hpos12_live[9:8] / rgb_hpos12_pb[9:8]
0x67E	R/W	0	rgb_hpos13_live[7:0] / rgb_hpos13_pb[7:0]
0x67F	R/W	0	rgb_hpos13_live[9:8] / rgb_hpos13_pb[9:8]

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x680	R/W	0	rgb_hpos14_live[7:0] / rgb_hpos14_pb[7:0]
0x681	R/W	0	rgb_hpos14_live[9:8] / rgb_hpos14_pb[9:8]
0x682	R/W	0	rgb_hpos15_live[7:0] / rgb_hpos15_pb[7:0]
0x683	R/W	0	rgb_hpos15_live[9:8] / rgb_hpos15_pb[9:8]
0x684	R/W	0	rgb_hpos16_pb[7:0]
0x685	R/W	0	rgb_hpos16_pb[9:8]
0x686	R/W	0	rgb_hpos17_pb[7:0]
0x687	R/W	0	rgb_hpos17_pb[9:8]
0x688	R/W	0	rgb_hpos18_pb[7:0]
0x689	R/W	0	rgb_hpos18_pb[9:8]
0x68A	R/W	0	rgb_hpos19_pb[7:0]
0x68B	R/W	0	rgb_hpos19_pb[9:8]
0x68C	R/W	0	rgb_hsize0_live[7:0] / rgb_hsize0_pb[7:0]
0x68D	R/W	0	rgb_hsize0_live[8] / rgb_hsize0_pb[8]
0x68E	R/W	0	rgb_hsize1_live[7:0] / rgb_hsize1_pb[7:0]
0x68F	R/W	0	rgb_hsize1_live[8] / rgb_hsize1_pb[8]
0x690	R/W	0	rgb_hsize2_live[7:0] / rgb_hsize2_pb[7:0]
0x691	R/W	0	rgb_hsize2_live[8] / rgb_hsize2_pb[8]
0x692	R/W	0	rgb_hsize3_live[7:0] / rgb_hsize3_pb[7:0]
0x693	R/W	0	rgb_hsize3_live[8] / rgb_hsize3_pb[8]
0x694	R/W	0	rgb_hsize4_live[7:0] / rgb_hsize4_pb[7:0]
0x695	R/W	0	rgb_hsize4_live[8] / rgb_hsize4_pb[8]
0x696	R/W	0	rgb_hsize5_live[7:0] / rgb_hsize5_pb[7:0]
0x697	R/W	0	rgb_hsize5_live[8] / rgb_hsize5_pb[8]
0x698	R/W	0	rgb_hsize6_live[7:0] / rgb_hsize6_pb[7:0]
0x699	R/W	0	rgb_hsize6_live[8] / rgb_hsize6_pb[8]
0x69A	R/W	0	rgb_hsize7_live[7:0] / rgb_hsize7_pb[7:0]
0x69B	R/W	0	rgb_hsize7_live[8] / rgb_hsize7_pb[8]
0x69C	R/W	0	rgb_hsize8_live[7:0] / rgb_hsize8_pb[7:0]
0x69D	R/W	0	rgb_hsize8_live[8] / rgb_hsize8_pb[8]
0x69E	R/W	0	rgb_hsize9_live[7:0] / rgb_hsize9_pb[7:0]
0x69F	R/W	0	rgb_hsize9_live[8] / rgb_hsize9_pb[8]
0x6A0	R/W	0	rgb_hsize10_live[7:0] / rgb_hsize10_pb[7:0]
0x6A1	R/W	0	rgb_hsize10_live[8] / rgb_hsize10_pb[8]
0x6A2	R/W	0	rgb_hsize11_live[7:0] / rgb_hsize11_pb[7:0]
0x6A3	R/W	0	rgb_hsize11_live[8] / rgb_hsize11_pb[8]
0x6A4	R/W	0	rgb_hsize12_live[7:0] / rgb_hsize12_pb[7:0]
0x6A5	R/W	0	rgb_hsize12_live[8] / rgb_hsize12_pb[8]
0x6A6	R/W	0	rgb_hsize13_live[7:0] / rgb_hsize13_pb[7:0]
0x6A7	R/W	0	rgb_hsize13_live[8] / rgb_hsize13_pb[8]
0x6A8	R/W	0	rgb_hsize14_live[7:0] / rgb_hsize14_pb[7:0]
0x6A9	R/W	0	rgb_hsize14_live[8] / rgb_hsize14_pb[8]
0x6AA	R/W	0	rgb_hsize15_live[7:0] / rgb_hsize15_pb[7:0]
0x6AB	R/W	0	rgb_hsize15_live[8] / rgb_hsize15_pb[8]
0x6AC	R/W	0	rgb_hsize16_pb[7:0]
0x6AD	R/W	0	rgb_hsize16_pb[8]
0x6AE	R/W	0	rgb_hsize17_pb[7:0]
0x6AF	R/W	0	rgb_hsize17_pb[8]
0x6B0	R/W	0	rgb_hsize18_pb[7:0]
0x6B1	R/W	0	rgb_hsize18_pb[8]
0x6B2	R/W	0	rgb_hsize19_pb[7:0]
0x6B3	R/W	0	rgb_hsize19_pb[8]

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x6B4	R/W	0	[7:4]: newfld_sel [3]: mode [2]: TST_IN_PB [1]: PALNT [0]: TST_IN
0x6B5	R/W	0	Test_timing_replace[7:0]
0x6B6	R/W	0	[7]: line_bigger_en_pb [6]: line_bigger_en [5]: use_novid [4:3]: skip_sel [2]: prot_en [1]: CHID_sel [0]: live_pb
0x6B7	R/W	0	[7:4]: pb1_chnum [3:0]: pb0_chnum
0x6B8	R/W	0	[7:4]: pb3_chnum [3:0]: pb2_chnum
0x6B9	R/W	0	[7:6]: IGNON_NONSTD[1:0] [5]: NONSTD_IRQ_MASK [4]: read select [3:0]: pb3_chnum_en – pb0_chnum_en
0x6BB	R/W	0	Pb_ch_frez[7:0]
0x6BC	R/W	0	Pb_ch_frez[15:8]
0x6BD	R/W	0	Prot_addr[7:0]
0x6BE	R/W	0	Prot_addr[15:8]
0x6BF	R/W	0	Prot_addr[21:16]
0x6C0	R/W	0	rgb_hstart0_live[7:0] / rgb_hstart0_pb[7:0]
0x6C1	R/W	0	rgb_hstart1_live[7:0] / rgb_hstart1_pb[7:0]
0x6C2	R/W	0	rgb_hstart2_live[7:0] / rgb_hstart2_pb[7:0]
0x6C3	R/W	0	rgb_hstart3_live[7:0] / rgb_hstart3_pb[7:0]
0x6C4	R/W	0	rgb_hstart4_live[7:0] / rgb_hstart4_pb[7:0]
0x6C5	R/W	0	rgb_hstart5_live[7:0] / rgb_hstart5_pb[7:0]
0x6C6	R/W	0	rgb_hstart6_live[7:0] / rgb_hstart6_pb[7:0]
0x6C7	R/W	0	rgb_hstart7_live[7:0] / rgb_hstart7_pb[7:0]
0x6C8	R/W	0	rgb_hstart8_live[7:0] / rgb_hstart8_pb[7:0]
0x6C9	R/W	0	rgb_hstart9_live[7:0] / rgb_hstart9_pb[7:0]
0x6CA	R/W	0	rgb_hstart10_live[7:0] / rgb_hstart10_pb[7:0]
0x6CB	R/W	0	rgb_hstart11_live[7:0] / rgb_hstart11_pb[7:0]
0x6CC	R/W	0	rgb_hstart12_live[7:0] / rgb_hstart12_pb[7:0]
06CD	R/W	0	rgb_hstart13_live[7:0] / rgb_hstart13_pb[7:0]
0x6CE	R/W	0	rgb_hstart14_live[7:0] / rgb_hstart14_pb[7:0]
0x6CF	R/W	0	rgb_hstart15_live[7:0] / rgb_hstart15_pb[7:0]
0x6D0	R/W	0	rgb_hstart16_pb[7:0]
0x6D1	R/W	0	rgb_hstart17_pb[7:0]
0x6D2	R/W	0	rgb_hstart18_pb[7:0]
0x6D3	R/W	0	rgb_hstart19_pb[7:0]
0x6D4	R/W	0	rgb_vstart0_live[7:0] / rgb_vstart0_pb[7:0]
0x6D5	R/W	0	rgb_vstart1_live[7:0] / rgb_vstart1_pb[7:0]
0x6D6	R/W	0	rgb_vstart2_live[7:0] / rgb_vstart2_pb[7:0]
0x6D7	R/W	0	rgb_vstart3_live[7:0] / rgb_vstart3_pb[7:0]
0x6D8	R/W	0	rgb_vstart4_live[7:0] / rgb_vstart4_pb[7:0]
0x6D9	R/W	0	rgb_vstart5_live[7:0] / rgb_vstart5_pb[7:0]
0x6DA	R/W	0	rgb_vstart6_live[7:0] / rgb_vstart6_pb[7:0]
0x6DB	R/W	0	rgb_vstart7_live[7:0] / rgb_vstart7_pb[7:0]
0x6DC	R/W	0	rgb_vstart8_live[7:0] / rgb_vstart8_pb[7:0]

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x6DD	R/W	0	rgb_vstart9_live[7:0] / rgb_vstart9_pb[7:0]
0x6DE	R/W	0	rgb_vstart10_live[7:0] / rgb_vstart10_pb[7:0]
0x6DF	R/W	0	rgb_vstart11_live[7:0] / rgb_vstart11_pb[7:0]
0x6E0	R/W	0	rgb_vstart12_live[7:0] / rgb_vstart12_pb[7:0]
06E1	R/W	0	rgb_vstart13_live[7:0] / rgb_vstart13_pb[7:0]
0x6E2	R/W	0	rgb_vstart14_live[7:0] / rgb_vstart14_pb[7:0]
0x6E3	R/W	0	rgb_vstart15_live[7:0] / rgb_vstart15_pb[7:0]
0x6E4	R/W	0	rgb_vstart16_pb[7:0]
0x6E5	R/W	0	rgb_vstart17_pb[7:0]
0x6E6	R/W	0	rgb_vstart18_pb[7:0]
0x6E7	R/W	0	rgb_vstart19_pb[7:0]
0x6E8	R/W	0	Live port 1, 0 correction control
0x6E9	R/W	0	Live port 3, 2 correction control
0x6EA	R/W	0	Live port 5, 4 correction control
0x6EB	R/W	0	Live port 7, 6 correction control
0x6EC	R/W	0	Live port 9, 8 correction control
0x6ED	R/W	0	Live port 11, 10 correction control
0x6EE	R/W	0	Live port 13, 12 correction control
0x6EF	R/W	0	Live port 15, 14 correction control
0x6F0	RO	0	linenum_pb0[7:0]
0x6F1	RO	0	linenum_pb0[11:8]
0x6F0	RW	0	PB port 1, 0 correction control, shared
0x6F1	RW	0	PB port 3, 2 correction control, shared
0x6F2	RO	0	linenum_pb1[7:0]
0x6F3	RO	0	linenum_pb1[11:8]
0x6F4	RO	0	linenum_pb2[7:0]
0x6F5	RO	0	linenum_pb2[11:8]
0x6F6	RO	0	linenum_pb3[7:0]
0x6F7	RO	0	linenum_pb3[11:8]
0x6F8	R/W	0	[7]: write to clear [3:0]: pb3_valid – pb0_valid
0x6F9	R/W	0	[7:0]: period2 external correction period
0x6FA	R/W	0	[7:4]: Enable ignore function [3:0]: pb_free_3 – pb_free_0
0x6FB	R/W	0x1C	[7:4]: fifo_cnt_limit [3]: fld_update [2]: fld_sel_fix [1]: fld_sel_en [0]: vstart_unit_pb
0x6FC	R/W	0	[7:6]: address select [5]: Force live use ols method [4]: seld [3]: test_960_720 [2]: CAS_EN [1]: hstart_unit_pb, 1= 8 pixels [0]: vinv_sel
0x6FD	R/W	0	pb_ch_en[7:0]
0x6FE	R/W	0	pb_ch_en[15:8]
0x6FF	R/W	0	period[7:0] internal correction period

Register

DISPLAY WRITE BUFFER CONTROL REGISTER – 0X600

Bit	R/W	Default	Description
7:4	R	0	**Reserved**
3	R/W	0	**Freeze** 1 = Enable 0 = Disable
2	R/W	0	**Buffer Operation** 1 = Enable 0 = Disable
1	R/W	0	**Horizontal Inversion** 1 = Enable 0 = Disable
0	R/W	0	**Vertical Inversion** 1 = Enable 0 = Disable

Similar registers are assigned to control Display Write Buffer 2 to 15 using register 0x601 – 0x60F respectively.

DISPLAY WRITE BUFFER CONTROL REGISTER – 0X610

Bit	R/W	Default	Description
7	R	0	**1 = No valid video signal present**
6	R/W	0	**FSEL_0** 0 = channel format equals 2'b11 1 = channel format equals fmt_sel_0
5:4	R/W	0	**fmt_sel_0** user channel format
3	R/W	0	**Freeze** 1 = Enable 0 = Disable
2	R/W	0	**Buffer Operation** 1 = Enable 0 = Disable
1	R/W	0	**Horizontal Inversion** 1 = Enable 0 = Disable
0	R/W	0	**Vertical Inversion** 1 = Enable 0 = Disable

Similar registers are assigned to control Display Write Buffer 17 to 20 using register 0x611 – 0x613, 0x6bd (shadow) respectively.

DISPLAY WRITE BUFFER VERTICAL POSITION REGISTER A – 0X614

Bit	R/W	Default	Description
7:0	R/W	0	Vertical Position[7:0]

DISPLAY WRITE BUFFER VERTICAL POSITION REGISTER B – 0X615

Bit	R/W	Default	Description
7:4	R	0	Reserved
3:0	R/W	0	Vertical Position[11:8]

Similar registers are assigned to control Display Write Buffer 2 to 20 using register 0x616 – 0x63B respectively.

NOTE: VERTICAL POSITION MUST BE EVEN NUMBER.

In auto mode, when register live_pb (0x6B6.0) is set to 0, these registers are for live channel 1-16 as rgb_vpos0_live to rgb_vpos15_live. When live_pb is set to 1, these registers are for PB channel 1-16 in auto mode as rgb_vpos0_pb to rgb_vpos15_pb. They share address in this configuration. Register rgb_vpos16_pb to rgb_vpos19_pb are used in normal mode for PB1-PB4. If CAS_EN (0x6fc.2) is set to one and live_pb (0x6B6.0) is set to 1, rgb_vpos12_pb to rgb_vpos15_pb is used as PB5 auto mode registers. If live_pb (0x6B6.0) is set to 0, then rgb_vpos12_live is set to PB5 normal register.

DISPLAY WRITE BUFFER VERTICAL SIZE REGISTER A – 0X63C

Bit	R/W	Default	Description
7:0	R/W	0	Vertical Size[7:0]

DISPLAY WRITE BUFFER VERTICAL SIZE REGISTER B – 0X63D

Bit	R/W	Default	Description
7:3	R	0	Reserved
2:0	R/W	0	Vertical Size[10:8]

Similar registers are assigned to control Display Write Buffer 2 to 20 using register 0x63E – 0x663 respectively.

Vertical size must be even number.

In auto mode, when register live_pb (0x6B6.0) is set to 0, these registers are for live channel 1-16 as rgb_vsize0_live to rgb_vsize15_live. When live_pb is set to 1, these registers are for PB channel 1-16 in auto mode as rgb_vsize0_pb to rgb_vsize15_pb. They share address in this configuration. Register rgb_vsize16_pb to rgb_vsize19_pb are used in normal mode for PB1-PB4. If CAS_EN (0x6fc.2) is set to one and live_pb (0x6B6.0) is set to 1, rgb_vsize12_pb to rgb_vsize15_pb is used as PB5 auto mode registers. If live_pb (0x6B6.0) is set to 0, then rgb_vsize12_live is set to PB5 normal register.

DISPLAY WRITE BUFFER HORIZONTAL POSITION REGISTER A – 0X664

Bit	R/W	Default	Description
7:0	R/W	0	Horizontal Position[7:0], unit is 4 pixels

DISPLAY WRITE BUFFER HORIZONTAL POSITION REGISTER B – 0X665

Bit	R/W	Default	Description
7:1	R	0	Reserved
0	R/W	0	Horizontal Position[8]

Similar registers are assigned to control Display Write Buffer 2 to 20 using register 0x666 – 0x68B respectively.

In auto mode, when register live_pb (0x6B6.0) is set to 0, these registers are for live channel 1-16 as rgb_hpos0_live to rgb_hpos15_live. When live_pb is set to 1, these registers are for PB channel 1-16 in auto mode as rgb_hpos0_pb to rgb_hpos15_pb. They share address in this configuration. Register rgb_hpos16_pb to rgb_hpos19_pb are used in normal mode for PB1-PB4. If CAS_EN (0x6fc.2) is set to one and live_pb (0x6B6.0) is set to 1, rgb_hpos12_pb to rgb_hpos15_pb is used as PB5 auto mode registers. If live_pb (0x6B6.0) is set to 0, then rgb_hpos12_live is set to PB5 normal register.

DISPLAY WRITE BUFFER HORIZONTAL SIZE REGISTER A – 0X68C

Bit	R/W	Default	Description
7:0	R/W	0	Horizontal Size[7:0]l, unit is 4 pixels

DISPLAY WRITE BUFFER HORIZONTAL SIZE REGISTER B – 0X68D

Bit	R/W	Default	Description
7:1	R	0	Reserved
0	R/W	0	Horizontal Size[8]

Similar registers are assigned to control Display Write Buffer 2 to 20 using register 0x68E – 0x6B3 respectively.

In auto mode, when register live_pb (0x6B6.0) is set to 0, these registers are for live channel 1-16 as rgb_hsize0_live to rgb_hsize15_live. When live_pb is set to 1, these registers are for PB channel 1-16 in auto mode as rgb_hsize0_pb to rgb_hsize15_pb. They share address in this configuration. Register rgb_hsize16_pb to rgb_hsize19_pb are used in normal mode for PB1-PB4. If CAS_EN (0x6fc.2) is set to one and live_pb (0x6B6.0) is set to 1, rgb_hsize12_pb to rgb_hsize15_pb is used as PB5 auto mode registers. If live_pb (0x6B6.0) is set to 0, then rgb_hsize12_live is set to PB5 normal register.

DISPLAY WRITE BUFFER CONTROL REGISTER 1 – 0X6B4

Bit	R/W	Default	Description
7:4	R/W	0	**Newfld_sel:** New field signal for LCD frame rate adjustment. There are total 16 live channels. Only one channel is selected for LCD frame rate adjustment.
3	R/W	0	**MODE:** This bit set play back channel buffer mode. 1: auto mode, use channel ID information, can support 16 channels in one PB port. 0: normal mode, support only one channel in one PB port
2	R/W	0	**TST_IN_PB:** Test pattern enable for PB channels
1	R/W	0	**PALNT:** Test pattern PAL/NTSC selection. 0: NTSC 1: PAL
0	R/W	0	**TST_IN:** Test pattern enable for live channels

NON STANDARD CONTROL REGISTER 1 – 0X6B5

Bit	R/W	Default	Description
7:2	R/W	0	**Reserve**
1:0	R/W	0	**TST_PAT_CH[1] (only live channel support)** 0: disable channel control using internal field 1: if some channel don't outfield signal, using internal field **TST_PAT_CH [0] (only live channel support)** 0: disable channel control using internal field 1: if some channel occur non standard, using internal field

MISC CONTROL REGISTER – 0X6B6

Bit	R/W	Default	Description
7	RW	0	**Line_bigger_en_pb:** This bit cut vactive signal when input video is crashed
6	RW	0	**Line_bigger_en:** This bit cut vactive signal when input video is crashed
5	RW	0	**Use_novid:** When enable this bit, no video signal from TW2864 will determine write or not.
4:3	RW	0	**Skip_sel:** Frame drop selection for live videos 00: no frame drop 01: every five frames will drop one frame 10: every six frames will drop one frame 11: every seven frames will drop one frame
2	RW	0	**Prot_en** When this bit turns on, rgb_interface will not write data to address bigger than prot_addr.
1	RW	0	**chid_sel** When this bit equals to one, the channel ID for each PB port will be fixed as 0x0123 for port 0, 0x4567 for port 1, 0x89AB for port 2 and 0xCDEF for port 3. When this bit is 0, channel ID will decode from VBI data.
0	R/W	0	**Live_Pb Select** 1: PB channels 0: live channels For register hpos0-15, vpos0-15, hsize0-15, vsize0-15, hstart0-15, vstart0-15, they share same address between live channels and PB channels. If this bit is set to low, live channels values can be read or write. If this bit is set to high, PB channels values can be read or write

PB FIRST CHANNEL NUMBER REGISTER 1 – 0X6B7

Bit	R/W	Default	Description
7:4	RW	0	**Pb1_chnum:** This is used in frame interleave mode. It should be set to first frame number in PB port 1
3:0	RW	0	**Pb0_chnum:** This is used in frame interleave mode. It should be set to first frame number in PB port 0

PB FIRST CHANNEL NUMBER REGISTER 2 – 0X6B8

Bit	R/W	Default	Description
7:4	RW	0	**Pb3_chnum:** This is used in frame interleave mode. It should be set to first frame number in PB port 3
3:0	RW	0	**Pb2_chnum:** This is used in frame interleave mode. It should be set to first frame number in PB port 2

PB FIRST CHANNEL NUMBER ENABLE REGISTER – 0X6B9

Bit	R/W	Default	Description
7:6	RW	2	**IGNOR_NONSTD[1] (only live channel support)** 0: enable using non standard status for write fifo 1: disable using non standard status for write fifo **IGNOR_NONSTD[0] (only live channel support)** 0: disable channel control using frame rate controller 1: if some channel occur non standard, frame rate controller disable this channel
5	RW	0	**IRQENA_NONSTD:** Non-standard interrupt masking bit 0: off (masked) 1: on
4	R/W	0	**Read out select** 0: normal 1: Read address 0x6f0, 0x6f1 will become the PB correction register
3	RW	0	**Pb3_chnum_en:** Same as channel 0
2	RW	0	**Pb2_chnum_en:** Same as channel 0
1	RW	0	**Pb1_chnum_en:** Same as channel 0
0	RW	0	**Pb0_chnum_en:** this is used in frame interleave mode. First channel number enable 0: update wr_page any time 1: update wr_page when chnum equals to pb0_chnum

PB CHANNEL FREEZE REGISTER 1 – 0X6BB

Bit	R/W	Default	Description
7:0	R/W	0	**Pb_ch_frez[7:0]** 1: freeze 0: normal operation

PB CHANNEL FREEZE REGISTER 2 – 0X6BC

Bit	R/W	Default	Description
7:0	R/W	0	**Pb_ch_frez[15:8]**

PROTECTION ADDRESS REGISTER 1 – 0X6BD

Bit	R/W	Default	Description
7:0	R/W	0	**Prot_addr[7:0]** Protection area. It is 8 bytes unit. RGB interface will not write data to address more than or equal to prot_addr.

PROTECTION ADDRESS REGISTER 2 – 0X6BE

Bit	R/W	Default	Description
7:0	R/W	0	**Prot_addr[15:8]**

PROTECTION ADDRESS REGISTER 3 – 0X6BF

Bit	R/W	Default	Description
7	RW	0	**pb4_chnum_en:** This bit enable the 5th PB
6	RW	0	**Reserved**
5:0	RW	0	**Prot_addr[21:16]**

The meaning of register 0x6bd, 0x6be, 0x6bf is controlled by 0x6fc[7:6]. It can be redefined as 5th PB control

5TH PB CONTROL REGISTER 1 – 0X6BD

Bit	R/W	Default	Description
7	R	0	**1 = No valid video signal present**
6	RW	0	**FSEL_4** 0 = channel format equals 2'b11 1 = channel format equals fmt_sel_4
5:4	RW	0	**fmt_sel_4:** User channel format
3:0	RW	F	rgb_wr_ctrl20 [3]: freeze20 [2]: wr_en20 [1]: hinv20 [0]: vinv20

5TH PB CONTROL REGISTER 2 – 0X6BE

Bit	R/W	Default	Description
7:4	RW	0	**ch_en_cas[3:0]:** This is for 5th PB, channel 17-20
3:0	RW	0	**ch_frez_cas[3:0]:** This is for 5th PB, channel 17-20

5TH PB CONTROL REGISTER 3 – 0X6BF

Bit	R/W	Default	Description
7:4	RW	3	**pb_con4[3:0]:** This is for 5th PB control
3:0	RW	0	**pb4_chnum[3:0]:** This is for 5th PB first channel

DISPLAY WRITE BUFFER HORIZONTAL START – 0X6C0

Bit	R/W	Default	Description
7:0	R/W	0	**Horizontal Start[7:0]** Image horizontal start position used for cropping. Unit is 4 pixels

Similar registers are assigned to control Display Write Buffer 2 to 20 using register 0x6C1 – 0x6D3 respectively.

In auto mode, when register live_pb (0x6B6) bit 0 is set to 0, these registers are for live channels. When live_pb is set to 1, these registers are for PB channels. Register rgb_hstart0_pb to rgb_hstart15_pb are used in auto mode. They share address with rgb_hstart0_live to rgb_hos15_live. Register rgb_hstart16_pb to rgb_hstart19_pb are used in normal mode.

DISPLAY WRITE BUFFER VERTICAL START – 0X6D4

Bit	R/W	Default	Description
7:0	R/W	0	**Vertical Start[7:0]** Image vertical start position used for cropping.

Similar registers are assigned to control Display Write Buffer 2 to 20 using register 0x6D5 – 0x6E7 respectively.

In auto mode, when register live_pb (0x6B6) is set to 0, these registers are for live channels. When live_pb is set to 1, these registers are for PB channels. Register rgb_vstart0_pb to rgb_vstart15_pb are used in auto mode. They share address with rgb_vstart0_live to rgb_hos15_live. Register rgb_vstart16_pb to rgb_vstart19_pb are used in normal mode. Unit is 2 lines for live channels. Unit can be changed for PB channels. When vstart_unit_pb is set to 1, the unit is 4 lines. When vstart_unit_pb is set to 0, the unit is 2 lines. In auto mode, vstart for PB has different meaning. Vstart0_pb to vstart3_pb are used for PB port 0. They are for 4 positions in Quad mode. Vstart4_pb to vstart7_pb are used for PB port 1. Vstart8_pb to Vstart11_pb are used for PB port 2. Vstart12_pb to vstart15_pb are used for PB port 3.

LIVE CHANNEL FRAME RATE CORRECTION CONTROL REGISTER 1 – 0X6E8

Bit	R/W	Default	Description
7:4	RW	F	**Correction Control[3:0]:** This is for channel 1
3:0	RW	F	**Correction Control[3:0]:** This is for channel 0 Bit 3: 1 = Enable nonstd FRSC correction Bit 2: 1 = Enable nonstd write page correction Bit 1: 1 = Enable external write page correction Bit 0: 1 = Enable internal write page correction

LIVE CHANNEL FRAME RATE CORRECTION CONTROL REGISTER 2 – 0X6E9

Bit	R/W	Default	Description
7:4	RW	F	**Correction Control[3:0]:** This is for channel 3
3:0	RW	F	**Correction Control[3:0]:** This is for channel 2

LIVE CHANNEL FRAME RATE CORRECTION CONTROL REGISTER 3 – 0X6EA

Bit	R/W	Default	Description
7:4	RW	F	**Correction Control[3:0]:** This is for channel 5
3:0	RW	F	**Correction Control[3:0]:** This is for channel 4

LIVE CHANNEL FRAME RATE CORRECTION CONTROL REGISTER 4 – 0X6EB

Bit	R/W	Default	Description
7:4	RW	F	**Correction Control[3:0]:** This is for channel 7
3:0	RW	F	**Correction Control[3:0]:** This is for channel 6

LIVE CHANNEL FRAME RATE CORRECTION CONTROL REGISTER 1 – 0X6EC

Bit	R/W	Default	Description
7:4	RW	F	**Correction Control[3:0]:** This is for channel 9
3:0	RW	F	**Correction Control[3:0]:** This is for channel 8

LIVE CHANNEL FRAME RATE CORRECTION CONTROL REGISTER 2 – 0X6ED

Bit	R/W	Default	Description
7:4	RW	F	**Correction Control[3:0]:** This is for channel 11
3:0	RW	F	**Correction Control[3:0]:** This is for channel 10

LIVE CHANNEL FRAME RATE CORRECTION CONTROL REGISTER 7 – 0X6EE

Bit	R/W	Default	Description
7:4	RW	F	**Correction Control[3:0]:** This is for channel 13
3:0	RW	F	**Correction Control[3:0]:** This is for channel 12

LIVE CHANNEL FRAME RATE CORRECTION CONTROL REGISTER 8 – 0X6EF

Bit	R/W	Default	Description
7:4	RW	F	**Correction Control[3:0]:** This is for channel 15
3:0	RW	F	**Correction Control[3:0]:** This is for channel 14

PB0 LINE NUMBER STATUS REGISTER 1 – 0X6F0 (READ ONLY)

Bit	R/W	Default	Description
7:0	RO	-	**Linenum_pb0[7:0]:** Total line number for PB port 0.

PB0 LINE NUMBER STATUS REGISTER 2 – 0X6F1 (READ ONLY)

Bit	R/W	Default	Description
7:4	RO	0	**Reserved**
3:0	RO	-	**Linenum_pb0[11:8]:** Total line number for PB port 0.

Register 0x6F2 to 0x6F7 are port 1 to 3, When 0x6b9[4] = 1, 0x6f0 and 0x6f1 is redefined as PB Correction Control Register.

PB CHANNEL FRAME RATE CORRECTION CONTROL REGISTER 1 – 0X6F0

Bit	R/W	Default	Description
7:4	RW	0x33	**Correction Control[3:0]:** This is for PB channel 1
3:0	RW	0x33	**Correction Control[3:0]:** This is for PB channel 0 Bit 3 = Double save mode control (1 = enable) Bit 2 = Select Top or Bottom field (1 = Bottom) Bit 1,0 (Auto mode) 1X = Set compatible mode 01 = Correction enable 00 = Free running Bit1,0 (Normal mode) 0X = Set compatible mode 11 = Correction enable 10 = Free running

PB CHANNEL FRAME RATE CORRECTION CONTROL REGISTER 2 – 0X6F1

Bit	R/W	Default	Description
7:4	RW	0x33	**Correction Control[3:0]:** This is for PB channel 3
3:0	RW	0x33	**Correction Control[3:0]:** This is for PB channel 2

PB VALID STATUS REGISTER – 0X6F8

Bit	R/W	Default	Description
7	W	0	**Write this bit to clear bit [3:0]**
6:4	RO	0	**Reserved**
3	RO	0	**Pb3_valid**: Valid signal bit for PB channel 3
2	RO	0	**Pb2_valid**: Valid signal bit for PB channel 2
1	RO	0	**Pb1_valid**: Valid signal bit for PB channel 1
0	RO	0	**Pb0_valid:** This bit will be high if there is valid field signal coming. This bit will be clear when write to this register.

LIVE CHANNEL EXTERNAL CORRECTION PERIOD REGISTER – 0X6F9

Bit	R/W	Default	Description
7:0	R/W	0x25	**period2[7:0]:** Control the write page self checking period, the unit is the LCD Vsync.

PB CHANNEL IGNORE AND FREE RUNNING REGISTER – 0X6FA

Bit	R/W	Default	Description
7	RW	0	**SEL_IG3:** Ignore control of channel 3
6	RW	0	**SEL_IG2:** Ignore control of channel 2
5	RW	0	**SEL_IG1:** Ignore control of channel 1
4	RW	0	**SEL_IG0:** Ignore control of channel 0 Set this bit to "1" and PB write buffer will use ignore bits in digital channel ID to determine which channel or channels should be disabled.
3	RW	0	**Pb_free_3:** Free running control of channel 3
2	RW	0	**Pb_free_2:** Free running control of channel 2

Bit	R/W	Default	Description
1	RW	0	**Pb_free_1:** Free running control of channel 1
0	RW	0	**Pb_free_0:** Free running control of channel 0 Set this bit to "1", PB video will be free running, write_page will automatically plus 1, frame rate control has no use.

FIFO COUNT LIMIT REGISTER – 0X6FB

Bit	R/W	Default	Description
7:4	RW	1	**Fifo_cnt_limit:** RGB FIFO count limit.
3	RW	1	**Fld_update:** In interlaced PB mode, when this bit set to 1, frame buffer only update when last field is even field and current field is odd filed.
2	RW	1	**Fld_sel_fix:** In progressive PB mode, when fld_sel_en set to 0, fld signal is fixed to setting value: fld_sel_fix.
1	RW	0	**Fld_sel_en:** In progressive PB mode, when this bit set to 0, fld signal is fixed to setting valued: fld_sel_fix. When this bit set to 1, fld signal is the detected fld signal.
0	RW	0	**Vstart_unit_pb:** Unit for vstart for pb channels 0: unit is 2 line 1: unit is 4 line, used for BT1120 or 4D1 case

VERTICAL INVERTER METHOD SELECTION – 0X6FC

Bit	R/W	Default	Description
7:6	RW	0	**Address Select** 00 = Protection address register 01 = Reserved 10 = Reserved 11 = PB5 releated control registers
5	RW	0	**1 = Force live channel to use old frame rate algorithm**
4	RW	1	**seld:** 1 = change the read content of 0x6b5 and 0x6b9
3	RW	0	**test_960_720**
2	RW	0	**CAS_EN: cascade enable**
1	RW	0	**Hstart_unit_pb:** Unit for hstart for pb channels 0: unit is 4 pixels 1: unit is 8 pixels, used for BT1120 or 4D1 case
0	RW	0	**Vinv_sel:** Vertical invert method selection. 0: odd field will write to even field 1: odd field will write to odd field

AUTO MODE PB CHANNEL ENABLE REGISTER 1 – 0X6FD

Bit	R/W	Default	Description
7:0	R/W	0	**PB_CH_EN[7:0]:** Control auto mode PB channel 7 - 0 1 = Playback channel enable

AUTO MODE PB CHANNEL ENABLE REGISTER 2 – 0X6FE

Bit	R/W	Default	Description
7:0	R/W	0	**PB_CH_EN[15:8]:** Control auto mode PB channel 15 - 8 1 = Playback channel enable

LIVE CHANNEL INTERNAL CORRECTION PERIOD REGISTER – 0X6FF

Bit	R/W	Default	Description
7:0	R/W	0x5	**PERIOD[7:0]:** Control the write page self checking period, the unit is the incoming channel Vsync.

DDR2 Memory Controller

Introduction

TW2828 implements a high speed 64-bit internal DRAM data bus to transfer data between the external DRAM memory and TW2828. The *internal BUS* and external DDR2 access is controlled by DRAM controller module (*DCM*). *DCM* is a unified DDR memory controller for all memory clients. For each of the clients, a weighted round-ribbon arbitration scheme is used to grant bus for clients.

Memory Organization

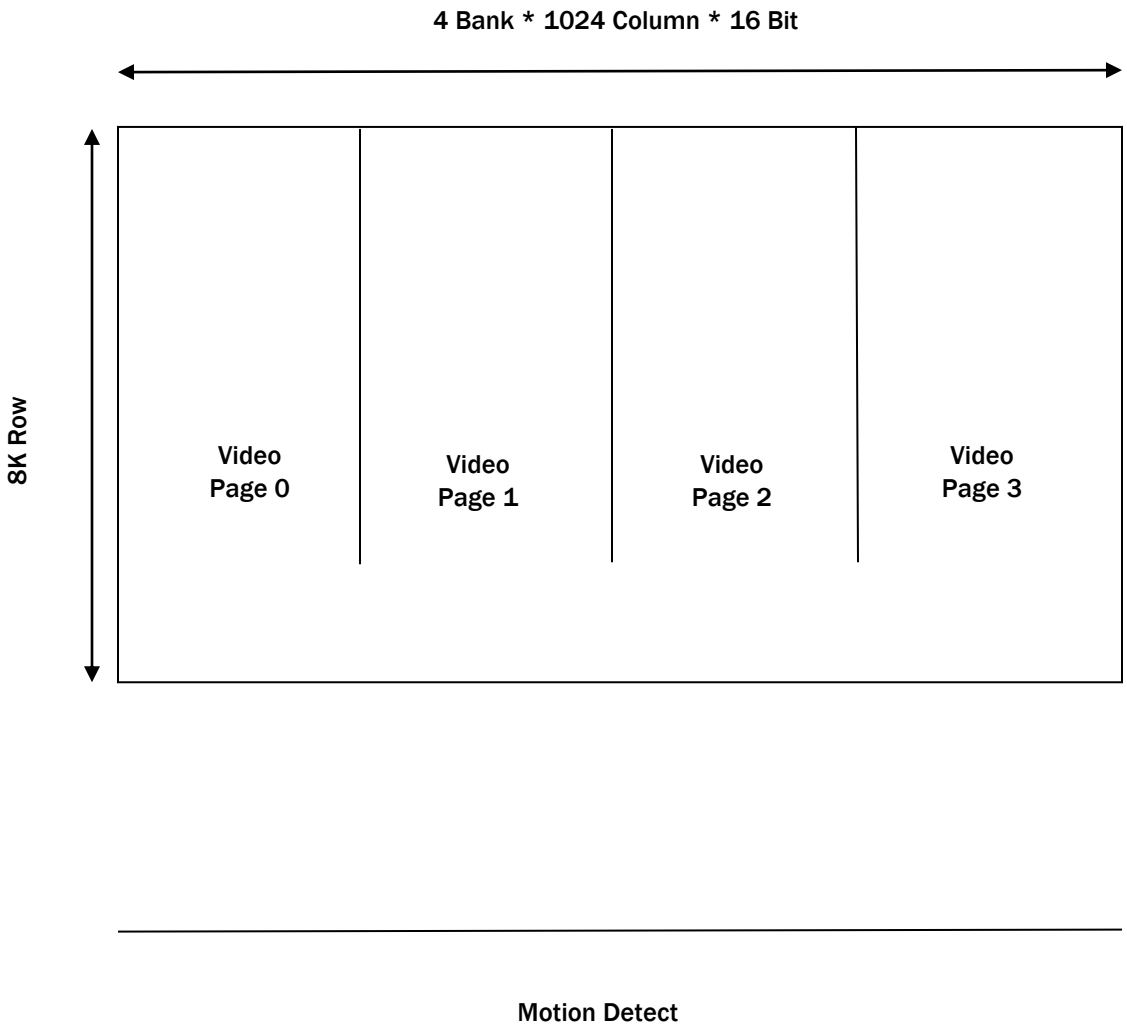
TW2828's DCM supports DDR2 SDRAM subsystem size up to 128 Mbytes by using 128, 256, 512 or 1024 Mbit generation DDR2 SDRAMs with 16 bits wide bus. The internal memory data bus is 64 bits wide. The operating speed is ranged from 200 MHz to 333 MHz.

The internal linear address (LA) for 64-bit Memory Data Bus is 25 bit and classified as:

2^{13} (Row) x 2^{10} (Column) x 2^{3} (Bank) x 2^{2} (16b x 2)= 2^{28} Bytes

The next table shows the resolutions and memory required.

Item		Total: 64 MByte installed
Video	1920 x 1024 x 2 x 4 = 15.36 MB	
MISC	3 MB	
		Total: 128 MByte installed
Video	1920 x 1024 x 2 x 4 = 15.36 MB	
Record	720 x 576 x 2 x 18 x 4 = 57 MB	
MISC	3 MB	


4 Bank * 1024 Column * 16 Bit
8K Row
Video Page 0
Video Page 1
Video Page 2
Video Page 3
Motion Detect
512 Mbit DDR2

DRAM Parameter Adjustments

The DRAM controller is designed to support different speed grades of DDR2 SDRAM from different manufacturers. Normally we suggest user use higher speed grade of DRAM because it will generate more bandwidth for the entire system. The DDR2 devices can be used in TW2828 based system are: -5 (200 MHz), -37 (266 MHz), -3 (333 MHz) and -25 (400 MHz). To determine whether a certain DRAM speed grade is suitable for a particular TW2828 system, we need to pay attentions to t_{RAS}, t_{RCD}, t_{RC}, t_{WR} , t_{RP}, t_{WS} and t_{WH} and other parameters for different DRAM venders. User should program DCM configuration register 0 to DCM configuration register 6 base on the DDR2 clock frequency.

PARAMETERS	EXPLANATION	
t_{RAS}	RAS to precharge time Min. 40ns	16T(400MHz), 14T(333MHz)
t_{RCD}	RAS to CAS time Min. 15 ns	6T(400MHz), 5T(333MHz)
t_{RC}	Access cycle time Min. 55 ns	22T(400MHz), 19T(333MHz)
t_{WR}	Write turn around time Min. 15 ns	6T(400MHz), 5T(333MHz)
t_{RP}	Bank address precharge time	6T, 5T
t_{DS}	Data setup time, same as address	0.25 ns
t_{DH}	Data hold time, same as address	0.25 ns

Based on this we can calculate the five important constants in the DRAM operations:

NAME	-25E	-25	-3E	-3	-37	-5E
t_{RAS}	16T	16T	14T	14T	11T	8T
t_{RCD}	5T	6T	4T	5T	4T	3T
t_{RC}	22T	22T	19T	19T	15T	11T
t_{WR}	6T	6T	5T	5T	4T	3T
t_{RP}	5T	6T	4T	5T	4T	3T

After this calculation user can make sure the device they choose are suitable running at certain frequencies. Foe example, a system run at 400 MHz can choose -37, -3 or -25 device.

Register Table

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x100	R/W	0	DCM Control Register
0x104	R/W	0	Reserved
0x108	R/W	0	DCM Service Port Selection
0x10C	R/W	0	DCM Service Priority
0x110	R/W	0	DCM Configuration Register 0
0x114	R/W	0	DCM Configuration Register 1
0x118	R/W	0	DCM Configuration Register 2
0x11C	R/W	0	DCM Configuration Register 3
0x120	R/W	0	DCM Configuration Register 4
0x124	R/W	0	DCM Configuration Register 5
0x128	R/W	0	DCM Configuration Register 6
0x130	R/W	0	DCM Mode Register 0
0x134	R/W	0	DCM Mode Register 1
0x138	R/W	0	DCM Mode Register 2
0x13C	R/W	0	DCM Mode Register 3
0x140	R/W	0	PHY Configuration Register 0
0x144	R/W	0	PHY Configuration Register 1
0x148	R/W	0	PHY Configuration Register 2
0x14C	R/W	0	PHY Configuration Register 3
0x151	R/W	0	PHY Loopback Register 1
0x152	R/W	0	PHY Loopback Register 2
0x153	R/W	40	PHY DQ Offset Register 1
0x154	R/W	20	PHY DQ Offset Register 2
0x155	R/W	0	PHY Gatelvl_init_ratio Register
0x157	R/W	0	PHY Gatelvl_init_mode Register
0x158	R/W	0	PHY Gatelvl_num_of_dq0 Register
0x159	R/W	80	PHY Ctrl Slave Ratio Register
0x15B	R/W	0	PHY Ctrl Slave Delay Register
0x15C	R/W	0	PHY Ctrl Slave Force Register
0x15D	R/W	40	PHY Rd Dqs Slave Ratio Register 1
0x15E	R/W	00	PHY Rd Dqs Slave Ratio Register 2
0x15F	R/W	01	PHY Rd Dqs Slave Force Register 3
0x160	R/W	0	PHY Rd Dqs Slave Delay Register
0x163	R/W	90	PHY FIFO We Slave Ratio Register 1
0x164	R/W	80	PHY FIFO We Slave Ratio Register 2
0x165	R/W	04	PHY FIFO We Slave Ratio Register 3
0x166	R/W	0	PHY FIFO We In Delay Register
0x168	R/W	0	PHY FIFO We In Force Register
0x169	R/W	40	PHY Wr Data Slave Ratio Register 1
0x16A	R/W	00	PHY Wr Data Slave Ratio Register 2
0x16B	R/W	01	PHY Wr Data Slave Ratio Register 3
0x16C	R/W	0	PHY Wr Data Slave Delay Register
0x16E	R/W	0	PHY Wr Data Slave Force Register
0x16F	R/W	1	PHY Wr RI Delay Register
0x170	R/W	1	PHY Rd RI Delay Register
0x171	R/W	11	PHY DLL Lock Diff Register
0x172	R/W	0	PHY MISC 0 Register

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x173	R/W	0	PHY MISC 1 Register
0x174	R/W	0	PHY MISC 2 Register
0x176	R/W	0	PHY MISC 3 Register
0x177	R/W	0	Rdlvl_fifowein_ratio Register
0x17A	R/W	0	DLL_slave_value Register
0x17C	R/W	0	In_delay_value Register
0x17E	R/W	0	Out_delay_value Register
0x17F	R/W	0	Lock_state Register
0x180	R/W	0	Phy_ctrl_dll_slave_value Register
0x182	R/W	0	Phy_ctrl_In_delay_value Register
0x184	R/W	0	Phy_ctrl_Out_delay_value Register
0x185	R/W	0	Phy_ctrl_Lock_state Register
0x186	R/W	0	Rd_dqs_slave_dll_value Register
0x189	R/W	0	Wr_data_slave_dll_value Register
0x18C	R/W	0	Fifo_we_slave_dll_value Register
0x18F	R/W	0	Phy_ctrl_slave_dll_value Register
0x190	R/W	0	Phy_ctrl_slave_dll_value Register
0x198	R/W	0	DCM Interrupt Status Register
0x19C	R/W	0	DCM Out-range Client Register
0x1A0	R/W	0	DCM client 0 upper limit register
0x1A4	R/W	0	DCM client 1 upper limit register
0x1A8	R/W	0	DCM client 2 upper limit register
0x1AC	R/W	0	DCM client 3 upper limit register
0x1B0	R/W	0	DCM client 0 lower limit register
0x1B4	R/W	0	DCM client 1 lower limit register
0x1B8	R/W	0	DCM client 2 lower limit register
0x1BC	R/W	0	DCM client 3 lower limit register
0x1C0	R/W	0	DCM protect upper limit register
0x1C4	R/W	0	DCM protect lower limit register
0x1D4	R	0	DCM Urgent Queue Register
0x1E0	R/W	0	DCM Debug Select Register
0x1E4	R	0	DCM Debug Status Register
0x1E8	R/W	0	DCM Test Mode Register
0x1FC	R/W	0	DCM DDR Command Register

Registers Description

DCM CONTROL REGISTER LOW – 0X100

Bit	R/W	Default	Description
0	R	0	**Init Done:** PHY calibration and DDR initialization done

DCM CONTROL REGISTER HIGH – 0X101

Bit	R/W	Default	Description
7	R	0	**Empty:** After FW issues command to turn off DCM normal service requests, it has to wait till ack becomes HIGH so that all pending DCM requests have been serviced.

DCM CONTROL REGISTER – 0X103

Bit	R/W	Default	Description
7	R/W	1	**Ready:** It specifies if DCM is ready to receive any normal service port requests. After all DCM registers have been programmed, FW write HIGH to this bit so that DCM can start taking normal service requests. FW can write LOW to this bit to turn off DCM normal service port.
6	R/W	1	**Linear buffer Ready:** It specifies if DCM is ready to receive any linear address requests.

DCM SERVICE PORT SELECTION – 0X108

Bit	R/W	Default	Description
4:0	R/W	0	**Port_num:** It specifies the DCM service port that is going to be programmed. TW2828 supports 24 normal service ports. Following table show port number for each module 0 : lcd 1 : rout5 2 : rout6 3 : rout7 4 : recw 5 : rgbw 6 : di_rd 7 : mdw 8 : cpu 9 : mdr A : dec_freeze B : freeze C : spw D : rout8 E : rout9 F : lcd_mouse

DCM SERVICE PRIORITY LOW– 0X10C

Bit	R/W	Default	Description
7:0	R/W	ff	**Priority[7:0]:** It specifies the DCM service weight factor for the port selected in DCM service port selection register. The priority is in terms of cycle count. The higher the service priority, the smaller the value of priority is. However, the value of priority can not be zero.

DCM SERVICE PRIORITY HIGH – 0X10D

Bit	R/W	Default	Description
3:0	R/W	f	**Priority[11:8]:**

DCM CONFIGURATION 0 REGISTER LOW – 0X110

Bit	R/W	Default	Description
4:0	R/W	3	**Cfg_RC:** Active to Active (same bank) command

DCM CONFIGURATION 0 REGISTER HIGH – 0X111

Bit	R/W	Default	Description
7:5	R/W	3	**Cfg_RCD:** Active-to-Read or Write delay
4:3	R/W	2	**Cfg_RRD:** Active Bank a to Active Bank b command
2:0	R/W	5	**Cfg_RP:** Precharge command period

DCM CONFIGURATION 1 REGISTER LOW – 0X114

Bit	R/W	Default	Description
7:2	R/W	19h	**Cfg_RFC:** Refresh-to-Active or Refresh-to-Refresh command interval
1:0	R/W	0	**Cfg_rowbits:** Number of bit of row address 00: 13-bit Row Address 01: 14-bit Row Address

DCM CONFIGURATION 1 REGISTER HIGH – 0X115

Bit	R/W	Default	Description
7:5	R/W	3	**Cfg_MRD:** Load Mode command cycle time
4:0	R/W	0	**Cfg_XSNR:** Exit self refresh to non-READ commandb

DCM CONFIGURATION 2 REGISTER LOW – 0X118

Bit	R/W	Default	Description
7:5	R/W	3	**Cfg_WL:** Write Latency - 1
4:3	R/W	2	**Cfg_WTR:** Write to Read Command delay

Bit	R/W	Default	Description
0	R/W	1	**Cfg_Colbits:** Number of bit of Column Address 0: 9-bit Column Address 1: 10-bit Column Address

DCM CONFIGURATION 2 REGISTER HIGH – 0X119

Bit	R/W	Default	Description
7:5	R/W	3	**Cfg_CL:** Cas Latency
4:3	R/W	0	**Reserved**
2:0	R/W	3	**Cfg_WR:** Write recovery time

DCM CONFIGURATION 3 REGISTER LOW – 0X11C

Bit	R/W	Default	Description
7:0	R/W	2	**Cfg_delay:** Power-up to CKE high delay

DCM CONFIGURATION 3 REGISTER HIGH – 0X11D

Bit	R/W	Default	Description
6	R/W	0	**Cfg_RDQSE:** Extended Mode RDQS Enable
5:3	R/W	1	**Cfg_WDL:** Delay between Write Command and dfi_wrdata_en.
2:0	R/W	0	**Cfg_AL:** Posted CAS Additive Latency

DCM CONFIGURATION 4 REGISTER LOW – 0X120

Bit	R/W	Default	Description
7:0	R/W	Ff	**Cfg_REF[7:0]:** Refresh period

DCM CONFIGURATION 4 REGISTER HIGH – 0X121

Bit	R/W	Default	Description
6:4	R/W	1	**Cfg_RED:** Delay between Read Command and dfi_rddata_en. It should be programmed to Cas Latency – 2.
3:0	R/W	f	**Cfg_REF[11:8]:** Refresh period

DCM CONFIGURATION 5 REGISTER LOW – 0X124

Bit	R/W	Default	Description
7	R/W	3	**Cfg_Rtt[0]** Extended Mode: ODT effective resistance, RTT
5	R/W	0	**Cfg_bankbits** 0: 2-bit bank address 1: 3-bit bank address
4:0	R/W	a	**Cfg_RAS** Active to Precharge command

DCM CONFIGURATION 5 REGISTER HIGH – 0X125

Bit	R/W	Default	Description
7	R/W	0	**Cfg_outen:** Extended Mode: outputs enable
6	R/W	0	**Cfg_drstrength** Extended Mode: output drive strength
5:2	R/W	2	**Cfg_b_size** Burst size, need to set to 2
1	R/W	0	**Cfg_dqse** Extended Mode: DQS enable
0	R/W	3	**Cfg_Rtt[1]** Extended Mode: ODT effective resistance, RTT

DCM CONFIGURATION 6 REGISTER LOW – 0X128

Bit	R/W	Default	Description
3:0	R/W	0	**Cfg_odtd:** ODT duration

DCM CONFIGURATION 6 REGISTER HIGH – 0X129

Bit	R/W	Default	Description
7	R/W	0	**Cfg_dqbits:** 0: 16-bit DQ 1: 32-bit DQ(not support)
2:0	R/W	0	**Cfg_odto:** Write command to ODT delay

DCM MODE REGISTER 0 LOW – 0X130

Bit	R/W	Default	Description
7:0	R/W	32	**Mode Register Definition[7:0]**

DCM MODE REGISTER 0 HIGH – 0X131

Bit	R/W	Default	Description
7:0	R/W	06	**Mode Register Definition[15:8]**

DCM MODE REGISTER 1 LOW – 0X134

Bit	R/W	Default	Description
7:0	R/W	0	**Extended Mode Register 2 Definition[7:0]**

DCM MODE REGISTER 1 HIGH – 0X135

Bit	R/W	Default	Description
7:0	R/W	0	**Extended Mode Register 2 Definition[15:8]**

DCM MODE REGISTER 2 LOW – 0X138

Bit	R/W	Default	Description
7:0	R/W	c4	EMR with OCD Default[7:0]

DCM MODE REGISTER 2 HIGH – 0X139

Bit	R/W	Default	Description
7:0	R/W	03	EMR with OCD Default[15:8]

DCM MODE REGISTER 3 LOW – 0X13C

Bit	R/W	Default	Description
7:0	R/W	44	EMR with OCD Exit[7:0]

DCM MODE REGISTER 3 HIGH – 0X13D

Bit	R/W	Default	Description
7:0	R/W	0	EMR with OCD Exit[15:8]

PHY CONFIGURATION REGISTER LOW – 0X14D

Bit	R/W	Default	Description
5	R/W	0	**Calibration Skip** Skip PHY calibration
4	R/W	0	**DDR PHY Enable** PHY calibration and initialization Start User must set this bit after PLL is stable to enable DDR PHY.

PHY CONFIGURATION REGISTER HIGH – 0X150

Bit	R/W	Default	Description
0	R/W	0	**PHY DLL Calibration Enable** PHY DLL calibration and training Start User must set this bit when starting read DQ eye training to update DLL frequency.

PHY LOOPBACK REGISTER 1 – 0X151

Bit	R/W	Default	Description
7:6	R/W	0	**External Board Loopback testing** 1: This Slice behaves as Transmitter for board loopback. 0: disable This port must be set „0" always except when in external board level loopback test mode.
5	R/W	0	**PHY CLK Stall level** This port determines whether delay line clock stalls at HIGH or LOW level. The expected input is a very slow clock to avoid asymmetric aging in delay lines.

Bit	R/W	Default	Description
7:6	R/W	0	**External Board Loopback testing** 1: This Slice behaves as Transmitter for board loopback. 0: disable This port must be set „0" always except when in external board level loopback test mode.
4	R/W	0	**At Speed ATPG** 1 = test with full clock speed but lower coverage. 0 = test with lower clock speed but higher coverage.
3	R/W	0	**Burst Length Control** 1: burst length 2 0: other burst length
2	R/W	0	**Loopback Testing** 1: enable, 0: disable

PHY LOOKBACK REGISTER 2 – 0X152

Bit	R/W	Default	Description
1:0	R/W	00	**External Board Loopback testing** 1: This Slice behaves as Receiver for board loopback. 0: disable This port must be set „0" always except when in external board level loopback test mode.

PHY DQ OFFSET REGISTER LOW – 0X153

Bit	R/W	Default	Description
7	R/W	0h	**DQ Offset 1[0]** Offset value from DQS to DQ. Default value: 0x40 (for 90 degree shift). 7 bits value for each 8 bit memory data slices.
6:0	R/W	40h	**DQ Offset 0[6:0]** Offset value from DQS to DQ. Default value: 0x40 (for 90 degree shift). 7 bits value for each 8 bit memory data slices.

PHY DQ OFFSET REGISTER HIGH – 0X154

Bit	R/W	Default	Description
5:0	R/W	20h	**DQ Offset 1[6:1]** Offset value from DQS to DQ. Default value: 0x40 (for 90 degree shift). 7 bits value for each 8 bit memory data slices.

PHY GATELVL_INIT_RATIO REGISTER LOW – 0X155

Bit	R/W	Default	Description
7:0	R/W	0h	**Gatelvl_init_ratio[7:0]** The recommended setting of reg_phy_gatelvl_init_ratio is half cycle less than total delay required on fifo_we_in to malign to DQS at PHY.

PHY GATELVL_INIT_RATIO REGISTER MID – 0X156

Bit	R/W	Default	Description
7:0	R/W	0h	Gatelvl_init_ratio[15:8]

PHY GATELVL_INIT_RATIO REGISTER HIGH – 0X157

Bit	R/W	Default	Description
5:0	R/W	0h	Gatelvl_init_ratio[21:16]

PHY GATELVL_INIT_MODE REGISTER – 0X157

Bit	R/W	Default	Description
6	R/W	0h	Gatelvl_init_mode The user programmable init ratio selection mode. 1: selects a starting ratio value based on reg_phy_gatelvl_init_ratio port. 0: selects a starting ratio value based on Write Leveling of the same data slice.

PHY GATELVL_NUM_OF_DQ0 REGISTER – 0X158

Bit	R/W	Default	Description
3:0	R/W	0h	Gatelvl_num_of_dq0 This register value determines the number of samples for dq0_in for each ratio increment by the Gate Training FSM.

PHY CTRL SLAVE RATIO REGISTER LOW – 0X159

Bit	R/W	Default	Description
7:0	R/W	80h	Phy_Ctrl_Slave_Ratio[7:0] Ratio value for address/command launch timing in phy_ctrl macro. This is the fraction of a clock cycle represented by the shift to be applied to the read DQS in units of 256ths. In other words, the full-cycle tap value from the master DLL will be scaled by this number over 256 to get the delay value for the slave delay line.

PHY CTRL SLAVE RATIO REGISTER HIGH – 0X15A

Bit	R/W	Default	Description
1:0	R/W	0h	Phy_Ctrl_Slave_Ratio[9:8]

PHY CTRL SLAVE DELAY REGISTER – 0X15B

Bit	R/W	Default	Description
7:0	R/W	00h	Phy_Ctrl_Slave_Delay[7:0] If reg_phy_rd_dqs_slave_force is 1, replace delay/tap value for address/command timing slave DLL with this value.

PHY CTRL SLAVE FORCE REGISTER – 0X15C

Bit	R/W	Default	Description
1	R/W	0h	Phy_Ctrl_Slave_Force 1: overwrite the delay/tap value for address/command timing slave DLL with the value of the reg_phy_rd_dqs_slave_delay bus.
0	R/W	00h	Phy_Ctrl_Slave_Delay[8]

PHY RD DQS SLAVE RATIO REGISTER 1 – 0X15D

Bit	R/W	Default	Description
7:0	R/W	40h	Phy_Rd_Dqs_Slave_Ratio 0[7:0] Ratio value for read DQS slave DLL. This is the fraction of a clock cycle represented by the shift to be applied to the read DQS in units of 256ths. In other words, the full-cycle tap value from the master DLL will be scaled by this number over 256 to get the delay value for the slave delay line.

PHY RD DQS SLAVE RATIO REGISTER 2 – 0X15E

Bit	R/W	Default	Description
7:2	R/W	00h	Phy_Rd_Dqs_Slave_Ratio 1[5:0] Ratio value for read DQS slave DLL. This is the fraction of a clock cycle represented by the shift to be applied to the read DQS in units of 256ths. In other words, the full-cycle tap value from the master DLL will be scaled by this number over 256 to get the delay value for the slave delay line.
1:0	R/W	00h	Phy_Rd_Dqs_Slave_Ratio 0[9:8]

PHY RD DQS SLAVE RATIO REGISTER 3 – 0X15F

Bit	R/W	Default	Description
5:4	R/W	0h	Phy_Rd_Dqs_Slave_Force 1: overwrite the delay/tap value for read DQS slave DLL with the value of the reg_phy_rd_dqs_slave_delay bus.
3:0	R/W	1h	Phy_Rd_Dqs_Slave_Ratio 1[9:6]

PHY RD DQS SLAVE DELAY REGISTER LOW – 0X160

Bit	R/W	Default	Description
7:0	R/W	00h	Phy_Rd_Dqs_Slave_Delay[7:0] If reg_phy_rd_dqs_slave_force is 1, replace delay/tap value for read DQS slave DLL with this value.

PHY RD DQS SLAVE DELAY REGISTER MID – 0X161

Bit	R/W	Default	Description
7:0	R/W	00h	Phy_Rd_Dqs_Slave_Delay[15:8]

PHY RD DQS SLAVE DELAY REGISTER HIGH – 0X162

Bit	R/W	Default	Description
1:0	R/W	00h	Phy_Rd_Dqs_Slave_Delay[17:16]

PHY FIFO WE SLAVE RATIO REGISTER LOW – 0X163

Bit	R/W	Default	Description
7:0	R/W	48090h	Phy_FIFO_We_Slave_Ratio[7:0] Ratio value for read fifo write enable slave DLL. This is the fraction of a clock cycle represented by the shift to be applied to the fifo we in units of 256ths. In other words, the full-cycle tap value from the master DLL will be scaled by this number over 256 to get the delay value for the slave delay line.

PHY FIFO WE SLAVE RATIO REGISTER MID – 0X164

Bit	R/W	Default	Description
7:0	R/W	48090h	Phy_FIFO_We_Slave_Ratio[15:8]

PHY FIFO WE SLAVE RATIO REGISTER HIGH – 0X165

Bit	R/W	Default	Description
5:0	R/W	48090h	Phy_FIFO_We_Slave_Ratio[21:16]

PHY FIFO WE IN DELAY REGISTER LOW – 0X166

Bit	R/W	Default	Description
7:0	R/W	00h	Phy_FIFO_We_In_Delay[7:0] If reg_phy_fifo_we_in_force is 1, replace delay/tap value for fifo we timing slave DLL with this value.

PHY FIFO WE IN DELAY REGISTER MID – 0X167

Bit	R/W	Default	Description
7:0	R/W	00h	Phy_FIFO_We_In_Delay[15:8]

PHY FIFO WE IN DELAY REGISTER HIGH – 0X168

Bit	R/W	Default	Description
1:0	R/W	00h	Phy_FIFO_We_In_Delay[17:16]
3:2	R/W	0h	Phy_FIFO_We_In_Force 1: overwrite the delay/tap value for address/command timing slave DLL with the value of the reg_phy_rd_dqs_slave_delay bus.

PHY WR DATA SLAVE RATIO REGISTER LOW – 0X169

Bit	R/W	Default	Description
7:0	R/W	40h	Phy_Wr_Data_Slave_Ratio[7:0] Ratio value for write data slave DLL. This is the fraction of a clock cycle represented by the shift to be applied to the write DQ muxes in units of 256ths. In other words, the full-cycle tap value from the master DLL will be scaled by this number over 256 to get the delay value for the slave delay line.

PHY WR DATA SLAVE RATIO REGISTER MID – 0X16A

Bit	R/W	Default	Description
7:0	R/W	00h	Phy_Wr_Data_Slave_Ratio[15:8]

PHY WR DATA SLAVE RATIO REGISTER HIGH – 0X16B

Bit	R/W	Default	Description
3:0	R/W	1h	Phy_Wr_Data_Slave_Ratio[19:16]

PHY WR DATA SLAVE DELAY REGISTER LOW – 0X16C

Bit	R/W	Default	Description
7:0	R/W	00h	Phy_Wr_Data_Slave_Delay[7:0] If reg_phy_wr_data_slave_force is 1, replace delay/tap value for write data slave DLL with this value.

PHY WR DATA SLAVE DELAY REGISTER MID – 0X16D

Bit	R/W	Default	Description
7:0	R/W	00h	Phy_Wr_Data_Slave_Delay[15:8]

PHY WR DATA SLAVE DELAY REGISTER HIGH – 0X16E

Bit	R/W	Default	Description
1:0	R/W	00h	Phy_Wr_Data_Slave_Delay[17:16]

PHY WR DATA SLAVE FORCE REGISTER – 0X16E

Bit	R/W	Default	Description
3:2	R/W	0h	**Phy_Wr_Data_Slave_Force** 1: overwrite the delay/tap value for write data slave DLL with the value of the reg_phy_wr_data_slave_delay bus.

PHY WR RL DELAY REGISTER – 0X16F

Bit	R/W	Default	Description
4:0	R/W	1h	**Phy_Wr_Rl_Delay** This delay determines when to select the active rank"s ratio logic delay for Write Data and Write DQS slave delay lines after PHY receives a write command at Control Interface. This must be programmed as (Write Latency -4) with a minimum value of 1.

PHY RD RL DELAY REGISTER – 0X170

Bit	R/W	Default	Description
4:0	R/W	1h	**Phy_Rd_Rl_Delay** This delay determines when to select the active rank"s ratio logic delay for FIFO_WE and Read DQS slave delay lines after PHY receives a read command at Control Interface This port must be programmed as (Read Latency -3) with a minimum value of 1.

PHY DLL LOCK DIFF REGISTER – 0X171

Bit	R/W	Default	Description
4	R/W	1h	**Phy_use_rank0_delays** Delay selection. 1- Rank 0 delays are used for all ranks 0- Each Rank uses its own delay This port must be set HIGH when write latency < 5.
3:0	R/W	1h	**Phy_Dll_Lock_Diff** The maximum number of delay line taps variation allowed while maintaining the master DLL lock. This is calculated as total jitter/ delay line tap size. Where total jitter is half of (incoming clock jitter (pp) + delay line jitter (pp)).

PHY MISC 0 REGISTER – 0X172

Bit	R/W	Default	Description
7:6	R/W	2h	**Wr_Local_Odt** Value to drive on the 2-bit local_odt PHY outputs when output is enabled for DQ and DQS. Typically this disables termination, as few systems use termination when writing.
5:4	R/W	1h	**Data_Slice_In_Use** Data bus width selection for Read FIFO RE generation. One bit for each data slice. 1: data slice is valid. 0: read data responses are ignored. Note: The Phy Data Slice 0 must always be enabled.

Bit	R/W	Default	Description
3:0	R/W	5h	**Phy_rdc_we_to_re_delay** number of clock cycles the delay between writing into the Read Capture FIFO and the read operation. This is valid only if „use_fixed_re" is high.

PHY MISC 1 REGISTER – 0X173

Bit	R/W	Default	Description
7	R/W	0h	**Rdc_fifo_rst_err_cnt_clr** Clear/reset for counter rdc_fifo_rst_err_cnt[3:0]. 0: no clear, 1: clear.
6	R/W	1h	**Dis_calib_rst** Disable the resetting of the Read Capture FIFO pointers with dll_calib (internally generated signal). The pointers are reset to ensure that the PHY can recover if the appropriate number of DQS edges is not observed after a read command (which can happen when the DQS squelch timing is manually overridden via the debug registers). 0: enable, 1: disable. .
5	R/W	1h	**Use_fixed_re** When 1: PHY generates FIFO read enable after fixed number of clock cycles as defined by reg_phy_rdc_we_to_re_delay[3:0]. When 0: PHY uses the not_empty method to do the read enable generation.
4	R/W	0h	**Use_rd_dqs_gate_level** Read DQS Gate training control. 0: Use register programmed ratio values 1: Use ratio for delay line calculated by DQS gate leveling *Note: This port must be set 0 when PHY is not working in DDR3 mode*
3:2	R/W	2h	**Idle_Local_Odt** Value to drive on the 2-bit local_odt PHY outputs when output enable is not asserted and a read is not in progress. Typically this is the value required to disable termination to save power when idle.
1:0	R/W	2h	**Rd_Local_Odt** Value to drive on the 2-bit local_odt PHY outputs when output enable is not asserted and a read is in progress (where „in progress" is defined as after a read command is issued and until all read data has been returned all the way to the controller.) Typically this is set to the value required to enable termination at the desired strength for read usage.

PHY MISC 2 REGISTER – 0X174

Bit	R/W	Default	Description
4	R/W	0h	**Phy_invert_clkout** Inverts the polarity of DRAM clock. 0: core clock is passed on to DRAM. 1: inverted core clock is passed on to DRAM. Used when the clock is leading DQS and leveling is required.
3	R/W	0h	**Dis_phy_ctrl_rstn** Disable the reset from Phy Ctrl macro. 1: PHY Ctrl macro reset port is always HIGH 0: PHY Ctrl macro gets power on reset.
2	R/W	0h	**Phy_Dif_Off** Value to drive to IO receiver enable pins when turning it OFF. *IOD is the size specified by the IO_DIFEN_SIZE parameter. Depends on the IO, one of these signals dif_on or dif_off can be used.*

Bit	R/W	Default	Description
1	R/W	0h	**Phy_Dif_On** Value to drive to IO receiver enable pins when turning it ON. *IOD is the size specified by the IO_DIFEN_SIZE parameter.*
0	R/W	0h	**Test_enable** 1=Enable scan mode; 0=functional mode.

PHY MISC 3 REGISTER – 0X176

Bit	R/W	Default	Description
5	R	0h	**Dfi_ctrlupd_ack** The dfi_ctrlupd_ack signal is asserted to acknowledge a MC initiated update request. The PHY asserts active High ack signal after 1 clock of receiving ddrc_dfi_ctrlupd_req and de-asserts it after 8 clocks.
1:0	R	0h	**Gatelvl_inc_fail** Incremental Gate Leveling Fail Status Flag. 1"b1: Incremental gate leveling test has failed. 1"b0: Incremental gate leveling test has passed.

RDLVL_FIFOWEIN_RATIO REGISTER LOW – 0X177

Bit	R/W	Default	Description
7:0	R	0h	**Rdlvl_fifowein_ratio [7:0]** Ratio value generated by Read Gate training FSM.

RDLVL_FIFOWEIN_RATIO REGISTER MID – 0X178

Bit	R/W	Default	Description
7:0	R	0h	**Rdlvl_fifowein_ratio [15:8].**

RDLVL_FIFOWEIN_RATIO REGISTER HIGH – 0X179

Bit	R/W	Default	Description
5:0	R	0h	**Rdlvl_fifowein_ratio [21:16]**

DLL_SLAVE_VALUE REGISTER LOW – 0X17A

Bit	R/W	Default	Description
7:0	R	0h	**DLL_slave_value [7:0]** Shows the current Coarse and Fine delay values going to all the Slave DLLs. [1:0] – Fine value [8:2] – Coarse value

DLL_SLAVE_VALUE REGISTER HIGH – 0X17B

Bit	R/W	Default	Description
0	R	0h	DLL_slave_value [8]

IN_DELAY_VALUE REGISTER LOW – 0X17C

Bit	R/W	Default	Description
7:0	R	0h	In_delay_value [7:0] The Coarse and Fine values going into the Output Filter in Master DLL. [1:0] – Fine value [8:2] – Coarse value

IN_DELAY_VALUE REGISTER HIGH – 0X17D

Bit	R/W	Default	Description
0	R	0h	In_delay_value [8]

OUT_DELAY_VALUE REGISTER LOW – 0X17E

Bit	R/W	Default	Description
7:0	R	0h	Out_delay_value [7:0] The Coarse and Fine values coming out of the Output Filter in Master DLL. [1:0] – Fine value [8:2] – Coarse value

OUT_DELAY_VALUE REGISTER HIGH – 0X17F

Bit	R/W	Default	Description
0	R	0h	Out_delay_value [8]

LOCK_STATE REGISTER – 0X17F

Bit	R/W	Default	Description
3	R	0h	DLL Lock Status signal: 1 – Master DLL is locked 0 – Master DLL is not locked
2:1	R	0h	In_lock_state Lock status from the Output Filter module inside the Master DLL. Bit[0] – Fine delay line lock status. 1: locked, 0: unlocked. Bit[1] – Coarse delay line lock status. 1: locked, 0: unlocked.

PHY_CTRL_DLL_SLAVE_VALUE REGISTER LOW – 0X180

Bit	R/W	Default	Description
7:0	R	0h	**Phy_ctrl_dll_slave_value [7:0]** Shows the current Coarse and Fine delay value going to the PHY_CTRL Slave DLL. [1:0] – Fine value [8:2] – Coarse value

PHY_CTRL_DLL_SLAVE_VALUE REGISTER HIGH – 0X181

Bit	R/W	Default	Description
0	R	0h	**Phy_ctrl_dll_slave_value [8]**

PHY_CTRL_IN_DELAY_VALUE REGISTER LOW – 0X182

Bit	R/W	Default	Description
7:0	R	0h	**Phy_ctrl_In_delay_value [7:0]** The Coarse and Fine values going into the Output Filter in PHY_CTRL Master DLL. [1:0] – Fine value [8:2] – Coarse value

PHY_CTRL_IN_DELAY_VALUE REGISTER HIGH – 0X183

Bit	R/W	Default	Description
0	R	0h	**Phy_ctrl_In_delay_value [8]**

PHY_CTRL_OUT_DELAY_VALUE REGISTER LOW – 0X184

Bit	R/W	Default	Description
7:0	R	0h	**Phy_ctrl_Out_delay_value [7:0]** The Coarse and Fine values coming out of the Output Filter in PHY_CTRL Master DLL. [1:0] – Fine value [8:2] – Coarse value

PHY_CTRL_OUT_DELAY_VALUE REGISTER HIGH – 0X185

Bit	R/W	Default	Description
0	R	0h	**Phy_ctrl_Out_delay_value [8]**

PHY_CTRL_LOCK_STATE REGISTER – 0X185

Bit	R/W	Default	Description
3	R	0h	**Phy_ctrl_DLL Lock** Status signal: 1 – Master DLL is locked 0 – Master DLL is not locked

Bit	R/W	Default	Description
2:1	R	0h	**Phy_ctrl_ln_lock_state** Lock status from the Output Filter module inside the PHY_CTRL Master DLL. Bit[0] – Fine delay line lock status. 1: locked, 0: unlocked. Bit[1] – Coarse delay line lock status. 1: locked, 0: unlocked.

RD_DQS_SLAVE_DLL_VALUE REGISTER LOW – 0X186

Bit	R/W	Default	Description
7:0	R	0h	**Rd_dqs_slave_dll_value [7:0]** Delay value applied to read DQS slave DLL.

RD_DQS_SLAVE_DLL_VALUE REGISTER MID – 0X187

Bit	R/W	Default	Description
7:0	R	0h	**Rd_dqs_slave_dll_value [15:8]** Delay value applied to read DQS slave DLL.

RD_DQS_SLAVE_DLL_VALUE REGISTER HIGH – 0X188

Bit	R/W	Default	Description
1:0	R	0h	**Rd_dqs_slave_dll_value [17:16]** Delay value applied to read DQS slave DLL.

WR_DATA_SLAVE_DLL_VALUE REGISTER LOW – 0X189

Bit	R/W	Default	Description
7:0	R	0h	**Wr_data_slave_dll_value [7:0]** Delay value applied to write data slave DLL.

WR_DATA_SLAVE_DLL_VALUE REGISTER MID – 0X18A

Bit	R/W	Default	Description
7:0	R	0h	**Wr_data_slave_dll_value [15:8]**

WR_DATA_SLAVE_DLL_VALUE REGISTER HIGH – 0X18B

Bit	R/W	Default	Description
1:0	R	0h	**Wr_data_slave_dll_value [17:16].**

FIFO_WE_SLAVE_DLL_VALUE REGISTER LOW – 0X18C

Bit	R/W	Default	Description
7:0	R	0h	**Fifo_we_slave_dll_value [7:0]** Delay value applied to FIFO WE slave DLL.

FIFO_WE_SLAVE_DLL_VALUE REGISTER MID – 0X18D

Bit	R/W	Default	Description
7:0	R	0h	**Fifo_we_slave_dll_value [15:8]**

FIFO_WE_SLAVE_DLL_VALUE REGISTER HIGH – 0X18E

Bit	R/W	Default	Description
1:0	R	0h	**Fifo_we_slave_dll_value [17:16].**

PHY_CTRL_SLAVE_DLL_VALUE REGISTER LOW – 0X18F

Bit	R/W	Default	Description
7:0	R	0h	**Phy_ctrl_slave_dll_value [7:0]** Delay value applied to PHY CTRL slave DLL.

PHY_CTRL_SLAVE_DLL_VALUE REGISTER HIGH – 0X190

Bit	R/W	Default	Description
0	R	0h	**Phy_ctrl_slave_dll_value [8]**

PHY_CTRL_SLAVE_DLL_VALUE REGISTER – 0X190

Bit	R/W	Default	Description
4:1	R	0h	**Rdc_fifo_rst_err_cnt** Counter for counting how many times the pointers of read data capture FIFO are reset when the FIFO is not empty (an error). It saturates after reaching 4"hf. Cleared by rdc_fifo_rst_err_cnt_clr.

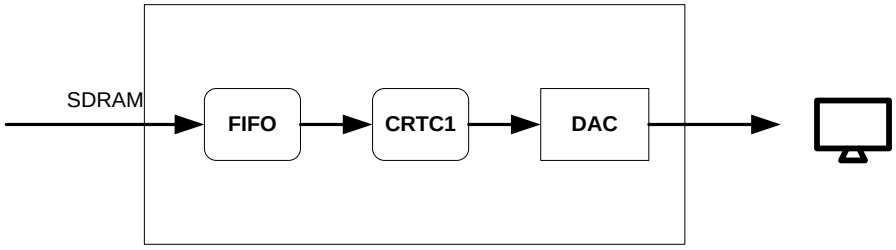
DCM CLIENT 1 LOWER LIMIT REGISTER – 0X1FD

Bit	R/W	Default	Description
3:0	R/W	04	**Command FIFO Depth** Arbiter command FIFO depth.

Display Controller

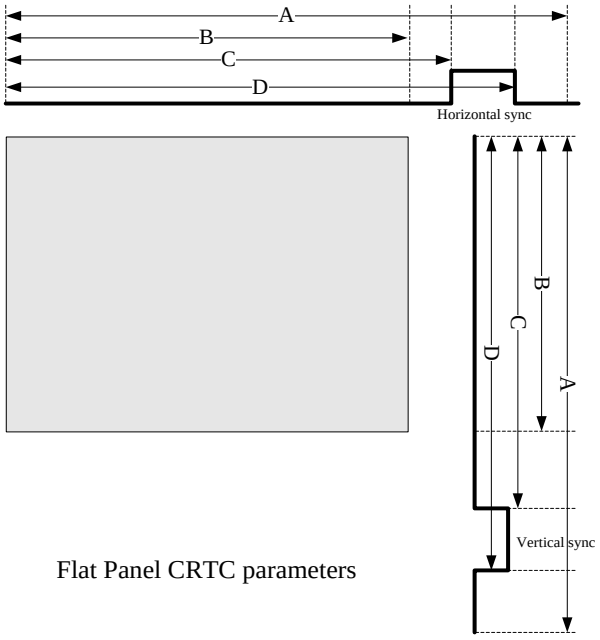
Introduction

TW2828 has glue-less video output interface capable of driving VGA-compatible display devices with screen size up to 1920x1080 at 60 Hz. As shown in the next diagram, display data is pulled from the SDRAM and sent to the VGA device through three 10 bit DACs according to the VGA timing. The display path used here is just and example, the detailed explanation of the display plane is in the next section.



TW2828 Display Controller

Display controller includes Frame buffer controller, CRT controller and DAC for the progressive data stream. Based on the display requirements, Data FIFO will raise request through DBUS and get display data in advance. When the display is active, the data will be sent to display device and a series of requests will go into DCU. The FIFOs are designed to fetch display data based on the display pattern.



Flat Panel CRTC parameters

The frame display size is determined by horizontal total register (unit in pixel clock) and vertical total register (unit in scan line). Display end register is used to determine whether they are in active display area and if not data stream request to the FIFO can be turned off. Synchronization pulses are used to generate frame pulse and line pulse to the panel. The sync pulse start time and end time can adjust to fit different panels.

Features

- Support BT.1120 output
- Support both interlaced mode and progressive mode
- Resolution up to 1080p
- Support 2D de-interlace
- Support upscale for video
- Support 16 live channel and 16 play back channel windows
- Support simple OSD for 32 channels
- Support 16 motion box
- Support 8 single box
- Support 2 layer mouse cursors
- Support up to 16 mouse shapes in DDR2 memory
- Support digital RGB gain control

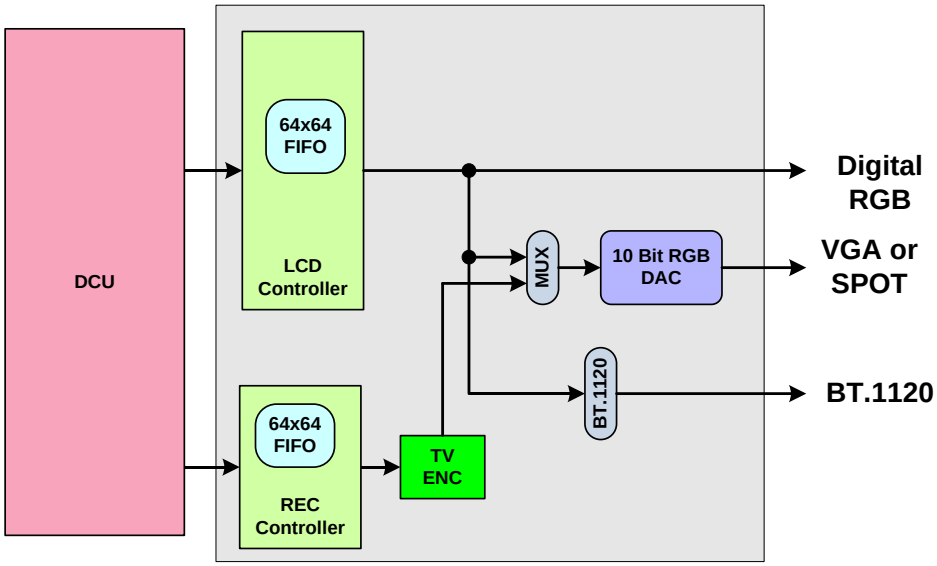
Frame Buffer Controller

Frame buffer controller is the display data agent responsible for raising the request to the DCU and getting the display data and put into the FIFO. The frame buffer is a virtual buffer as it is actually a piece of DRAM address space and the fetch locations are controlled by the display buffer starting address. For progressive device the address counter will get reset when vertical end is reached. A reset in display buffer address occurs when a sequence of odd / even fields reach the vertical ends. At the end of the horizontal line CPU need to pad zero if the data is not aligned to the DWORD boundary. Line end is from horizontal display end.

Output Interface

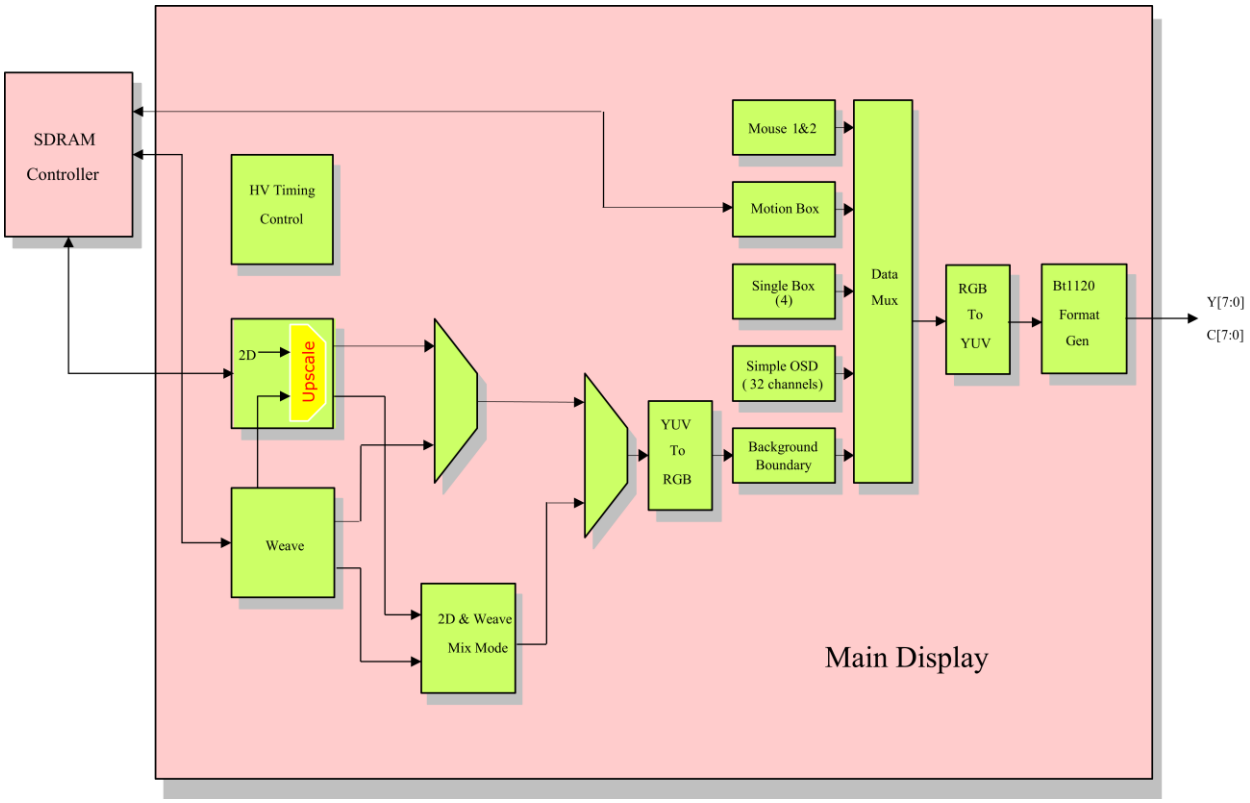
TW2828 supports three display output interface formats on three different ports. These ports can be turned on and off independently. The main output port supports standard VGA socket (HD15).

Another output is the 24 bit RGB output port and the pins are shared with live video inputs. To use this output, Incoming video decoder has to run at 108 MHz mode and user needs to turn on live video pin function control. The DualView port will be covered in next section and is not mentioned here anymore.

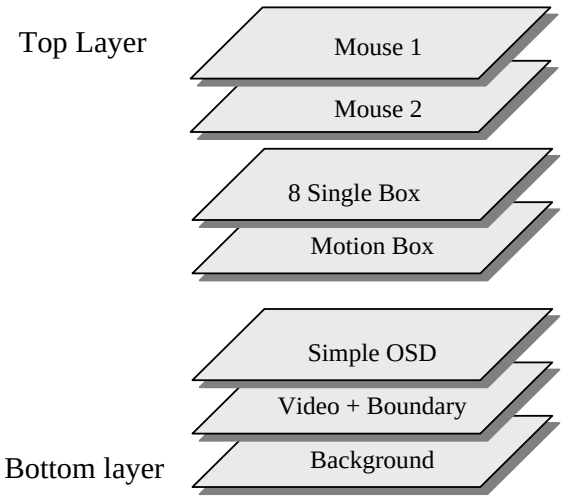


Block Diagram

There are ten display planes in the TW2828 display subsystem. There are, from the highest precedence to lowest: mouse, text cursor, Single Box, MD box, external OSD, simple OSD, live display, boundary and background. We have detailed description of each plane in the subsequent sections. The live display windows and background are compared and displayed on a pixel by pixel basis.



Display Layers



Display Resolutions

RESOLUTION	VCLK	HTT	HDE	HS	HSPW	HPOL	VTT	VDE	VS	VSPW	VSPOL
1280x1024	108	1688	1280	48	112	1	1066	1024	1	3	1
1440x900	106.5	1904	1440	80	152	0	934	900	3	6	1
1680x1050r	119	1840	1680	48	32	1	1080	1050	3	6	0
1920x1080p	148.5	2200	1920	88	44	1	1125	1080	4	5	0
1920x1080r	138.5	2080	1920	48	32	1	1111	1080	3	5	0
1920x1080	173	2576	1920	128	200	0	1120	1080	3	5	1
1920x1080i	74.25	2200	1920	88	44	1	562	540	2	5	0
1280x720	74.25	1650	1280	110	40	1	750	720	5	5	1
NTSC (480i)	13.5	858	720	16	64	1	262	240	3	4	0
PAL (576i)	13.5	864	720	16	64	1	312	288	3	4	0

This table is based on VESA standard. Some registers need to minus 1 such as HTT, HDE, VTT and VDE. 1920x1080p and 1920x1080i are based on EIA/CEA-861-D standard. “r” means reduced blank.

De-interlacing

TW2828 is equipped with advanced motion adaptive de-interlacing circuit. If multi-channel display is desired, set the de-interlacing mode to MD or by-pass to use original Weave method. If one or two particular channels zoom up view are needed, user can only turn on few channels and pipe the data through scale up circuit to get the blow up view. The biggest size of the incoming video stream is limited to 1920 pixels. There are two de-interlacing methods: Weave or 2D. In weave mode, no upscale supported.

Upscale

Up scaling function is only supported in 2D de-interlaced mode is selected. TW2828’s upscaler does not support channel based upscaling activities. That means all channels must be upscaled at the same time with the same ratio. When upscaling function is enabled, original channel position, size and boundaries will be changed. User must set POS_UPS_EN and POS_HSCALE and POS_VSCALE register accordingly to prevent wrong image.

Mouse Interface

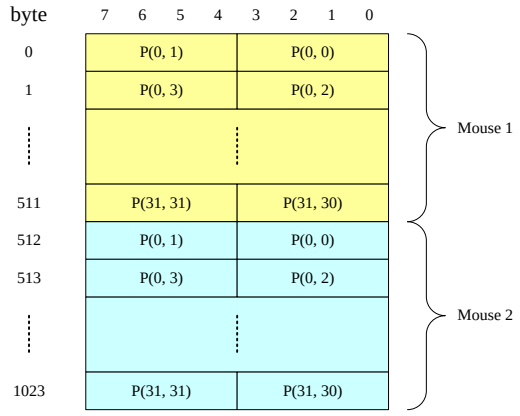
TW2828 supports two identical 32x32 mouse pointer. One will be used as text cursor and the other will be used as mouse pointer. The location of the mouse0 is controlled by MOUSE0_HPOS and MOUSE0_VPOS register. User can write mouse data to local SRAM directly. Or user can write up to 16 mouse shape to SDRAM and then hardware load mouse shape to local SRAM automatically. Each mouse pixel has 4 bits.

BIT	DESCRIPTION
3	Blinking Control **1: Blink** **0: Static**
2	Mixing Control **1: Based on mouse mix control** **0: mouse color**
1:0	Mouse Type **00: Transparent** **01: Filled with white color** **10: Foreground color** **11: Background color**

To load mouse data to SRAM. There are total 1024 bytes in local SRAM. One mouse uses 512 bytes. Sample code is shown below:

```
for (i=0;i<1024;i=i+4)

begin

  PWRITE(12'h54c, i/4);  //mouse data location

  PWRITE(12'h54d, mouse_data[i]);  //mouse data

  PWRITE(12'h54d, mouse_data[i+1]);  //mouse data

  PWRITE(12'h54d, mouse_data[i+2]);  //mouse data

  PWRITE(12'h54d, mouse_data[i+3]);  //mouse data

  PWRITE(12'h54f, 8'h00);  //mouse data write enable

End
```

Mouse_data is 8 bit which is combined by two pixels. Bit[7:4] is p1, bit[3:0] is p0. Here is the SRAM allocation:



To load mouse shape to SDRM, sample code is shown below:

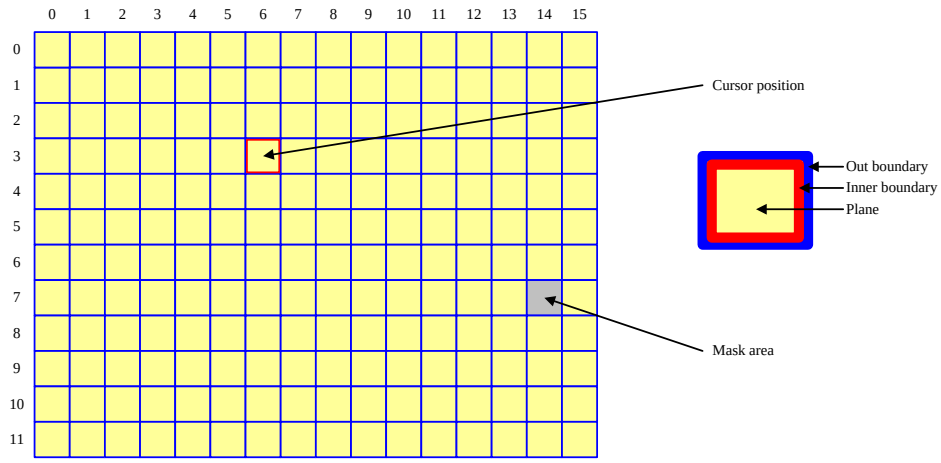
```
MOUSE_BASE_ADDR = 24'h3ffc00;
PWRITE(12'h47a, MOUSE_BASE_ADDR[7:0]); //MOUSE_BASE_ADDR[7:0]
PWRITE(12'h47b, MOUSE_BASE_ADDR[15:8]); //MOUSE_BASE_ADDR[15:8]
PWRITE(12'h47c, MOUSE_BASE_ADDR[23:16]); //MOUSE_BASE_ADDR[23:16]

host_dram_addr = MOUSE_BASE_ADDR;
PWRITE(12'h003, 8'he0); //dram_rw_ctrl, [7]:0:r, 1:w, [6]: enable, [5:0] bl

for(j=0;j<16;j=j+1)
begin
  PWRITE(12'h000, host_dram_addr[7:0]); //dram_addr_l
  PWRITE(12'h001, host_dram_addr[15:8]); //dram_addr_m
  PWRITE(12'h002, host_dram_addr[23:16]); //dram_addr_h

  for (i=0;i<256;i=i+1) PWRITE(12'h004, mouse_data[i]); //dram_data
  PREAD(12'h044); //check status, if bit 0 is high, done

  host_dram_addr = host_dram_addr + 8'h20;


  PWRITE(12'h000, host_dram_addr[7:0]); //dram_addr_l
  PWRITE(12'h001, host_dram_addr[15:8]); //dram_addr_m
  PWRITE(12'h002, host_dram_addr[23:16]); //dram_addr_h

  for (i=256;i<512;i=i+1) PWRITE(12'h004, mouse_data[i]); //dram_data
  PREAD(12'h044); //check status, if bit 0 is high, done

  host_dram_addr = host_dram_addr + 8'h20;
end

PWRITE(12'h47d, 8'h00); //MOUSE_BUF,MOUSE_INDEX
```

PWRITE(12'h490, 8'h01); //MOUSE_UPDATE_EN

PREAD(12'h490); //check bit 0, if 0 done

Motion Box

TW2828 supports 16 motion box for SD live channels and 4 Motion Box for HD live channel . Motion box positions and size can be set by registers. User must set these register according to live channels down scale ratio.



User can enable plane, out boundary and inner boundary. Cursor and motion are using inner boundary.

HD Motion Box has addition adjustable unit to fit Display channel window through Reg0x710 ~ 717 in Horizontal pixel, Reg0x718 ~ 0x71E in Vertical line.

Single Box

TW2828 provides 8 single boxes which can be used for highlighting portion of the display. The effects includes a single box or box cursor, a masking box and a box blending with a plane color. Each box has programmable location and sizes and controlled by BOX_HL (0x513 - 0x51A), BOX_HW (0x51B - 0x522), BOX_VT (0x523 – 0x52A) and BOX_VW (0x52B – 0x532) registers. The BOX_HL is the horizontal location of box with 2 pixel unit and the BOX_HW is the horizontal size of box with 2 pixel unit. The BOX_VT is the vertical location of box with 1 line unit and the BOX_VW is the vertical size of box with 1 line unit.

The display option is controlled by registers (0x50C – 0x510). BOX_PLNEN bit in these register enables each plane color and its R, G, B components are defined by registers 0x536, 0x537, 0x538 for box 1-4, by registers 0x496, 0x497, 0x498 for box 5-8. The color of box boundary is enabled via the BOX_BNDEN bit in the control registers and its color is defined by registers 0x533, 0x534, 0x535 for box 1-4, 0x493, 0x494, 0x495 for box 5-8.

In case that several boxes have same region specified, there will be a conflict of what to display for that region. Generally the TW2828 defines that box 0 has priority over box 7. So if a conflict happens between more than 2 boxes, box 0 will be displayed first as top layer and box 1 to box 7 are hidden beneath that are not supported for pop-up attribute unlike channel display.

Peak Function

TW2828 support peak function. This function make video looks sharp. It applies both horizontal and vertical directions.

Simple OSD

TW2828 support 32 channel simple OSD. Simple OSD is font based OSD. In each channel, it can support 8 font channel number information and 32x32 pictures. In whole screen, it support 32 title and 32 time information. Detail descriptions are in OSD charpter.

Background and Channel Boundary

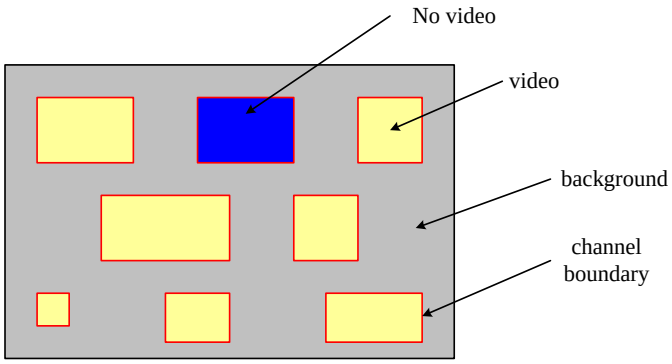
The area without video will show background. Background color is 24bit color which can be set by registers.

Each channel has its own boundary. TW2828 can support 32 channel boundary. Channel position and size information are got from rgb_interface related registers. If upscale is enable, user must turn on pos_ups_en and set correct pos_hscale and pos_vscale registers. In some cases, video is not turn on, user still want to show boundary for this channel. User must set the following registers:

[0x4EC] to [0x4EF]: BND_CH_EN

[0x4DA] bit 4: BND_CH_EN_SEL, this bit must be set to "1"

[0x4F4] to [0x4F6]: NOVID_R/G/B



Display Background and Boundary

Digital Gain

Digital gain is the last stage of the video pipe and is operated on the RGB color space. The formular is:

R = R * R_GAIN + R_OFFSET

G = G * G_GAIN + G_OFFSET

B = B * B_GAIN + B_OFFSET

Gain and offset are set by register. 0x40 is default value which gain is "1". Offset is 2's complement value. "0" means no offset. 0x7f is maximum offset. 0x80 is -128 and 0xFF is -1.

Register Table

Here are page 4 and page 5. Page 1 for simple OSD is described in a separate section.

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x400	R/W	0xF0	rg_man_wr_height[7:0]
0x401	R/W	0x00	rg_man_wr_height[10:8]
0x402	R/W	0xD0	rg_man_wr_width[7:0]
0x403	R/W	0x02	rg_man_wr_width[10:8]
0x404	R/W	0x00	[7:4]: rg_ups1_vsharp_gain [1]: rg_ups1_vlimit_on [0]: rg_disable_man_disp
0x405	R/W	0x00	rg_BGcolor
0x406	R/W	0x00	rg_ups1_hscale[7:0]
0x407	R/W	0x10	rg_ups1_hscale[12:8]
0x408	R/W	0x00	rg_ups1_vscale[7:0]
0x409	R/W	0x04	rg_ups1_vscale[10:8]
0x40A	R/W	0x00	rg_ups1_Xst[7:0]
0x40B	R/W	0x00	rg_ups1_Xst[10:8]
0x40C	R/W	0x00	rg_ups1_Yst[7:0]
0x40D	R/W	0x00	rg_ups1_Yst[10:8]
0x40E	R/W	0xD0	rg_ups1_Xmax[7:0]
0x40F	R/W	0x02	rg_ups1_Xmax[10:8]
0x410	R/W	0xE0	rg_ups1_Ymax[7:0]
0x411	R/W	0x01	rg_ups1_Ymax[10:8]
0x412	R/W	0x00	rg_ups1_Xoff
0x413	R/W	0x00	rg_ups1_Yoff
0x414	R/W	0x00	[7]: rg_panorama [6]: rg_ups1_hs_type [5:4]: rg_ups1_hs_step [3:0]: rg_ups1_hs_inc
0x415	R/W	0x00	rg_ups1_hs_center[7:0]
0x416	R/W	0x00	rg_ups1_hs_center[12:8]
0x417	R/W	0x00	rg_ups1_dbg
0x418	R/W	0x00	MDBOXH0_CTRL[7:0]
0x419	R/W	0x00	MDBOXH1_CTRL[7:0]
0x41A	R/W	0x00	MDBOXH2_CTRL[7:0]
0x41B	R/W	0x00	MDBOXH3_CTRL[7:0]
0x41C	R/W	0x00	[7:6]: MDBOXH1_V_LINE [5:4]: MDBOXH1_H_LINE [3:2]: MDBOXH0_V_LINE [1:0]: MDBOXH0_H_LINE
0x41D	R/W	0x00	[7:6]: MDBOXH3_V_LINE [5:4]: MDBOXH3_H_LINE [3:2]: MDBOXH2_V_LINE [1:0]: MDBOXH2_H_LINE
0x41E	R/W	0x00	MDBOXH0_HL[7:0]
0x41F	R/W	0x00	MDBOXH0_HL[10:8]
0x420	R/W	0x00	MDBOXH1_HL[7:0]
0x421	R/W	0x00	MDBOXH1_HL[10:8]
0x422	R/W	0x00	MDBOXH2_HL[7:0]
0x423	R/W	0x00	MDBOXH2_HL[10:8]
0x424	R/W	0x00	MDBOXH3_HL[7:0]
0x425	R/W	0x00	MDBOXH3_HL[10:8]
0x426	R/W	0x00	MDBOXH0_VT[7:0]
0x427	R/W	0x00	MDBOXH0_VT[10:8]

0x428	R/W	0x00	MDBOXH1_VT[7:0]
0x429	R/W	0x00	MDBOXH1_VT[10:8]
0x42A	R/W	0x00	MDBOXH2_VT[7:0]
0x42B	R/W	0x00	MDBOXH2_VT[10:8]
0x42C	R/W	0x00	MDBOXH3_VT[7:0]
0x42D	R/W	0x00	MDBOXH3_VT[10:8]
0x42E	R/W	0x00	MDBOXH0_HS[7:0]
0x42F	R/W	0x00	MDBOXH0_HS[10:8]
0x430	R/W	0x00	MDBOXH1_HS[7:0]
0x431	R/W	0x00	MDBOXH1_HS[10:8]
0x432	R/W	0x00	MDBOXH2_HS[7:0]
0x433	R/W	0x00	MDBOXH2_HS[10:8]
0x434	R/W	0x00	MDBOXH3_HS[7:0]
0x435	R/W	0x00	MDBOXH3_HS[10:8]
0x436	R/W	0x00	MDBOXH0_VS[7:0]
0x437	R/W	0x00	MDBOXH0_VS[10:8]
0x438	R/W	0x00	MDBOXH1_VS[7:0]
0x439	R/W	0x00	MDBOXH1_VS[10:8]
0x43A	R/W	0x00	MDBOXH2_VS[7:0]
0x43B	R/W	0x00	MDBOXH2_VS[10:8]
0x43C	R/W	0x00	MDBOXH3_VS[7:0]
0x43D	R/W	0x00	MDBOXH3_VS[10:8]
0x43E	R/W	0xFF	[5:0]: MDBOXH0_HCELL
0x43F	R/W	0xFF	[5:0]: MDBOXH1_HCELL
0x440	R/W	0xFF	[5:0]: MDBOXH2_HCELL
0x441	R/W	0xFF	[5:0]: MDBOXH3_HCELL
0x442	R/W	0xBB	[5:0]: MDBOXH0_VCELL
0x443	R/W	0xBB	[5:0]: MDBOXH1_VCELL
0x444	R/W	0xBB	[5:0]: MDBOXH1_VCELL
0x445	R/W	0xBB	[5:0]: MDBOXH2_VCELL
0x446	R/W	0x00	[5:0]: CURH0_HPOS
0x447	R/W	0x00	[5:0]: CURH1_HPOS
0x448	R/W	0x00	[5:0]: CURH2_HPOS
0x449	R/W	0x00	[5:0]: CURH3_HPOS
0x44A	R/W	0x00	[5:0]: CURH0_VPOS
0x44B	R/W	0x00	[5:0]: CURH1_VPOS
0x44C	R/W	0x00	[5:0]: CURH2_VPOS
0x44D	R/W	0x00	[5:0]: CURH3_VPOS
0x44E	R/W	0x00	SBOX4_CTRL[4:0]
0x44F	R/W	0x00	SBOX5_CTRL[4:0]
0x450	R/W	0x00	SBOX6_CTRL[4:0]
0x451	R/W	0x00	SBOX7_CTRL[4:0]
0x452	R/W	0x00	[7:6]: SBOX5_V_LINE [5:4]: SBOX5_H_LINE [3:2]: SBOX4_V_LINE [1:0]: SBOX4_H_LINE
0x453	R/W	0x00	[7:6]: SBOX5_V_LINE [5:4]: SBOX5_H_LINE [3:2]: SBOX4_V_LINE [1:0]: SBOX4_H_LINE
0x454	R/W	0x00	SBOX4_HL[7:0]
0x455	R/W	0x00	SBOX4_HL[10:8]
0x456	R/W	0x00	SBOX5_HL[7:0]
0x457	R/W	0x00	SBOX5_HL[10:8]
0x458	R/W	0x00	SBOX6_HL[7:0]
0x459	R/W	0x00	SBOX6_HL[10:8]

0x45A	R/W	0x00	SBOX7_HL[7:0]
0x45B	R/W	0x00	SBOX7_HL[10:8]
0x45C	R/W	0x00	SBOX4_HR[7:0]
0x45D	R/W	0x00	SBOX4_HR[10:8]
0x45E	R/W	0x00	SBOX5_HR[7:0]
0x45F	R/W	0x00	SBOX5_HR[10:8]
0x460	R/W	0x00	SBOX6_HR[7:0]
0x461	R/W	0x00	SBOX6_HR[10:8]
0x462	R/W	0x00	SBOX7_HR[7:0]
0x463	R/W	0x00	SBOX7_HR[10:8]
0x464	R/W	0x00	SBOX4_VT[7:0]
0x465	R/W	0x00	SBOX4_VT[10:8]
0x466	R/W	0x00	SBOX5_VT[7:0]
0x467	R/W	0x00	SBOX5_VT[10:8]
0x468	R/W	0x00	SBOX6_VT[7:0]
0x469	R/W	0x00	SBOX6_VT[10:8]
0x46A	R/W	0x00	SBOX7_VT[7:0]
0x46B	R/W	0x00	SBOX7_VT[10:8]
0x46C	R/W	0x00	SBOX4_VB[7:0]
0x46D	R/W	0x00	SBOX4_VB[10:8]
0x46E	R/W	0x00	SBOX5_VB[7:0]
0x46F	R/W	0x00	SBOX5_VB[10:8]
0x470	R/W	0x00	SBOX6_VB[7:0]
0x471	R/W	0x00	SBOX6_VB[10:8]
0x472	R/W	0x00	SBOX7_VB[7:0]
0x473	R/W	0x00	SBOX7_VB[10:8]
0x474	R/W	0x00	BBR2: Box border R
0x475	R/W	0x00	BBG2: Box border G
0x476	R/W	0x00	BBB2: Box border B
0x477	R/W	0x00	BPR2: Box plane R
0x478	R/W	0x00	BPG2: Box plane G
0x479	R/W	0x00	BPB2: Box plane B
0x47A	R/W	0x00	MOUSE_BASE_ADDR[7:0]
0x47B	R/W	0x00	MOUSE_BASE_ADDR[15:8]
0x47C	R/W	0x00	MOUSE_BASE_ADDR[23:16]
0x47D	R/W	0x00	[4]: MOUSE_BUF [3:0]: MOUSE_INDEX
0x47E	R/W	0x00	VPOS_32[7:0]
0x47F	R/W	0x00	HPOS_32[7:0]
0x480	R/W	0x00	VSIZE_32[7:0]
0x481	R/W	0x00	HSIZE_32[7:0]
0x482	RW	0x00	[5:4]:HPOS_32[9:8] [3:0]: VPOS_32[11:8]
0x483	R/W	0x00	[4]:HSIZE_32[8] [2:0]: VSIZE_32[10:8]
0x484	R/W	0x00	[2]: CH32 FREEZE EN [1]: CH32_BND_EN [0]: CH32_EN
0x485	R/W	0x80	[7]: OUT_DIS [6]: MDBOX_POS_SEL [5]: Reserved [4]: BND_EN [3]: COLBAR_EN [2]: SWITCH_EN [1]: HSPOL [0]: VSPOL
0x486	R/W	0x2F	[7:4]: BND_WIDTH

			[3:0]: VSDEL
0x487	R/W	0xFF	BND_R: Channel Boundary R
0x488	R/W	0xFF	BND_G: Channel Boundary G
0x489	R/W	0xFF	BND_B: Channel Boundary B
0x48A	R/W	0x00	MOTION_BASE_ADDR[7:0]
0x48B	R/W	0x00	MOTION_BASE_ADDR[15:8]
0x48C	R/W	0x00	MOTION_BASE_ADDR[23:16]
0x48D	R/W	0x00	MOTION_HD_BASE_ADDR[7:0]
0x48E	R/W	0x00	MOTION_HD_BASE_ADDR[15:8]
0x48F	R/W	0x00	MOTION_HD_BASE_ADDR[23:16]
0x490	R/W	0x00	[0]: MOUSE_UPDATE_EN, MOUSE_UPDATE_BUSY
0x491	R/W	0x00	POS_HSCALE[7:0]
0x492	R/W	0x10	POS_HSCALE[15:8]
0x493	R/W	0x00	POS_VSCALE[7:0]
0x494	R/W	0x10	POS_VSCALE[15:8]
0x495	R/W	0x00	[0]: POS_UPS_EN
0x496	R/W	0x00	[1:0]: OSD_BLINK_TIME
0x497	R/W	0x00	[7:4]: CUR1_VPOS [3:0]: CUR0_VPOS
0x498	R/W	0x00	[7:4]: CUR3_VPOS [3:0]: CUR2_VPOS
0x499	R/W	0x00	[7:4]: CUR5_VPOS [3:0]: CUR4_VPOS
0x49A	R/W	0x00	[7:4]: CUR7_VPOS [3:0]: CUR6_VPOS
0x49B	R/W	0x00	[7:4]: CUR9_VPOS [3:0]: CUR8_VPOS
0x49C	R/W	0x00	[7:4]: CUR11_VPOS [3:0]: CUR10_VPOS
0x49D	R/W	0x00	[7:4]: CUR13_VPOS [3:0]: CUR12_VPOS
0x49E	R/W	0x00	[7:4]: CUR15_VPOS [3:0]: CUR14_VPOS
0x49F	R/W	0x00	MDBOX_OBR
0x4A0	R/W	0x00	MDBOX_OBG
0x4A1	R/W	0x00	MDBOX_OBB
0x4A2	R/W	0x00	MDBOX_IBR
0x4A3	R/W	0x00	MDBOX_IBG
0x4A4	R/W	0x00	MDBOX_IBB
0x4A5	R/W	0x00	MDBOX_MSKR
0x4A6	R/W	0x00	MDBOX_MSKG
0x4A7	R/W	0x00	MDBOX_MSKB
0x4A8	R/W	0x00	MDBOX_PR
0x4A9	R/W	0x00	MDBOX_PG
0x4AA	R/W	0x00	MDBOX_PB
0x4AC	R/W	0x00	HSTART[7:0]
0x4AD	R/W	0x00	HSTART[9:8]
0x4AE	R/W	0x00	VSTART[7:0]
0x4AF	R/W	0x00	VSTART[11:8]
0x4B0	R/W	0xFF	VTT_WIN
0x4B1	R/W	0x00	[2]: VTT_ADJUST [1]: VTT_ADJUST_MODE [0]: VTT_ADJUST_EN
0x4B2	RO	-	NEW_VTT_RGBW[7:0]
0x4B3	RO	-	NEW_VTT_RGBW[11:8]
0x4B4	RO	-	NEW_VTT[7:0]
0x4B5	RO	-	NEW_VTT[10:8]

0x4B6	R/W	0xFF	[7:4]: BND_EN_1 [3:0]: BND_EN_0
0x4B7	R/W	0xFF	[7:4]: BND_EN_3 [3:0]: BND_EN_2
0x4B8	R/W	0xFF	[7:4]: BND_EN_5 [3:0]: BND_EN_4
0x4B9	R/W	0xFF	[7:4]: BND_EN_7 [3:0]: BND_EN_6
0x4BA	R/W	0xFF	[7:4]: BND_EN_9 [3:0]: BND_EN_8
0x4BB	R/W	0xFF	[7:4]: BND_EN_11 [3:0]: BND_EN_10
0x4BC	R/W	0xFF	[7:4]: BND_EN_13 [3:0]: BND_EN_12
0x4BD	R/W	0xFF	[7:4]: BND_EN_15 [3:0]: BND_EN_14
0x4BE	R/W	0xFF	[7:4]: BND_EN_17 [3:0]: BND_EN_16
0x4BF	R/W	0xFF	[7:4]: BND_EN_19 [3:0]: BND_EN_18
0x4C0	R/W	0xFF	[7:4]: BND_EN_34 [3:0]: BND_EN_33
0x4C1	R/W	0xFF	[7:4]: BND_EN_36 [3:0]: BND_EN_35
0x4C2	R/W	0xFF	BND_CH_EN[35:32]
0x4C3	R/W	0xFF	FRSC_CH_EN[35:32]
0x4C4	R/W	0x91	Y value for live or PB test pattern generator solid color
0x4C5	R/W	0x36	CB value for live or PB test pattern generator solid color
0x4C6	R/W	0x22	CR value for live or PB test pattern generator solid color
0x4C7	R/W	0x00	[4]: EOSD_SEL [3]: EOSD_EN [2]: EOSD_MODE [1]: EOSD_EN_DIS [0]: EOSD_ALPHA_EN
0x4C8	R/W	0x00	[3:0]: EOSD_ALPHA
0x4C9	R/W	0x00	EOSD_R
0x4CA	R/W	0x00	EOSD_G
0x4CB	R/W	0x00	EOSD_B
0x4CC ~0x4CD	R/W	0xFF	Reserved
0x4CE	R/W	0x00	FRSC_DBG_CTRL [7]: rd_buf_id_toggle [6]: rd_buf_inc [5]: wr_page_fix [4]: rd_page_fix [3:2]: wr_page_sel [1:0]: rd_page_sel
0x4CF	R/W	0x60	[7:5]: WR_BUF_OFST [4]: INTERLACE_DBG [3]: VTT_INV [2]:EVEN_REPEAT [1]:DMON_VS_EN [0]:interlace
0x4D0	R/W	0xFF	[7:4]: BND_EN_21 [3:0]: BND_EN_20
0x4D1	R/W	0xFF	[7:4]: BND_EN_23 [3:0]: BND_EN_22
0x4D2	R/W	0xFF	[7:4]: BND_EN_25

			[3:0]: BND_EN_24
0x4D3	R/W	0xFF	[7:4]: BND_EN_27 [3:0]: BND_EN_26
0x4D4	R/W	0xFF	[7:4]: BND_EN_29 [3:0]: BND_EN_28
0x4D5	R/W	0xFF	[7:4]: BND_EN_31 [3:0]: BND_EN_30
0x4D6	R/W	0x00	Reserved
0x4D7	R/W	0x00	Reserved
0x4D8	R/W	0x00	Reserved
0x4D9	R/W	0x00	Reserved
0x4DA	R/W	0x00	[6]: OSD_CH_EN_SEL [5]: NOVID_SWITCH_EN [4]: BND_CH_EN_SEL [3]: PEAK_C_DUP [2]: GAIN_EN [1]: READ_DLY [0]: GAMA_EN
0x4DB	R/W	0x00	FRSC_DBG_CTRL[15:8] [5:4]: rd_buf_id_sel_dm [3:2]: rd_buf_id_sel [1]: fld_inv [0]: all_available
0x4DC	R/W	0x30	WE_2D_SEL[7:0]
0x4DD	R/W	0x00	WE_2D_SEL[15:8]
0x4DE	R/W	0x00	WE_2D_SEL[23:16]
0x4DF	R/W	0x00	WE_2D_SEL[31:24]
0x4E0	R/W	0x00	WE_2D_SEL[36:32]
0x4E1	R/W	0x8f	HDE_W[7:0]
0x4E2	R/W	0x06	HDE_W [10:8]
0x4E3	R/W	0x19	VDE_W[7:0]
0x4E4	R/W	0x04	VDE_W [10:8]
0x4E5	R/W	0x00	MIX_MODE_SET
0x4E6	R/W	0x40	R_GAIN
0x4E7	R/W	0x40	G_GAIN
0x4E8	R/W	0x40	B_GAIN
0x4E9	R/W	0	R_OFST
0x4EA	R/W	0	G_OFST
0x4EB	R/W	0	B_OFST
0x4EC	R/W	0	BND_CH_EN[7:0]
0x4ED	R/W	0	BND_CH_EN[15:8]
0x4EE	R/W	0	BND_CH_EN[23:16]
0x4EF	R/W	0	BND_CH_EN[31:24]
0x4F0	R/W	0xFF	FRSC_CH_EN[7:0]
0x4F1	R/W	0xFF	FRSC_CH_EN[15:8]
0x4F2	R/W	0xFF	FRSC_CH_EN[23:16]
0x4F3	R/W	0xFF	FRSC_CH_EN[31:24]
0x4F4	R/W	0	NOVID_R
0x4F5	R/W	0	NOVID_G
0x4F6	R/W	0xFF	NOVID_B
0x4F7	R/W	0x00	rg_2ddi_ctl
0x4F8	R/W	0x28	rg_2ddi_thd1
0x4F9	R/W	0x1E	rg_2ddi_thd2
0x4FA	R/W	0x28	rg_2ddi_thd3
0x4FB	R/W	0x10	rg_2ddi_thd4
0x4FC	R/W	0x24	rg_2ddi_thd5
0x4FD	R/W	0x6F	rg_2ddi_thd6

0x4FE	R/W	0x20	[6]: rg_afm_ctl [5]: ups_interlace_off [4]: weave_interlace_off [3]: weave_up_en [2]: rg_di_use_bob [1]: weave_2d_mix_en [0]: rg_force_2ddi
0x4FF	R/W	0x00	HD_CH_SEL[1:0]
0x500	R/W	0x2F	HTT[7:0]
0x501	R/W	0x07	HTT[12:8]
0x502	R/W	0x37	VTT[7:0]
0x503	R/W	0x04	VTT[10:8]
0x504	R/W	0x8F	HDE[7:0]
0x505	R/W	0x06	HDE[10:8]
0x506	R/W	0x19	VDE[7:0]
0x507	R/W	0x04	VDE[10:8]
0x508	R/W	0x30	PHSYNC[8:1]
0x509	R/W	0x02	PVSYNC[7:0]
0x50A	R/W	0x20	HSPW[7:0]
0x50B	R/W	0x06	VSPW[7:0]
0x50C	R/W	0x00	SBOX0_CTRL[4:0]
0x50D	R/W	0x00	SBOX1_CTRL[4:0]
0x50E	R/W	0x00	SBOX2_CTRL[4:0]
0x50F	R/W	0x00	SBOX3_CTRL[4:0]
0x511	R/W	0x00	[7:6]: SBOX3_V_LINE [5:4]: SBOX3_H_LINE [3:2]: SBOX2_V_LINE [1:0]: SBOX2_H_LINE
0x512	R/W	0x00	[7:6]: SBOX1_V_LINE [5:4]: SBOX1_H_LINE [3:2]: SBOX0_V_LINE [1:0]: SBOX0_H_LINE
0x513	R/W	0x00	SBOX0_HL[7:0]
0x514	R/W	0x00	SBOX0_HL[10:8]
0x515	R/W	0x00	SBOX1_HL[7:0]
0x516	R/W	0x00	SBOX1_HL[10:8]
0x517	R/W	0x00	SBOX2_HL[7:0]
0x518	R/W	0x00	SBOX2_HL[10:8]
0x519	R/W	0x00	SBOX3_HL[7:0]
0x51A	R/W	0x00	SBOX3_HL[10:8]
0x51B	R/W	0x00	SBOX0_HR[7:0]
0x51C	R/W	0x00	SBOX0_HR[10:8]
0x51D	R/W	0x00	SBOX1_HR[7:0]
0x51E	R/W	0x00	SBOX1_HR[10:8]
0x51F	R/W	0x00	SBOX2_HR[7:0]
0x520	R/W	0x00	SBOX2_HR[10:8]
0x521	R/W	0x00	SBOX3_HR[7:0]
0x522	R/W	0x00	SBOX3_HR[10:8]
0x523	R/W	0x00	SBOX0_VT[7:0]
0x524	R/W	0x00	SBOX0_VT[10:8]
0x525	R/W	0x00	SBOX1_VT[7:0]
0x526	R/W	0x00	SBOX1_VT[10:8]
0x527	R/W	0x00	SBOX2_VT[7:0]
0x528	R/W	0x00	SBOX2_VT[10:8]
0x529	R/W	0x00	SBOX3_VT[7:0]

0x52A	R/W	0x00	SBOX3_VT[10:8]
0x52B	R/W	0x00	SBOX0_VB[7:0]
0x52C	R/W	0x00	SBOX0_VB[10:8]
0x52D	R/W	0x00	SBOX1_VB[7:0]
0x52E	R/W	0x00	SBOX1_VB[10:8]
0x52F	R/W	0x00	SBOX2_VB[7:0]
0x530	R/W	0x00	SBOX2_VB[10:8]
0x531	R/W	0x00	SBOX3_VB[7:0]
0x532	R/W	0x00	SBOX3_VB[10:8]
0x533	R/W	0x00	BBR: Box border R
0x534	R/W	0x00	BBG: Box border G
0x535	R/W	0x00	BBB: Box border B
0x536	R/W	0x00	BPR: Box plane R
0x537	R/W	0x00	BPG: Box plane G
0x538	R/W	0x00	BPB: Box plane B
0x539	R/W	0x00	BAR: Background R
0x53A	R/W	0x00	BAG: Background G
0x53B	R/W	0x00	BAB: Background B
0x53C	R/W	0x00	MOUSE0_HPOS[7:0]
0x53D	R/W	0x00	MOUSE0_HPOS[10:8]
0x53E	R/W	0x00	MOUSE0_VPOS[7:0]
0x53F	R/W	0x00	MOUSE0_VPOS[10:8]
0x540	R/W	0x00	MOUSE1_HPOS[7:0]
0x541	R/W	0x00	MOUSE1_HPOS[10:8]
0x542	R/W	0x00	MOUSE1_VPOS[7:0]
0x543	R/W	0x00	MOUSE1_VPOS[10:8]
0x544	R/W	0x00	[6:4]: MOUSE1_CTRL [2:0]: MOUSE0_CTRL
0x545	R/W	0x00	BR: mouse background R
0x546	R/W	0x00	BG: mouse background G
0x547	R/W	0x00	BB: mouse background B
0x548	R/W	0x00	FR: mouse foreground R
0x549	R/W	0x00	FG: mouse foreground G
0x54A	R/W	0x00	FB: mouse foreground B
0x54B	R/W	0x00	DMODE[1:0]
0x54C	R/W	0x00	MOUSE_WR_LOC[7:0]
0x54D	R/W	0x00	MOUSE_WR_DATA
0x54E	R/W	0x01	MOUSE_REG_UPDATE
0x54F	WO	0x00	MOUSE_WR_EN
0x550	R/W	0x00	MDBOX0_CTRL[7:0]
0x551	R/W	0x00	MDBOX1_CTRL[7:0]
0x552	R/W	0x00	MDBOX2_CTRL[7:0]
0x553	R/W	0x00	MDBOX3_CTRL[7:0]
0x554	R/W	0x00	MDBOX4_CTRL[7:0]
0x555	R/W	0x00	MDBOX5_CTRL[7:0]
0x556	R/W	0x00	MDBOX6_CTRL[7:0]
0x557	R/W	0x00	MDBOX7_CTRL[7:0]
0x558	R/W	0x00	MDBOX8_CTRL[7:0]
0x559	R/W	0x00	MDBOX9_CTRL[7:0]
0x55A	R/W	0x00	MDBOX10_CTRL[7:0]
0x55B	R/W	0x00	MDBOX11_CTRL[7:0]
0x55C	R/W	0x00	MDBOX12_CTRL[7:0]
0x55D	R/W	0x00	MDBOX13_CTRL[7:0]
0x55E	R/W	0x00	MDBOX14_CTRL[7:0]
0x55F	R/W	0x00	MDBOX15_CTRL[7:0]
0x560	R/W	0x00	[7:6]: MDBOX1_V_LINE

			[5:4]: MDBOX1_H_LINE [3:2]: MDBOX0_V_LINE [1:0]: MDBOX0_H_LINE
0x561	R/W	0x00	[7:6]: MDBOX3_V_LINE [5:4]: MDBOX3_H_LINE [3:2]: MDBOX2_V_LINE [1:0]: MDBOX2_H_LINE
0x562	R/W	0x00	[7:6]: MDBOX5_V_LINE [5:4]: MDBOX5_H_LINE [3:2]: MDBOX4_V_LINE [1:0]: MDBOX4_H_LINE
0x563	R/W	0x00	[7:6]: MDBOX7_V_LINE [5:4]: MDBOX7_H_LINE [3:2]: MDBOX6_V_LINE [1:0]: MDBOX6_H_LINE
0x564	R/W	0x00	[7:6]: MDBOX9_V_LINE [5:4]: MDBOX9_H_LINE [3:2]: MDBOX8_V_LINE [1:0]: MDBOX8_H_LINE
0x565	R/W	0x00	[7:6]: MDBOX11_V_LINE [5:4]: MDBOX11_H_LINE [3:2]: MDBOX10_V_LINE [1:0]: MDBOX10_H_LINE
0x566	R/W	0x00	[7:6]: MDBOX13_V_LINE [5:4]: MDBOX13_H_LINE [3:2]: MDBOX12_V_LINE [1:0]: MDBOX12_H_LINE
0x567	R/W	0x00	[7:6]: MDBOX15_V_LINE [5:4]: MDBOX15_H_LINE [3:2]: MDBOX14_V_LINE [1:0]: MDBOX14_H_LINE
0x568	R/W	0x00	MDBOX0_HL[7:0]
0x569	R/W	0x00	MDBOX0_HL[10:8]
0x56A	R/W	0x00	MDBOX1_HL[7:0]
0x56B	R/W	0x00	MDBOX1_HL[10:8]
0x56C	R/W	0x00	MDBOX2_HL[7:0]
0x56D	R/W	0x00	MDBOX2_HL[10:8]
0x56E	R/W	0x00	MDBOX3_HL[7:0]
0x56F	R/W	0x00	MDBOX3_HL[10:8]
0x570	R/W	0x00	MDBOX4_HL[7:0]
0x571	R/W	0x00	MDBOX4_HL[10:8]
0x572	R/W	0x00	MDBOX5_HL[7:0]
0x573	R/W	0x00	MDBOX5_HL[10:8]
0x574	R/W	0x00	MDBOX6_HL[7:0]
0x575	R/W	0x00	MDBOX6_HL[10:8]
0x576	R/W	0x00	MDBOX7_HL[7:0]
0x577	R/W	0x00	MDBOX7_HL[10:8]
0x578	R/W	0x00	MDBOX8_HL[7:0]
0x579	R/W	0x00	MDBOX8_HL[10:8]
0x57A	R/W	0x00	MDBOX9_HL[7:0]
0x57B	R/W	0x00	MDBOX9_HL[10:8]
0x57C	R/W	0x00	MDBOX10_HL[7:0]
0x57D	R/W	0x00	MDBOX10_HL[10:8]
0x57E	R/W	0x00	MDBOX11_HL[7:0]
0x57F	R/W	0x00	MDBOX11_HL[10:8]
0x580	R/W	0x00	MDBOX12_HL[7:0]
0x581	R/W	0x00	MDBOX12_HL[10:8]

0x582	R/W	0x00	MDBOX13_HL[7:0]
0x583	R/W	0x00	MDBOX13_HL[10:8]
0x584	R/W	0x00	MDBOX14_HL[7:0]
0x585	R/W	0x00	MDBOX14_HL[10:8]
0x586	R/W	0x00	MDBOX15_HL[7:0]
0x587	R/W	0x00	MDBOX15_HL[10:8]
0x588	R/W	0x00	MDBOX0_VT[7:0]
0x589	R/W	0x00	MDBOX0_VT[10:8]
0x58A	R/W	0x00	MDBOX1_VT[7:0]
0x58B	R/W	0x00	MDBOX1_VT[10:8]
0x58C	R/W	0x00	MDBOX2_VT[7:0]
0x58D	R/W	0x00	MDBOX2_VT[10:8]
0x58E	R/W	0x00	MDBOX3_VT[7:0]
0x58F	R/W	0x00	MDBOX3_VT[10:8]
0x590	R/W	0x00	MDBOX4_VT[7:0]
0x591	R/W	0x00	MDBOX4_VT[10:8]
0x592	R/W	0x00	MDBOX5_VT[7:0]
0x593	R/W	0x00	MDBOX5_VT[10:8]
0x594	R/W	0x00	MDBOX6_VT[7:0]
0x595	R/W	0x00	MDBOX6_VT[10:8]
0x596	R/W	0x00	MDBOX7_VT[7:0]
0x597	R/W	0x00	MDBOX7_VT[10:8]
0x598	R/W	0x00	MDBOX8_VT[7:0]
0x599	R/W	0x00	MDBOX8_VT[10:8]
0x59A	R/W	0x00	MDBOX9_VT[7:0]
0x59B	R/W	0x00	MDBOX9_VT[10:8]
0x59C	R/W	0x00	MDBOX10_VT[7:0]
0x59D	R/W	0x00	MDBOX10_VT[10:8]
0x59E	R/W	0x00	MDBOX11_VT[7:0]
0x59F	R/W	0x00	MDBOX11_VT[10:8]
0x5A0	R/W	0x00	MDBOX12_VT[7:0]
0x5A1	R/W	0x00	MDBOX12_VT[10:8]
0x5A2	R/W	0x00	MDBOX13_VT[7:0]
0x5A3	R/W	0x00	MDBOX13_VT[10:8]
0x5A4	R/W	0x00	MDBOX14_VT[7:0]
0x5A5	R/W	0x00	MDBOX14_VT[10:8]
0x5A6	R/W	0x00	MDBOX15_VT[7:0]
0x5A7	R/W	0x00	MDBOX15_VT[10:8]
0x5A8	R/W	0x00	MDBOX0_HS[7:0]
0x5A9	R/W	0x00	MDBOX0_HS[10:8]
0x5AA	R/W	0x00	MDBOX1_HS[7:0]
0x5AB	R/W	0x00	MDBOX1_HS[10:8]
0x5AC	R/W	0x00	MDBOX2_HS[7:0]
0x5AD	R/W	0x00	MDBOX2_HS[10:8]
0x5AE	R/W	0x00	MDBOX3_HS[7:0]
0x5AF	R/W	0x00	MDBOX3_HS[10:8]
0x5B0	R/W	0x00	MDBOX4_HS[7:0]
0x5B1	R/W	0x00	MDBOX4_HS[10:8]
0x5B2	R/W	0x00	MDBOX5_HS[7:0]
0x5B3	R/W	0x00	MDBOX5_HS[10:8]
0x5B4	R/W	0x00	MDBOX6_HS[7:0]
0x5B5	R/W	0x00	MDBOX6_HS[10:8]
0x5B6	R/W	0x00	MDBOX7_HS[7:0]
0x5B7	R/W	0x00	MDBOX7_HS[10:8]
0x5B8	R/W	0x00	MDBOX8_HS[7:0]
0x5B9	R/W	0x00	MDBOX8_HS[10:8]

0x5BA	R/W	0x00	MDBOX9_HS[7:0]
0x5BB	R/W	0x00	MDBOX9_HS[10:8]
0x5BC	R/W	0x00	MDBOX10_HS[7:0]
0x5BD	R/W	0x00	MDBOX10_HS[10:8]
0x5BE	R/W	0x00	MDBOX11_HS[7:0]
0x5BF	R/W	0x00	MDBOX11_HS[10:8]
0x5C0	R/W	0x00	MDBOX12_HS[7:0]
0x5C1	R/W	0x00	MDBOX12_HS[10:8]
0x5C2	R/W	0x00	MDBOX13_HS[7:0]
0x5C3	R/W	0x00	MDBOX13_HS[10:8]
0x5C4	R/W	0x00	MDBOX14_HS[7:0]
0x5C5	R/W	0x00	MDBOX14_HS[10:8]
0x5C6	R/W	0x00	MDBOX15_HS[7:0]
0x5C7	R/W	0x00	MDBOX15_HS[10:8]
0x5C8	R/W	0x00	MDBOX0_VS[7:0]
0x5C9	R/W	0x00	MDBOX0_VS[10:8]
0x5CA	R/W	0x00	MDBOX1_VS[7:0]
0x5CB	R/W	0x00	MDBOX1_VS[10:8]
0x5CC	R/W	0x00	MDBOX2_VS[7:0]
0x5CD	R/W	0x00	MDBOX2_VS[10:8]
0x5CE	R/W	0x00	MDBOX3_VS[7:0]
0x5CF	R/W	0x00	MDBOX3_VS[10:8]
0x5D0	R/W	0x00	MDBOX4_VS[7:0]
0x5D1	R/W	0x00	MDBOX4_VS[10:8]
0x5D2	R/W	0x00	MDBOX5_VS[7:0]
0x5D3	R/W	0x00	MDBOX5_VS[10:8]
0x5D4	R/W	0x00	MDBOX6_VS[7:0]
0x5D5	R/W	0x00	MDBOX6_VS[10:8]
0x5D6	R/W	0x00	MDBOX7_VS[7:0]
0x5D7	R/W	0x00	MDBOX7_VS[10:8]
0x5D8	R/W	0x00	MDBOX8_VS[7:0]
0x5D9	R/W	0x00	MDBOX8_VS[10:8]
0x5DA	R/W	0x00	MDBOX9_VS[7:0]
0x5DB	R/W	0x00	MDBOX9_VS[10:8]
0x5DC	R/W	0x00	MDBOX10_VS[7:0]
0x5DD	R/W	0x00	MDBOX10_VS[10:8]
0x5DE	R/W	0x00	MDBOX11_VS[7:0]
0x5DF	R/W	0x00	MDBOX11_VS[10:8]
0x5E0	R/W	0x00	MDBOX12_VS[7:0]
0x5E1	R/W	0x00	MDBOX12_VS[10:8]
0x5E2	R/W	0x00	MDBOX13_VS[7:0]
0x5E3	R/W	0x00	MDBOX13_VS[10:8]
0x5E4	R/W	0x00	MDBOX14_VS[7:0]
0x5E5	R/W	0x00	MDBOX14_VS[10:8]
0x5E6	R/W	0x00	MDBOX15_VS[7:0]
0x5E7	R/W	0x00	MDBOX15_VS[10:8]
0x5E8	R/W	0xFF	[7:4]: MDBOX1_HCELL [3:0]: MDBOX0_HCELL
0x5E9	R/W	0xFF	[7:4]: MDBOX3_HCELL [3:0]: MDBOX2_HCELL
0x5EA	R/W	0xFF	[7:4]: MDBOX5_HCELL [3:0]: MDBOX4_HCELL
0x5EB	R/W	0xFF	[7:4]: MDBOX7_HCELL [3:0]: MDBOX6_HCELL
0x5EC	R/W	0xFF	[7:4]: MDBOX9_HCELL [3:0]: MDBOX8_HCELL

0x5ED	R/W	0xFF	[7:4]: MDBOX11_HCELL [3:0]: MDBOX10_HCELL
0x5EE	R/W	0xFF	[7:4]: MDBOX13_HCELL [3:0]: MDBOX12_HCELL
0x5EF	R/W	0xFF	[7:4]: MDBOX15_HCELL [3:0]: MDBOX14_HCELL
0x5F0	R/W	0xBB	[7:4]: MDBOX1_VCELL [3:0]: MDBOX0_VCELL
0x5F1	R/W	0xBB	[7:4]: MDBOX3_VCELL [3:0]: MDBOX2_VCELL
0x5F2	R/W	0xBB	[7:4]: MDBOX5_VCELL [3:0]: MDBOX4_VCELL
0x5F3	R/W	0xBB	[7:4]: MDBOX7_VCELL [3:0]: MDBOX6_VCELL
0x5F4	R/W	0xBB	[7:4]: MDBOX9_VCELL [3:0]: MDBOX8_VCELL
0x5F5	R/W	0xBB	[7:4]: MDBOX11_VCELL [3:0]: MDBOX10_VCELL
0x5F6	R/W	0xBB	[7:4]: MDBOX13_VCELL [3:0]: MDBOX12_VCELL
0x5F7	R/W	0xBB	[7:4]: MDBOX15_VCELL [3:0]: MDBOX14_VCELL
0x5F8	R/W	0x00	[7:4]: CUR1_HPOS [3:0]: CUR0_HPOS
0x5F9	R/W	0x00	[7:4]: CUR3_HPOS [3:0]: CUR2_HPOS
0x5FA	R/W	0x00	[7:4]: CUR5_HPOS [3:0]: CUR4_HPOS
0x5FB	R/W	0x00	[7:4]: CUR7_HPOS [3:0]: CUR6_HPOS
0x5FC	R/W	0x00	[7:4]: CUR9_HPOS [3:0]: CUR8_HPOS
0x5FD	R/W	0x00	[7:4]: CUR11_HPOS [3:0]: CUR10_HPOS
0x5FE	R/W	0x00	[7:4]: CUR13_HPOS [3:0]: CUR12_HPOS
0x5FF	R/W	0x00	[7:4]: CUR15_HPOS [3:0]: CUR14_HPOS

Register

HEIGHT OF ONE FIELD IN BUFFER REGISTER LOW BYTE – 0X400

Bit	R/W	Default	Description
7:0	R/W	0xF0	rg_man_wr_height [7:0] This number specifies the number of lines in the field. It is half of frame height.

HEIGHT OF ONE FIELD IN BUFFER REGISTER HIGH BYTE – 0X401

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	rg_man_wr_height [10:8] This number specifies the number of lines in the field. It is half of frame height.

WIDTH OF ONE FIELD IN BUFFER REGISTER LOW BYTE – 0X402

Bit	R/W	Default	Description
7:0	R/W	0xD0	rg_man_wr_width [7:0] This number specifies the number of pixels per line in the buffer.

WIDTH OF ONE FIELD IN BUFFER REGISTER HIGH BYTE – 0X403

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x2	rg_man_wr_width [10:8] This number specifies the number of pixels per line in the buffer.

UP-SCALE CONTROL REGISTER – 0X404

Bit	R/W	Default	Description
7:4	R/W	0x0	rg_ups1_vsharp_gain There is a sharpener before upscaler. This register controls the sharpening weighting.
3:2	R/W	0x0	Reserved
1	R/W	0x0	rg_ups1_vlimit_on 1 = remove overshoot 0 = turn off overshoot removal
0	R/W	0x0	rg_disable_man_disp 1 = black out the panel 0 = normal operation

UP-SCALE BACKGROUND COLOR – 0X405

Bit	R/W	Default	Description
7:0	R/W	0x00	rg_BGcolor The background color used when there is no valid data in the main stream. This is also the color used in the border of the video window. The color is specified as 2 bit Y, 3 bit Cb, 2 bit Cr

UP-SCALE HORIZONTAL FACTOR LOW BYTE REGISTER – 0X406

Bit	R/W	Default	Description
7:0	R/W	0x00	rg_ups1_hscale [7:0] When rg_ups1_hscale == 0x1000, the horizontal scaling factor is 1. When rg_ups1_hscale is any number smaller than 0x1000, the main path picture is up scaled horizontally. When rg_ups1_hscale Is larger than 0x1000, the main video window is down scaled horizontally. The down scaling has to be less than 0x2000

UP-SCALE HORIZONTAL FACTOR HIGH BYTE REGISTER – 0X407

Bit	R/W	Default	Description
7:5	R	0x0	Reserved
4:0	R/W	0x10	rg_ups1_hscale [12:8] When rg_ups1_hscale == 0x1000, the horizontal scaling factor is 1. When rg_ups1_hscale is any number smaller than 0x1000, the main path picture is up scaled horizontally. When rg_ups1_hscale Is greater than 0x1000, the main video window is down scaled horizontally. The down scaling has to be less than 0x2000

UP-SCALE VERTICAL FACTOR LOW BYTE REGISTER – 0X408

Bit	R/W	Default	Description
7:0	R/W	0x00	rg_ups1_vscale [7:0] When rg_ups1_vscale == 0x400, the vertical scaling factor is 1 When rg_ups1_vscale is any number smaller than 0x400, the main path picture is up scaled vertically. When rg_ups1_vscale is any number greater than 0x400, the main path picture is down scaled vertically The downscaling has to be less than 0x500

UP-SCALE VERTICAL FACTOR HIGH BYTE REGISTER – 0X409

Bit	R/W	Default	Description
7:3	R	0x0	Reserved

Bit	R/W	Default	Description
2:0	R/W	0x4	rg_ups1_vscale [10:8] When rg_ups1_vscale == 0x400, the vertical scaling factor is 1 When rg_ups1_vscale is any number smaller than 0x400, the main path picture is up scaled vertically. When rg_ups1_vscale is any number greater than 0x400, the main path picture is down scaled vertically The downscaling has to be less than 0x500

UP-SCALE HORIZONTAL START LOW BYTE REGISTER – 0X40A

Bit	R/W	Default	Description
7:0	R/W	0x00	rg_ups1_Xst [7:0] Main Video Window Horizontal Starting location, unit is pixel

UP-SCALE HORIZONTAL START HIGH BYTE REGISTER – 0X40B

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	rg_ups1_Xst [10:8] Main Video Window Horizontal Starting location, unit is pixel

UP-SCALE VERTICAL START LOW BYTE REGISTER – 0X40C

Bit	R/W	Default	Description
7:0	R/W	0x00	rg_ups1_Yst [7:0] Main Video Window Vertical Starting location, unit is line

UP-SCALE VERTICAL START HIGH BYTE REGISTER – 0X40D

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	rg_ups1_Yst [10:8] Main Video Window Vertical Starting location, unit is line

UP-SCALE OUTPUT WIDTH LOW BYTE REGISTER – 0X40E

Bit	R/W	Default	Description
7:0	R/W	0xD0	rg_ups1_Xmax [7:0] Main Video Window width after scaling, unit is pixel

UP-SCALE OUTPUT WIDTH HIGH BYTE REGISTER – 0X40F

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x2	rg_ups1_Xmax [10:8] Main Video Window width after scaling, unit is pixel

UP-SCALE OUTPUT HEIGHT LOW BYTE REGISTER – 0X410

Bit	R/W	Default	Description
7:0	R/W	0xE0	rg_ups1_Ymax [7:0] Main Video Window height after scaling, unit is line

UP-SCALE OUTPUT HEIGHT HIGH BYTE REGISTER – 0X411

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x1	rg_ups1_Ymax [10:8] Main Video Window height after scaling, unit is line

UP-SCALE X BOUNDARY WIDTH REGISTER – 0X412

Bit	R/W	Default	Description
7:0	R/W	0x00	rg_ups1_Xoff Main Video Window horizontal colored boundary width. When the panorama / Water glass mode is on, this offset specifies the width of the band at two side of the picture that will be scaled into panorama / water glass

UP-SCALE Y BOUNDARY WIDTH REGISTER – 0X413

Bit	R/W	Default	Description
7:0	R/W	0x00	rg_ups1_Yoff Main Video Window vertical colored boundary width.

UP-SCALE PANORAMA / WATER GLASS CONTROL REGISTER – 0X414

Bit	R/W	Default	Description
7	R/W	0x0	rg_ups1_panorama 1 = Enable Panorama / Water glass scaling. 0 = Disable Panorama / Water glass scaling

Bit	R/W	Default	Description
6	R/W	0x0	**rg_ups1_hs_type** 0 = Concave (Panorama) 1 = Convex (Water Glass)
5:4	R/W	0x0	**rg_ups1_hs_step** When Panorama / Water glass is on, the scaling factor increased/decresed every N pixels at the input side. 0 : N = 1, 1: N = 2, 2: N = 4, 3: N = 8.
3:0	R/W	0x0	**rg_ups1_hs_inc** The scaling factor change between steps of input pixels as specified in bit 5:4. This change is added/subtracted from the scaling factor of the previous step closer to the center.

UP-SCALE HORIZONTAL CENTER SCALE FACTOR LOW BYTE REGISTER – 0X415

Bit	R/W	Default	Description
7:0	R/W	0x00	**rg_ups1_hs_center [7:0]** The scaling factor at the center portion. When panorama/water glass mode is on, the horizontal scaling factor rg_ups1_hscale is not used. Instead, rg_ups1_hs_center is used for the center portion.

UP-SCALE HORIZONTAL CENTER SCALE FACTOR HIGH BYTE REGISTER – 0X416

Bit	R/W	Default	Description
7:5	R	0x00	**Reserved**
4:0	R/W	0x00	**rg_ups1_hs_center [12:8]** The scaling factor at the center portion. When panorama/water glass mode is on, the horizontal scaling factor rg_ups1_hscale is not used. Instead, rg_ups1_hs_center is used for the center portion.

UPSCALER OPTION REGISTER – 0X417

Bit	R/W	Default	Description
7:2	R	0	**Reserved**
1	R/W	0	**Ups1_dbg[1]** Vertical upscale parameter select
0	R/W	0	**Ups1_dbg[0]** Horizontal upscale parameter select

HD MD BOX CONTROL REGISTER 0 – 0X418

Bit	R/W	Default	Description
7	R/W	0x0	**MD Box Enable**

Bit	R/W	Default	Description
6	R/W	0x0	**MD Box operation mode select** 0 = table mode 1 = motion display mode
5	R/W	0x0	**Cursor Cell Enable** 0 = disable 1 = enable
4	R/W	0x0	**Out Boundary Cell Enable** 0 = disable 1 = enable
3	R/W	0x0	**Masking Plane Enable** 0 = disable 1 = enable
2	R/W	0x0	**Detection Plane Enable** 0 = disable 1 = enable
1:0	R/W	0x0	**Mixing control** 00 = 75% original pixel value / 25% plane (boundary) color mix 01 = 50% original pixel value / 50% plane (boundary) color mix 10 = 25% original pixel value / 75% plane (boundary) color mix 11 = plane (boundary) color

This register is for HD channel 1. Similar register 0x419 – 0x41B is for HD channel 2 – HD channel 4.

HD MD BOX LINE WIDTH CONTROL REGISTER 0 – 0X41C

Bit	R/W	Default	Description
7:6	R/W	0x0	**Box1 Vertical line width control** 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line
5:4	R/W	0x0	**Box1 Horizontal line width control** 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line
3:2	R/W	0x0	**Box0 Vertical line width control** 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line
1:0	R/W	0x0	**Box0 Horizontal line width control** 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line

This register is for box0, 1. Similar register 0X41D is for box 2, 3.

HD MD BOX 0 HORIZONTAL LEFT POSITION REGISTER 1 – 0X41E

Bit	R/W	Default	Description
7:0	R/W	0x0	Box 0 Horizontal Left Position MDBOX0_HL[7:0]

HD MD BOX 0 HORIZONTAL LEFT POSITION REGISTER 2 – 0X41F

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	Box 0 Horizontal Left Position MDBOX0_HL[10:8]

This register is for box0. Similar register 0x420 – 0x425 is for box 1 – box 3.

HD MD BOX 0 VERTICAL TOP POSITION REGISTER 1 – 0X426

Bit	R/W	Default	Description
7:0	R/W	0x0	Box 0 Vertical Top Position MDBOX0_VT[7:0]

HD MD BOX 0 VERTICAL TOP POSITION REGISTER 2 – 0X427

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	Box 0 Vertical Top Position MDBOX0_VT[10:8]

This register is for box0. Similar register 0x428 – 0x42D is for box 1 – box 3.

HD MD BOX 0 HORIZONTAL SIZE REGISTER 1 – 0X42E

Bit	R/W	Default	Description
7:0	R/W	0x0	Box 0 Horizontal Size Position MDBOX0_HS[7:0]

HD MD BOX 0 HORIZONTAL SIZE REGISTER 2 – 0X42F

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	Box 0 Horizontal Size Position MDBOX0_HS[10:8]

This register is for box0. Similar register 0x430 – 0x435 is for box 1 – box 3.

HD MD BOX 0 VERTICAL SIZE REGISTER 1 – 0X436

Bit	R/W	Default	Description
7:0	R/W	0x0	**Box 0 Vertical Size Position** MDBOX0_VS[7:0]

HD MD BOX 0 VERTICAL SIZE REGISTER 2 – 0X437

Bit	R/W	Default	Description
7:3	R	0x0	**Reserved**
2:0	R/W	0x0	**Box 0 Vertical Size Position** MDBOX0_VS[10:8]

This register is for box0. Similar register 0x438 – 0x43D is for box 1 – box 3.

HD MD BOX HCELL REGISTER 0 – 0X43E

Bit	R/W	Default	Description
7:6	R	0x0	**Reserved**
5:0	R/W	0x0	**Box 0 Horizontal Cell Number** MDBOX0_HNUM[3:0]

This register is for box0. Similar register 0x43F – 0x441 is for box 1 – box 3.

HD MD BOX VCELL REGISTER 0 – 0X442

Bit	R/W	Default	Description
7:6	R	0x0	**Reserved**
5:0	R/W	0x0	**Box 0 Vertical Cell Number** MDBOX0_VNUM[3:0]

This register is for box0, 1. Similar register 0x443 – 0x445 is for box 1 – box 3.

HD MD BOX CURSOR HORIZONTAL POSITION REGISTER 0 – 0X446

Bit	R/W	Default	Description
7:4	R/W	0x0	**Box 1 Horizontal Cursor Position** CUR1_HPOS[3:0]
3:0	R/W	0x0	**Box 0 Horizontal Cursor Position** CUR0_HPOS[3:0]

This register is for box0. Similar register 0x447 – 0x449 is for box 1 – box 3.

HD MD BOX CURSOR VERTICAL POSITION REGISTER 0 – 0X44A

Bit	R/W	Default	Description
7:4	R/W	0x0	**Box 1 Vertical Cursor Position** CUR1_VPOS[3:0]
3:0	R/W	0x0	**Box 0 Vertical Cursor Position** CUR0_VPOS[3:0]

This register is for box0. Similar register 0x44B – 0x44D is for box 1 – box 3.

SINGLE BOX 4 TO 7 REGISTER – 0X44E TO 0X479

Single box 4 to 7 are same as single box 0 to 3. Please refer to register 0x50C 0x538

MOUSE BASE ADDRESS LOW BYTE REGISTER – 0X47A

Bit	R/W	Default	Description
7:0	R/W	0x00	**MOUSE_BASE_ADDR[7:0]** There are 16 mouse shape can be written to SDRAM. This is address for the first mouse. All mouse data is continuous. This address is 8 bytes unit.

MOUSE BASE ADDRESS MIDDLE BYTE REGISTER – 0X47B

Bit	R/W	Default	Description
7:0	R/W	0x00	**MOUSE_BASE_ADDR[15:8]** There are 16 mouse shape can be written to SDRAM. This is address for the first mouse. All mouse data is continuous. This address is 8 bytes unit.

MOUSE BASE ADDRESS HIGH BYTE REGISTER – 0X47C

Bit	R/W	Default	Description
7:0	R/W	0x00	**MOUSE_BASE_ADDR[23:16]** There are 16 mouse shape can be written to SDRAM. This is address for the first mouse. All mouse data is continuous. This address is 8 bytes unit.

MOUSE INDEX REGISTER – 0X47D

Bit	R/W	Default	Description
7:5	R	0	Reserved
4	R/W	0	**MOUSE_BUF:** This bit select which buffer will be updated. 0: first mouse buffer 1: second mouse buffer
3:0	R/W	0	**MOUSE_INDEX[3:0]** This register set which mouse shape will be loaded from SDRAM. Up to 16 mouse shapes can be saved in SDRAM. If user wants more than 16 mouse shape, user can set different mouse base address.

WINDOW 32 VERTICAL POSITION REGISTER LOW BYTE – 0X47E

Bit	R/W	Default	Description
7:0	R/W	0	**VPOS_32[7:0]** Window 32 vertical position. This window will show memory content instead of video. It can be used for LOGO display. 1 line unit.

WINDOW 32 HORIZONTAL POSITION REGISTER LOW BYTE – 0X47F

Bit	R/W	Default	Description
7:0	R/W	0	**HPOS_32[7:0]** Window 32 horizontal position. This window will show memory content instead of video. It can be used for LOGO display. 4 pixels unit.

WINDOW 32 VERTICAL SIZE REGISTER LOW BYTE – 0X480

Bit	R/W	Default	Description
7:0	R/W	0	**VSIZE_32[7:0]** Window 32 vertical size. This window will show memory content instead of video. It can be used for LOGO display. 1 line unit.

WINDOW 32 HORIZONTAL SIZE REGISTER LOW BYTE – 0X481

Bit	R/W	Default	Description
7:0	R/W	0	**HSIZE_32[7:0]** Window 32 horizontal size. This window will show memory content instead of video. It can be used for LOGO display. 4 pixels unit.

WINDOW 32 VERTICAL AND HORIZONTAL POSITION REGISTER HIGH BYTE – 0X482

Bit	R/W	Default	Description
7:6	R	0	Reserved

Bit	R/W	Default	Description
5:4	R/W	0	**HPOS_32[9:8]** Window 32 horizontal position. This window will show memory content instead of video. It can be used for LOGO display. 4 pixels unit.
3:0	R/W	0	**VPOS_32[11:8]** Window 32 vertical position. This window will show memory content instead of video. It can be used for LOGO display. 1 line unit.

WINDOW 32 VERTICAL AND HORIZONTAL SIZE REGISTER HIGH BYTE – 0X483

Bit	R/W	Default	Description
7:5	R	0	**Reserved**
4	R/W	0	**HSIZE_32[8]** Window 32 horizontal size. This window will show memory content instead of video. It can be used for LOGO display. 4 pixels unit.
2:0	R/W	0	**VSIZE_32[10:8]** Window 32 vertical size. This window will show memory content instead of video. It can be used for LOGO display. 1 line unit.

WINDOW 32 ENABLE REGISTER – 0X484

Bit	R/W	Default	Description
7:3	R	0	**Reserved**
2	R/W	0	**CH32_FREEZE_EN** Window 32 freeze enable
1	R/W	0	**CH32_BND_EN** Window 32 boundary enable
0	R/W	0	**CH32_EN** Window 32 DRAM data display enable

DISPLAY MISC. CONTROL REGISTER – 0X485

Bit	R/W	Default	Description
7	R/W	1	**OUT_DIS:** Output disable. If set to high, VGA output will have all signals low.
6	R/W	0	**MDBOX_POS_SEL** Motion box position selection. If set to high, motion box position is automatically set to channel position
5	R/W	0	**Reserved**
4	R/W	0	**BND_EN:** Channel boundary enable. Only enabled channel has boundary.
3	R/W	0	**COLBAR_EN:** Color bar enable. Output is color bar instead of live video.
2	R/W	0	**SWITCH_EN** Switch to SDRAM contents if channel is disabled. If this bit is set to low, disabled channel will show background. If this bit is set to high, background is not shown. The contents in SDRAM will shows up. This is used for debug

Bit	R/W	Default	Description
1	R/W	0	**HS_POL:** Horizontal sync polarity 1: positive 0: negative
0	R/W	0	**VS_POL:** Vertical sync polarity 1: positive 0: negative

VERITAL SYNC DELAY AND BOUNDARY WIDTH REGISTER – 0X486

Bit	R/W	Default	Description
7:4	R/W	0x02	**BND_WIDTH:** Boundary width. Unit is pixel.
3:0	R/W	0x0F	**VSDEL:** Vertical sync delay cycle after horizontal sync

BOUNDRARY RED COLOR INTENSITY REGISTER – 0X487

Bit	R/W	Default	Description
7:0	R/W	0xFF	**BND_R[7:0]:** Boundary red color.

BOUNDRARY GREEN COLOR INTENSITY REGISTER – 0X488

Bit	R/W	Default	Description
7:0	R/W	0xFF	**BND_G[7:0]:** Boundary green color.

BOUNDRARY BLUE COLOR INTENSITY REGISTER – 0X489

Bit	R/W	Default	Description
7:0	R/W	0xFF	**BND_B[7:0]:** Boundary blue color.

MOTION BASE ADDRESS LOW BYTE REGISTER – 0X48A

Bit	R/W	Default	Description
7:0	R/W	0x00	**MOTION_BASE_ADDR[7:0]** This is starting address for SD motion. (line * pixel)

MOTION BASE ADDRESS MIDDLE BYTE REGISTER – 0X48B

Bit	R/W	Default	Description
7:0	R/W	0x00	**MOTION_BASE_ADDR[15:8]** This is starting address for SD motion. (line * pixel)

MOTION BASE ADDRESS HIGH BYTE REGISTER – 0X48C

Bit	R/W	Default	Description
7:0	R/W	0x00	MOTION_BASE_ADDR[23:16] This is starting address for SD motion. (line * pixel)

HD MOTION BASE ADDRESS LOW BYTE REGISTER – 0X48D

Bit	R/W	Default	Description
7:0	R/W	0x00	MOTION_HD_BASE_ADDR[7:0] This is starting address for HD motion. (line * pixel)

HD MOTION BASE ADDRESS MIDDLE BYTE REGISTER – 0X48E

Bit	R/W	Default	Description
7:0	R/W	0x00	MOTION_HD_BASE_ADDR[15:8] This is starting address for HD motion. (line * pixel)

HD MOTION BASE ADDRESS HIGH BYTE REGISTER – 0X48F

Bit	R/W	Default	Description
7:0	R/W	0x00	MOTION_HD_BASE_ADDR[23:16] This is starting address for HD motion. (line * pixel)

MOUSE UPDATE ENABLE REGISTER – 0X490

Bit	R/W	Default	Description
7:1	R	0	Reserved
0	R/W	0	MOUSE_UPDATE_EN Set this bit to high, hardware will automatically load mouse data from SDRAM to local SRAM. This bit will be clear when load is done.

HORIZONTAL UPSCALE FACTOR LOW BYTE REGISTER – 0X491

Bit	R/W	Default	Description
7:0	R/W	0x00	POS_HSCALE[7:0] Channel position information upscale factor. 0x1000 means no upscale. Value more than 0x1000 means upscale. If image is upscaled, this register must be set correctly.

HORIZONTAL UPSCALE FACTOR HIGH BYTE REGISTER – 0X492

Bit	R/W	Default	Description
7:0	R/W	0x10	**POS_HSCALE[15:8]** Channel position information upscale factor. 0x1000 means no upscale. Value more than 0x1000 means upscale. If image is upscaled, this register must be set correctly.

VERTICAL UPSCALE FACTOR LOW BYTE REGISTER – 0X493

Bit	R/W	Default	Description
7:0	R/W	0x00	**POS_VSCALE[7:0]** Channel position information upscale factor. 0x1000 means no upscale. Value more than 0x1000 means upscale. If image is upscaled, this register must be set correctly.

VERTICAL UPSCALE FACTOR HIGH BYTE REGISTER – 0X494

Bit	R/W	Default	Description
7:0	R/W	0x10	**POS_VSCALE[15:8]** Channel position information upscale factor. 0x1000 means no upscale. Value more than 0x1000 means upscale. If image is upscaled, this register must be set correctly.

POSITION UPSCALE ENABLE REGISTER – 0X495

Bit	R/W	Default	Description
7:1	R	0	**Reserved**
0	R/W	0	**POS_UPS_EN** Use upscaled position information if this bit set to high.

OSD BLINK RATE REGISTER – 0X496

Bit	R/W	Default	Description
7:2	R	0	**Reserved**
1:0	R/W	0x00	**OSD_BLINK_TIME:** OSD blinking frequency control 00: blinking on each 32 frames 01: blinking on each 16 frames 10: blinking on each 8 frames 11: blinking on each 4 frames

MOTION BOX CURSOR VERTICAL POSITION REGISTER – 0X497

Bit	R/W	Default	Description
7:4	R/W	0	CUR1_VPOS[3:0] Channel 1 Cursor Vertical Position
3:0	R/W	0	CUR0_VPOS[3:0] Channel 0 Cursor Vertical Position

Similar registers are assigned to control channel 2 to 16 using register 0x498 – 0x49E respectively.

MOTION BOX OUT BOUNDARY RED COLOR REGISTER – 0X49F

Bit	R/W	Default	Description
7:0	R/W	0	MDBOX_OBR[7:0] Red color for motion box out boundary

MOTION BOX OUT BOUNDARY GREEN COLOR REGISTER – 0X4A0

Bit	R/W	Default	Description
7:0	R/W	0	MDBOX_OBG[7:0] Green color for motion box out boundary

MOTION BOX OUT BOUNDARY BLUE COLOR REGISTER – 0X4A1

Bit	R/W	Default	Description
7:0	R/W	0	MDBOX_OBB[7:0] Blue color for motion box out boundary

MOTION BOX INNER BOUNDARY RED COLOR REGISTER – 0X4A2

Bit	R/W	Default	Description
7:0	R/W	0	MDBOX_IBR[7:0] Red color for motion box Inner boundary

MOTION BOX INNER BOUNDARY GREEN COLOR REGISTER – 0X4A3

Bit	R/W	Default	Description
7:0	R/W	0	MDBOX_IBG[7:0] Green color for motion box Inner boundary

MOTION BOX INNER BOUNDARY BLUE COLOR REGISTER – 0X4A4

Bit	R/W	Default	Description
7:0	R/W	0	MDBOX_IBB[7:0] Blue color for motion box Inner boundary

MOTION BOX MASK RED COLOR REGISTER – 0X4A5

Bit	R/W	Default	Description
7:0	R/W	0	MDBOX_MSKR[7:0] Red color for motion box mask area

MOTION BOX MASK GREEN COLOR REGISTER – 0X4A6

Bit	R/W	Default	Description
7:0	R/W	0	MDBOX_MSKG[7:0] Green color for motion box mask area

MOTION BOX MASK BLUE COLOR REGISTER – 0X4A7

Bit	R/W	Default	Description
7:0	R/W	0	MDBOX_MSKB[7:0] Blue color for motion box mask area

MOTION BOX PLANE RED COLOR REGISTER – 0X4A8

Bit	R/W	Default	Description
7:0	R/W	0	MDBOX_PR[7:0] Red color for motion box plane area

MOTION BOX PLANE GREEN COLOR REGISTER – 0X4A9

Bit	R/W	Default	Description
7:0	R/W	0	MDBOX_PG[7:0] Green color for motion box plane area

MOTION BOX PLANE BLUE COLOR REGISTER – 0X4AA

Bit	R/W	Default	Description
7:0	R/W	0	MDBOX_PB[7:0] Blue color for motion box plane area

HORIZONTAL START LOW BYTE REGISTER – 0X4AC

Bit	R/W	Default	Description
7:0	R/W	0	HSTART[7:0] Horizontal start in SDARM for read out. Unit is 4 pixels

HORIZONTAL START HIGH BYTE REGISTER – 0X4AD

Bit	R/W	Default	Description
7:2	RO	-	Reserved
1:0	R/W	0	HSTART[9:8] Horizontal start in SDARM for read out. Unit is 4 pixels

VERTICAL START LOW BYTE REGISTER – 0X4AE

Bit	R/W	Default	Description
7:0	R/W	0	VSTART[7:0] Vertical start in SDARM for read out. Unit is 1 line.

VERTICAL START HIGH BYTE REGISTER – 0X4AF

Bit	R/W	Default	Description
7:4	RO	-	Reserved
3:0	R/W	0	VSTART[11:8] Vertical start in SDARM for read out. Unit is 1 line.

VERTICAL TOTAL WINDOW REGISTER – 0X4B0

Bit	R/W	Default	Description
7:0	R/W	0xFF	VTT_WIN[7:0] Vertical Total can be changed according to input video frame rate. If difference is more than this number, VTT will not be adjusted. Unit is 1 line.

VERTICAL TOTAL ADJUST MODE REGISTER – 0X4B1

Bit	R/W	Default	Description
7:3	RO	-	Reserved
2	R/W	0x00	VTT_ADJUST It is used for manual mode. After set this bit, VTT will be changed according to current input video frame rate.
1	R/W	0	VTT_ADJUST_MODE 1: auto mode, adjust VTT each frame 0: manual mode, adjust VTT after set VTT_ADJUST
0	R/W	0	VTT_ADJUST_EN Enable VTT adjustment. If set to 0, use register setting. If set to 1, use input video frame rate.

VERTICAL TOTAL FROM INPUT VIDEO LOW BYTE REGISTER – 0X4B2

Bit	R/W	Default	Description
7:0	RO	-	NEW_VTT_RGBW[7:0] It is calculated from input video. The number is for two fields.

VERTICAL TOTAL FROM INPUT VIDEO HIGH BYTE REGISTER – 0X4B3

Bit	R/W	Default	Description
7:4	RO	-	Reserved
3:0	RO	-	NEW_VTT_RGBW[11:8] It is calculated from input video. The number is for two fields.

VERTICAL TOTAL AFTER ADJUSTMENT BYTE REGISTER – 0X4B4

Bit	R/W	Default	Description
7:0	RO	-	NEW_VTT[7:0] It is new VTT which is used in output timing. The number is for one field.

VERTICAL TOTAL AFTER ADJUSTMENT HIGH REGISTER – 0X4B5

Bit	R/W	Default	Description
7:3	RO	-	Reserved
2:0	RO	-	NEW_VTT[10:8] It is new VTT which is used in output timing. The number is for one field.

BOUNDARY ENABLE REGISTER – 0X4B6

Bit	R/W	Default	Description
7:4	R/W	0xF	**BND_EN_1[3:0]: Boundary Enable for Channel 1** [0]: left side boundary enable [1]: right side boundary enable [2]: top side boundary enable [3]: bottom side boundary enable
3:0	R/W	0xF	**BND_EN_0[3:0]: Boundary Enable for Channel 0** [0]: left side boundary enable [1]: right side boundary enable [2]: top side boundary enable [3]: bottom side boundary enable

Similar register 0x4B7 – 0X4C1 are assigned to control channel 12 – 19, 33 - 36 respectively.

BOUNDARY CHANNEL ENABLE REGISTER 5 – 0X4C2

Bit	R/W	Default	Description
7:0	RW	0	**BND_CH_EN[35:32]:** Control live channel 33 - 36 Boundary channel enable. This register is only used when BND_CH_EN_SEL is high. This is only used when user want to show boundary when channel is not enable.

FRAME RATE CONTROL ENABLE REGISTER 5 – 0X4C3

Bit	R/W	Default	Description
7:0	RW	0xFF	**FRSC_CH_EN[35:32]:** Control live channel 33 - 36 This register and the next three form a group. These 32 bits will determine which channels are included in the frame rate control decision. This is only for debugging purpose. In default, all channels will be included.

TEST PATTERN GENERATOR Y REGISTER – 0X4C4

Bit	R/W	Default	Description
7:0	RW	0x91	**CUSTOM_Y[7:0]:** 8bit Luminance value for live and PB test pattern generator

TEST PATTERN GENERATOR CB REGISTER – 0X4C5

Bit	R/W	Default	Description
7:0	RW	0x36	**CUSTOM_CB[7:0]:** 8bit CB value for live and PB test pattern generator

TEST PATTERN GENERATOR CR REGISTER – 0X4C6

Bit	R/W	Default	Description
7:0	RW	0x22	**CUSTOM_CR[7:0]:** 8bit CR value for live and PB test pattern generator

EXTERNAL OSD CONTROL REGISTER– 0X4C7

Bit	R/W	Default	Description
7:5	RO	-	Reserved
4	R/W	0	EOSD_SEL 0: select external OSD 1: select internal pure color
3	R/W	0	EOSD_EN 1 = External OSD enable
2	R/W	0	EOSD_MODE 0: ex_osd_en high active 1: ex_osd_en low active
1	R/W	0	EOSD_EN_DIS 0: use ex_osd_en 1: always enable, no transparent
0	R/W	0	EOSD_ALPHA_EN 1 = External OSD alpha blending enable

EXTERNAL OSD ALPHA REGISTER– 0X4C8

Bit	R/W	Default	Description
7:4	RO	-	Reserved
3:0	R/W	0	EOSD_ALPHA Alpha blending alpha number for external OSD layer. The output image will be: Video_data * alpha + eosd_data * (1 – alpha). Here alpha = OSD_ALPHA / 16. Maximum is 15.

EXTERNAL OSD COLOR R REGISTER– 0X4C9

Bit	R/W	Default	Description
7:0	R/W	0	EOSD_R Red Color for external OSD. It is used when EOSD_SEL is set to high.

EXTERNAL OSD COLOR G REGISTER– 0X4CA

Bit	R/W	Default	Description
7:0	R/W	0	**EOSD_G** Green Color for external OSD. It is used when EOSD_SEL is set to high.

EXTERNAL OSD COLOR B REGISTER– 0X4CB

Bit	R/W	Default	Description
7:0	R/W	0	**EOSD_B** Blue Color for external OSD. It is used when EOSD_SEL is set to high.

FRAME RATE CONTROL DEBUG REGISTER– 0X4CE

Bit	R/W	Default	Description
7	R/W	0	rd_buf_id_toggle 1: read buffer ID always toggle between odd and even 0: odd or even can be repeat
6	R/W	0	Rd_buf_inc 1: read buffer ID free running 0: increase read buffer ID according to write buffer ID
5	R/W	0	**WR_PAGE_EN** Manual set write page enable, 1 = enable
4	R/W	0	**RD_PAGE_EN** Manual set read page enable
3:2	R/W	0	**WR_PAGE** Used in manual mode
1:0	R/W	0	**RD_PAGE** Used in manual mode

MISC CONTROL REGISTER – 0X4CF

Bit	R/W	Default	Description
7:5	R/W	3	**WR_BUF_OFST** This register should be set to 3.
4	R/W	0	**INTERLACE_DBG** Interlaced mode debugging use.
3	R/W	0	**VTT_INV** It is used in interlaced mode, it should be set to 0
2	R/W	0	**EVEN_REPEAT** 0: repeat odd or even when needed 1: repeat even only

Bit	R/W	Default	Description
1	R/W	0	**DMON_VS_EN** 0: not use dual monitor vsync 1: use dual monitor vsync. This is used when main display data goes to dual monitor display.
0	R/W	0	**INTERLACE** 0: progressive mode 1: interlaced mode

BOUNDARY ENABLE REGISTER 2 – 0X4D0

Bit	R/W	Default	Description
7:4	R/W	0xF	**BND_EN_21[3:0]: Boundary Enable for Channel 21** [0]: left side boundary enable [1]: right side boundary enable [2]: top side boundary enable [3]: bottom side boundary enable
3:0	R/W	0xF	**BND_EN_20[3:0]: Boundary Enable for Channel 20** [0]: left side boundary enable [1]: right side boundary enable [2]: top side boundary enable [3]: bottom side boundary enable

Similar register 0x4D1– 0X4D5 are assigned to control channel 22 – 31 respectively.

IMAGE CONTROL REGISTER – 0X4DA

Bit	R/W	Default	Description
7	RO	-	**Reserved**
6	R/W	0	**OSD_CH_EN_SEL:** Simple OSD channel enable select 0: use rgb_interface channel enable 1: use another register set, [0x4F0] to [0x4F3]
5	R/W	0	**NOVID_SWITCH_EN** In normal case, this bit set to 0. No video color will show up. If this bit set to 1, SDRAM data will show up.
4	R/W	0	**BND_CH_EN_SEL:** Boundary channel enable select. 0: use rgb_interface channel enable 1: use another register set, [0x4F0] to [0x4F3]
3	R/W	1	**Reserved**
2	R/W	0	**GAIN_EN:** 1 = RGB digital gain enable
1	R/W	0	**READ_DLY : when enable after disable channel, see garbage** 0: Garbage remain 1: Garbage remove
0	R	0	**Reserved**

WEAVE OR 2D SELECTION REGISTER1 – 0X4DC

Bit	R/W	Default	Description

7:0	R/W	0x00	**WE_2D_SEL[7:0] :** select weave or 2D mode for channel 1 ~ channel 8 . 0: weave mode 1: 2D mode

WEAVE OR 2D SELECTION REGISTER1 – 0X4DD

Bit	R/W	Default	Description
7:0	R/W	0x00	**WE_2D_SEL[15:8] :** select weave or 2D mode for channel 9 ~ channel 16 . 0: weave mode 1: 2D mode

WEAVE OR 2D SELECTION REGISTER1 – 0X4DE

Bit	R/W	Default	Description
7:0	R/W	0x00	**WE_2D_SEL[23:16] :** select weave or 2D mode for channel 17 ~ channel 24 . 0: weave mode 1: 2D mode

WEAVE OR 2D SELECTION REGISTER1 – 0X4DF

Bit	R/W	Default	Description
7:0	R/W	0x00	**WE_2D_SEL[31:24] :** select weave or 2D mode for channel 25 ~ channel 32 . 0: weave mode 1: 2D mode

WEAVE OR 2D SELECTION REGISTER1 – 0X4E0

Bit	R/W	Default	Description
7:0	R/W	0x00	**WE_2D_SEL[36:32] :** select weave or 2D mode for channel 33 ~ channel 37. 0: weave mode 1: 2D mode

HORIZONTAL ACTIVE PIXEL FOR WEAVE LOW REGISTER – 0X4E1

Bit	R/W	Default	Description
7:0	R/W	0x8f	**HDE_W[7:0]:** It is active pixel number for weave mode.

HORIZONTAL ACTIVE PIXEL FOR WEAVE HIGH REGISTER – 0X4E2

Bit	R/W	Default	Description
7:3	R/W	-	Reserved
2:0	R/W	0x06	**HDE_W[10:8]:** It is active pixel number for weave mode.

VERTICAL ACTIVE LINE FOR WEAVE LOW REGISTER – 0X4E3

Bit	R/W	Default	Description
7:0	R/W	0x19	**VDE_W[7:0]:** It is active line number for weave mode.

VERTICAL ACTIVE LINE FOR WEAVE HIGH REGISTER – 0X4E4

Bit	R/W	Default	Description
7:3	R/W	-	Reserved
2:0	R/W	0x04	**VDE_W[10:8]:** It is active line number for weave mode.

SETTING NEW HDE/VDE VALUE – 0X4E5

Bit	R/W	Default	Description
7:1	R/W	-	Reserved
0	R/W	0x0	**MIX_MODE_SET:** It use 2d/weave mixed mode. "0" : Weave use HDE/VDE from 0x504~0x507 register value "1" : Weave use HDE/VDE from 0x4e1~0x4e4 register value

DIGITAL R GAIN REGISTER – 0X4E6

Bit	R/W	Default	Description
7:0	R/W	0x40	**R_GAIN:** R digital gain. 0x40 is no gain. More than 0x40 means gain more than 1.

DIGITAL G GAIN REGISTER – 0X4E7

Bit	R/W	Default	Description
7:0	R/W	0x40	**G_GAIN:** G digital gain. 0x40 is no gain. More than 0x40 means gain more than 1.

DIGITAL B GAIN REGISTER – 0X4E8

Bit	R/W	Default	Description
7:0	R/W	0x40	**B_GAIN:** B digital gain. 0x40 is no gain. More than 0x40 means gain more than 1.

R OFFSET REGISTER – 0X4E9

Bit	R/W	Default	Description
7:0	R/W	0x00	**R_OFST[7:0]** R offset. Rout = Rin * R_GAIN + R_OFST. This value is 2's complement value. R_OFST can be negative data.

G OFFSET REGISTER – 0X4EA

Bit	R/W	Default	Description
7:0	R/W	0x00	**G_OFST[7:0]** G offset. Rout = Rin * R_GAIN + R_OFST. This value is 2's complement value. R_OFST can be negative data.

B OFFSET REGISTER – 0X4EB

Bit	R/W	Default	Description
7:0	R/W	0x00	**B_OFST[7:0]** B offset. Rout = Rin * R_GAIN + R_OFST. This value is 2's complement value. R_OFST can be negative data.

BOUNDARY CHANNEL ENABLE REGISTER 1 – 0X4EC

Bit	R/W	Default	Description
7:0	RW	0	**BND_CH_EN[7:0]:** Control channel 7 - 0 Boundary channel enable. This register is only used when BND_CH_EN_SEL is high. This is only used when user want to show boundary when channel is not enable.

BOUNDARY CHANNEL ENABLE REGISTER 2 – 0X4ED

Bit	R/W	Default	Description
7:0	RW	0	**BND_CH_EN[15:8]:** Control live channel 15 - 8 Boundary channel enable. This register is only used when BND_CH_EN_SEL is high. This is only used when user want to show boundary when channel is not enable.

BOUNDARY CHANNEL ENABLE REGISTER 3 – 0X4EE

Bit	R/W	Default	Description
7:0	RW	0	**BND_CH_EN[23:16]:** Control live channel 23 - 16 Boundary channel enable. This register is only used when BND_CH_EN_SEL is high. This is only used when user want to show boundary when channel is not enable.

BOUNDARY CHANNEL ENABLE REGISTER 4 – 0X4EF

Bit	R/W	Default	Description
7:0	RW	0	**BND_CH_EN[31:24]:** Control live channel 31 - 24 Boundary channel enable. This register is only used when BND_CH_EN_SEL is high. This is only used when user want to show boundary when channel is not enable.

FRAME RATE CONTROL ENABLE REGISTER 1 – 0X4F0

Bit	R/W	Default	Description
7:0	RW	0xFF	**FRSC_CH_EN[7:0]:** Control live channel 7 - 0 This register and the next three forms a group. These 32 bits will determine which channel are included in the frame rate control decision. This is only for debugging purpose. In default, all channels will be included.

FRAME RATE CONTROL ENABLE REGISTER 2 – 0X4F1

Bit	R/W	Default	Description
7:0	RW	0xFF	**FRSC_CH_EN[15:8]:** Control live channel 15 - 8

FRAME RATE CONTROL ENABLE REGISTER 3 – 0X4F2

Bit	R/W	Default	Description
7:0	RW	0xFF	**FRSC_CH_EN[23:16]:** Control PB channel 7 - 0

FRAME RATE CONTROL ENABLE REGISTER 4 – 0X4F3

Bit	R/W	Default	Description
7:0	RW	0xFF	**FRSC_CH_EN[31:24]:** Control PB channel 15 - 8

RED COLOR FOR NO VIDEO CHANNEL – 0X4F4

Bit	R/W	Default	Description
7:0	RW	0	**NOVID_R:** This color will show up when the channel boundary is enable, but channel has no video.

GREEN COLOR FOR NO VIDEO CHANNEL – 0X4F5

Bit	R/W	Default	Description
7:0	RW	0	**NOVID_G:** This color will show up when the channel boundary is enable, but channel has no video.

BLUE COLOR FOR NO VIDEO CHANNEL – 0X4F6

Bit	R/W	Default	Description
7:0	RW	0xFF	**NOVID_B:** This color will show up when the channel boundary is enable, but channel has no video.

2D DE-INTERLACE CONTROL REGISTER – 0X4F7

Bit	R/W	Default	Description

7:0	R/W	0x00	rg_2ddi_ctl

2D DE-INTERLACE THRESHOLD 1 REGISTER – 0X4F8

Bit	R/W	Default	Description
7:0	R/W	0x28	rg_2ddi_thd1

2D DE-INTERLACE THRESHOLD 2 REGISTER – 0X4F9

Bit	R/W	Default	Description
7:0	R/W	0x1E	rg_2ddi_thd2

2D DE-INTERLACE THRESHOLD 3 REGISTER – 0X4FA

Bit	R/W	Default	Description
7:0	R/W	0x28	rg_2ddi_thd3

2D DE-INTERLACE THRESHOLD 4 REGISTER – 0X4FB

Bit	R/W	Default	Description
7:0	R/W	0x28	rg_2ddi_thd4

2D DE-INTERLACE THRESHOLD 5 REGISTER – 0X4FC

Bit	R/W	Default	Description
7:0	R/W	0x24	rg_2ddi_thd5

2D DE-INTERLACE THRESHOLD 6 REGISTER – 0X4FD

Bit	R/W	Default	Description
7:0	R/W	0x6F	rg_2ddi_thd6

DE-INTERLACE MODE SELECTION REGISTER 1 – 0X4FE

Bit	R/W	Default	Description
7	R/W	-	Reserve
6	R/W	0	rg_afm_ctl
5	R/W	1	ups_interlace_off 1 = turn off ups interlace 0 = turn on ups interlace
4	R/W	0	Weave_interlace_off: if users use weave 2x zoom, this register set "1" 1 = turn off weave mode interlace 0 = turn on weave mode interlace
3	R/W	0	WEAVE_UP_EN: Weave mode up-scaler on/off control 1 = turn on up-scaler 0 = turn off up-scaler
2	R/W	0	rg_di_use_bob 1: Use BOB for 2D de-interlace. 0: Use low angle 2D de-interlace.
1	R/W	0	Weave_2d_mix_en 1 = turn on weave and 2D mixed mode 0 = turn off weave and 2D mixed mode
0	R/W	0	rg_force_2ddi 1 = turn on 2D de-interlace 0 = turn off 2D de-interlace

HD REGISTER PAGE SELECT FOR MOTION DETECTER– 0X4FF

Bit	R/W	Default	Description
7	R/W	0	GND_L, 1 = ignore live channel field signal in frame rate controller, used in low speed PB
6	R/W	0	GND_P, 1 = ignore PB channel field signal in frame rate controller, used in low speed PB
5	R/W	0	GND_C, 1 = ignore cascade channel field signal in frame rate controller, used in low speed PB
4:3	R	-	Reserved
2	R/W	0	NEW_V, used in interlaced mode 0 = vertical back porch aligned 1 = vertical front porch aligned
1:0	R/W	0	HD_CH_SEL[1:0] 0 = HD channel 1 register page setting for motion detector 1 = HD channel 2 register page setting for motion detector 2 = HD channel 3 register page setting for motion detector 3 = HD channel 4 register page setting for motion detector

HORIZONTAL TOTAL REGISTER 1 – 0X500

Bit	R/W	Default	Description
7:0	R/W	0x2F	**HTT[7:0]:** Pixel count of one horizontal line including blanking. This value should minus 1 by real horizontal total. In interlace mode, if down scaler and TV encoder is used, the vclk is set to 108MHz, so HTT will be set to 4*1716-1=6863

HORIZONTAL TOTAL REGISTER 2 – 0X501

Bit	R/W	Default	Description
7:4	R	-	**Reserved**
3:0	R/W	0x07	**HTT[12:8]:** Pixel count of one horizontal line including blanking. This value should minus 1 by real horizontal total. In interlace mode, if down scaler and TV encoder is used, the vclk is set to 108MHz, so HTT will be set to 4*1716-1=6863

VERTICAL TOTAL REGISTER 1 – 0X502

Bit	R/W	Default	Description
7:0	R/W	0x37	**VTT[7:0]:** Line count of one display frame including blanking. This value should minus 1 by real vertical total. In interlace mode, this value is set to lines of odd filed. Even field is this value plus 1.

VERTICAL TOTAL REGISTER 2 – 0X503

Bit	R/W	Default	Description
7:3	R	-	**Reserved**
2:0	R/W	0x04	**VTT[10:8]:** Line count of one display frame including blanking. This value should minus 1 by real vertical total. In interlace mode, this value is set to lines of odd filed. Even field is this value plus 1.

HORIZONTAL DISPLAY END REGISTER 1 – 0X504

Bit	R/W	Default	Description
7:0	R/W	0x8F	**HDE[7:0]** Active display pixel count of one horizontal line. This value should minus 1 by real value.

HORIZONTAL DISPLAY END REGISTER 2 – 0X505

Bit	R/W	Default	Description
7	R/W	0	PHSYNC[9]
6:3	R	-	Reserved
2:0	R/W	0x06	HDE[10:8] Active display pixel count of one horizontal line. This value should minus 1 by real value.

VERTICAL DISPLAY END REGISTER 1 – 0X506

Bit	R/W	Default	Description
7:0	R/W	0x19	VDE[7:0] Line count of active display frame. This value should minus 1 by real value. This value is set to active lines in one field.

VERTICAL DISPLAY END REGISTER 2 – 0X507

Bit	R/W	Default	Description
7:3	R	-	Reserved
2:0	R/W	0x04	VDE[10:8] Line count of active display frame. This value should minus 1 by real value. This value is set to active lines in one field.

HORIZONTAL SYNC STARTING POSITION REGISTER – 0X508

Bit	R/W	Default	Description
7:0	R/W	0x30	PHSYNC[8:1] Horizontal sync pulse starting position after HDE (in two pixels increment)

VERTICAL SYNC STARTING POSITION REGISTER – 0X509

Bit	R/W	Default	Description
7:0	R/W	0x02	PVSYNC[7:0] Vertical sync pulse starting position after VDE

HORIZONTAL SYNC WIDTH REGISTER – 0X50A

Bit	R/W	Default	Description
7:0	R/W	0x20	HSPW[7:0] Horizontal sync pulse width

VERTICAL SYNC WIDTH REGISTER – 0X50B

Bit	R/W	Default	Description
7:0	R/W	0x06	VSPW[7:0] Vertical sync pulse width

SBOX0 CONTROL REGISTER – 0X50C

Bit	R/W	Default	Description
7:5	R/W	0x0	Reserved
4	R/W	0x0	Boundary Line enable 0 = disable 1 = enable
3	R/W	0x0	Box plane enable 0 = disable 1 = enable
2	R/W	0x0	Blinking enable 0 = disable 1 = enable
1:0	R/W	0x0	Mixing control 00 = 75% original pixel value / 25% plane (boundary) color mix 01 = 50% original pixel value / 50% plane (boundary) color mix 10 = 25% original pixel value / 75% plane (boundary) color mix 11 = plane (boundary) color

SBOX LINE WIDTH CONTROL REGISTER 1 – 0X511

Bit	R/W	Default	Description
7:6	R/W	0x0	Box3 Vertical line width control 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line
5:4	R/W	0x0	Box3 Horizontal line width control 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line
3:2	R/W	0x0	Box2 Vertical line width control 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line
1:0	R/W	0x0	Box2 Horizontal line width control 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line

SBOX LINE WIDTH CONTROL REGISTER 2 – 0X512

Bit	R/W	Default	Description
7:6	R/W	0x0	Box1 Vertical line width control 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line
5:4	R/W	0x0	Box1 Horizontal line width control 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line
3:2	R/W	0x0	Box0 Horizontal line width control 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line
1:0	R/W	0x0	Box0 Horizontal line width control 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line

SBOX0 HL CONTROL REGISTER 1 – 0X513

Bit	R/W	Default	Description
7:0	R/W	0x0	Box0 Left Horizontal point SBOX0_HL[7:0], unit is pixel

SBOX0 HL CONTROL REGISTER 2 – 0X514

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	Box0 Left Horizontal point SBOX0_HL[10:8], unit is pixel

SBOX0 HR CONTROL REGISTER 1 – 0X51B

Bit	R/W	Default	Description
7:0	R/W	0x0	Box0 Right Horizontal point SBOX0_HR[7:0], unit is pixel

SBOX0 HR CONTROL REGISTER 2 – 0X51C

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	Box0 Right Horizontal point SBOX0_HR[10:8], unit is pixel

SBOX0 VT CONTROL REGISTER 1 – 0X523

Bit	R/W	Default	Description
7:0	R/W	0x0	Box0 Top Vertical point SBOX0_VT[7:0], unit is line

SBOX0 VT CONTROL REGISTER 2 – 0X524

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	Box0 Top Vertical point SBOX0_VT[10:8], unit is line

SBOX0 VB CONTROL REGISTER 1 – 0X52B

Bit	R/W	Default	Description
7:0	R/W	0x0	Box0 Bottom Vertical point SBOX0_VB[7:0], unit is line

SBOX0 VB CONTROL REGISTER 2 – 0X52C

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	Box0 Bottom Vertical point SBOX0_VB[10:8], unit is line

BOX BOUNDARY COLOR R BYTE – 0X533

Bit	R/W	Default	Description
7:0	R/W	0x0	Color red byte[7:0]

BOX BOUNDARY COLOR G BYTE – 0X534

Bit	R/W	Default	Description
7:0	R/W	0x0	Color green byte[7:0]

BOX BOUNDARY COLOR B BYTE – 0X535

Bit	R/W	Default	Description
7:0	R/W	0x0	Color blue byte[7:0]

BOX PLANE COLOR R BYTE – 0X536

Bit	R/W	Default	Description
7:0	R/W	0x0	Color red byte[7:0]

BOX PLANE COLOR G BYTE – 0X537

Bit	R/W	Default	Description
7:0	R/W	0x0	Color green byte[7:0]

BOX PLANE COLOR B BYTE – 0X538

Bit	R/W	Default	Description
7:0	R/W	0x0	Color blue byte[7:0]

SCREEN BACKGROUND COLOR R BYTE – 0X539

Bit	R/W	Default	Description
7:0	R/W	0x0	Color red byte[7:0]

SCREEN BACKGROUND COLOR G BYTE – 0X53A

Bit	R/W	Default	Description
7:0	R/W	0x0	Color green byte[7:0]

SCREEN BACKGROUND COLOR B BYTE – 0X53B

Bit	R/W	Default	Description
7:0	R/W	0x0	Color blue byte[7:0]

MOUSE0 HORIZONTAL POSITION REGISTER 1 – 0X53C

Bit	R/W	Default	Description
7:0	R/W	0x0	Mouse0 Horizontal position MOUSE0_HPOS[7:0]

MOUSE0 HORIZONTAL POSITION REGISTER 2 – 0X53D

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	Mouse0 Horizontal position MOUSE0_HPOS[10:8]

MOUSE0 VERTICAL POSITION REGISTER 1 – 0X53E

Bit	R/W	Default	Description
7:0	R/W	0x0	Mouse0 Vertical position MOUSE0_VPOS[7:0]

MOUSE0 VERTICAL POSITION REGISTER 2 – 0X53F

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	Mouse0 Vertical position MOUSE0_VPOS[10:8]

MOUSE1 HORIZONTAL POSITION REGISTER 1 – 0X540

Bit	R/W	Default	Description
7:0	R/W	0x0	Mouse0 Horizontal position MOUSE1_HPOS[7:0]

MOUSE1 HORIZONTAL POSITION REGISTER 2 – 0X541

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	Mouse0 Horizontal position MOUSE1_HPOS[10:8]

MOUSE1 VERTICAL POSITION REGISTER 1 – 0X542

Bit	R/W	Default	Description
7:0	R/W	0x0	Mouse0 Vertical position MOUSE1_VPOS[7:0]

MOUSE1 VERTICAL POSITION REGISTER 2 – 0X543

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	Mouse0 Vertical position MOUSE1_VPOS[10:8]

MOUSE CONTROL REGISTER – 0X544

Bit	R/W	Default	Description
7	R	0x0	Reserved
6	R/W	0x0	Mouse1 Enable 0 = disable 1= enable
5:4	R/W	0x0	Mouse1 Mixing control 00 = 75% original pixel value / 25% mouse color mix 01 = 50% original pixel value / 50% mouse color mix 10 = 25% original pixel value / 75% mouse color mix 11 = mouse color
3	R	0x0	Reserved
2	R/W	0x0	Mouse0 Enable 0 = disable 1= enable
1:0	R/W	0x0	Mouse0 Mixing control 00 = 75% original pixel value / 25% mouse color mix 01 = 50% original pixel value / 50% mouse color mix 10 = 25% original pixel value / 75% mouse color mix 11 = mouse color

MOUSE BACKGROUND COLOR R BYTE – 0X545

Bit	R/W	Default	Description
7:0	R/W	0x0	Color red byte[7:0]

MOUSE BACKGROUND COLOR G BYTE – 0X546

Bit	R/W	Default	Description
7:0	R/W	0x0	Color green byte[7:0]

MOUSE BACKGROUND COLOR B BYTE – 0X547

Bit	R/W	Default	Description
7:0	R/W	0x0	Color blue byte[7:0]

MOUSE FOREGROUND COLOR R BYTE – 0X548

Bit	R/W	Default	Description
7:0	R/W	0x0	Color red byte[7:0]

MOUSE FOREGROUND COLOR G BYTE – 0X549

Bit	R/W	Default	Description
7:0	R/W	0x0	Color green byte[7:0]

MOUSE FOREGROUND COLOR B BYTE – 0X54A

Bit	R/W	Default	Description
7:0	R/W	0x0	Color blue byte[7:0]

DISPLAY MODE CONTROL REGISTER – 0X54B

Bit	R/W	Default	Description
7	R/W	0x0	DM_MD_SET: Dual monitor motion box enable (motion box, cursor) 1 : dual monitor motion box register set 0 : Main motion box register set
6:3	R	0x0	Reserved
2	R/W	0x0	LCD_YC_SWAP Control luma and chroma position for BT1120 output
1	R/W	0x0	DIS_VIDEO 1: disable video 0: enable video
0	R/W	0x0	DE_INTLACE 0: weave 1: 2D

MOUSE RAM ADDRESS REGISTER – 0X54C

Bit	R/W	Default	Description
7:0	R/W	0x0	MOUSE_WR_LOC[7:0]

MOUSE RAM DATA REGISTER – 0X54D

Bit	R/W	Default	Description
7:0	R/W	0x0	MOUSE_WR_DATA

MOUSE REGISTER UPDATE ENABLE REGISTER – 0X54E

Bit	R/W	Default	Description
7:4	R/W	0x3	Repeat frame expected value
3	R/W	0x0	Enable
2	R/W	0x1	Disable
1	R/W	0x0	Masking Bit
0	R/W	0x1	MOUSE_REG_UPDATE 0: not update mouse related registers. 1: update mouse related registers Before set mouse position registers, set this bit to 0. After set done, set this bit to 1.

MOUSE RAM WRITE ENABLE REGISTER – 0X54F

Bit	R/W	Default	Description
0	R/W	0x0	MOUSE_WR_EN

MD BOX CONTROL REGISTER 0 – 0X550

Bit	R/W	Default	Description
7	R/W	0x0	MD Box Enable
6	R/W	0x0	MD Box operation mode select 0 = table mode 1 = motion display mode
5	R/W	0x0	Cursor Cell Enable 0 = disable 1 = enable
4	R/W	0x0	Out Boundary Cell Enable 0 = disable 1 = enable
3	R/W	0x0	Masking Plane Enable 0 = disable 1 = enable
2	R/W	0x0	Detection Plane Enable 0 = disable 1 = enable
1:0	R/W	0x0	Mixing control 00 = 75% original pixel value / 25% plane (boundary) color mix 01 = 50% original pixel value / 50% plane (boundary) color mix 10 = 25% original pixel value / 75% plane (boundary) color mix 11 = plane (boundary) color

This register is for channel 1. Similar register 0x551 – 0x55F is for channel 2 – channel 16.

MD BOX LINE WIDTH CONTROL REGISTER 0 – 0X560

Bit	R/W	Default	Description
7:6	R/W	0x0	Box1 Vertical line width control 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line
5:4	R/W	0x0	Box1 Horizontal line width control 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line

Bit	R/W	Default	Description
3:2	R/W	0x0	Box0 Vertical line width control 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line
1:0	R/W	0x0	Box0 Horizontal line width control 00 = 1 line 01 = 2 line 10 = 3 line 11 = 4 line

This register is for box0, 1. Similar register 0x561 – 0x567 is for box 2 – box 16.

MD BOX 0 HORIZONTAL LEFT POSITION REGISTER 1 – 0X568

Bit	R/W	Default	Description
7:0	R/W	0x0	Box 0 Horizontal Left Position MDBOX0_HL[7:0]

MD BOX 0 HORIZONTAL LEFT POSITION REGISTER 2 – 0X569

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	Box 0 Horizontal Left Position MDBOX0_HL[10:8]

This register is for box0. Similar register 0x56A – 0x587 is for box 1 – box 16.

MD BOX 0 VERTICAL TOP POSITION REGISTER 1 – 0X588

Bit	R/W	Default	Description
7:0	R/W	0x0	Box 0 Vertical Top Position MDBOX0_VT[7:0]

MD BOX 0 VERTICAL TOP POSITION REGISTER 2 – 0X589

Bit	R/W	Default	Description
7:3	R	0x0	Reserved
2:0	R/W	0x0	Box 0 Vertical Top Position MDBOX0_VT[10:8]

This register is for box0. Similar register 0x58A – 0x5A7 is for box 1 – box 16.

MD BOX 0 HORIZONTAL SIZE REGISTER 1 – 0X5A8

Bit	R/W	Default	Description
7:0	R/W	0x0	**Box 0 Horizontal Size Position** MDBOX0_HS[7:0]

MD BOX 0 HORIZONTAL SIZE REGISTER 2 – 0X5A9

Bit	R/W	Default	Description
7:3	R	0x0	**Reserved**
2:0	R/W	0x0	**Box 0 Horizontal Size Position** MDBOX0_HS[10:8]

This register is for box0. Similar register 0x5AA – 0x5C7 is for box 2 – box 16.

MD BOX 0 VERTICAL SIZE REGISTER 1 – 0X5C8

Bit	R/W	Default	Description
7:0	R/W	0x0	**Box 0 Vertical Size Position** MDBOX0_VS[7:0]

MD BOX 0 VERTICAL SIZE REGISTER 2 – 0X5C9

Bit	R/W	Default	Description
7:3	R	0x0	**Reserved**
2:0	R/W	0x0	**Box 0 Vertical Size Position** MDBOX0_VS[10:8]

This register is for box0. Similar register 0x5CA – 0x5E7 is for box 2 – box 16.

MD BOX HCELL REGISTER 0 – 0X5E8

Bit	R/W	Default	Description
7:4	R/W	0x0	**Box 1 Horizontal Cell Number** MDBOX1_HNUM[3:0]
3:0	R/W	0x0	**Box 0 Horizontal Cell Number** MDBOX0_HNUM[3:0]

This register is for box0. Similar register 0x5E9 – 0x5EF is for box 2 – box 16.

MD BOX VCELL REGISTER 0 – 0X5F0

Bit	R/W	Default	Description
7:4	R/W	0x0	**Box 1 Vertical Cell Number** MDBOX1_VNUM[3:0]
3:0	R/W	0x0	**Box 0 Vertical Cell Number** MDBOX0_VNUM[3:0]

This register is for box0, 1. Similar register 0x5F1 – 0x5F7 is for box 2 – box 16.

MD BOX CURSOR HORIZONTAL POSITION REGISTER 0 – 0X5F8

Bit	R/W	Default	Description
7:4	R/W	0x0	**Box 1 Horizontal Cursor Position** CUR1_HPOS[3:0]
3:0	R/W	0x0	**Box 0 Horizontal Cursor Position** CUR0_HPOS[3:0]

This register is for box0, 1. Similar register 0x5F8 – 0x5FF is for box 2 – box 16.

Registers Table

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x080	R/W	0	[4]: OSD_TITLE_EN [3]: OSD_TIME_EN [2]: OSD_CHPIC_EN [1]: OSD_CHNUM_EN [0]: OSD_EN
0x081	R/W	0	[7:6]: ASIAN FONT [5]: OSD_CHPIC_BLINK [4]: OSD_CHPIC_TRANS [3]: OSD_TITLE_MIX [2]: OSD_TIME_MIX [1]: OSD_CHPIC_MIX [0]: OSD_CHNUM_MIX
0x082	R/W	0x4F	[7:6]: OSD_CHPIC_POS [5:4]: OSD_CHNUM_POS [3:2]: OSD_FONT_VSIZE [1:0]: OSD_FONT_HSIZE
0x083	R/W	0	OSD_CHNUM_HPOS[7:0]
0x084	R/W	0	OSD_CHNUM_HPOS[10:8]
0x085	R/W	0	OSD_CHNUM_VPOS[7:0]
0x086	R/W	0	OSD_CHNUM_VPOS[10:8]
0x087	R/W	0	OSD_CHPIC_HPOS[7:0]
0x088	R/W	0	OSD_CHPIC_HPOS[10:8]
0x089	R/W	0	OSD_CHPIC_VPOS[7:0]
0x08A	R/W	0	OSD_CHPIC_VPOS[10:8]
0x08B	R/W	0	OSD_TIME_HPOS[7:0]
0x08C	R/W	0	OSD_TIME_HPOS[10:8]
0x08D	R/W	0	OSD_TIME_VPOS[7:0]
0x08E	R/W	0	OSD_TIME_VPOS[10:8]
0x08F	R/W	0	OSD_TITLE_HPOS[7:0]

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x090	R/W	0	OSD_TITLE_HPOS[10:8]
0x091	R/W	0	OSD_TITLE_VPOS[7:0]
0x092	R/W	0	OSD_TITLE_VPOS[10:8]
0x093	R/W	0	OSD_FONT_R1[7:0]
0x094	R/W	0	OSD_FONT_G1[7:0]
0x095	R/W	0	OSD_FONT_B1[7:0]
0x096	R/W	0	OSD_FONT_R2[7:0]
0x097	R/W	0	OSD_FONT_G2[7:0]
0x098	R/W	0	OSD_FONT_B2[7:0]
0x099	R/W	0	OSD_FONT_R3[7:0]
0x09A	R/W	0	OSD_FONT_G3[7:0]
0x09B	R/W	0	OSD_FONT_B3[7:0]
0x09C	R/W	0	OSD_PIC_R0[7:0]
0x09D	R/W	0	OSD_PIC_G0[7:0]
0x09E	R/W	0	OSD_PIC_B0[7:0]
0x09F	R/W	0	OSD_PIC_R1[7:0]
0x0A0	R/W	0	OSD_PIC_G1[7:0]
0x0A1	R/W	0	OSD_PIC_B1[7:0]
0x0A2	R/W	0	OSD_PIC_R2[7:0]
0x0A3	R/W	0	OSD_PIC_G2[7:0]
0x0A4	R/W	0	OSD_PIC_B2[7:0]
0x0A5	R/W	0	OSD_PIC_R3[7:0]
0x0A6	R/W	0	OSD_PIC_G3[7:0]
0x0A7	R/W	0	OSD_PIC_B3[7:0]
0x0A8	W	0	OSD_FRAM_ADDR[7:0]
0x0A9	W	0	OSD_FRAM_ADDR[10:8]
0x0AA	W	0	OSD_FRAM_DATA[7:0]
0x0AB	W	0	OSD_FRAM_DATA[15:8]
0x0AC	W	0	OSD_FRAM_DATA[23:16]
0x0AD	W	0	OSD_FRAM_DATA[31:24]
0x0AE	W	0	OSD_FRAM_DATA[39:32]
0x0AF	W	0	OSD_FRAM_DATA[43:40]
0x0B0	W	0	OSD_DRAM_ADDR[7:0]
0x0B1	W	0	OSD_DRAM_ADDR[8]
0x0B2	W	0	OSD_DRAM_DATA[5:0]

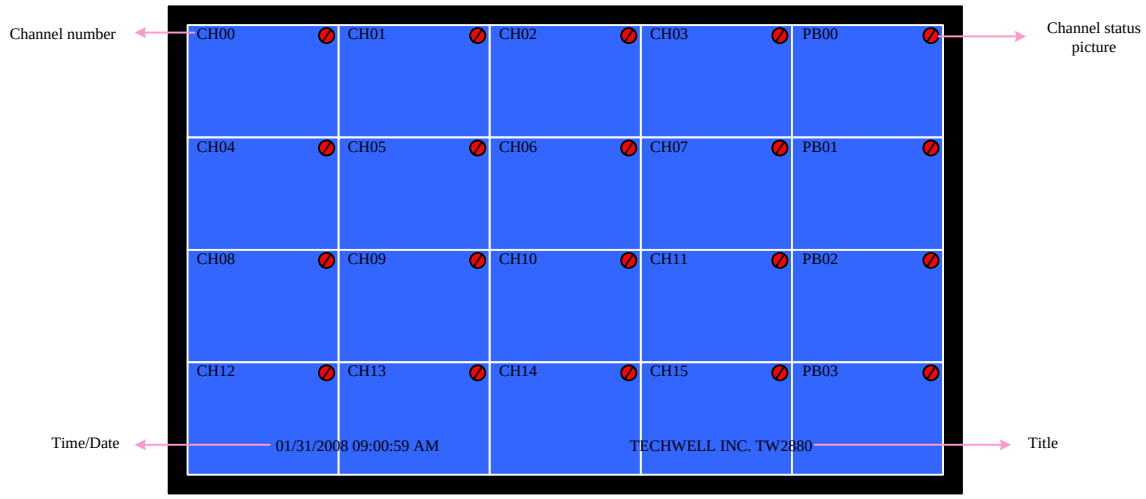
OSD for Display Path

Introduction

TW2828 OSD controller for display path is a complementary to OSG. Since OSG need a lot of SDRAM bandwidth, this simple OSD controller does not need SDRAM bandwidth. All font tables are stored in local SRAM. It can display channel information for each channel. Channel information includes 8 characters and 1 picture. All information can be selected from 64 fonts and 4 pictures saved in SRAM. Font width can be selected from 6, 8, 12, 16 or 22. Font height can be selected from 8, 10, 16, 20 or 22. Picture size is fixed to 32x32. OSD can also display time and data with 32 characters, and title with 32 characters.

Features

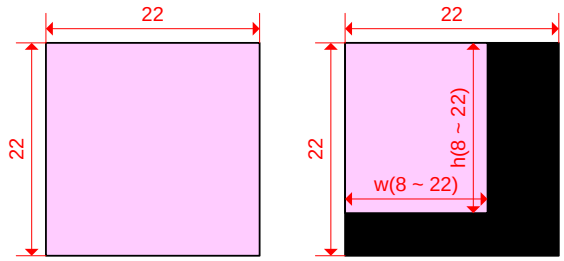
- Supports 16 live channels and 20 playback channels
- 64 fonts table
- 4 pictures table
- 8 characters Channel information with one picture
- 32 characters title
- 32 characters time/date
- 2 bit color for font and picture



Font and Picture Library

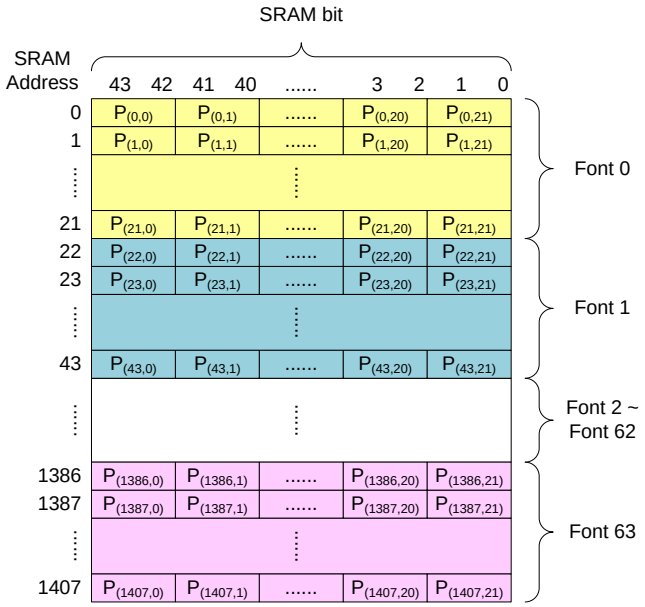
FONT

There are totally 64 fonts which can be saved in SRAM. The font size saved in SRAM is fixed to 22x22. But displayed font size can be changed. Horizontal can display four sizes: 6, 8, 12, 16 or 22. Size 12 or 16 are doubled from size 6 or 8. If 6 or 12 are selected, fonts saved in SRAM must have small size. But additional two pixels must be saved in SRAM. Vertical can display four sizes: 8, 10, 16, 20 or 22. Size 16 or 20 are doubled from size 8 or 10. If 8 or 16 are selected, fonts saved in SRAM must have small size. But additional two lines must be saved in SRAM. The following picture shows SRAM data. For 22x22 font, all SRAM data are valid. For 6x8 font, only 6x8 area are valid. Black area is for dummy data.



There are 2 bits for each pixel color. 00 means transparent, color 01, 10 and 11 can be set by registers: OSD_FONT_R1 (G1, B1), OSD_FONT_R2 (G2, B2) and OSD_FONT_R3 (G3, B3).

Data saved in SRAM is shown below. There are totally 64x22x22*2=1408x44 bits in SRAM. Data are saved font by font. For each font, data is saved line by line. Pixel data in each line is in big endian.



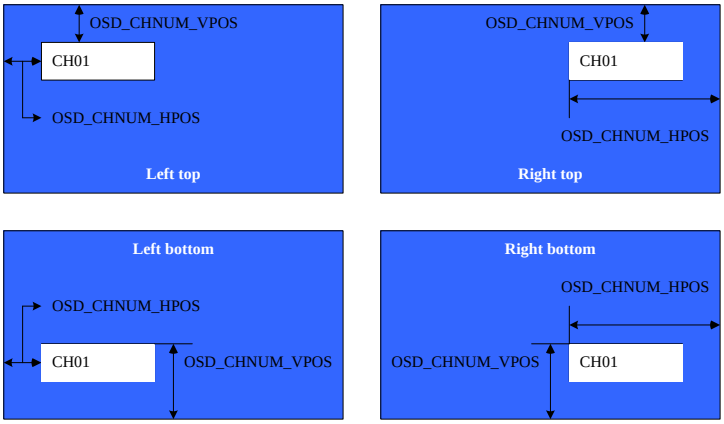
PICTURE

The picture is used for channel status. Each channel has picture display. The picture size in SRAM is fixed to 32x32. The display picture size is also fixed to 32x32. Same as font, it uses 2 bits for picture color. So there are four colors which can be set by registers: OSD_PIC_R0 (G0, B0), OSD_PIC_R1 (G1, B1), OSD_PIC_R2 (G2, B2) and OSD_PIC_R3 (G3, B3). There are four pictures saved in SRAM. Data in SRAM are same as fonts. Data are saved picture by picture. And in one picture, data are line by line. In one byte data, pixel data is stored in big endian. There are totally 32x32x4x2 = 512x16 bits in SRAM.

Display Information

CHANNEL NUMBER

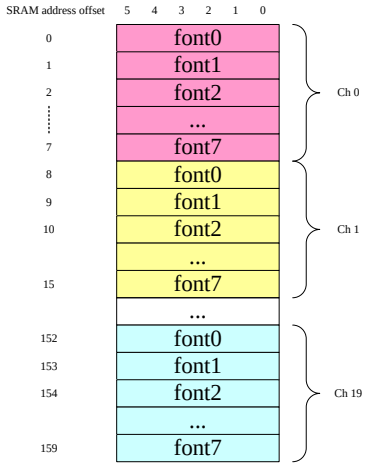
For each channel, there is a 8-font channel number information. Each font is selected from 64-font table. So index for each font is 6 bit. Channel number can be enabled by setting register OSD_CHNUM_EN and OSD_EN to high. Channel number can be mixed with video data by setting register OSD_CHNUM_MIX to high. Mix percentage is 50% video plus 50% channel number. The positions for each channel are same. They can be in four positions: left top, right top, left bottom and right bottom. It is set by register OSD_CHNUM_POS. For each position, horizontal offset and vertical offset can be set by OSD_CHNUM_HPOS and OSD_CHNUM_VPOS. For each position, the meaning for HPOS and VPOS is different because each channel size may be different.



If channel number information has less than 8 fonts, you can set the remaining font to space. So you need to put space font in the 64-font table.

The font size can be changed according to register OSD_FONT_HSIZE and OSD_FONT_VSIZE. But remember the fonts saved in memory are always 8x10. If double size is selected, just repeat every pixel twice.

Channel information for display is saved in display SRAM. It contains 32x8x6=256x6. The sequence is channel by channel. In each channel, the sequence is font by font. SRAM is shown below:



CHANNEL PICTURE

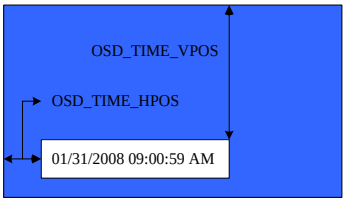
For each channel, there is a picture which can show channel status such as no camera. It can be enabled by setting register OSD_CHPIC_EN and OSD_EN to high. The picture can also be mixed with video by setting register OSD_CHPIC_MIX. The mix method is 50% video and 50% picture. If you want to make some pixels transparent, you can set OSD_CHPIC_TRANS to high. The pixels in color index “00” will be transparent. There is a blink option. If OSD_CHPIC_BLINK is high, picture index 00 and 01 will not blink, and picture index “10” and “11” will blink. So if you put “no video” picture in picture index “10” or “11”, these pictures will blink every 32 frames.

Picture index information for each channel will be saved in SRAM. It needs totally 32x2=64 bits. But for design easily, we use 32x6 bits. Each 6 bit is for each channel, but only LSB 2 bits are used.

Picture position can also be programmed same as channel number. The register setting is shown below.

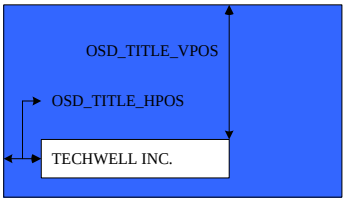
DATE AND TIME

Date and time are only display once on whole screen, not channel by channel. There are totally 32 fonts can be displayed including space. Like other display information, the position for date and time can be programmed. And it can also be disabled and be mixed with video. The font index is saved in display SRAM. It needs 32x6 bits.



TITLE

Title is same as date and time. It has 32 fonts. It needs 32x6 SRAM size.

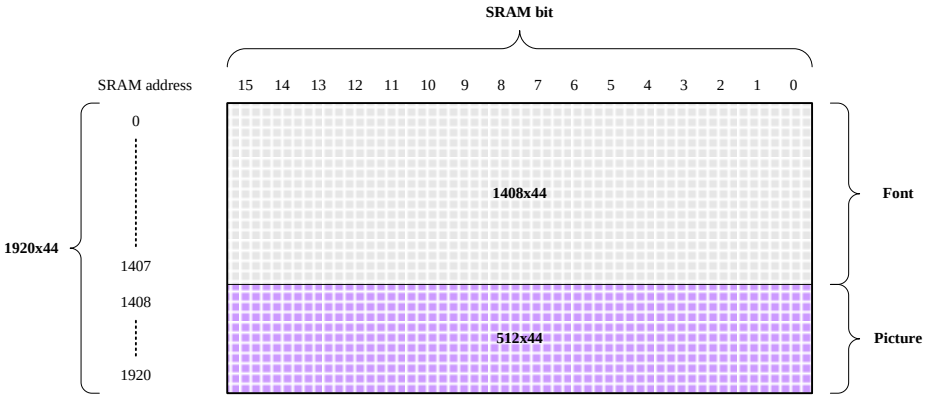


SRAM Allocation

There are two SRAM blocks in this design. One is for font and picture. The other is for display information.

FONT AND PICTURE SRAM

Font and picture are saved in one SRAM block. Font needs 1408x44 bits, and picture needs 512x44 bits. So the total SRAM size is 1920x44 bits.



During system initialization, host need to write font and picture data in this SRAM. The write sequence is:

1. OSD_FRAM_ADDR[7:0]

2. OSD_FRAM_ADDR[10:0]

3. OSD_FRAM_DATA[7:0]

4. OSD_FRAM_DATA[15:8]

5. OSD_FRAM_DATA[23:16]

6. OSD_FRAM_DATA[31:24]

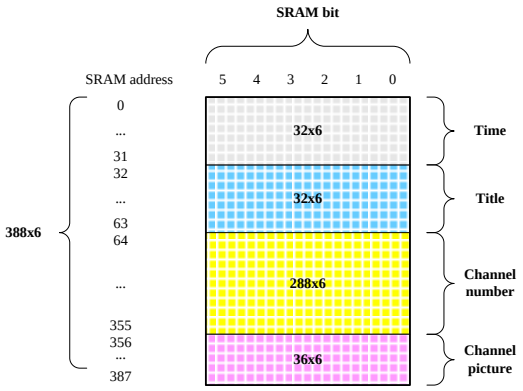
7. OSD_FRAM_DATA[39:32]

8. OSD_FRAM_DATA[43:40]

OSD_FRAM_DATA[43:40] must be the last one.

DISPLAY SRAM

Display SRAM includes channel number, channel picture, date/time and title information. Channel number needs 36x8x6=288x6 bits, channel picture needs 36x6 bits, date/time needs 32x6 bits and title needs 32x6 bits. So the total SRAM size is 388x6 bits.



During display, host need to write index data in this SRAM. The write sequence is:

Set OSD_DRAM_ADDR, and then set OSD_DRAM_DATA.

Register Descriptions

OSD CONTROL REGISTER – 0X080

Bit	R/W	Default	Description
4	RW	0	**OSD_TITLE_EN** Display title enable 1: enable 0: disable
3	RW	0	**OSD_TIME_EN** Display time and date enable 1: enable 0: disable
2	RW	0	**OSD_CHPIC_EN** Display picture for each channel 1: enable 0: disable
1	RW	0	**OSD_CHNUM_EN** Display channel number for each channel 1: enable 0: disable
0	RW	0	**OSD_EN** All OSD information enable or disable. If set to 1, each information is enabled by bit [4:1]. If set to 0, all OSD is disabled. 1: enable 0: disable

OSD MODE REGISTER – 0X081

Bit	R/W	Default	Description
7:6	RW	0	**ASIAN_FONT[1:0]** [1] select height [0] select width
5	RW	0	**OSD_CHPIC_BLINK** If set to 1, picture for each channel blink in picture index 2 and 3. Picture 0 and 1 will not blink 1: enable 0: disable
4	RW	0	**OSD_CHPIC_TRANS** If set to 1, picture in color index “00” will be transparent 1: enable 0: disable
3	RW	0	**OSD_TITLE_MIX** Display title mix enable bit. If set to 1, title will be 50% blending with video 1: enable 0: disable

Bit	R/W	Default	Description
2	RW	0	OSD_TIME_MIX Display time and date mix enable bit. If set to 1, time/date will be 50% blending with video 1: enable 0: disable
1	RW	0	OSD_CHPIC_MIX Display picture mix enable bit. If set to 1, picture will be 50% blending with video 1: enable 0: disable
0	RW	0	OSD_CHNUM_MIX Display channel number information mix enable bit. If set to 1, channel information will be 50% blending with video 1: enable 0: disable

OSD FONT SIZE REGISTER – 0X082

Bit	R/W	Default	Description
7:6	RW	0x1	OSD_CHPIC_POS Channel picture corner position. 00: left top 01: right top 10: left bottom 11: right bottom
5:4	RW	0	OSD_CHNUM_POS Channel number corner position. 00: left top 01: right top 10: left bottom 11: right bottom
3:2	RW	0x3	OSD_FONT_VSIZE Font vertical size for display. There are four choices. 00: 8 01: 10 10: 16, scale up from 8 11: 20, scale up from 10
1:0	RW	0x3	OSD_FONT_HSIZE Font horizontal size for display. There are four choices. 00: 6 01: 8 10: 12, scale up from 6 11: 16, scale up from 8

OSD CHANNNEL NUMBER HORIZONTAL POSITION LOW BYTE REGISTER – 0X083

Bit	R/W	Default	Description
7:0	RW	0	OSD_CHNUM_HPOS[7:0] Channel number information horizontal position offset to each channel horizontal start position. It is one pixel unit.

OSD CHANNNEL NUMBER HORIZONTAL POSITION HIGH BYTE REGISTER – 0X084

Bit	R/W	Default	Description
2:0	RW	0	OSD_CHNUM_HPOS[10:8] Channel number information horizontal position offset to each channel horizontal start position. It is one pixel unit.

OSD CHANNNEL NUMBER VERTICAL POSITION LOW BYTE REGISTER – 0X085

Bit	R/W	Default	Description
7:0	RW	0	OSD_CHNUM_VPOS[7:0] Channel number information vertical position offset to each channel vertical start position. It is one pixel unit.

OSD CHANNNEL NUMBER HORIZONTAL POSITION HIGH BYTE REGISTER – 0X086

Bit	R/W	Default	Description
2:0	RW	0	OSD_CHNUM_VPOS[10:8] Channel number information vertical position offset to each channel vertical start position. It is one pixel unit.

OSD CHANNNEL PICTURE HORIZONTAL POSITION LOW BYTE REGISTER – 0X087

Bit	R/W	Default	Description
7:0	RW	0	OSD_CHPIC_HPOS[7:0] Channel picture information horizontal position offset to each channel horizontal start position. It is one pixel unit.

OSD CHANNNEL PICTURE HORIZONTAL POSITION HIGH BYTE REGISTER – 0X088

Bit	R/W	Default	Description
2:0	RW	0	OSD_CHPIC_HPOS[10:8] Channel picture information horizontal position offset to each channel horizontal start position. It is one pixel unit.

OSD CHANNNEL PICTURE VERTICAL POSITION LOW BYTE REGISTER – 0X089

Bit	R/W	Default	Description
7:0	RW	0	OSD_CHPIC_VPOS[7:0] Channel picture information vertical position offset to each channel vertical start position. It is one pixel unit.

OSD CHANNNEL PICTURE HORIZONTAL POSITION HIGH BYTE REGISTER – 0X08A

Bit	R/W	Default	Description
2:0	RW	0	OSD_CHPIC_VPOS[10:8] Channel number information vertical position offset to each channel vertical start position. It is one pixel unit.

OSD TIME AND DATE HORIZONTAL POSITION LOW BYTE REGISTER – 0X08B

Bit	R/W	Default	Description
7:0	RW	0	OSD_TIME_HPOS[7:0] Time and Date information horizontal position. It is one pixel unit.

OSD TIME AND DATE HORIZONTAL POSITION HIGH BYTE REGISTER – 0X08C

Bit	R/W	Default	Description
2:0	RW	0	OSD_TIME_HPOS[10:8] Time and Date information horizontal position. It is one pixel unit.

OSD TIME AND DATE VERTICAL POSITION LOW BYTE REGISTER – 0X08D

Bit	R/W	Default	Description
7:0	RW	0	OSD_TIME_VPOS[7:0] Time and Date information vertical position. It is one pixel unit.

OSD TIME AND DATE HORIZONTAL POSITION HIGH BYTE REGISTER – 0X08E

Bit	R/W	Default	Description
2:0	RW	0	OSD_TIME_VPOS[10:8] Time and Date information vertical position. It is one pixel unit.

OSD TITLE HORIZONTAL POSITION LOW BYTE REGISTER – 0X08F

Bit	R/W	Default	Description
7:0	RW	0	OSD_TITLE_HPOS[7:0] Title information horizontal position. It is one pixel unit.

OSD TITLE HORIZONTAL POSITION HIGH BYTE REGISTER – 0X090

Bit	R/W	Default	Description
2:0	RW	0	OSD_TITLE_HPOS[10:8] Title information horizontal position. It is one pixel unit.

OSD TITLE VERTICAL POSITION LOW BYTE REGISTER – 0X091

Bit	R/W	Default	Description
7:0	RW	0	OSD_TITLE_VPOS[7:0] Title information vertical position. It is one pixel unit.

OSD TITLE HORIZONTAL POSITION HIGH BYTE REGISTER – 0X092

Bit	R/W	Default	Description
2:0	RW	0	OSD_TITLE_VPOS[10:8] Title information vertical position. It is one pixel unit.

OSD FONT RED COLOR 1 REGISTER – 0X093

Bit	R/W	Default	Description
7:0	RW	0	OSD_FONT_R1[7:0] Font red color for color index 1.

OSD FONT GREEN COLOR 1 REGISTER – 0X094

Bit	R/W	Default	Description
7:0	RW	0	OSD_FONT_G1[7:0] Font green color for color index 1.

OSD FONT BLUE COLOR 1 REGISTER – 0X095

Bit	R/W	Default	Description
7:0	RW	0	OSD_FONT_B1[7:0] Font blue color for color index 1.

OSD FONT RED COLOR 2 REGISTER – 0X096

Bit	R/W	Default	Description
7:0	RW	0	OSD_FONT_R2[7:0] Font red color for color index 2.

OSD FONT GREEN COLOR 2 REGISTER – 0X097

Bit	R/W	Default	Description
7:0	RW	0	OSD_FONT_G2[7:0] Font green color for color index 2.

OSD FONT BLUE COLOR 2 REGISTER – 0X098

Bit	R/W	Default	Description
7:0	RW	0	OSD_FONT_B2[7:0] Font blue color for color index 2.

OSD FONT RED COLOR 3 REGISTER – 0X099

Bit	R/W	Default	Description
7:0	RW	0	OSD_FONT_R3[7:0] Font red color for color index 3.

OSD FONT GREEN COLOR 3 REGISTER – 0X09A

Bit	R/W	Default	Description
7:0	RW	0	OSD_FONT_G3[7:0] Font green color for color index 3.

OSD FONT BLUE COLOR 3 REGISTER – 0X09B

Bit	R/W	Default	Description
7:0	RW	0	OSD_FONT_B3[7:0] Font blue color for color index 3.

OSD PICTURE RED COLOR 0 REGISTER – 0X09C

Bit	R/W	Default	Description
7:0	RW	0	OSD_PIC_R0[7:0] Picture red color for color index 0.

OSD PICTURE GREEN COLOR 0 REGISTER – 0X09D

Bit	R/W	Default	Description
7:0	RW	0	OSD_PIC_G0[7:0] Picture green color for color index 0.

OSD PICTURE BLUE COLOR 0 REGISTER – 0X09E

Bit	R/W	Default	Description
7:0	RW	0	OSD_PIC_B0[7:0] Picture blue color for color index 0.

OSD PICTURE RED COLOR 1 REGISTER – 0X09F

Bit	R/W	Default	Description
7:0	RW	0	OSD_PIC_R1[7:0] Picture red color for color index 1.

OSD PICTURE GREEN COLOR 1 REGISTER – 0X0A0

Bit	R/W	Default	Description
7:0	RW	0	OSD_PIC_G1[7:0] Picture green color for color index 1.

OSD PICTURE BLUE COLOR 1 REGISTER – 0X0A1

Bit	R/W	Default	Description
7:0	RW	0	OSD_PIC_B1[7:0] Picture blue color for color index 1.

OSD PICTURE RED COLOR 2 REGISTER – 0X0A2

Bit	R/W	Default	Description
7:0	RW	0	OSD_PIC_R2[7:0] Picture red color for color index 2.

OSD PICTURE GREEN COLOR 2 REGISTER – 0X0A3

Bit	R/W	Default	Description
7:0	RW	0	OSD_PIC_G2[7:0] Picture green color for color index 2.

OSD PICTURE BLUE COLOR 2 REGISTER – 0X0A4

Bit	R/W	Default	Description
7:0	RW	0	OSD_PIC_B2[7:0] Picture blue color for color index 2.

OSD PICTURE RED COLOR 3 REGISTER – 0X0A5

Bit	R/W	Default	Description
7:0	RW	0	OSD_PIC_R3[7:0] Picture red color for color index 3.

OSD PICTURE GREEN COLOR 3 REGISTER – 0X0A6

Bit	R/W	Default	Description
7:0	RW	0	OSD_PIC_G3[7:0] Picture green color for color index 3.

OSD PICTURE BLUE COLOR 3 REGISTER – 0X0A7

Bit	R/W	Default	Description
7:0	RW	0	OSD_PIC_B3[7:0] Picture blue color for color index 3.

OSD FONT AND PICTURE RAM ADDRESS LOW BYTE REGISTER – 0X0A8

Bit	R/W	Default	Description
7:0	RW	0	OSD_FRAM_ADDR[7:0] Font and Picture SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1920x44. Font size is 1408x44, Picture size is 512x16.

OSD FONT AND PICTURE RAM ADDRESS HIGH BYTE REGISTER – 0X0A9

Bit	R/W	Default	Description
2:0	RW	0	OSD_FRAM_ADDR[10:8] Font and Picture SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1920x44. Font size is 1408x44, Picture size is 512x16.

OSD FONT AND PICTURE RAM DATA LOW BYTE REGISTER – 0X0AA

Bit	R/W	Default	Description
7:0	RW	0	OSD_FRAM_DATA[7:0] Font and Picture SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1920x44. Font size is 1408x44, Picture size is 512x16.

OSD FONT AND PICTURE RAM DATA HIGH BYTE REGISTER – 0X0AB

Bit	R/W	Default	Description
7:0	RW	0	OSD_FRAM_DATA[15:8] Font and Picture SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1920x44. Font size is 1408x44, Picture size is 512x16.

OSD FONT AND PICTURE RAM DATA HIGH BYTE REGISTER – 0X0AC

Bit	R/W	Default	Description
7:0	RW	0	OSD_FRAM_DATA[23:16] Font and Picture SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1920x44. Font size is 1408x44, Picture size is 512x16.

OSD FONT AND PICTURE RAM DATA HIGH BYTE REGISTER – 0X0AD

Bit	R/W	Default	Description
7:0	RW	0	OSD_FRAM_DATA[31:24] Font and Picture SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1920x44. Font size is 1408x44, Picture size is 512x16.

OSD FONT AND PICTURE RAM DATA HIGH BYTE REGISTER – 0X0AE

Bit	R/W	Default	Description
7:0	RW	0	OSD_FRAM_DATA[39:32] Font and Picture SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1920x44. Font size is 1408x44, Picture size is 512x16.

OSD FONT AND PICTURE RAM DATA HIGH BYTE REGISTER – 0X0AF

Bit	R/W	Default	Description
7:0	RW	0	OSD_FRAM_DATA[43:40] Font and Picture SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1920x44. Font size is 1408x44, Picture size is 512x16.

OSD DISPLAY RAM ADDRESS REGISTER – 0X0B0

Bit	R/W	Default	Description
7:0	RW	0	OSD_DRAM_ADDR[7:0] Display SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 388x6. Channel number size is 288x6, time/date size is 32x6, title size is 32x6 and picture index size is 32x6.

OSD DISPLAY RAM ADDRESS REGISTER – 0X0B1

Bit	R/W	Default	Description
0	RW	0	OSD_DRAM_ADDR[8] Display SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 388x6. Channel number size is 288x6, time/date size is 32x6, title size is 32x6 and picture index size is 32x6.

OSD DISPLAY RAM DATA REGISTER – 0X0B2

Bit	R/W	Default	Description
7:0	RW	0	OSD_DRAM_DATA[5:0] Display SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 388x6. Channel number size is 288x6, time/date size is 32x6, title size is 32x6 and picture index size is 32x6.

Motion Detection Unit

Introduction

TW2828 has Motion Detection (MD) circuitry for each incoming video channel (all together the number is 20 (16 SD + 4 HD)). The source for MD circuitry is the 16 D1 and 4 HD streams coming from the input. TW2828 divides the first field of each stream into a 16x12 (SD) cell array to perform motion detection. A unique signature for each cell is extracted and saved into DRAM buffer for later use. The second field of each frame is discarded for simplicity and cost purposes. The motion detection algorithm compares the difference of luminance value between current field and reference field to determine whether a motion has occurred.

TW2828 also supports blind and night detection using the same detection engine.

Below is the number of motion cells and cell size information for different video input formats:

INPUT FORMAT	NUMBER OF MD CELLS (HXV)	CELL HORIZONTAL SIZE (PIXELS)	CELL VERTICAL SIZE (LINES)
SD / XD(960H) 60 Hz	16x12	44	20
SD / XD(960H) 50 Hz	16x12	44	24
720p HD	40x36	32	20
1080i HD	60x27	32	20
1080p HD	60x54	32	20

The MD cell array numbering is shown in Figure 1 below for the SD formats.

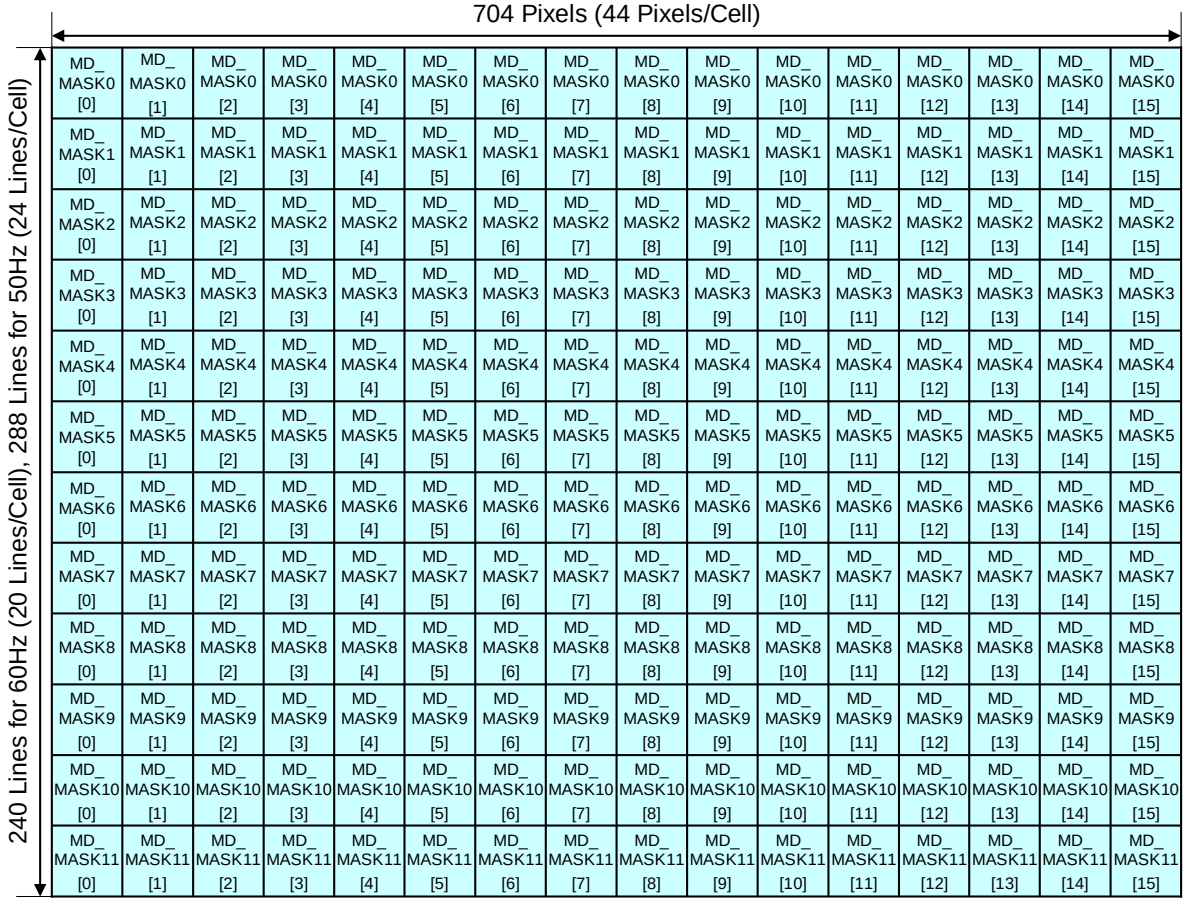


FIGURE 1. MOTION DETECTION MASK AND CELL DEFINITION

Motion Data Extraction

Motion data extraction process follows the scan order, from left to right in horizontal direction and from top to bottom performed on a line by line basis. First, the luminance value of each pixel within a cell is added together and divided by a fixed value. The result is stored into a 16x13 FIFO. Note that the number of horizontal pixels is flexible, so the number of pixels in each cell line varies. This adding and dividing process will repeat itself until it reaches the end of the cell where it will repeat 20 times. Each time a new line luminance value is created; it will be added with the previous one and divided with a fixed number. In the end, an 8 bit number is extracted to represent each cell. So for each motion frame, the data storage needed is 16x12 = 192 bytes (SD formats).

Mask and Detection Region Selection

The motion detection algorithm utilizes the full screen video data and detects individual motion of 16x12 (1920x1080P : 60x54, 1920x1080I : 60x27, 1280x720P : 40x36) cells. Like the extraction process, this full screen for motion detection consists of 704 pixels and 240 lines for NTSC and 288 lines for PAL, and 1920x1080P/1920x1080I/1280x720P for HD formats.

Each cell can be masked via the MD_MASK registers. If the mask bit in specific cell is programmed to high, the related cell is ignored for motion detection.

The motion detection result is stored in Motion Detection Cell Line Result registers, where a “1” indicates motion has been detected and a “0” denotes no motion has been detected in the cell.

To detect motion properly according to various conditions, TW2828 provides several sensitivity and velocity control parameters for each motion detector. TW2828 supports manual strobe function to update motion detection so that it is more appropriate for user-defined motion sensitivity control.

When no-video, motion, blind and night conditios are detected in any video inputs, TW2828 provides an interrupt request to host via the IRQ pin if the request line is enabled. The host processor can read the information of no-video, motion, blind or night detection by accessing the No Video IRQ Status Register (0x2BC~0x2BE), Motion IRQ Status Register (0x2BF~0x2C1), Blind Detection IRQ Status Register (0x2C2~0x2C4) and the Night Detection IRQ Status Register (0x2C5~0x2C7). This status information is updated in the vertical blank period of each input.

TW2828 supports an overlay function to display the motion detection result in the picture with 2D arrayed box. Motion detection information can be displayed using the 2-D Box in RGB Path. Record Path can display by Channel ID type. We can get this information from host interface (Status Read) or used by Interrupt / General Purpose IO pin.

Sensitivity Control

The motion detector has 4 sensitivity parameters to control threshold of motion detection such as the level sensitivity via the MD_LVSENS register, the spatial sensitivity via the MD_SPSENS and MD_CELSENS registers, and the temporal sensitivity parameter via the MD_TMPSENS register.

LEVEL SENSITIVITY

In built-in motion detection algorithm, the motion is detected when luminance level difference between current and reference fields is greater than MD_LVSENS value. Motion detector is more sensitive for the smaller MD_LVSENS value and less sensitive for the larger. When the MD_LVSENS is too small, the motion detector may be weak in filtering noise.

SPATIAL SENSITIVITY

The TW2828 uses SD/XD : 16x12 (1920x1080P : 60x54, 1920x1080I : 60x27, 1280x720P : 40x36) detection cells in full screen for motion detection. Each detection cell is composed of 44 pixels and 20 lines for NTSC and 24 lines for PAL(HD : 32 pixels/20 lines). Motion detection from luminance level difference between two fields alone is very weak in filtering spatial random noise. To prevent fake motion detection caused by random noise, the TW2828 supports a spatial filter via the MD_SPSENS register, which defines the number of detected cells to decide motion detection in full size image. A larger MD_SPSENS value increases the immunity to spatial random noise.

Each detection cell is composed of 4 sub-cells. Motion detection of each cell comes from the results of sub-cells in it. The MD_CELSENS defines the number of detected sub-cells to decide motion detection in the cell. That is, a larger MD_CELSENS value increases the immunity to spatial random noise in detection cell.

TEMPORAL SENSITIVITY

Similarly, temporal filter is used to remove the fake motion detection caused by temporal random noise. The MD_TMPSENS regulates the number of taps in the temporal filter to control the temporal sensitivity. A larger MD_TMPSENS value increases the immunity to temporal random noise.

VELOCITY CONTROL

The motion has various velocities. That is, in fast motion, an object appears and disappears rapidly between the adjacent fields while in slow motion it is to the contrary. As the built-in motion detection algorithm uses just the luminance level difference between two adjacent fields, a slow motion is inferior in detection rate to a fast motion. To compensate this weakness, MD_SPEED parameter is used which is controllable up to 64 fields (2 seconds) for NTSC and 30 fields (2 seconds) for PAL. MD_SPEED parameter adjusts the field interval in which the luminance level is compared. Thus, for detection of a fast motion, a small value is needed and for a slow motion a large value is required. The parameter MD_SPEED value should be greater than MD_TMPSENS value.

Additionally, TW2828 has 2 more parameters to control the selection of reference field. The MD_FIELD[1:0] bit is a field selection parameter such as odd, even, any field or frame.

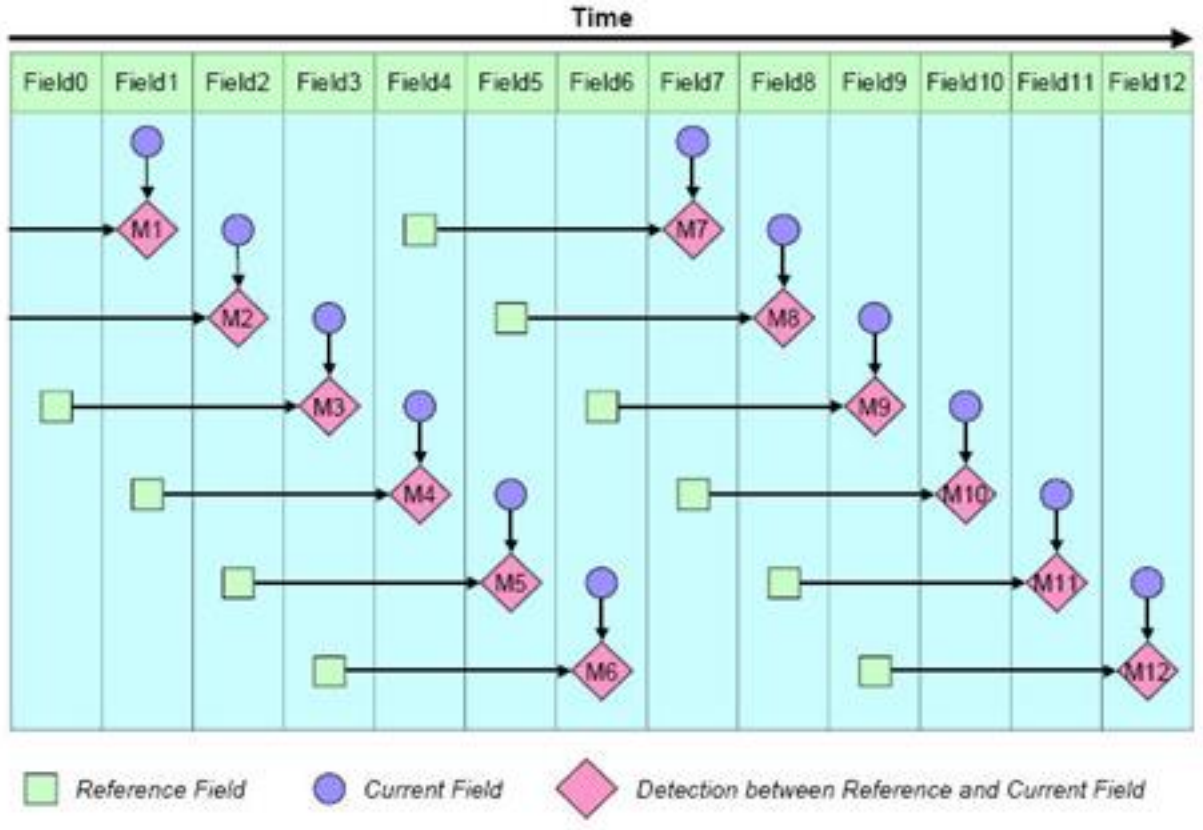


FIGURE 2. THE RELATIONSHIP BETWEEN CURRENT AND REFERENCE FIELDS WHEN MD_REFFLD = "0"

The MD_REFFLD bit is designed to control the updating period of reference field. If MD_REFFLD = “0”, the interval from current field to reference field is always same as the MD_SPEED. It means that the reference field is always updated every field. The Figure 2 shows the relationship between current and reference field for motion detection when MD_REFFLD is set to 0.

TW2828 can update the reference field only at the period of MD_SPEED when the MD_REFFLD is high. For this case, the TW2828 can detect a motion with sense of a various velocity. The Figure 3 shows the relationship between current and reference fields for motion detection when the MD_REFFLD equals to “1”.

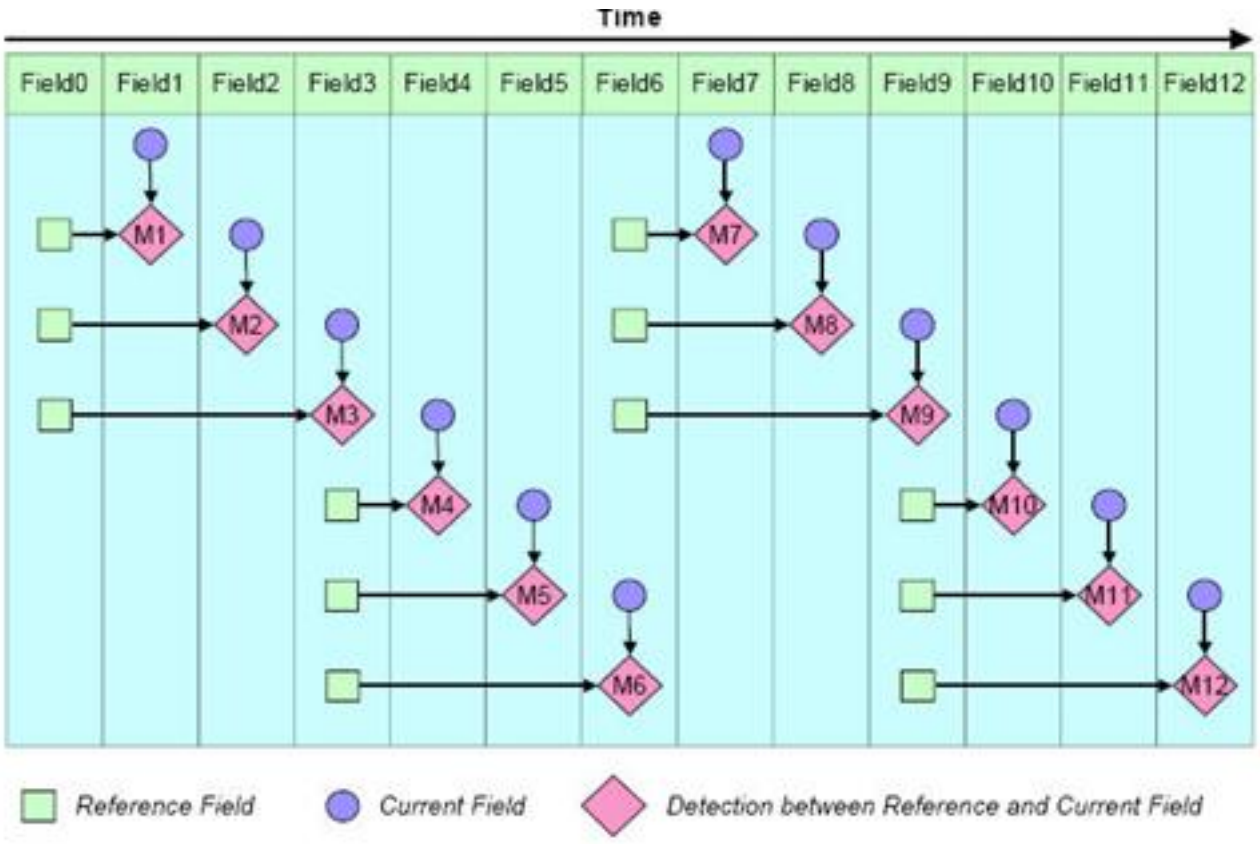


FIGURE 3. THE RELATIONSHIP BETWEEN CURRENT AND REFERENCE FIELDS WHEN MD_REFFLD = "1"

TW2828 also supports the manual detection timing control of the reference field/frame via the MD_STRB_EN and MD_STRB register bits in the MD control registers. If MD_STRB_EN is set to 0, the reference field/frame is automatically updated and reserved on every reference field/frame. If MD_STRB_EN is set to1, the reference field/frame is updated and reserved only when MD_STRB bit is set to 1. If an external strobing signal is used, one can set the mode to 1x and select it. The strobe signal is coming from outside via trigger_in pin. In these two modes, the interval between current and reference field/frame is controlled by user's strobe timing and are very useful for some specific purposes like non-periodical velocity control and very slow motion detection.

Blind Detection

If the luminosity level of a video frame in every corner area is almost equal to the average luminosity level due to camera got covered by something, this input is defined as blind input. TW2828 supports blind detection individually for all 16 video inputs and generates an interrupt to host CPU.

TW2828 uses two sensitivity parameters to detect blind input. One is the level sensitivity via the BD_LVSENS register and the other is spatial sensitivity via the BD_CELSENS register. The TW2828 uses a total of 192 (16x12) cells in full screen for blind detection. The BD_LVSENS parameter controls the threshold of level between cell and field average. The BD_CELSENS parameter defines the number of cells to detect blind. For BD_CELSENS = "0", the number of cells whose level are the same as average of field should be over than 60% to detect blind, 70% for BD_CELSENS = "1", 80% for BD_CELSENS = "2", and 90% for BD_CELSENS = "3". That is, a larger value of BD_LVSENS and BD_CELSENS makes blind detector less sensitive.

TW2828 also supports dual detection mode for non real time applications such as pseudo 8ch application via the MD_DUAL_EN register. The host can read blind detection information for both VIN_A and VIN_B input via the IRQENA_BD (0x2B6~0x2B8) register.

Night Detection

TW2828 uses a user defined, fixed value to determine whether a video input is in a broad day light or at night situations. If the average of luminosity level is lower than this fixed value, this input is defined as night input. Likewise, the opposite is defined as day input. The TW2828 supports night detection for all 16 video inputs and will generated interrupts to host CPU if triggered.

Two parameters are used to detect night input. One is the level sensitivity via the ND_LVSENS register and the other is temporal sensitivity via the ND_TMPSENS register. The ND_LVSENS parameter controls threshold level of day and night. The ND_TMPSENS parameter regulates the number of taps in the temporal low pass filter to control the temporal sensitivity. The large value of ND_LVSENS and ND_TMPSENS makes night detector less sensitive.

The TW2828 also supports dual detection mode for non-real-time application such as pseudo 8ch application via the MD_DUAL_EN register. The host can read night detection information for both VIN_A and VIN_B input via the IRQENA_ND (0x2B9~0x2BB) register.

Register Table

Address	R/W	Default	Description
0x800	R/W	0x00	Motion Detection Cell Line 0 Mask Register 1
0x801	R/W	0x00	Motion Detection Cell Line 0 Mask Register 2
0x802	R/W	0x00	Motion Detection Cell Line 1 Mask Register 1
0x803	R/W	0x00	Motion Detection Cell Line 1 Mask Register 2
0x804	R/W	0x00	Motion Detection Cell Line 2 Mask Register 1
0x805	R/W	0x00	Motion Detection Cell Line 2 Mask Register 1
0x806	R/W	0x00	Motion Detection Cell Line 3 Mask Register 2
0x807	R/W	0x00	Motion Detection Cell Line 3 Mask Register 1
0x808	R/W	0x00	Motion Detection Cell Line 4 Mask Register 2
0x809	R/W	0x00	Motion Detection Cell Line 4 Mask Register 1
0x80A	R/W	0x00	Motion Detection Cell Line 5 Mask Register 1
0x80B	R/W	0x00	Motion Detection Cell Line 5 Mask Register 2
0x80C	R/W	0x00	Motion Detection Cell Line 6 Mask Register 1
0x80D	R/W	0x00	Motion Detection Cell Line 6 Mask Register 2
0x80E	R/W	0x00	Motion Detection Cell Line 7 Mask Register 1
0x80F	R/W	0x00	Motion Detection Cell Line 7 Mask Register 2
0x810	R/W	0x00	Motion Detection Cell Line 8 Mask Register 1
0x811	R/W	0x00	Motion Detection Cell Line 8 Mask Register 2
0x812	R/W	0x00	Motion Detection Cell Line 9 Mask Register 1
0x813	R/W	0x00	Motion Detection Cell Line 9 Mask Register 2
0x814	R/W	0x00	Motion Detection Cell Line 10 Mask Register 1
0x815	R/W	0x00	Motion Detection Cell Line 10 Mask Register 2
0x816	R/W	0x00	Motion Detection Cell Line 11 Mask Register 1
0x817	R/W	0x00	Motion Detection Cell Line 11 Mask Register 2
0x818	R/W	0x00	Motion Detection Control Register 1
0x819	R/W	0x00	Motion Detection Control Register 2
0x81A	R/W	0x00	Motion Detection Control Register 3
0x81B	R/W	0x00	Motion Detection Control Register 4
0x81E	R/W	0x00	Motion Detection Control Register 5
0x81F	R/W	0x00	Motion Detection Control Register 6
0x820	R/W	0x00	Motion Detection Cell Line 0 Result Register 1
0x821	R/W	0x00	Motion Detection Cell Line 0 Result Register 2
0x822	R/W	0x00	Motion Detection Cell Line 1 Result Register 1
0x823	R/W	0x00	Motion Detection Cell Line 1 Result Register 2
0x824	R/W	0x00	Motion Detection Cell Line 2 Result Register 1
0x825	R/W	0x00	Motion Detection Cell Line 2 Result Register 2
0x826	R/W	0x00	Motion Detection Cell Line 3 Result Register 1

Address	R/W	Default	Description
0x827	R/W	0x00	Motion Detection Cell Line 3 Result Register 2
0x828	R/W	0x00	Motion Detection Cell Line 4 Result Register 1
0x829	R/W	0x00	Motion Detection Cell Line 4 Result Register 2
0x82A	R/W	0x00	Motion Detection Cell Line 5 Result Register 1
0x82B	R/W	0x00	Motion Detection Cell Line 5 Result Register 2
0x82C	R/W	0x00	Motion Detection Cell Line 6 Result Register 1
0x82D	R/W	0x00	Motion Detection Cell Line 6 Result Register 2
0x82E	R/W	0x00	Motion Detection Cell Line 7 Result Register 1
0x82F	R/W	0x00	Motion Detection Cell Line 7 Result Register 2
0x830	R/W	0x00	Motion Detection Cell Line 8 Result Register 1
0x831	R/W	0x00	Motion Detection Cell Line 8 Result Register 2
0x832	R/W	0x00	Motion Detection Cell Line 9 Result Register 1
0x833	R/W	0x00	Motion Detection Cell Line 9 Result Register 2
0x834	R/W	0x00	Motion Detection Cell Line 10 Result Register 1
0x835	R/W	0x00	Motion Detection Cell Line 10 Result Register 2
0x836	R/W	0x00	Motion Detection Cell Line 11 Result Register 1
0x837	R/W	0x00	Motion Detection Cell Line 11 Result Register 2

Register Table (HD Motion Detector)

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x700	R/W	0x00	Motion Detection Mask Register 1
0x701	R/W	0x00	Motion Detection Mask Register 2
0x702	R/W	0x00	Motion Detection Mask Register 3
0x703	R/W	0x00	Motion Detection Mask Register 4
0x704	R/W	0x00	Motion Detection Mask Register 5
0x705	R/W	0x00	Motion Detection Mask Register 6
0x706	R/W	0x00	Motion Detection Mask Register 7
0x707	R/W	0x00	Motion Detection Mask Register 8
0x708	R/W	0x00	Motion Detection Mask Line Register
0x709 ~ 0x70F			Reserved
0x710	R/W	0x00	Motion Box Horizontal One Plus Register 1
0x711	R/W	0x00	Motion Box Horizontal One Plus Register 2
0x712	R/W	0x00	Motion Box Horizontal One Plus Register 3
0x713	R/W	0x00	Motion Box Horizontal One Plus Register 4
0x714	R/W	0x00	Motion Box Horizontal One Plus Register 5
0x715	R/W	0x00	Motion Box Horizontal One Plus Register 6
0x716	R/W	0x00	Motion Box Horizontal One Plus Register 7
0x717	R/W	0x00	Motion Box Horizontal One Plus Register 8
0x718	R/W	0x00	Motion Box Vertical One Plus Register 1
0x719	R/W	0x00	Motion Box Vertical One Plus Register 2
0x71A	R/W	0x00	Motion Box Vertical One Plus Register 3
0x71B	R/W	0x00	Motion Box Vertical One Plus Register 4
0x71C	R/W	0x00	Motion Box Vertical One Plus Register 5
0x71D	R/W	0x00	Motion Box Vertical One Plus Register 6
0x71E	R/W	0x00	Motion Box Vertical One Plus Register 7
0x71F ~ 0x76F			Reserved
0x770	R/W	0x00	Motion Detection Control Register 1
0x771	R/W	0x00	Motion Detection Control Register 2

0x772	R/W	0x00	Motion Detection Control Register 3
0x773	R/W	0x00	Motion Detection Control Register 4
0x774	R/W	0x00	Motion Detection Control Register 5
0x775	R/W	0x00	Motion Detection Control Register 6
0x780	R/W	0x00	Motion Detection Cell Line 0/14/28/42 Result Register 1
0x781	R/W	0x00	Motion Detection Cell Line 0/14/28/42 Result Register 2
0x782	R/W	0x00	Motion Detection Cell Line 0/14/28/42 Result Register 3
0x783	R/W	0x00	Motion Detection Cell Line 0/14/28/42 Result Register 4
0x784	R/W	0x00	Motion Detection Cell Line 0/14/28/42 Result Register 5
0x785	R/W	0x00	Motion Detection Cell Line 0/14/28/42 Result Register 6
0x786	R/W	0x00	Motion Detection Cell Line 0/14/28/42 Result Register 7
0x787	R/W	0x00	Motion Detection Cell Line 0/14/28/42 Result Register 8
0x788	R/W	0x00	Motion Detection Cell Line 1/15/29/43 Result Register 1
0x789	R/W	0x00	Motion Detection Cell Line 1/15/29/43 Result Register 2
0x78A	R/W	0x00	Motion Detection Cell Line 1/15/29/43 Result Register 3
0x78B	R/W	0x00	Motion Detection Cell Line 1/15/29/43 Result Register 4
0x78C	R/W	0x00	Motion Detection Cell Line 1/15/29/43 Result Register 5
0x78D	R/W	0x00	Motion Detection Cell Line 1/15/29/43 Result Register 6
0x78E	R/W	0x00	Motion Detection Cell Line 1/15/29/43 Result Register 7
0x78F	R/W	0x00	Motion Detection Cell Line 1/15/29/43 Result Register 8
0x790	R/W	0x00	Motion Detection Cell Line 2/16/30/44 Result Register 1
0x791	R/W	0x00	Motion Detection Cell Line 2/16/30/44 Result Register 2
0x792	R/W	0x00	Motion Detection Cell Line 2/16/30/44 Result Register 3
0x793	R/W	0x00	Motion Detection Cell Line 2/16/30/44 Result Register 4
0x794	R/W	0x00	Motion Detection Cell Line 2/16/30/44 Result Register 5
0x795	R/W	0x00	Motion Detection Cell Line 2/16/30/44 Result Register 6
0x796	R/W	0x00	Motion Detection Cell Line 2/16/30/44 Result Register 7
0x797	R/W	0x00	Motion Detection Cell Line 2/16/30/44 Result Register 8
0x798	R/W	0x00	Motion Detection Cell Line 3/17/31/45 Result Register 1
0x799	R/W	0x00	Motion Detection Cell Line 3/17/31/45 Result Register 2
0x79A	R/W	0x00	Motion Detection Cell Line 3/17/31/45 Result Register 3
0x79B	R/W	0x00	Motion Detection Cell Line 3/17/31/45 Result Register 4
0x79C	R/W	0x00	Motion Detection Cell Line 3/17/31/45 Result Register 5
0x79D	R/W	0x00	Motion Detection Cell Line 3/17/31/45 Result Register 6
0x79E	R/W	0x00	Motion Detection Cell Line 3/17/31/45 Result Register 7
0x79F	R/W	0x00	Motion Detection Cell Line 3/17/31/45 Result Register 8
0x7A0	R/W	0x00	Motion Detection Cell Line 4/18/32/46 Result Register 1
0x7A1	R/W	0x00	Motion Detection Cell Line 4/18/32/46 Result Register 2
0x7A2	R/W	0x00	Motion Detection Cell Line 4/18/32/46 Result Register 3
0x7A3	R/W	0x00	Motion Detection Cell Line 4/18/32/46 Result Register 4
0x7A4	R/W	0x00	Motion Detection Cell Line 4/18/32/46 Result Register 5
0x7A5	R/W	0x00	Motion Detection Cell Line 4/18/32/46 Result Register 6
0x7A6	R/W	0x00	Motion Detection Cell Line 4/18/32/46 Result Register 7
0x7A7	R/W	0x00	Motion Detection Cell Line 4/18/32/46 Result Register 8
0x7A8	R/W	0x00	Motion Detection Cell Line 5/19/33/47 Result Register 1
0x7A9	R/W	0x00	Motion Detection Cell Line 5/19/33/47 Result Register 2
0x7AA	R/W	0x00	Motion Detection Cell Line 5/19/33/47 Result Register 3
0x7AB	R/W	0x00	Motion Detection Cell Line 5/19/33/47 Result Register 4
0x7AC	R/W	0x00	Motion Detection Cell Line 5/19/33/47 Result Register 5
0x7AD	R/W	0x00	Motion Detection Cell Line 5/19/33/47 Result Register 6
0x7AE	R/W	0x00	Motion Detection Cell Line 5/19/33/47 Result Register 7
0x7AF	R/W	0x00	Motion Detection Cell Line 5/19/33/47 Result Register 8
0x7B0	R/W	0x00	Motion Detection Cell Line 6/20/34/48 Result Register 1
0x7B1	R/W	0x00	Motion Detection Cell Line 6/20/34/48 Result Register 2
0x7B2	R/W	0x00	Motion Detection Cell Line 6/20/34/48 Result Register 3
0x7B3	R/W	0x00	Motion Detection Cell Line 6/20/34/48 Result Register 4

0x7B4	R/W	0x00	Motion Detection Cell Line 6/20/34/48 Result Register 5
0x7B5	R/W	0x00	Motion Detection Cell Line 6/20/34/48 Result Register 6
0x7B6	R/W	0x00	Motion Detection Cell Line 6/20/34/48 Result Register 7
0x7B7	R/W	0x00	Motion Detection Cell Line 6/20/34/48 Result Register 8
0x7B8	R/W	0x00	Motion Detection Cell Line 7/21/35/49 Result Register 1
0x7B9	R/W	0x00	Motion Detection Cell Line 7/21/35/49 Result Register 2
0x7BA	R/W	0x00	Motion Detection Cell Line 7/21/35/49 Result Register 3
0x7BB	R/W	0x00	Motion Detection Cell Line 7/21/35/49 Result Register 4
0x7BC	R/W	0x00	Motion Detection Cell Line 7/21/35/49 Result Register 5
0x7BD	R/W	0x00	Motion Detection Cell Line 7/21/35/49 Result Register 6
0x7BE	R/W	0x00	Motion Detection Cell Line 7/21/35/49 Result Register 7
0x7BF	R/W	0x00	Motion Detection Cell Line 7/21/35/49 Result Register 8
0x7C0	R/W	0x00	Motion Detection Cell Line 8/22/36/50 Result Register 1
0x7C1	R/W	0x00	Motion Detection Cell Line 8/22/36/50 Result Register 2
0x7C2	R/W	0x00	Motion Detection Cell Line 8/22/36/50 Result Register 3
0x7C3	R/W	0x00	Motion Detection Cell Line 8/22/36/50 Result Register 4
0x7C4	R/W	0x00	Motion Detection Cell Line 8/22/36/50 Result Register 5
0x7C5	R/W	0x00	Motion Detection Cell Line 8/22/36/50 Result Register 6
0x7C6	R/W	0x00	Motion Detection Cell Line 8/22/36/50 Result Register 7
0x7C7	R/W	0x00	Motion Detection Cell Line 8/22/36/50 Result Register 8
0x7C8	R/W	0x00	Motion Detection Cell Line 9/23/37/51 Result Register 1
0x7C9	R/W	0x00	Motion Detection Cell Line 9/23/37/51 Result Register 2
0x7CA	R/W	0x00	Motion Detection Cell Line 9/23/37/51 Result Register 3
0x7CB	R/W	0x00	Motion Detection Cell Line 9/23/37/51 Result Register 4
0x7CC	R/W	0x00	Motion Detection Cell Line 9/23/37/51 Result Register 5
0x7CD	R/W	0x00	Motion Detection Cell Line 9/23/37/51 Result Register 6
0x7CE	R/W	0x00	Motion Detection Cell Line 9/23/37/51 Result Register 7
0x7CF	R/W	0x00	Motion Detection Cell Line 9/23/37/51 Result Register 8
0x7D0	R/W	0x00	Motion Detection Cell Line 10/24/38/52 Result Register 1
0x7D1	R/W	0x00	Motion Detection Cell Line 10/24/38/52 Result Register 2
0x7D2	R/W	0x00	Motion Detection Cell Line 10/24/38/52 Result Register 3
0x7D3	R/W	0x00	Motion Detection Cell Line 10/24/38/52 Result Register 4
0x7D4	R/W	0x00	Motion Detection Cell Line 10/24/38/52 Result Register 5
0x7D5	R/W	0x00	Motion Detection Cell Line 10/24/38/52 Result Register 6
0x7D6	R/W	0x00	Motion Detection Cell Line 10/24/38/52 Result Register 7
0x7D7	R/W	0x00	Motion Detection Cell Line 10/24/38/52 Result Register 8
0x7D8	R/W	0x00	Motion Detection Cell Line 11/25/39/53 Result Register 1
0x7D9	R/W	0x00	Motion Detection Cell Line 11/25/39/53 Result Register 2
0x7DA	R/W	0x00	Motion Detection Cell Line 11/25/39/53 Result Register 3
0x7DB	R/W	0x00	Motion Detection Cell Line 11/25/39/53 Result Register 4
0x7DC	R/W	0x00	Motion Detection Cell Line 11/25/39/53 Result Register 5
0x7DD	R/W	0x00	Motion Detection Cell Line 11/25/39/53 Result Register 6
0x7DE	R/W	0x00	Motion Detection Cell Line 11/25/39/53 Result Register 7
0x7DF	R/W	0x00	Motion Detection Cell Line 11/25/39/53 Result Register 8
0x7E0	R/W	0x00	Motion Detection Cell Line 12/26/40 Result Register 1
0x7E1	R/W	0x00	Motion Detection Cell Line 12/26/40 Result Register 2
0x7E2	R/W	0x00	Motion Detection Cell Line 12/26/40 Result Register 3
0x7E3	R/W	0x00	Motion Detection Cell Line 12/26/40 Result Register 4
0x7E4	R/W	0x00	Motion Detection Cell Line 12/26/40 Result Register 5
0x7E5	R/W	0x00	Motion Detection Cell Line 12/26/40 Result Register 6
0x7E6	R/W	0x00	Motion Detection Cell Line 12/26/40 Result Register 7
0x7E7	R/W	0x00	Motion Detection Cell Line 12/26/40 Result Register 8
0x7E8	R/W	0x00	Motion Detection Cell Line 13/27/41 Result Register 1
0x7E9	R/W	0x00	Motion Detection Cell Line 13/27/41 Result Register 2
0x7EA	R/W	0x00	Motion Detection Cell Line 13/27/41 Result Register 3
0x7EB	R/W	0x00	Motion Detection Cell Line 13/27/41 Result Register 4

0x7EC	R/W	0x00	Motion Detection Cell Line 13/27/41 Result Register 5
0x7ED	R/W	0x00	Motion Detection Cell Line 13/27/41 Result Register 6
0x7EE	R/W	0x00	Motion Detection Cell Line 13/27/41 Result Register 7
0x7EF	R/W	0x00	Motion Detection Cell Line 13/27/41 Result Register 8

Registers Description

MOTION DETECTION CELL LINE 0 MASK REGISTER 1 – 0X800

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK0[7:0]

This is for channel 0. For other channel the assignments are: 0x840, 0x880, 0x8C0, 0x900, 0x940, 0x980, 0x9C0, 0xA00, 0xA40, 0xA80, 0xAC0, 0xB00, 0xB40, 0xB80, 0xBC0 respectively

MOTION DETECTION CELL LINE 0 MASK REGISTER 2 – 0X801

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK0[15:8]

MOTION DETECTION CELL LINE 1 MASK REGISTER 1 – 0X802

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK1[7:0]

MOTION DETECTION CELL LINE 1 MASK REGISTER 2 – 0X803

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK1[15:8]

MOTION DETECTION CELL LINE 2 MASK REGISTER 1 – 0X804

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK2[7:0]

MOTION DETECTION CELL LINE 2 MASK REGISTER 2 – 0X805

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK2[15:8]

MOTION DETECTION CELL LINE 3 MASK REGISTER 1 – 0X806

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK3[7:0]

MOTION DETECTION CELL LINE 3 MASK REGISTER 2 – 0X807

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK3[15:8]

MOTION DETECTION CELL LINE 4 MASK REGISTER 1 – 0X808

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK4[7:0]

MOTION DETECTION CELL LINE 4 MASK REGISTER 2 – 0X809

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK4[15:8]

MOTION DETECTION CELL LINE 5 MASK REGISTER 1 – 0X80A

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK5[7:0]

MOTION DETECTION CELL LINE 5 MASK REGISTER 2 – 0X80B

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK5[15:8]

MOTION DETECTION CELL LINE 6 MASK REGISTER 1 – 0X80C

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK6[7:0]

MOTION DETECTION CELL LINE 6 MASK REGISTER 2 – 0X80D

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK6[15:8]

MOTION DETECTION CELL LINE 7 MASK REGISTER 1 – 0X80E

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK7[7:0]

MOTION DETECTION CELL LINE 7 MASK REGISTER 2 – 0X80F

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK7[15:8]

MOTION DETECTION CELL LINE 8 MASK REGISTER 1 – 0X810

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK8[7:0]

MOTION DETECTION CELL LINE 8 MASK REGISTER 2 – 0X811

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK8[15:8]

MOTION DETECTION CELL LINE 9 MASK REGISTER 1 – 0X812

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK9[7:0]

MOTION DETECTION CELL LINE 9 MASK REGISTER 2 – 0X813

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK9[15:8]

MOTION DETECTION CELL LINE 10 MASK REGISTER 1 – 0X814

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK10[7:0]

MOTION DETECTION CELL LINE 10 MASK REGISTER 2 – 0X815

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK10[15:8]

MOTION DETECTION CELL LINE 11 MASK REGISTER 1 – 0X816

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK11[7:0]

MOTION DETECTION CELL LINE 11 MASK REGISTER 2 – 0X817

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK11[15:8]

MOTION DETECTION CONTROL REGISTER 1 – 0X818

Bit	R/W	Default	Description
7	R/W	0x0	**MD_DIS,** channel disable, 1 = disable
6	R/W	0x0	**Reserved**
5:4	R/W	0x0	**BD_CELLSENS,** blind cell sensitivity adjust 00 = 60% 01 = 70% 10 = 80% 11 = 90%
3:0	R/W	0x0	**BD_LVSENS,** Blind level sensitivity select

MOTION DETECTION CONTROL REGISTER 2 – 0X819

Bit	R/W	Default	Description
7:4	R/W	0x0	**ND_LVSENS,** night detection level sensitivity adjust
3:0	R/W	0x0	**ND_TMPSENS,** night detection temporal sensitivity adjust

MOTION DETECTION CONTROL REGISTER 3 – 0X81A

Bit	R/W	Default	Description
7:6	R/W	0x0	**MD_FIELD,** motion detection field select
5	R/W	0x0	**Reserved**
4:0	R/W	0x0	**MD_LVSENS,** motion detection level sensitivity adjust

MOTION DETECTION CONTROL REGISTER 4 – 0X81B

Bit	R/W	Default	Description
7	R/W	0x0	**Reserved**
6	R/W	0x0	**MD_REFFLD,** Reference Field Update Mode 0 : Update Every Field, 1 : Update Every MD_SPEED Period
5:0	R/W	0x0	**MD_SPEED,** temporal sensitivity adjust

MOTION DETECTION CONTROL REGISTER 5 – 0X81E

Bit	R/W	Default	Description
7:4	R/W	0x0	**MD_TMPSENS,** motion detection temporal sensitivity adjust
3:0	R/W	0x0	**MD_SPSENS,** motion spatial sensitivity adjust

MOTION DETECTION CONTROL REGISTER 6 – 0X81F

Bit	R/W	Default	Description
7	R/W	0x0	**MD_VINV,** motion detection display mode, 1 = vertical invert
6	R/W	0x0	**MD_HINV,** motion detection display mode, 1 = horizontal invert
5:4	R/W	0x0	**MD_CELLSENS,** Define the threshold of sub-cell number for motion detection 0 = Motion is detected if 1 sub-cell has motion(default) 1 = Motion is detected if 2 sub-cell has motion 2 = Motion is detected if 3 sub-cell has motion 3 = Motion is detected if 4 sub-cell has motion(less sensitive)
3	R/W	0x0	**Reserved**
2	R/W	0x0	**MD_STRB,** internal user strobe signal
1:0	R/W	0x0	**Strobe mode** 00 = automatic mode 01 = internal strobe mode, **MD_STRB_EN = 1** 1x = external strobe mode

MOTION DETECTION CELL LINE 0 RESULT REGISTER 1 – 0X820

Bit	R/W	Default	Description
7:0	R	0x0	**md_det0[7:0]**

This is for channel 0. For other channel the assignments are: 0x860, 0x8A0, 0x8E0, 0x920, 0x960, 0x9A0, 0x9E0, 0xA20, 0xA60, 0xAA0, 0xAE0, 0xB20, 0xB60, 0xBA0, 0xBE0 respectively

MOTION DETECTION CELL LINE 0 RESULT REGISTER 2 – 0X821

Bit	R/W	Default	Description
7:0	R	0x0	md_det0[15:8]

MOTION DETECTION CELL LINE 1 RESULT REGISTER 1 – 0X822

Bit	R/W	Default	Description
7:0	R	0x0	md_det1[7:0]

MOTION DETECTION CELL LINE 1 RESULT REGISTER 2 – 0X823

Bit	R/W	Default	Description
7:0	R	0x0	md_det1[15:8]

MOTION DETECTION CELL LINE 2 RESULT REGISTER 1 – 0X824

Bit	R/W	Default	Description
7:0	R	0x0	md_det2[7:0]

MOTION DETECTION CELL LINE 2 RESULT REGISTER 2 – 0X825

Bit	R/W	Default	Description
7:0	R	0x0	md_det2[15:8]

MOTION DETECTION CELL LINE 3 RESULT REGISTER 1 – 0X826

Bit	R/W	Default	Description
7:0	R	0x0	md_det3[7:0]

MOTION DETECTION CELL LINE 3 RESULT REGISTER 2 – 0X827

Bit	R/W	Default	Description
7:0	R	0x0	md_det3[15:8]

MOTION DETECTION CELL LINE 4 RESULT REGISTER 1 – 0X828

Bit	R/W	Default	Description
7:0	R	0x0	md_det4[7:0]

MOTION DETECTION CELL LINE 4 RESULT REGISTER 2 – 0X829

Bit	R/W	Default	Description
7:0	R	0x0	md_det4[15:8]

MOTION DETECTION CELL LINE 5 RESULT REGISTER 1 – 0X82A

Bit	R/W	Default	Description
7:0	R	0x0	md_det5[7:0]

MOTION DETECTION CELL LINE 5 RESULT REGISTER 2 – 0X82B

Bit	R/W	Default	Description
7:0	R	0x0	md_det5[15:8]

MOTION DETECTION CELL LINE 6 RESULT REGISTER 1 – 0X82C

Bit	R/W	Default	Description
7:0	R	0x0	md_det6[7:0]

MOTION DETECTION CELL LINE 6 RESULT REGISTER 2 – 0X82D

Bit	R/W	Default	Description
7:0	R	0x0	md_det6[15:8]

MOTION DETECTION CELL LINE 7 RESULT REGISTER 1 – 0X82E

Bit	R/W	Default	Description
7:0	R	0x0	md_det7[7:0]

MOTION DETECTION CELL LINE 7 RESULT REGISTER 2 – 0X82F

Bit	R/W	Default	Description
7:0	R	0x0	md_det7[15:8]

MOTION DETECTION CELL LINE 8 RESULT REGISTER 1 – 0X830

Bit	R/W	Default	Description
7:0	R	0x0	md_det8[7:0]

MOTION DETECTION CELL LINE 8 RESULT REGISTER 2 – 0X831

Bit	R/W	Default	Description
7:0	R	0x0	md_det8[15:8]

MOTION DETECTION CELL LINE 9 RESULT REGISTER 1 – 0X832

Bit	R/W	Default	Description
7:0	R	0x0	md_det9[7:0]

MOTION DETECTION CELL LINE 9 RESULT REGISTER 2 – 0X833

Bit	R/W	Default	Description
7:0	R	0x0	md_det9[15:8]

MOTION DETECTION CELL LINE 10 RESULT REGISTER 1 – 0X834

Bit	R/W	Default	Description
7:0	R	0x0	md_det10[7:0]

MOTION DETECTION CELL LINE 10 RESULT REGISTER 2 – 0X835

Bit	R/W	Default	Description
7:0	R	0x0	md_det10[15:8]

MOTION DETECTION CELL LINE 11 RESULT REGISTER 1 – 0X836

Bit	R/W	Default	Description
7:0	R	0x0	md_det11[7:0]

MOTION DETECTION CELL LINE 11 RESULT REGISTER 2 – 0X837

Bit	R/W	Default	Description
7:0	R	0x0	md_det11[15:8]

Register Descriptions(HD Motion Detector)

MOTION DETECTION MASK REGISTER 1 – 0X700

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK[7:0]

This is for channel 0. channel 1 : 0x4FF[1:0] = 1, channel 2 : 0x4FF[1:0] = 2, channel 3 : 0x4FF[1:0] = 3

MOTION DETECTION MASK REGISTER 2 – 0X701

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK[15:8]

MOTION DETECTION MASK REGISTER 3 – 0X702

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK[23:16]

MOTION DETECTION MASK REGISTER 4 – 0X703

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK[31:24]

MOTION DETECTION MASK REGISTER 5 – 0X704

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK[39:32]

MOTION DETECTION MASK REGISTER 6 – 0X705

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK[47:40]

MOTION DETECTION MASK REGISTER 7 – 0X706

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK[55:48]

MOTION DETECTION MASK REGISTER 8 – 0X707

Bit	R/W	Default	Description
7:0	R/W	0x0	MD_MASK[59:56]

MOTION DETECTION MASK LINE REGISTER – 0X708

Bit	R/W	Default	Description
7	R/W	0x0	WR_RD 0 = Read mask data 1 = Write mask data
6			Reserve
5:0	R/W	0x0	MASK Line [5:0] : Select setting mask line

MOTION BOX HORIZONTAL ONE PLUS REGISTER 1 – 0X710

Bit	R/W	Default	Description
7:0	R/W	0x0	H_PLUS[7:0] : 1 to 8 cell 0 = This cell uses same setting value as motion box H size (MDBOX_HS) 1 = This cell uses plus 1 setting value as motion box H size (MDBOX_HS + 1)

This is for channel 0. channel 1 : 0x4FF[1:0] = 1, channel 2 : 0x4FF[1:0] = 2, channel 3 : 0x4FF[1:0] = 3

MOTION BOX HORIZONTAL ONE PLUS REGISTER 2 – 0X711

Bit	R/W	Default	Description
7:0	R/W	0x0	H_PLUS[15:8]

MOTION BOX HORIZONTAL ONE PLUS REGISTER 3 – 0X712

Bit	R/W	Default	Description
7:0	R/W	0x0	H_PLUS[23:16]

MOTION BOX HORIZONTAL ONE PLUS REGISTER 4 – 0X713

Bit	R/W	Default	Description
7:0	R/W	0x0	H_PLUS[31:24]

MOTION BOX HORIZONTAL ONE PLUS REGISTER 5 – 0X714

Bit	R/W	Default	Description
7:0	R/W	0x0	H_PLUS[39:32]

MOTION BOX HORIZONTAL ONE PLUS REGISTER 6 – 0X715

Bit	R/W	Default	Description
7:0	R/W	0x0	H_PLUS[47:40]

MOTION BOX HORIZONTAL ONE PLUS REGISTER 7 – 0X716

Bit	R/W	Default	Description
7:0	R/W	0x0	H_PLUS[55:48]

MOTION BOX HORIZONTAL ONE PLUS REGISTER 8 – 0X717

Bit	R/W	Default	Description
7:0	R/W	0x0	H_PLUS[59:56]

MOTION BOX VERTICAL ONE PLUS REGISTER 1 – 0X718

Bit	R/W	Default	Description
7:0	R/W	0x0	V_PLUS[7:0] : 1 to 8 cell 0 = This cell uses same setting value as motion box V size (MDBOX_VS) 1 = This cell uses plus 1 setting value as motion box V size (MDBOX_VS + 1)

This is for channel 0. channel 1 : 0x4FF[1:0] = 1, channel 2 : 0x4FF[1:0] = 2, channel 3 : 0x4FF[1:0] = 3

MOTION BOX VERTICAL ONE PLUS REGISTER 2 – 0X719

Bit	R/W	Default	Description
7:0	R/W	0x0	V_PLUS[15:8]

MOTION BOX VERTICAL ONE PLUS REGISTER 3 – 0X71A

Bit	R/W	Default	Description
7:0	R/W	0x0	V_PLUS[23:16]

MOTION BOX VERTICAL ONE PLUS REGISTER 4 – 0X71B

Bit	R/W	Default	Description
7:0	R/W	0x0	V_PLUS[31:24]

MOTION BOX VERTICAL ONE PLUS REGISTER 5 – 0X71C

Bit	R/W	Default	Description
7:0	R/W	0x0	V_PLUS[39:32]

MOTION BOX VERTICAL ONE PLUS REGISTER 6 – 0X71D

Bit	R/W	Default	Description
7:0	R/W	0x0	V_PLUS[47:40]

MOTION BOX VERTICAL ONE PLUS REGISTER 7 – 0X71E

Bit	R/W	Default	Description
7:6			Reserve
5:0	R/W	0x0	V_PLUS[53:48]

MOTION DETECTION CONTROL REGISTER 1 – 0X770

Bit	R/W	Default	Description
7:6	R/W	0x0	MASK_SEL 00 = line 0 ~ line 13 mask & result control 01 = line 14 ~ line 27 mask & result control 10 = line 28 ~ line 41 mask & result control 11 = line 42 ~ line 53 mask & result control
5:4	R/W	0x0	BD_CELLSENS, blind cell sensitivity adjust 00 = 60% 01 = 70% 10 = 80% 11 = 90%
3:0	R/W	0x0	BD_LVSENS, Blind level sensitivity select

MOTION DETECTION CONTROL REGISTER 2 – 0X771

Bit	R/W	Default	Description
7:4	R/W	0x0	ND_LVSENS, night detection level sensitivity adjust
3:0	R/W	0x0	ND_TMPSENS, night detection temporal sensitivity adjust

MOTION DETECTION CONTROL REGISTER 3 – 0X772

Bit	R/W	Default	Description
7:6	R/W	0x0	MD_FIELD, motion detection field select
5	R/W	0x0	MD_DIS, channel disable, 1 = disable
4:0	R/W	0x0	MD_LVSENS, motion detection level sensitivity adjust

MOTION DETECTION CONTROL REGISTER 4 – 0X773

Bit	R/W	Default	Description
7:6	R/W	0x0	HD mode 0x = 720p 10 = 1080i 11 = 1080p
5	R/W	0x0	MD_REFFLD, Reference Field Update Mode 0 : Update Every Field, 1 : Update Every MD_SPEED Period
4:0	R/W	0x0	MD_SPEED, temporal sensitivity adjust

MOTION DETECTION CONTROL REGISTER 6 – 0X774

Bit	R/W	Default	Description
7:4	R/W	0x0	**MD_SPSENS,** motion spatial sensitivity adjust
3	R/W	0x0	**MD_VINV,** motion detection display mode, 1 = vertical invert
2	R/W	0x0	**MD_HINV,** motion detection display mode, 1 = horizontal invert
1	R/W	0x0	**MD_STRB,** internal user strobe signal
0	R/W	0x0	**MD_STRB_EN** 0 = automatic mode 1 = internal strobe mode

MOTION DETECTION CONTROL REGISTER 5 – 0X775

Bit	R/W	Default	Description
7:4	R/W	-	**Reserve**
3:0	R/W	0x0	**MD_TMPSENS,** motion detection temporal sensitivity adjust

MOTION DETECTION CELL LINE 0/14/28/42 RESULT REGISTER 1 – 0X780

Bit	R/W	Default	Description
7:0	R	0x0	md_det0[7:0]

This is for channel 0. channel 1 : 0x4FF[1:0] = 1, channel 2 : 0x4FF[1:0] = 2, channel 3 : 0x4FF[1:0] = 3

line 0 : 0x770[7:6] = 0, line 14 : 0x770[7:6] = 1, line 28 : 0x770[7:6] = 2, line 42 : 0x770[7:6] = 3

MOTION DETECTION CELL LINE 0/14/28/42 RESULT REGISTER 2 – 0X781

Bit	R/W	Default	Description
7:0	R	0x0	md_det0[15:8]

MOTION DETECTION CELL LINE 0/14/28/42 RESULT REGISTER 3 – 0X782

Bit	R/W	Default	Description
7:0	R	0x0	md_det0[23:16]

MOTION DETECTION CELL LINE 0/14/28/42 RESULT REGISTER 4 – 0X783

Bit	R/W	Default	Description
7:0	R	0x0	md_det0[31:24]

MOTION DETECTION CELL LINE 0/14/28/42 RESULT REGISTER 5 – 0X784

Bit	R/W	Default	Description
7:0	R	0x0	md_det0[39:32]

MOTION DETECTION CELL LINE 0/14/28/42 RESULT REGISTER 6 – 0X785

Bit	R/W	Default	Description
7:0	R	0x0	md_det0[47:40]

MOTION DETECTION CELL LINE 0/14/28/42 RESULT REGISTER 7 – 0X786

Bit	R/W	Default	Description
7:0	R	0x0	md_det0[55:48]

MOTION DETECTION CELL LINE 0/14/28/42 RESULT REGISTER 8 – 0X787

Bit	R/W	Default	Description
7:0	R	0x0	md_det0[59:56]

Similar registers are assigned to control line 1 to 53 using register 0x788 – 0x7EF respectively.

Channel ID Encoder Unit

Channel ID Encoder

The video output sequences from each of the TW2828 output port have critical system information embedded in the VBI area called channel ID. This information is very useful for the people who try to capture and utilize the video sequence later on. TW2828 supports three kinds of channel ID: User channel ID, Detection channel ID and Auto channel ID. The output order of these IDs in a TW2828 generated video sequence is fixed as Auto -> Repeat Auto(only in analog format) -> Detection -> User Channel ID. Definitions of each channel ID are described in detailed in the following sections. Each channel ID unit for each output port can be enabled and disabled independently. The Channel ID Format of TW2828 is very similar to TW2835, but total amount of data increase a little bit.

Channel ID Definition

AUTO CHANNEL ID

TW2828's Auto channel ID is 5 bytes long and is used for automatic identification of picture configuration such as video input path number, analog switch, event, region enable, field/frame mode information and CIF channel info. The ID information will repeat once.

TYPE	BIT	NAME	FUNCTION
Auto Channel ID	[39:38]	ID_TYPE	2'b00 = Auto Channel ID
	[37:36]	LINE_NUM	Line Number : 0 : 1st Line, 1 : 2nd Line (auto repeat)
	[35]	F_OUT	Encoder Field Polarity. 0 : Odd, 1 : Even
	[34:32]	Record port	3 – 7 = Port 9(value 3), Port 5(value 4) – Port 8(value 7)
	[31:28]	CH_NUM1	1/4 Quadrant Channel Number
	[27:24]	CH_NUM2	2/4 Quadrant Channel Number
	[23:20]	CH_NUM3	3/4 Quadrant Channel Number
	[19:16]	CH_NUM4	4/4 Quadrant Channel Number
	[15]	Interleave	0: Frame, 1: Field
	[14]	Interlace	In frame interleave, 0: Progressive, 1: Interlaced. In field interleave, 0: non field switch, 1: field switch
	[13:12]	Resolution	0 : Full D1, 1 : CIF, 2 : 4D1, 3 : BT1120
	[11]	H_SPLIT	0: no split, 1: split
	[10]	V_SPLIT	0: no split, 1: split
	[9]	FLD_MODE	0: top field is 0, 1: top field is 1
	[8]	-	0: [7:4] use for no video, 1: [7:4] is used for ignored bit
	[7:0]	DET_INFO	[7]: No video or ignored function for 1/4 quadrant channel [6]: No video or ignored function for 2/4 quadrant channel [5]: No video or ignored function for 3/4 quadrant channel [4]: No video or ignored function for 4/4 quadrant channel [3]: Blind for 1/4 quadrant channel [2]: Blind for 2/4 quadrant channel [1]: Blind for 3/4 quadrant channel [0]: Blind for 4/4 quadrant channel

DETECTION CHANNEL ID

Detection channel ID is composed of 40 byte data (8 lines) and is used for real time detected information such as motion, video loss, blind and night detection.

TYPE	BIT	NAME	FUNCTION
Detection Channel ID	[39:38]	ID_TYPE	Detection Channel ID = 2'b10
	[37:36]	LINE_NUM	Line Number : 0 : 1st Line, 1 : 2nd Line
	[35]	F_OUT	Encoder Field Polarity. 0 : Odd, 1 : Even
	[34:32]	Record port	3 – 7 = Port 9(value 3), Port 5(value 4) – Port 8(value 7)
	[31:0]	DET_INFO	[31:28] : 0/8 Ch DET_INFO (two lines) ~~ [03:00] : 7/15 Ch DET_INFO DET_INFO[3] : Video Loss Information DET_INFO[2] : Motion Information DET_INFO[1] : Blind Information DET_INFO[0] : Night Information

196-bit motion detection information is also included in Detection channel ID, total is 24 bytes (6 lines). Two lines use ID_TYPE 2'b10, the rest four lines use ID_TYPE 2'b01;

TYPE	BIT	NAME	FUNCTION
Detection Channel ID	[39:38]	ID_TYPE	Motion Detection Channel ID = 2'b10 (shared)
	[37:36]	LINE_NUM	Line Number : 2 : 3rd Line, 3 : 4th Line
	[35:32]	MD_SEL	Which channel is shown on 192 bits.
	[31:0]	DET_INFO	Line2: MD_DET[191:160] : Motion Detection Info Line3: MD_DET[159:128] : Motion Detection Info

TYPE	BIT	NAME	FUNCTION
Detection Channel ID	[39:38]	ID_TYPE	Motion Detection Channel ID = 2'b01
	[37:36]	LINE_NUM	Line Number : 0 : 5 th Line, 1 : 6th Line, 2 : 7th line, 3 : 8th line
	[35:32]	MD_SEL	Which channel is shown on 192 bits.
	[31:0]	DET_INFO	Line 0: MD_DET[127:96] : Motion Detection Info Line 1: MD_DET[95:64] : Motion Detection Info Line 2: MD_DET[63: 32] : Motion Detection Info Line 3: MD_DET[31:0] : Motion Detection Info

192 bit motion information is only for one channel. Each channel is divided by 16x12=192 windows. Each bit indicates 1 window motion status. To select different channel motion data, configure register MOTION_SEL.

USER CHANNEL ID

User Channel ID is composed of 15 bytes data (three lines) and is used for indicating customized information such as system information and date.

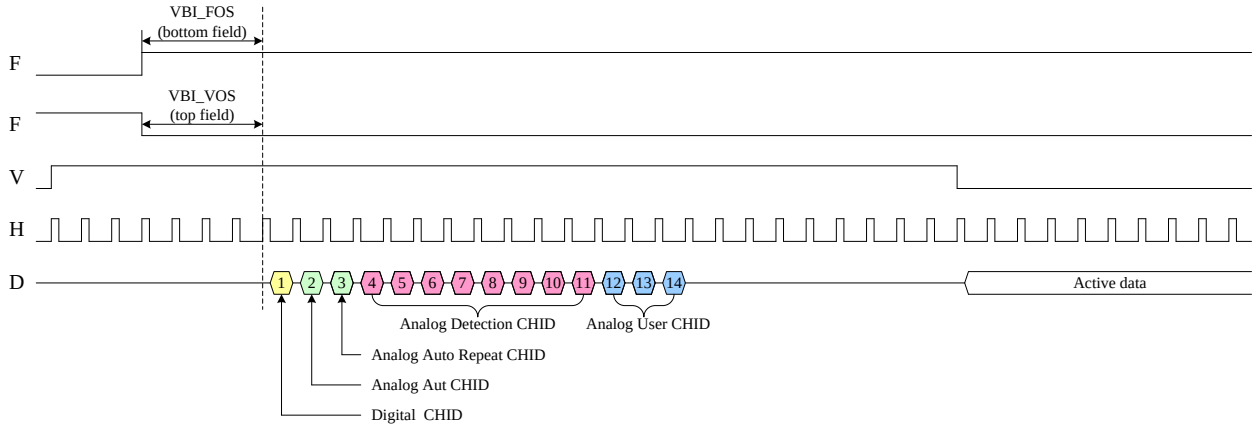
TYPE	BIT	NAME	FUNCTION
User Channel ID	[39:38]	ID_TYPE	2'b11 = User Channel ID
	[37:36]	LINE_NUM	Line Number : 0 : 1st Line, 1 : 2nd Line, 2 : 3rd Line
	[35]	F_OUT	Encoder Field Polarity. 0 : Odd, 1 : Even
	[34:32]	Record port	3 – 7 = Port 9(value 3), Port 5(value 4) – Port 8(value 7)
	[31:0]	MAN_ID	[31:0] : Manual User ID

Channel ID Output Method

TW2828 has two ways of transmitting channel ID: analog type channel ID and digital type channel ID. There are totally 14 lines channel ID data, which include 1 line of digital channel ID and 13 lines of analog channel ID. In analog channel ID, there are 1 line of auto channel ID, 1 line repeat auto channel ID, 8 lines of detection channel ID and 3 lines of user channel ID.

1	Digital channel ID
2	Analog auto channel ID
3	Analog auto repeat channel ID
4	Analog detection channel ID 1
5	Analog detection channel ID 2
6	Analog detection channel ID 3
7	Analog detection channel ID 4
8	Analog detection channel ID 5
9	Analog detection channel ID 6
10	Analog detection channel ID 7
11	Analog detection channel ID 8
12	Analog user channel ID 1
13	Analog user channel ID 2
14	Analog user channel ID 3

CHANNEL ID LINE NUMBER



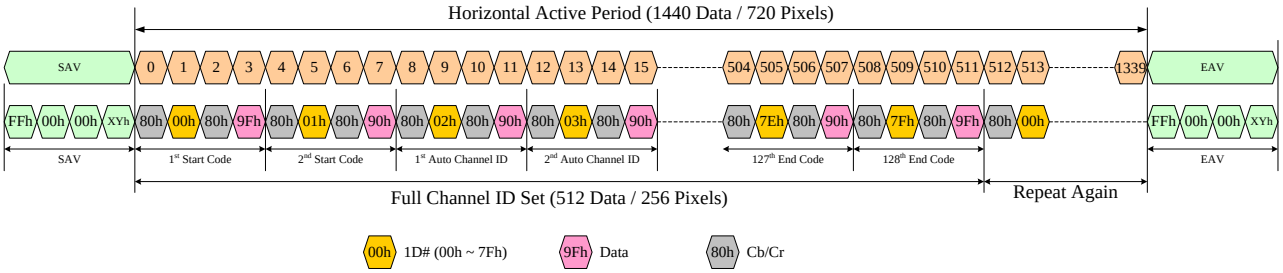
TIMING DIAGRAM OF CHANNEL ID

DIGITAL CHANNEL ID

TW2828 provides the digital type channel ID during VBI period. It's useful for DSP application because the channel ID can be inserted in just one line with special format. The digital channel ID is located before analog channel ID line. The digital channel ID can be enabled via the VIS_CODE_EN register.

The digital channel ID is inserted in Y data in BT.656 or BT1120 stream and composed of ID # and channel information. The ID # indicates the index of digital type channel ID including the start code, auto/detection/user channel ID and end code. The ID number has 0 ~ 0x7F index and each channel information of one byte is divided into 2 bytes of 4 LSB that takes "0x90" offset against ID # for discrimination. The start code is located in ID# 0 ~1 and auto channel ID is situated in ID # 2 ~ 11. The detection channel ID is located in ID # 12 ~ 91 and the user channel ID is situated in ID # 92 ~ 121. The end codes occupied the others. The digital channel ID will be repeated during horizontal active period. There is no repeat auto channel ID in digital format. The following figure shows the illustration of digital channel ID.

In the TW2828 output sequence, the vertical offset of odd field is controlled by the VIS_LINE_VOS register with 1 line unit and even field is control by the VIS_LINE_FOS register with 1 line unit. Channel ID can be flexibly enabled by register VIS_ID_OEN and VIS_ID_EEN for odd field and even field respectively. These registers make it possible to insert channel ID in vertical active region if user required.



DIGITAL CHANNEL ID TIMING DIAGRAM

1D#	DATA	DESCRIPTION
0 (00h)	9Fh	Start Code
1 (01h)	90h	
2 (02h)	{9, A0_MSB}	Auto Channel ID (5x2=10 bytes)
3 (03h)	{9, A0_LSB}	
...	...	
10 (0Ah)	{9, A4_MSB}	
11 (0Bh)	{9, A4_LSB}	
12 (0Ch)	{9, D0_MSB}	Detection Channel ID (40x2=80) bytes
13 (0Dh)	{9, D0_LSB}	
...	...	
90 (5Ah)	{9, D39_MSB}	
91 (5Bh)	{9, D39_LSB}	
92 (5Ch)	{9, U0_MSB}	User Channel ID (15x2=30 bytes)
93 (5Dh)	{9, U0_LSB}	
...	...	
120 (78h)	{9, D14_MSB}	
121 (79h)	{9, D14_LSB}	
122 (7Ah)	90h	End Code
123 (7Bh)	9Fh	
124 (7Ch)	90h	End Code
125 (7Dh)	9Fh	
126 (7Eh)	90h	End Code
127 (7Fh)	9Fh	

DIGITAL CHANNEL ID DATA FORMAT

Digital channel ID data sequence is: Cb, ID#, Cr, 9Xh, Cb ID#, Cr, 9Xh, ... After one full set, same data must be repeated in active area.

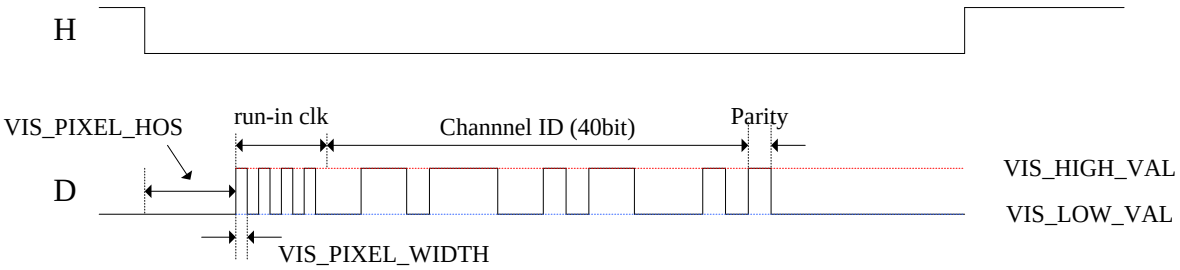
ANALOG CHANNEL ID

TW2828 supports analog type channel ID during VBI period. The analog channel ID can include an Auto channel ID, Repeat auto channel ID, Detection channel ID and User channel ID. Each channel ID can be enabled via the VIS_AUTO_EN, AUTO_RPT_EN, VIS_DET_EN, VIS_USER_EN registers. Auto channel ID requires one line basically, but can need one more line for repetition. Detection channel ID requires 8 lines and User channel ID require three lines so that total thirteen lines are used for analog type channel ID.

Analog channel ID is located right after digital channel ID line. Default starting position is right after SAV. The horizontal starting position offset is defined via VIS_PIXEL_HOS register with 1 pixel unit for data insertion and run in clock. The vertical start point is defined via VIS_VOS for odd field and VIS_FOS is for even field in one line offset. The pixel width of each bit is controlled by the VIS_PIXEL_WIDTH register and the magnitude of each bit is defined by the VIS_HIGH_VAL and VIS_LOW_VAL register.

The analog channel ID consists of run-in clock, channel ID data, type and parity bit. The run-in clock insertion is enabled via the VIS_RIC_EN register. There are four run in clock cycles. The channel ID data can include 4 byte

information and the channel ID type contains 2 bits that “0” is meant for Auto channel ID and repeated channel ID, “2” and “4” for Detection channel ID, “3” for User channel ID of VIS_MAN0~5. The parity is 1 bit width and used for even parity. This definition is used for both digital and analog channel ID. There are five bytes plus 1 parity data in one line.



ANALOG CHANNEL ID FORMAT

In each line of analog channel ID, there are 4 run in clock cycle, 40 channel ID data cycle and 1 parity cycle. Each cycle has “VIS_PIXEL_WIDTH x 2” pixels. Analog channel ID is only located in Y position.

Channel ID in Active Region

For CODECs that do not have the capability or bandwidth to process channel ID in the vertical blanking period, TW2828 also provides a simple way to let the channels to identify themselves. The kind of channel ID is stored in the active video area in a way that is robust against horizontal and vertical scaling. To insert the channel ID, each channel will have a 2x2 luma pixel slot in the first two lines in the active region for each field. In this slot the luma value is substituted to 0x01 or the value stored in the register 0xDAF. Take next diagram for example, channel 0 will have luma pixels Y0 and Y1, channel 1 will have luma pixels Y2 and Y3, channel 2 will have luma pixels Y4 and Y5 change to 0x01 for the first two lines.

Line 0

FF	00	00	SAV	CB0	Y0	CR0	Y1	CB1	Y2	CR1	Y3	CB2	Y4	CR2	Y5

Line 1

FF	00	00	SAV	CB0	Y0	CR0	Y1	CB1	Y2	CR1	Y3	CB2	Y4	CR2	Y5

The CODEC's firmware should recover the channel ID and replaced with a interpolated value from the adjacent pixels to minimize the impact. Next diagram illustrate the output for channel 0.

Line 0

FF	00	00	SAV	CB0	01	CR0	01	CB1	Y2	CR1	Y3	CB2	Y4	CR2	Y5

Line 1

FF	00	00	SAV	CB0	01	CR0	01	CB1	Y2	CR1	Y3	CB2	Y4	CR2	Y5

The substitution rule basically stay the same for 16 bit output. In this configuration, two adjacent luma pixels will get replaced while the chroma section is untouched. Registers 0xDAD and 0xDAE is used for limit the active channel ID only appears in the first frame of a output sequence. This is useful for the customers that already knows the output sequence of the incoming video and only want TW2828 to help identifying the first channel.

Registers Table

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xD48	R/W	0x07	[7]: FLDMODE_PB5 [6]: INVALID_MD_PB5 [5:3]: VIN_SEL_PB5 [2:0]: VIS_PIXEL_WIDTH_PB5
0xD49	R/W	0xFF	[7]: VIS_ID_OEN_PB5 [6]: VIS_AUTO_EN_PB5 [5]: VIS_RPT_EN_PB5 [4]: VIS_DET_EN_PB5 [3]: VIS_USER_EN_PB5 [2]: VIS_CODE_EN_PB5 [1]: VIS_RIC_PB5 [0]: VIS_ID_EEN_PB5
0xD4A	R/W	0x00	VIS_HOS_PB5[7:0]
0xD4B	R/W	0x3F	VIS_HIGH_VAL_PB5[7:0]
0xD4C	R/W	0x05	VIS_LOW_VAL_PB5[7:0]
0xD4D	R/W	0x00	[4:0]: VIS_VOS_PB5
0xD4E	R/W	0x00	[7:0]: VIS_MAN0_PB5_L
0xD4F	R/W	0x00	[7:0]: VIS_MAN0_PB5_H
0xD50	R/W	0x00	[7:0]: VIS_MAN1_PB5_L
0xD51	R/W	0x00	[7:0]: VIS_MAN1_PB5_H
0xD52	R/W	0x00	[7:0]: VIS_MAN2_PB5_L
0xD53	R/W	0x00	[7:0]: VIS_MAN2_PB5_H
0xD54	R/W	0x00	[7:0]: VIS_MAN3_PB5_L
0xD55	R/W	0x00	[7:0]: VIS_MAN3_PB5_H
0xD56	R/W	0x00	[7:0]: VIS_MAN4_PB5_L
0xD57	R/W	0x00	[7:0]: VIS_MAN4_PB5_H
0xD58	R/W	0x00	[7:0]: VIS_MAN5_PB5_L
0xD59	R/W	0x00	[7:0]: VIS_MAN5_PB5_H
0xD5A	R/W	0x07	[7]: FLDMODE_PB6 [6]: INVALID_MD_PB6 [5:3]: VIN_SEL_PB6 [2:0]: VIS_PIXEL_WIDTH_PB6
0xD5B	R/W	0xFF	[7]: VIS_ID_OEN_PB6 [6]: VIS_AUTO_EN_PB6 [5]: VIS_RPT_EN_PB6 [4]: VIS_DET_EN_PB6 [3]: VIS_USER_EN_PB6 [2]: VIS_CODE_EN_PB6 [1]: VIS_RIC_PB6 [0]: VIS_ID_EEN_PB6
0xD5C	R/W	0x00	VIS_HOS_PB6[7:0]
0xD5D	R/W	0x3F	VIS_HIGH_VAL_PB6[7:0]
0xD5E	R/W	0x05	VIS_LOW_VAL_PB6[7:0]
0xD5F	R/W	0x00	[4:0]: VIS_VOS_PB6
0xD60	R/W	0x00	[7:0]: VIS_MAN0_PB6_L
0xD61	R/W	0x00	[7:0]: VIS_MAN0_PB6_H
0xD62	R/W	0x00	[7:0]: VIS_MAN1_PB6_L
0xD63	R/W	0x00	[7:0]: VIS_MAN1_PB6_H
0xD64	R/W	0x00	[7:0]: VIS_MAN2_PB6_L
0xD65	R/W	0x00	[7:0]: VIS_MAN2_PB6_H
0xD66	R/W	0x00	[7:0]: VIS_MAN3_PB6_L
0xD67	R/W	0x00	[7:0]: VIS_MAN3_PB6_H
0xD68	R/W	0x00	[7:0]: VIS_MAN4_PB6_L

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xD69	R/W	0x00	[7:0]: VIS_MAN4_PB6_H
0xD6A	R/W	0x00	[7:0]: VIS_MAN5_PB6_L
0xD6B	R/W	0x00	[7:0]: VIS_MAN5_PB6_H
0xD6C	R/W	0x07	[7]: FLDMODE_PB7 [6]: INVALID_MD_PB7 [5:3]: VIN_SEL_PB7 [2:0]: VIS_PIXEL_WIDTH_PB7
0xD6D	R/W	0xFF	[7]: VIS_ID_OEN_PB7 [6]: VIS_AUTO_EN_PB7 [5]: VIS_RPT_EN_PB7 [4]: VIS_DET_EN_PB7 [3]: VIS_USER_EN_PB7 [2]: VIS_CODE_EN_PB7 [1]: VIS_RIC_PB7 [0]: VIS_ID_EEN_PB7
0xD6E	R/W	0x00	VIS_HOS_PB7[7:0]
0xD6F	R/W	0x3F	VIS_HIGH_VAL_PB7[7:0]
0xD70	R/W	0x05	VIS_LOW_VAL_PB7[7:0]
0xD71	R/W	0x00	[4:0]: VIS_VOS_PB7
0xD72	R/W	0x00	[7:0]: VIS_MAN0_PB7_L
0xD73	R/W	0x00	[7:0]: VIS_MAN0_PB7_H
0xD74	R/W	0x00	[7:0]: VIS_MAN1_PB7_L
0xD75	R/W	0x00	[7:0]: VIS_MAN1_PB7_H
0xD76	R/W	0x00	[7:0]: VIS_MAN2_PB7_L
0xD77	R/W	0x00	[7:0]: VIS_MAN2_PB7_H
0xD78	R/W	0x00	[7:0]: VIS_MAN3_PB7_L
0xD79	R/W	0x00	[7:0]: VIS_MAN3_PB7_H
0xD7A	R/W	0x00	[7:0]: VIS_MAN4_PB7_L
0xD7B	R/W	0x00	[7:0]: VIS_MAN4_PB7_H
0xD7C	R/W	0x00	[7:0]: VIS_MAN5_PB7_L
0xD7D	R/W	0x00	[7:0]: VIS_MAN5_PB7_H
0xD7E	R/W	0x07	[7]: FLDMODE_PB8 [6]: INVALID_MD_PB8 [5:3]: VIN_SEL_PB8 [2:0]: VIS_PIXEL_WIDTH_PB8
0xD7F	R/W	0xFF	[7]: VIS_ID_OEN_PB8 [6]: VIS_AUTO_EN_PB8 [5]: VIS_RPT_EN_PB8 [4]: VIS_DET_EN_PB8 [3]: VIS_USER_EN_PB8 [2]: VIS_CODE_EN_PB8 [1]: VIS_RIC_PB8 [0]: VIS_ID_EEN_PB8
0xD80	R/W	0x00	VIS_HOS_PB8[7:0]
0xD81	R/W	0x3F	VIS_HIGH_VAL_PB8[7:0]
0xD82	R/W	0x05	VIS_LOW_VAL_PB8[7:0]
0xD83	R/W	0x00	[4:0]: VIS_VOS_PB8
0xD84	R/W	0x00	[7:0]: VIS_MAN0_PB8_L
0xD85	R/W	0x00	[7:0]: VIS_MAN0_PB8_H
0xD86	R/W	0x00	[7:0]: VIS_MAN1_PB8_L
0xD87	R/W	0x00	[7:0]: VIS_MAN1_PB8_H
0xD88	R/W	0x00	[7:0]: VIS_MAN2_PB8_L
0xD89	R/W	0x00	[7:0]: VIS_MAN2_PB8_H
0xD8A	R/W	0x00	[7:0]: VIS_MAN3_PB8_L
0xD8B	R/W	0x00	[7:0]: VIS_MAN3_PB8_H

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xD8C	R/W	0x00	[7:0]: VIS_MAN4_PB8_L
0xD8D	R/W	0x00	[7:0]: VIS_MAN4_PB8_H
0xD8E	R/W	0x00	[7:0]: VIS_MAN5_PB8_L
0xD8F	R/W	0x00	[7:0]: VIS_MAN5_PB8_H
0xD94	R/W	0x00	[4:0]: VIS_FOS_PB5
0xD95	R/W	0x00	[4:0]: VIS_FOS_PB6
0xD96	R/W	0x00	[4:0]: VIS_FOS_PB7
0xD97	R/W	0x00	[4:0]: VIS_FOS_PB8
0xD98	R/W	0x07	[7]: FLDMODE_PB9 [6]: INVALID_MD_PB9 [5:3]: VIN_SEL_PB9 [2:0]: VIS_PIXEL_WIDTH_PB9
0xD99	R/W	0xFF	[7]: VIS_ID_OEN_PB9 [6]: VIS_AUTO_EN_PB9 [5]: VIS_RPT_EN_PB9 [4]: VIS_DET_EN_PB9 [3]: VIS_USER_EN_PB9 [2]: VIS_CODE_EN_PB9 [1]: VIS_RIC_PB9 [0]: VIS_ID_EEN_PB9
0xD9A	R/W	0x00	VIS_HOS_PB9[7:0]
0xD9B	R/W	0x3F	VIS_HIGH_VAL_PB9[7:0]
0xD9C	R/W	0x05	VIS_LOW_VAL_PB9[7:0]
0xD9D	R/W	0x00	[4:0]: VIS_VOS_PB9
0xD9E	R/W	0x00	[7:0]: VIS_MAN0_PB9_L
0xD9F	R/W	0x00	[7:0]: VIS_MAN0_PB9_H
0xDA0	R/W	0x00	[7:0]: VIS_MAN1_PB9_L
0xDA1	R/W	0x00	[7:0]: VIS_MAN1_PB9_H
0xDA2	R/W	0x00	[7:0]: VIS_MAN2_PB9_L
0xDA3	R/W	0x00	[7:0]: VIS_MAN2_PB9_H
0xDA4	R/W	0x00	[7:0]: VIS_MAN3_PB9_L
0xDA5	R/W	0x00	[7:0]: VIS_MAN3_PB9_H
0xDA6	R/W	0x00	[7:0]: VIS_MAN4_PB9_L
0xDA7	R/W	0x00	[7:0]: VIS_MAN4_PB9_H
0xDA8	R/W	0x00	[7:0]: VIS_MAN5_PB9_L
0xDA9	R/W	0x00	[7:0]: VIS_MAN5_PB9_H
0xDAA	R/W	0x00	[4:0]: VIS_FOS_PB9
0xDAB	R/W	0x00	[7]: ACTIVE_chid_EN_PB8 [6]: ACTIVE_chid_EN_PB7 [5]: ACTIVE_chid_EN_PB6 [4]: ACTIVE_chid_EN_PB5 [3]: ACTIVE_chid_EN_PB4 [2]: ACTIVE_chid_EN_PB3 [1]: ACTIVE_chid_EN_PB2 [0]: ACTIVE_chid_EN_PB1
0xDAC	R/W	0x00	[0]: ACTIVE_chid_EN_PB9
0xDAD	R/W	0x00	[7]: FIRST_FRAME_EN_P8 [6]: FIRST_FRAME_EN_P7 [5]: FIRST_FRAME_EN_P6 [4]: FIRST_FRAME_EN_P5 [3]: FIRST_FRAME_EN_P4 [2]: FIRST_FRAME_EN_P3 [1]: FIRST_FRAME_EN_P2 [0]: FIRST_FRAME_EN_P1
0xDAE	R/W	0x00	[0]: FIRST_FRAME_EN_P9

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xDAF	R/W	0x01	[0]: ACTIVE_CHID
0xDB2	R/W	0x00	[7:4]: MOTION_SEL_6 [3:0]: MOTION_SEL_5
0xDB3	R/W	0x00	[7:4]: MOTION_SEL_8 [3:0]: MOTION_SEL_7
0xDB4	R/W	0x00	[3:0]: MOTION_SEL_9
0xDB5	R/W	0x00	FLD_SEL[7:0]
0xDB6	R/W	0x00	FLD_SEL[8]

Register Descriptions

PB5 CHANNEL ID ENC MISC REGISTER – 0XD48

Bit	R/W	Default	Description
7	RW	0	**FLDMODE_PB5:** Encoder field parity 1: 1 for top field 0: 0 for top field
6	RW	0	**INVALID_MD_PB5:** Invalid motion detection 1: enable. CHID enc generates 0 in V and H blanking. 0: disable. CHID enc generates 0x80/0x10 in V and H blanking
5:3	RW	0	**VIN_SEL_PB5:** Record port selection. 3: port9 4: port5 5: port6 6: port7 7: port8
2:0	RW	4	**VIS_PIXEL_WIDTH_PB5** Define analog CHID data sample rate. The value is half period of data period. Unit is 1 pixel.

PB5 CHANNEL ID ENC ENABLE REGISTER – 0XD49

Bit	R/W	Default	Description
7	RW	1	**VIS_ID_OEN_PB5:** Enable output of D CHID and A CHID in odd field 1: enable 0: disable
6	RW	1	**VIS_AUTO_EN_PB5:** Enable analog auto CHID encoding. 1: enable 0: disable
5	RW	1	**VIS_RPT_EN_PB5:** Enable analog auto repeat CHID encoding. 1: enable 0: disable
4	RW	1	**VIS_DET_EN_PB5:** Enable analog detection CHID encoding. 1: enable 0: disable
3	RW	1	**VIS_USER_EN_PB5:** Enable analog user CHID encoding. 1: enable 0: disable
2	RW	1	**VIS_CODE_EN_PB5:** Enable digital CHID encoding. 1: enable 0: disable
1	RW	1	**VIS_RIC_PB5:** Enable run in clock for analog CHID 1: enable 0: disable

Bit	R/W	Default	Description
0	RW	1	**VIS_ID_EEN_PB5:** Enable output of D CHID and A CHID in even field 1: enable 0: disable

PB5 CHANNEL ID ENC HORIZONTAL OFFSET REGISTER – 0XD4A

Bit	R/W	Default	Description
7:0	RW	0	**VIS_HOS_PB5** Horizontal offset for analog CHID in unit of pixel.

PB5 CHANNEL ID ENC HIGH VALUE REGISTER – 0XD4B

Bit	R/W	Default	Description
7:0	RW	3f	**VIS_HIGH_VAL_PB5** Define high value of analog CHID data bit if it is 1.

PB5 CHANNEL ID ENC LOW VALUE REGISTER – 0XD4C

Bit	R/W	Default	Description
7:0	RW	5	**VIS_LOW_VAL_PB5** Define low value of analog CHID data bit if it is 0.

PB5 ODD FIELD VERTICAL LINE OFFSET REGISTER – 0XD4D

Bit	R/W	Default	Description
4:0	RW	0	**VIS_VOS_PB5** Vertical offset of channel ID in odd field.

PB5 CHANNEL ID ENC MAN0 LSB REGISTER – 0XD4E

Bit	R/W	Default	Description
7:0	RW	0	**VIS_MAN0_PB5_L** User CHID.

PB5 CHANNEL ID ENC MAN0 MSB REGISTER – 0XD4F

Bit	R/W	Default	Description
7:0	RW	0	**VIS_MAN0_PB5_H** User CHID.

PB5 CHANNEL ID ENC MAN1 LSB REGISTER – 0XD50

	R/W	Default	Description
7:0	RW	0	VIS_MAN1_PB5_L User CHID.

PB5 CHANNEL ID ENC MAN1 SB REGISTER – 0XD51

Bit	R/W	Default	Description
7:0	RW	0	VIS_MAN1_PB5_H User CHID.

PB5 CHANNEL ID ENC MAN2 LSB REGISTER – 0XD52

Bit	R/W	Default	Description
7:0	RW	0	VIS_MAN2_PB5_L User CHID.

PB5 CHANNEL ID ENC MAN2 MSB REGISTER – 0XD53

Bit	R/W	Default	Description
7:0	RW	0	VIS_MAN2_PB5_H User CHID.

PB5 CHANNEL ID ENC MAN3 LSB REGISTER – 0XD54

Bit	R/W	Default	Description
7:0	RW	0	VIS_MAN3_PB5_L User CHID.

PB5 CHANNEL ID ENC MAN3 MSB REGISTER – 0XD55

Bit	R/W	Default	Description
7:0	RW	0	VIS_MAN3_PB5_H User CHID.

PB5 CHANNEL ID ENC MAN4 LSB REGISTER – 0XD56

Bit	R/W	Default	Description
7:0	RW	0	VIS_MAN4_PB5_L User CHID.

PB5 CHANNEL ID ENC MAN4 MSB REGISTER – 0XD57

Bit	R/W	Default	Description
7:0	RW	0	VIS_MAN4_PB5_H User CHID.

PB5 CHANNEL ID ENC MAN5 LSB REGISTER – 0XD58

Bit	R/W	Default	Description
7:0	RW	0	VIS_MAN5_PB5_L User CHID.

PB5 CHANNEL ID ENC MAN5 MSB REGISTER – 0XD59

Bit	R/W	Default	Description
7:0	RW	0	VIS_MAN5_PB5_H User CHID.

This is for record unit 5. For record unit 6 – 8, the assignments are: 0xD5A – 0xD8F, for unit 9, 0xD98 – 0xDAA

PB5 EVEN FIELD VERTICAL OFFSET REGISTER – 0XD94

Bit	R/W	Default	Description
4:0	RW	0	VIS_FOS_PB5 Vertical offset of channel ID in even field.

This is for record unit 5. For record unit 6 – 8, the assignments are: 0xD95 – 0xD97, for unit 9, 0xDAA

ACTIVE AREA CHANNEL ID ENABLE REGISTER 1 – 0XDAB

Bit	R/W	Default	Description
7:0	RW	0	ACTIVE_CHID_EN Simple channel ID in active area using “0x01” in first two lines [7]: ACTIVE_chid_EN_PB8 [6]: ACTIVE_chid_EN_PB7 [5]: ACTIVE_chid_EN_PB6 [4]: ACTIVE_chid_EN_PB5

ACTIVE AREA CHANNEL ID ENABLE REGISTER 2 – 0XDAC

Bit	R/W	Default	Description
0	RW	0	ACTIVE_CHID_EN Simple channel ID in active area using “0x01” in first two lines [0]: ACTIVE_chid_EN_PB9

ACTIVE AREA CHANNEL ID IN FIRST FRAME REGISTER 1 – 0XDAD

Bit	R/W	Default	Description
7:0	RW	0	FIRST_FRAME_EN Active Channel ID only in first frame. [7]: FIRST_FRAME_EN_P8 [6]: FIRST_FRAME_EN_P7 [5]: FIRST_FRAME_EN_P6 [4]: FIRST_FRAME_EN_P5

ACTIVE AREA CHANNEL ID IN FIRST FRAME REGISTER 2 – 0XDAE

Bit	R/W	Default	Description
7:0	RW	0	FIRST_FRAME_EN Active Channel ID only in first frame. [0]: FIRST_FRAME_EN_P9

ACTIVE AREA CHANNEL ID DATA REGISTER – 0XDAF

Bit	R/W	Default	Description
7:0	RW	0x01	ACTIVE_CHID Active Channel ID data. If the video data is same as active channel ID data, the LSB of video data will be inverted.

MOTION CHANNEL SELECTION REGISTER – 0XDB2

Bit	R/W	Default	Description
7:4	RW	0x00	MOTION_SEL_6 This register is used for which channel motion information will be shown in 192 bit motion channel ID. It's for read out port 6.
3:0	RW	0x00	MOTION_SEL_5 This register is used for which channel motion information will be shown in 192 bit motion channel ID. It's for read out port 5.

Register 0xDB3 to 0xDB4 are for port 2 to 9

FIELD SELECTION REGISTER – 0XDB5

Bit	R/W	Default	Description
7:4	RW	0x00	FLD_SEL[7:4] This register is used for field switch mode. They are for record port 5(bit 7) to 7(bit 4). 0: odd field 1: even field
3:0	RW	0x00	Reserved

FIELD SELECTION REGISTER – 0XDB6

Bit	R/W	Default	Description
0	RW	0x00	FLD_SEL[8] This register is used for field switch mode. It is for port 9. 0: odd field 1: even field

Recording and SPOT Unit

Introduction

Recording unit consists of 24 write agents and 5 read agents. Each write agent is capable of choosing camera number, recording resolution, recording format and location of the video information inside the DDR buffer. 8 write agents support only D1, half-D1 and CIF resolution. The other 16 write agents have pre-downscaler and support two more resolutions, QCIF and 1/3 D1 size. Recording unit shares DDR with display path and has bandwidth limitation. This unit supports up to 2-SPOT display and up to 4 recording ports. SPOT display supports D1, Quad, 9-CH and 16-QCIF display with NTSC and PAL format and supports channel rotation without rolling.

Functional Description

The block diagram of recording path is as below:

- Downscaler$_1$ unit is shared with display unit but is used with different outputs. For recording path, following fixed resolution outputs are available: D1, Half D1 and CIF.
- Live video stream are stored into proper places in the DDR memory buffer according to register setting. Simple Weave de-interlacing technique is used if frame interleaved format is specified.
- A buffer of 4 frames / 4 fields is used for storing video streams. This is needed to prevent video tearing. TW2828 has frame detection / repeat circuitry to ensure the proper read / write sequences.
- Channels with similar setup should group together to facilitate simple read out functions.
- Downscaler$_2$ unit makes QCIF or 1/3 D1 size image for 16-QCIF or 9-channel display
- There are four record outputs. Two ports share I/O pins with display BT.1120 output and the other two ports share I/O pins with GPIO for saving the number of I/O pin.

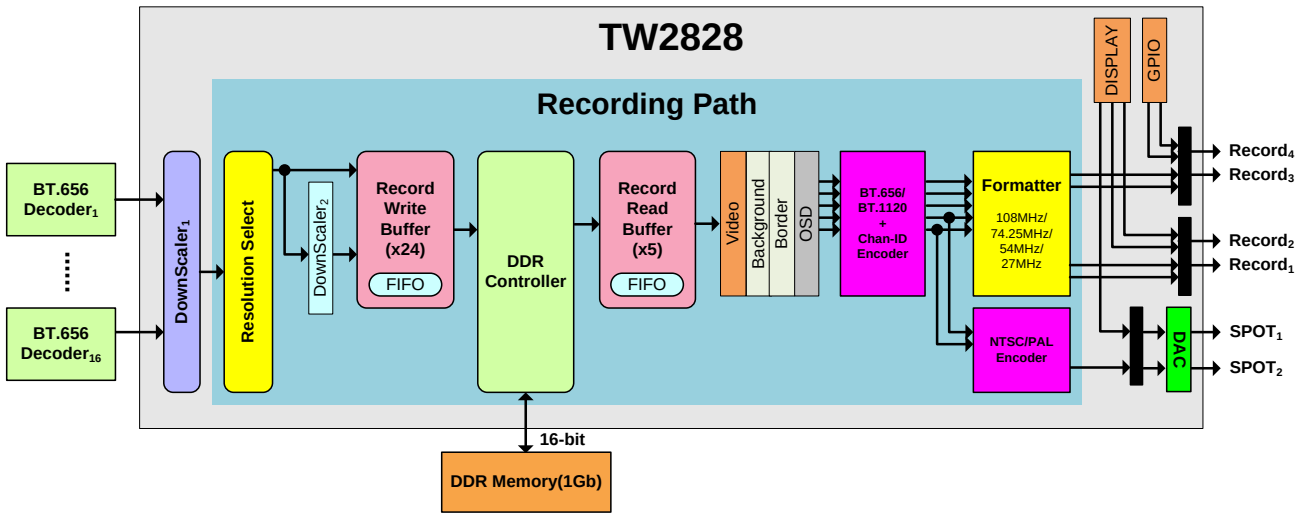


FIGURE 4. BLOCK DIAGRAM FOR RECORD OPERATION

Frame Buffer Positioning

TW2828 recording unit supports DDR2 memory with 1Gb or 512Mb densities and 16-bit data width.

Because record unit shares frame buffer with display, this unit needs to use any position of DDR memory. This function can be done by setting the following registers .

v_pos, h_pos

v_pos_offset, h_pos_offset

v_size, h_size

rec_pitch

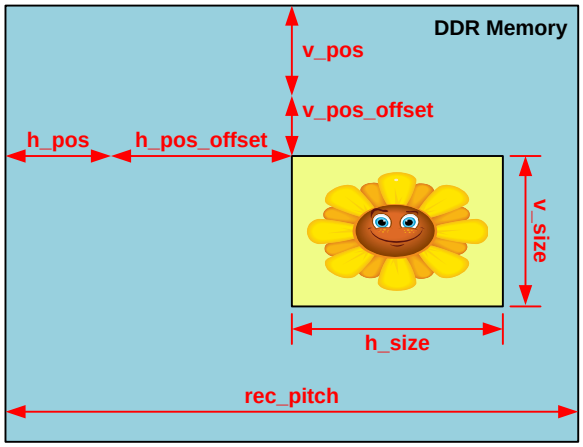


FIGURE 5. FRAME BUFFER POSITIONING BY SETTING REGISTER

There are two group of write buffers. One is record buffer and the other is SPOT buffer. Each group has its own 'v_pos' and 'h_pos' and record buffers and SPOT buffers can have a different start position. Each group also has a different offset of position.

Record write buffers can support only D1, QUAD and CIF resolution and have the following offset of position.

Line Number 6VGA	Line Number PAL	Line Number NTSC	Pixel Number 320	640	960	1280	1600	1920	2240	6VGA
			360	720	1080	1440	1800	2160	2520	D1, QUAD, CIF
135	144	120	(0,0)	(1,0)	(2,0)	(3,0)	(4,0)	(5,0)	(6,0)	(7,0)
270	288	240	(0,1)	(1,1)	(2,1)	(3,1)	(4,1)	(5,1)	(6,1)	(7,1)
405	432	360	(0,2)	(1,2)	(2,2)	(3,2)	(4,2)	(5,2)	(6,2)	(7,2)
540	576	480	(0,3)	(1,3)	(2,3)	(3,3)	(4,3)	(5,3)	(6,3)	(7,3)
675	720	600	(0,4)	(1,4)	(2,4)	(3,4)	(4,4)	(5,4)	(6,4)	(7,4)
810	864	720	(0,5)	(1,5)	(2,5)	(3,5)	(4,5)	(5,5)	(6,5)	(7,5)
945	1008	840	(0,6)	(1,6)	(2,6)	(3,6)	(4,6)	(5,6)	(6,6)	(7,6)
			(0,7)	(1,7)	(2,7)	(3,7)	(4,7)	(5,7)	(6,7)	(7,7)

(Horizontal Offset, Vertical Offset)

FIGURE 6. POSITION OFFSET OF RECORD WRITE BUFFERS

SPOT write buffers can support more resolutions, QCIF and 1/3 D1 and have the following offset of position.

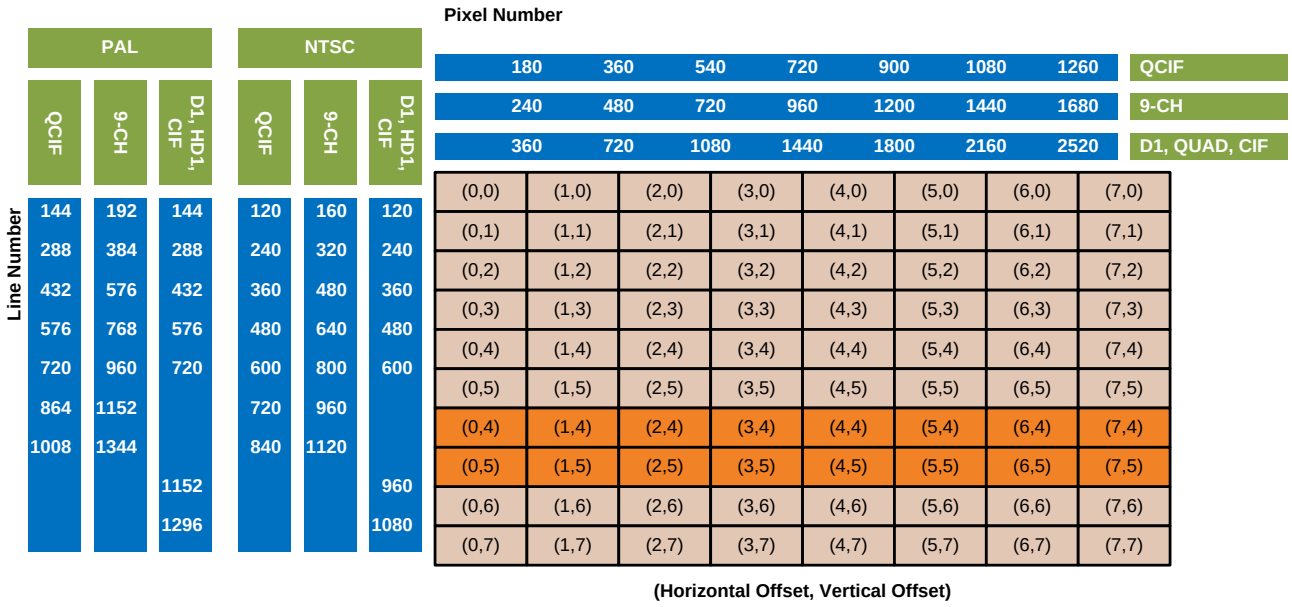


FIGURE 7. POSITION OFFSET OF SPOT WRITE BUFFERS

Frame Rate Control Unit

To prevent video tearing on the record output, 4 frames or 4 fields are used to control frame rate. Each write buffers can select their own read side bank reference from record read ports.

Record Channels Arrangement Example

Here are some memory allocation examples for TW2828.

16 D1 CHANNEL FRAME/FIELD INTERLEAVED REAL TIME OUTPUT

This mode is designed for newer high-end system as all 16 channels are output in D1 resolution. To output the video data to the CODEC, the read out unit can be configured at running at 108 MHz (four ports, frame/field interleaved). The following two figures (Figure 8 and Figure 9) show the examples of these configurations. In these examples, main display has 1920x1080 resolution and record uses next area of main display.

TWO SPOT DISPLAY OUTPUT

For two SPOT outputs, three D1 size buffers are needed. Two buffers are for current SPOT display and the other is for next SPOT display in case of rotation. Figure 10 is the example that supports one 16-QCIF display and one QUAD display and next display is QUAD.

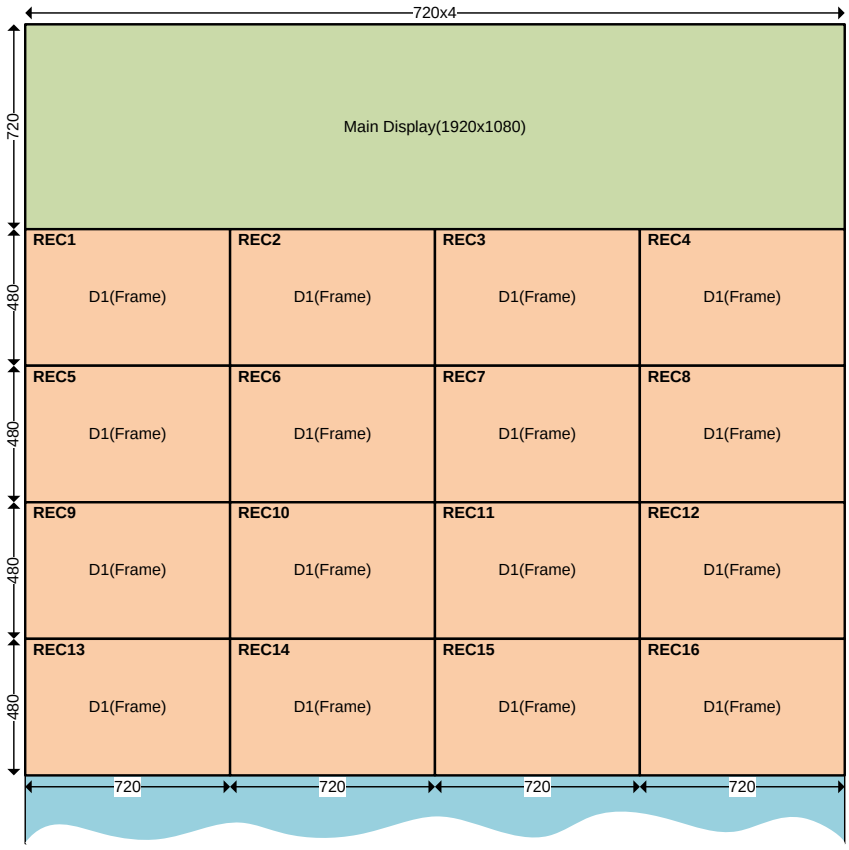


FIGURE 8. RECORDING CHANNEL ARRANGEMENT EXAMPLE OF 16 D1 FRAME INTERLEAVED REAL TIME RECORD

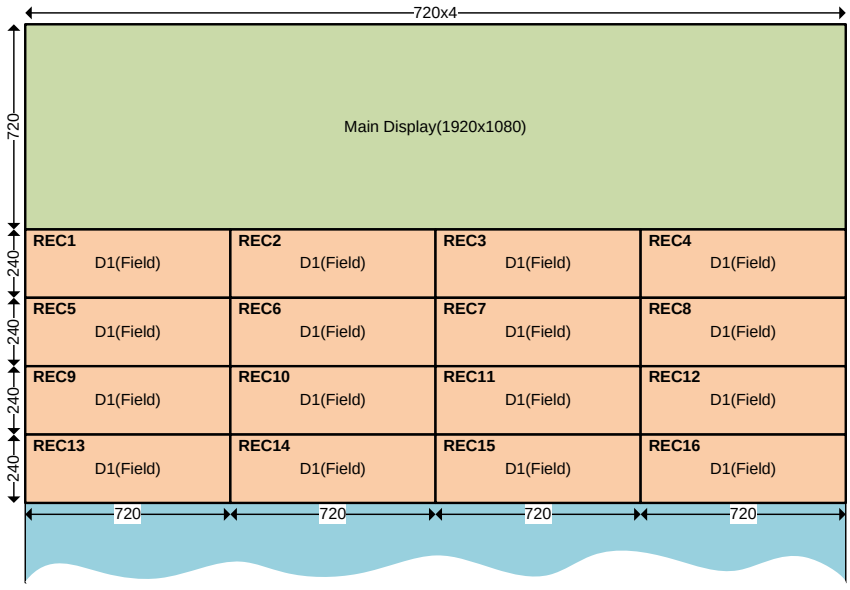


FIGURE 9. RECORDING CHANNEL ARRANGEMENT EXAMPLE OF 16 D1 FIELD INTERLEAVED REAL TIME RECORD

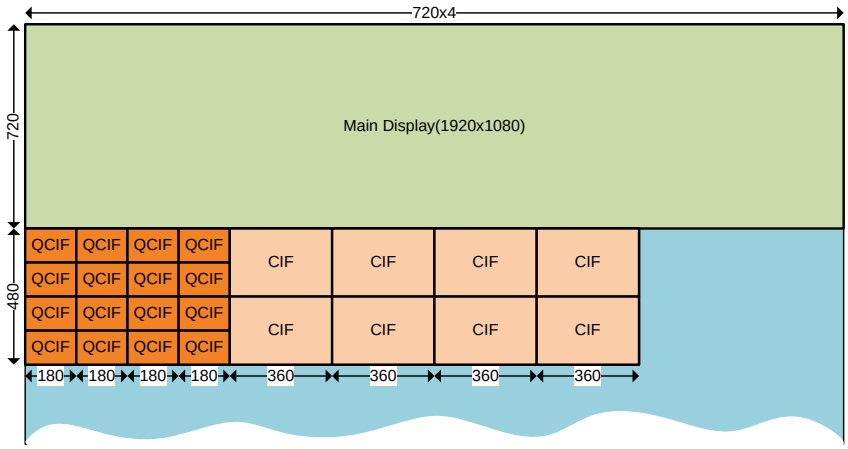


FIGURE 10. SPOT CHANNEL ARRANGEMENT EXAMPLE OF 16-QCIF AND QUAD DISPLAY

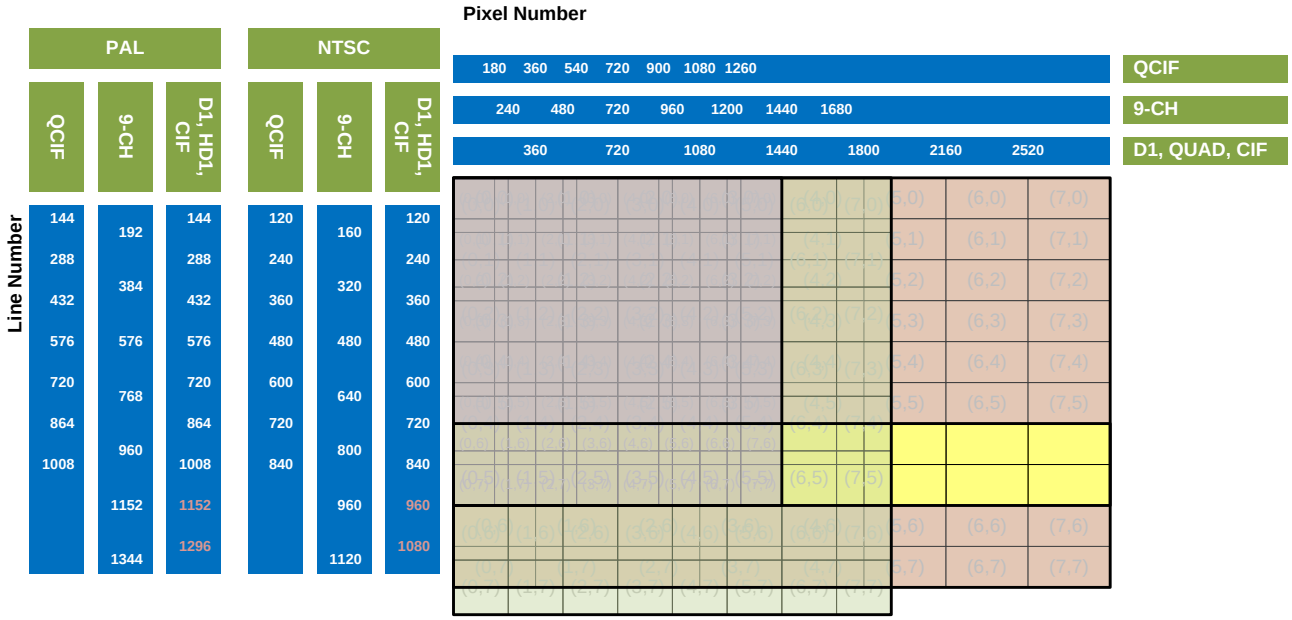


FIGURE 11. DETAILED POSITION OF DDR MAPPING FOR WRITE BUFFERS

RECORD POSTIONS IN DETAILED

The above diagram shows all kinds of possibilities in choosing channel positions. These positions are selected in recording/SPOT buffer control register B where the user selects a pre-determined horizontal and vertical position. Because there are too many possible locations to choose from so please refer to manual for actual settings. The offset within a channel is also possible. This is done by changing the starting positions of each channel (Xstart and Ystart). The Xsize and Ysize are determined by the output format. If the size is small than the recording format chosen, cropping will occur. The variable starting position is used to chop off unnecessary artifact in the beginning of the channel.

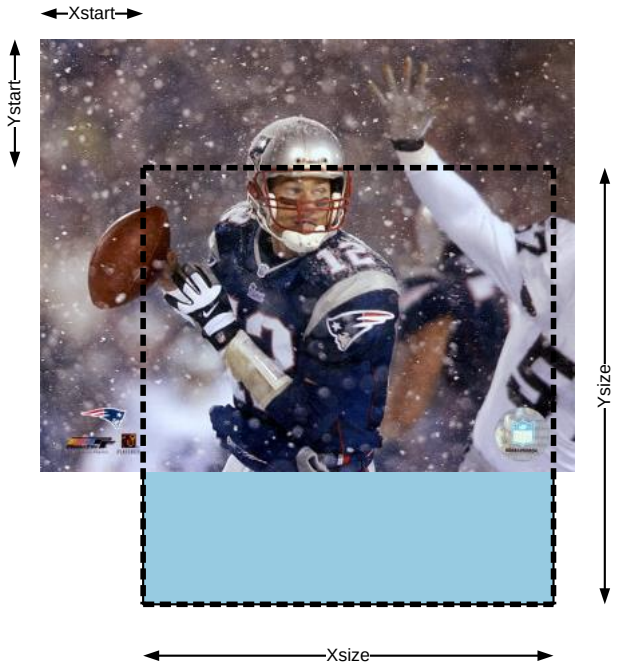


FIGURE 12. CHANNEL RECORD POSITION CONTROL

SPOT WRITE BUFFER

SPOT write buffers function the same way as recording buffer and support QCIF and 1/3 D1 resolution. SPOT write buffer can be used by recording unit as a possible input.

Recording unit

INTRODUCTION

TW2828 provides very powerful and versatile recording options and interfaces to the backend CODEC. The functions and output formats for each port are discussed in details in the subsequent sections. There are five regular output units shared four output pin ports and two SPOT outputs in TW2828. User can configure each port independently to run at different frequencies and output formats. However, due to the bandwidth limit, not all the output ports can run at the highest frequencies at the same time. These output ports have a flexible output option that even one frame per second for a certain channel is supported.

RECORD OUT FORMAT CONTROL

The basic output format of TW2828 is followed the BT.656 standard with EAV-HBI-SAV-ACTIVE style of coding. The D1 output sequence is illustrated in the next two figures. The differences between each output format lies in the number of bytes in each format and flags in the HBI area. In the subsequent sections, when we mention a field output or frame output, what we really meant is a series of EAV-HBI-SAV-ACTIVE lines shifting out follow these rules and output continuously to the outside world.

Several things determined the output video stream:

- Output frequency:Each port can be configured to run at 108, 54 or 27 MHz. Higher the frequency, higher the data rate and hence more channels supported.
- Output format: Three formats are supported, (1) Field interleaved. (2) Progressive Frame interleaved (3) Interlaced Frame interleaved
- Output resolution: Four resolutions are supported: D1, special CIF, 4D1, 720p and 1080i or 6VGA.
- Output channel selection: This will determine which channel will output from this channel. Because the channel format has been set in the recording side, this setting is actually adjusting the read out DRAM area and order.

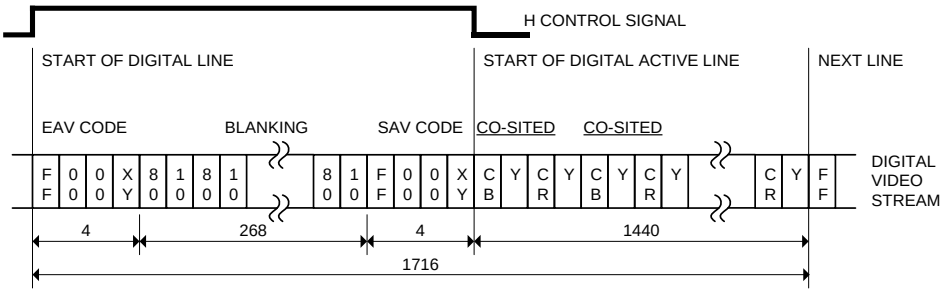


FIGURE 13. BT.656 8-BIT PARALLEL INTERFACE DATA FORMAT FOR 525/60 VIDEO SYSTEMS

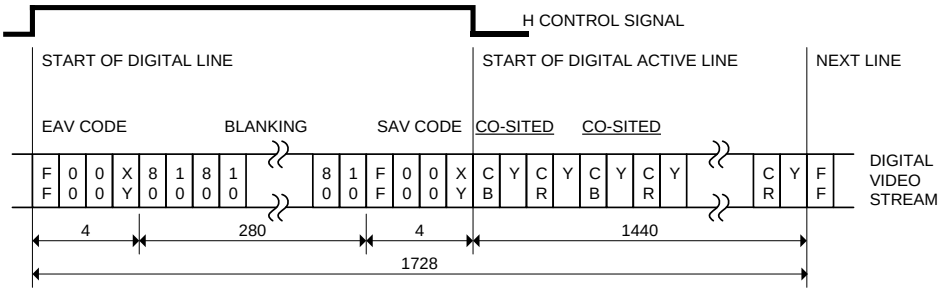


FIGURE 14. BT.656 8-BIT PARALLEL INTERFACE DATA FORMAT FOR 625/50 VIDEO SYSTEMS

D1 VIDEO FRAME DATA ARRANGE

Total byte number in a NTSC frame is: 1716 X 525 = 900,900 Bytes where PAL frame has: 1728 x 625 = 1080,000 Bytes. One thing needs to point is the vertical resolution is 525 lines divided as 262 / 263 in the NTSC and 625 lines divided into 312 / 313 in PAL. If frame-interleaved sequence is sent via this interface, the TW2828 will not toggle FLD flag in the VBI status word like when TW2828 send out the interlaced sequence. For a multi-channel sequence, the output clock will get double or quadruple to maintain the output frame rate. The actual frame data will be sent out sequentially follow CH1-CH2-CH3 style and on to the next frame.

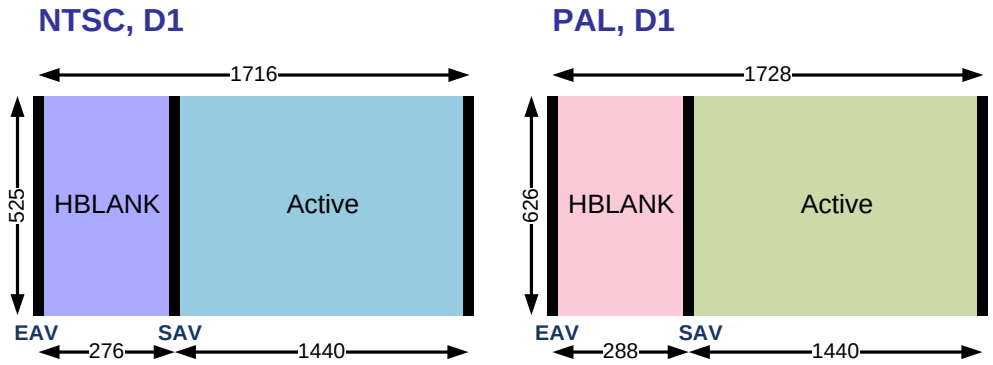


FIGURE 15. FRAME DATA ARRANGE OF D1 VIDEO

CIF VIDEO FRAME DATA ARRANGE

TW2828 support a special mode where the output resolution is a quarter of the original D1 frame. The mode is called CIF frame. In NTSC case, the number of byte in a CIF frame is: 900,900 byte / 4 = 225,225 bytes. This number cannot be evenly divided by two. The number of bytes in each section is difficult to assign. TW2828 is using 828 x 272 for a CIF frame with the fourth frame's VBI includes an extra 36 clocks.

828 x 272 x 4 + 36 = 900,900

As for PAL, the number is 750 x 360 x 4 = 1,080,000 Bytes.

The CIF is only different in the number of bytes in the output format. The rest is the same as the normal frame output. This format is especially useful when a great number of channels need to be output in a single port. For example, a port running at 108 MHz with a 16 channels in CIF resolution can be accomplished.

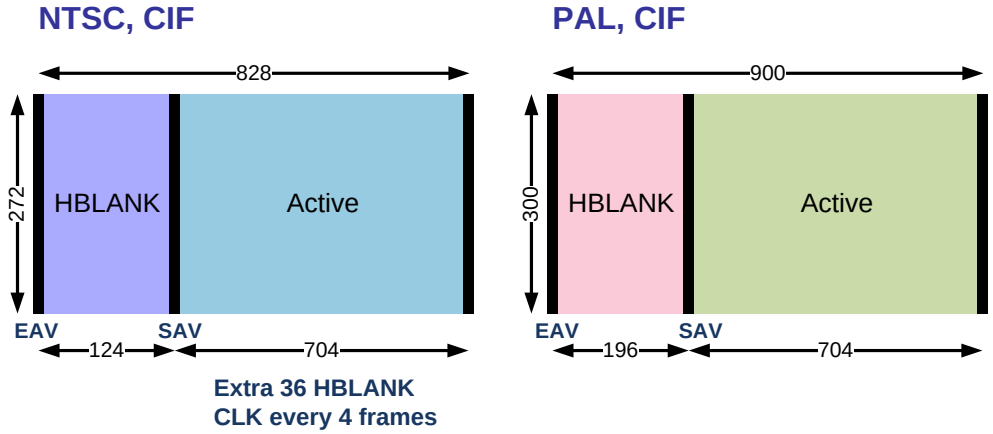


FIGURE 16. FRAME DATA ARRANGE OF CIF VIDEO

16 BIT VIDEO FRAME DATA ARRANGE

In addition to the 8 bit BT.656 interface, TW2828 also supports 16 bit video interface with embedded sync (BT.1120) format. Data port in both format are divided into upper byte as Y data and lower byte as C data. For the BT.1120 format output TW2828 will output the correct EAV, SAV syntax with the 10 bit exteantion. Both formats can be program into different timing and clock rate to send out non-standard video stream.

RECORD OUTPUT METHOD

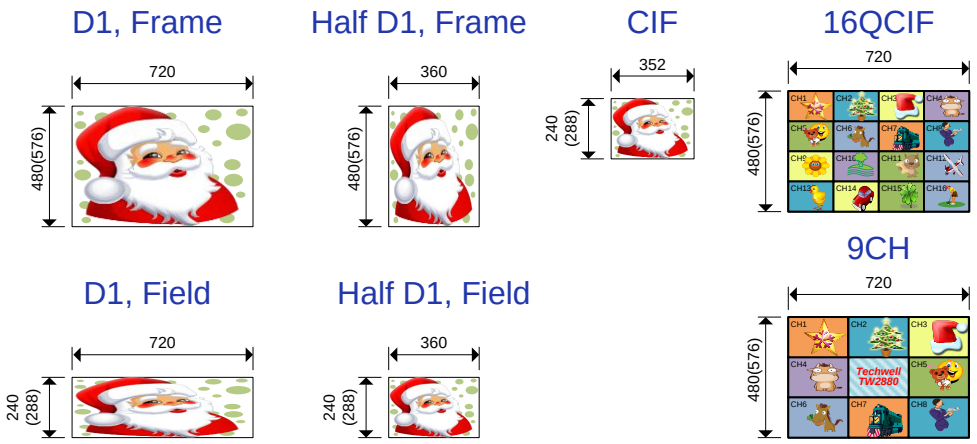
Two kinds of output methods are provided: real time mode and switch mode. The most important feature provided by the real time mode is synchronization. The different channels in the same video output sequence are guaranteed to start from the beginning. Other benefits include less interrupt to the host and easy data management. Switch mode is provided to user don't care about the frame but care much flexibilities especially in the low frame rate low storage requirement environment.

MULTI-MODE FORMAT CONTROL

This is a special mode to let user achieve the ultimate flexibility in outputting recording channel information. Recording output ports have a long source channel select option that support up to 128 depths. So if configured as running at 27 MHz, user can reduce the recording frame rate to less than one frame per second. Although the channel selection is quite flexible, similar resolution item must be grouped into a single frame except D1 selection. For example, a QUAD frame will consume four CIF selections in the list and if not satisfied garbage data will appear in the sequence. That is to say, if quad frame is output through the sequence, only 32 frames can be entered.

RECORDING FORMAT EXAMPLE

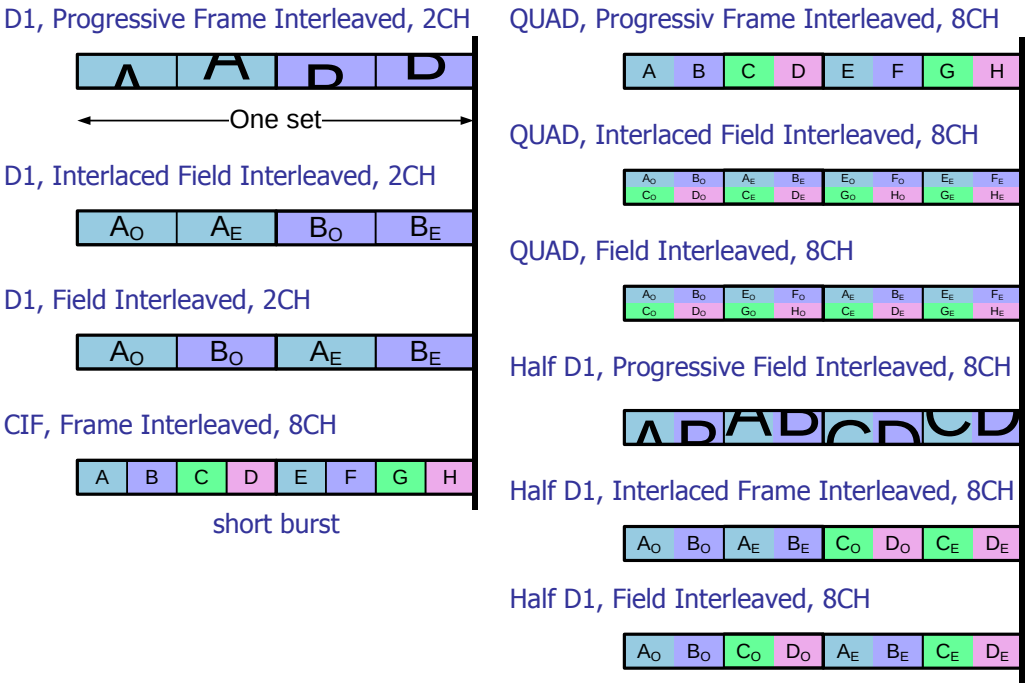
The following diagrams are the recording resolutions and sizes that TW2828 supports. D1 frame means record in full D1 resolution and do frame interleaved output. This is implied when the vertical sync comes, half of picture is sent followed by the other half. Frame mode has two output methods: progressive and interlaced. D1 field means record in full D1 resolution and do field interleaved output. The odd scan lines will be sent first followed by even scan lines.



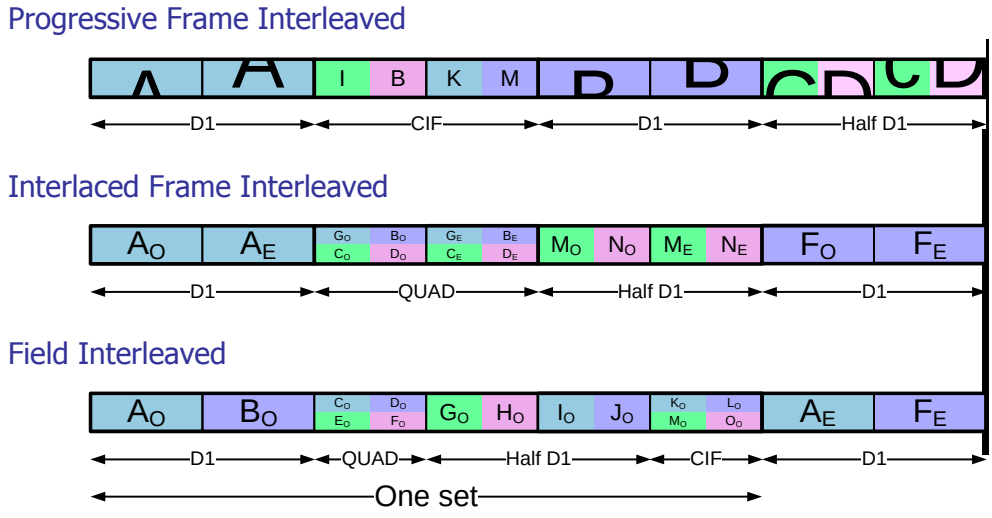
RECORD OUT CHANNEL OUTPUT EXAMPLE

The following is an illustrated example about the possible output sequence of one port running at 54 MHz.

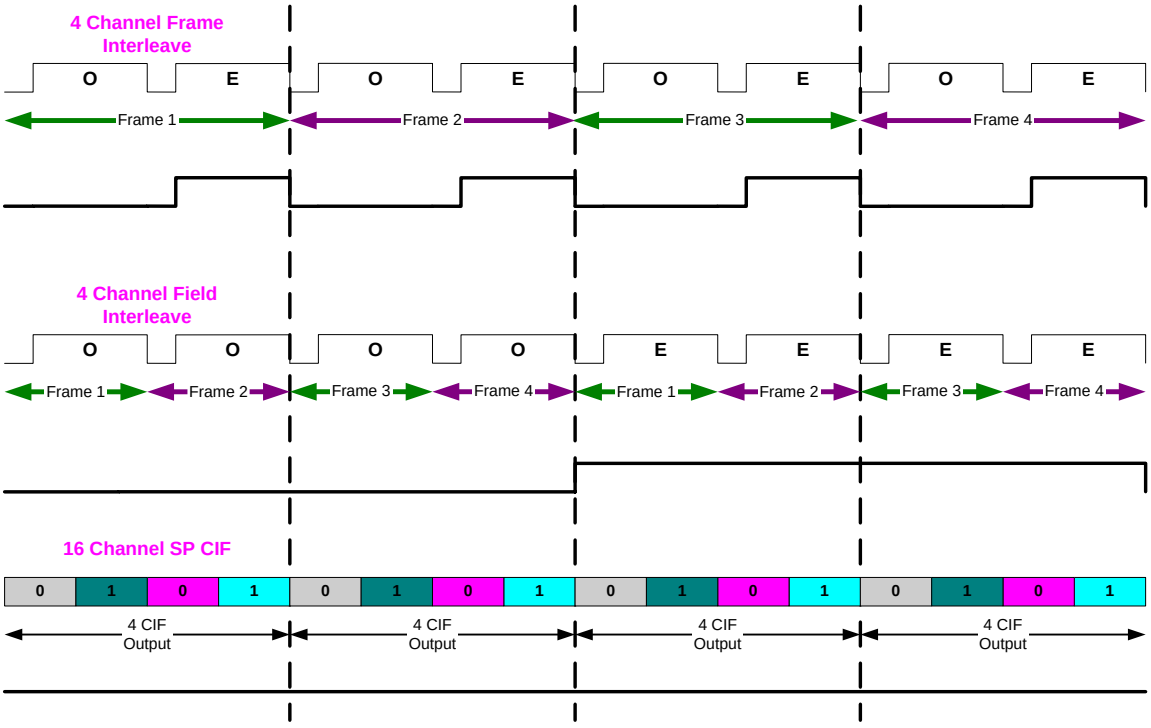
Record out Option @ 54 MHz



Multi-mode record out @ 27 MHz



From the above sequence, one can easily tell the difference between frame-interleaved and field-interleaved. This also has great impact on the receiving CODEC because if synchronization between the channels happens, FMI mode will repeat the same frame and FLI mode will repeat the same field and might causing problems for the backend. The scan line output order in the FMI mode has two choices, the default one is the scan lines are output sequentially and followed the picture's nature order. In addition to this progressive FMI mode, TW2828 also support another method which the output scan lines are followed the even and odd field orders into a so called "interlaced FMI mode". This mode is designed to accommodate different CODEC input format.



RECORD PORT MISC. ITEMS

Multi mode port has 128 entries to constitute a customary output sequence. This sequence also has the straight mode and the automatic mode for grabbing the images. The table sequence programming can be done even during the port is enabled. The register write operation will always has the priority over the internal state machine. User can adjust the sequence whenever they seem fit.

Output resolution if selected as CIF, this port will output four small CIF frames according to the source registers. If specify as D1 and source size is CIF or Half-D1, four or two source images output in a single D1 frame. In this case, the location of these sources needs not to be adjacent in the DRAM memory map.

Special Output Format

The previous section is mainly discussing output format in D1 or in special CIF resolutions. These two formats can be accepted by most CODEC manufacturers in a multi-channel environment. However, there are situations where CODEC manufacturer does not want to decode EAV-SAV field mark and still want to do multi-channel encoding. For this kind of application, TW2828 supports two more modes to output multi-channel material but with high strobe clock (i.e. 108 MHz), namely, the 4D1 mode and BT.1120 (6VGA) mode. Theses two modes are the products of utilizing the new transmission standards in the HD era.

Basically, 4D1 mode evolves from the old BT.656 mode to accommodate four D1 channel at the same time. It keep the EAV-SAV field mark but enlarge the horizontal pixels to 1440 so two D1 frame can be transmitted. In the vertical area it follows the interlaced format that odd field of the first two D1 streams are transmitted followed by the even fields.

The output clock has to set to 108 MHz if real-time recording is desired. Lower output clock will cut down the frame rate.

The 6VGA mode is basically the same except the data arrangement and the output clock. The storing selection needs to set as VGA (640) and use Hstart to center the channels. Output clock has to be 148.5 MHz to make it BT.1120 legal.

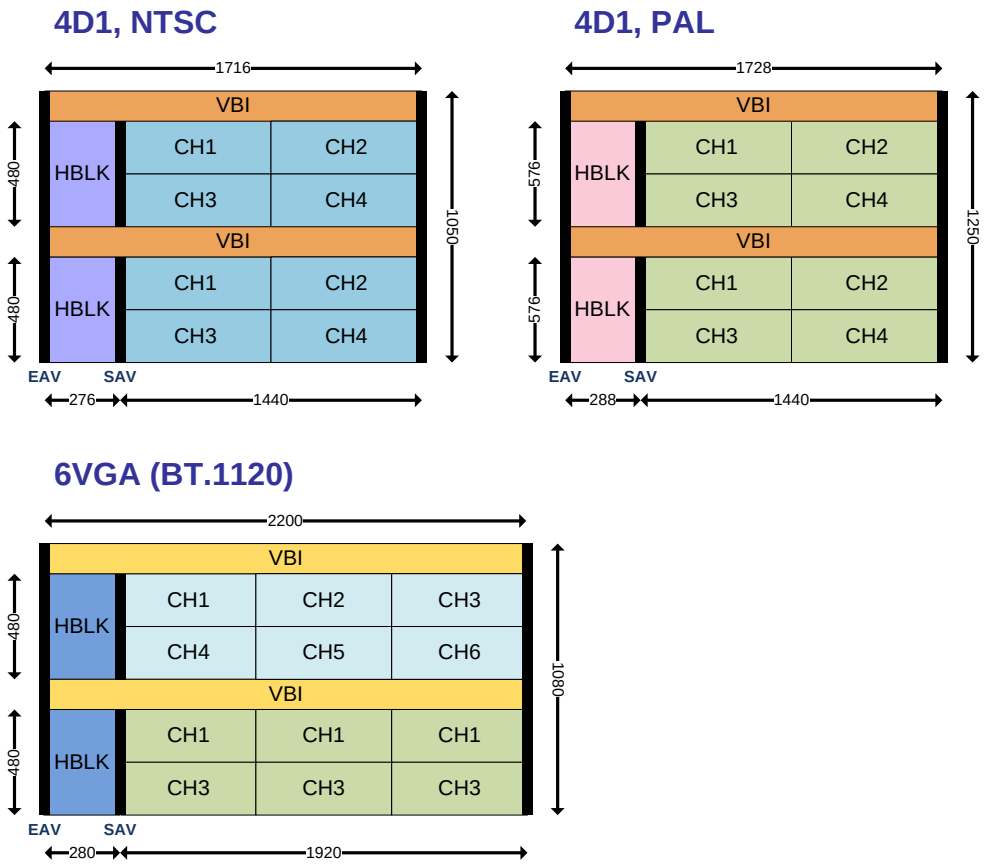


FIGURE 17. SPECIAL OUTPUT FORMAT OF RECORDING PATH

Record Port Capability Chart

FORMAT	SPECIAL	FIELD INTERLEAVED	INTERLACED FMI	PROGRESSIVE FMI
CIF	O	N/A	N/A	N/A
D1	N/A	O	O	O
4D1	N/A	O	O	N/A
BT.1120	N/A	O	O	N/A

NOTE: O : SUPPORT, N/A : NO SUPPORT

One thing needs to point out is the user has the highest flexibilities when composing the D1, and 4D1 recording streams. For example, a D1 resolution stream can have be a quad and the 4 channels needed can be reside in any legal locations of the DRAM buffer. Similarly, 4D1 resolution can be used to send 16 CIF through one output pin port. BT.1120 output stream, however, due to the 6 channels nature, does not have this freedom. All channels in the streams needs to be put into adjacent locations.

Multi-mode Record Port Programming Example

Recording output port can accommodate 128 channel images in a single output stream. By using these options, user can composite the ultimate video stream to the subsequent back end. The source list of the multi-port output is controlled by the three control registers. For example, In case of port 5, register 0xC35, 0xC36 and 0xC37 need to be set. 0xC35 specify the location of the table and 0xC36 specify the recording buffer number (not to be confused with the channel number). The reason not to use channel number here is: for one channel user can select different size of image to store. So the important thing to record here is the buffer number. 0xC37 stores the number of valid entry in the table. It doesn't have to be full length.

Recording port should be off (not enable) when inputting the source into the table. If users choose the output resolution to be D1, sources smaller than the D1 size will be merged into one D1 frame based on the current size. If users choose the output resolution to be CIF then entry table entry represents a source. This is done for obvious reason. Please pay attention when input the source list into the table otherwise garbage data may appear at the output.

There is no restriction on how to arrange the source list other than the resolution limit described above. Table mode is designed for covering the most of the channel with the lease amount of video data generated in regular non-alarming use. User can adjust or repeat a same buffer several times to increase the total coverage based on importance. Real time coverage is also possible but user needs to remember since output clock has only few selections so it limits the number of sources.

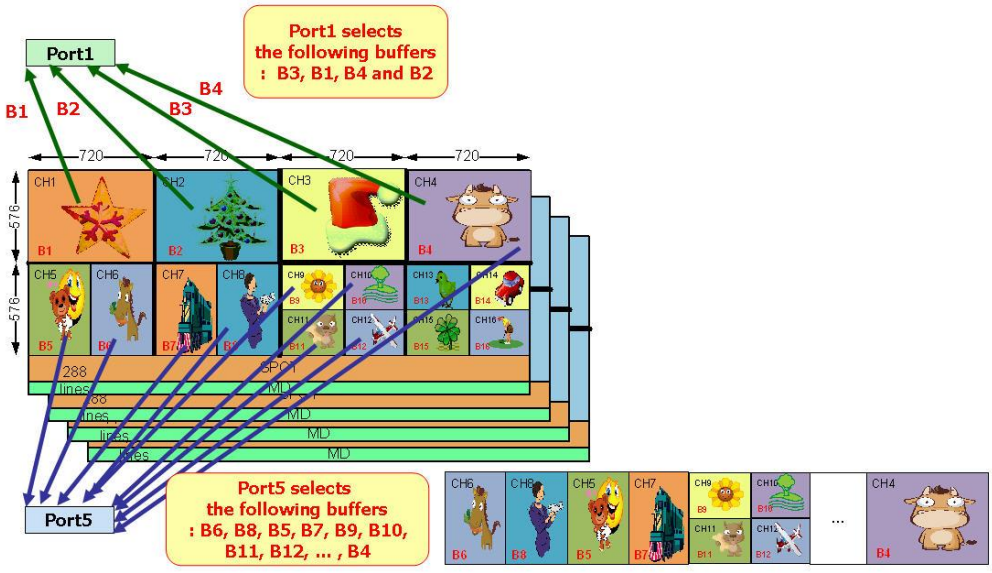


FIGURE 18. EXAMPLE OF MULTI-MODE RECORDING PROGRAMMING

Output Port

INTRODUCTION

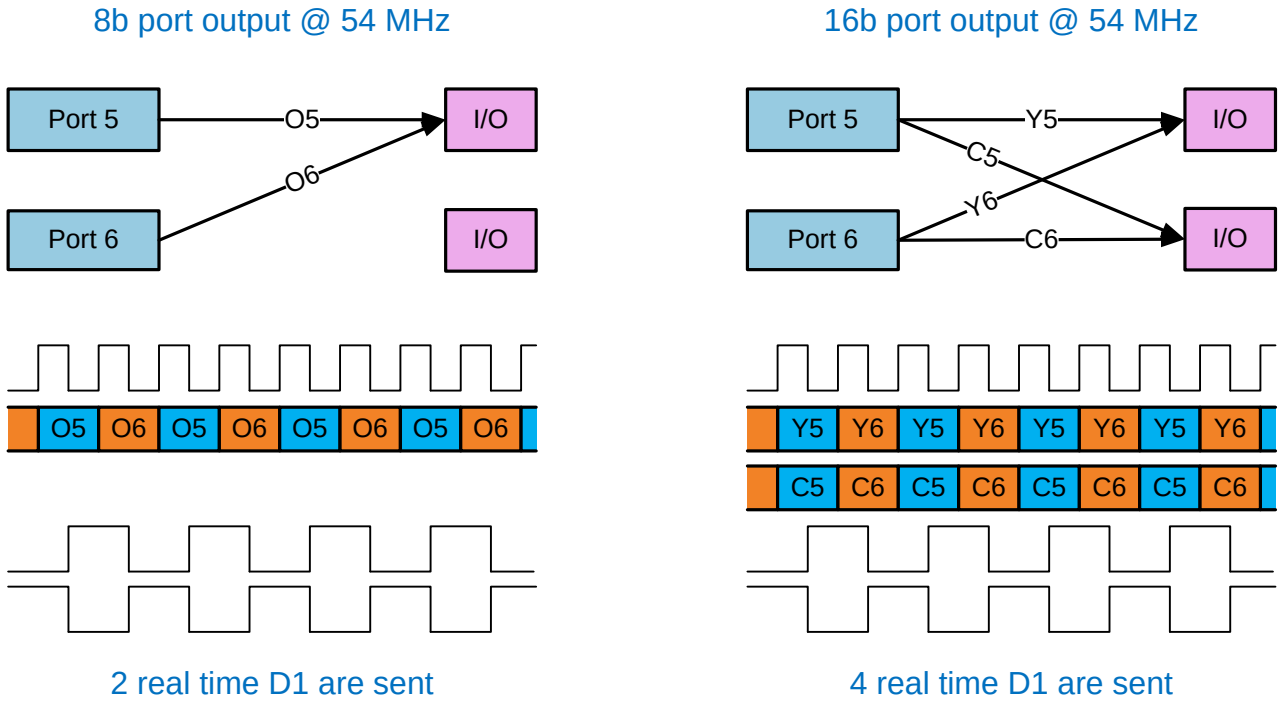


FIGURE 19. TIMING DIAGRAM OF OUTPUT PORT

TW2828 has 5 record units and 4 set of physical ports. Two set of physical ports are shared with GPIO to save pins. The output data and clocks have several rather complicated relationships. The following paragraph is used to clarify this:

Suppose we set the two output ports running at 54 MHz which will output 2 real-time D1 stream on each port. The user can set the output port running at 54 MHz. For 8 bit mode, the output data stream will run at 108 MHz with two out-of-phase clocks running at 54 MHz to differentiate the video data. The diagram on the right shows the relationship between the output data and the output clock. One pin set can output two 2-D1 streams to two CODEC chips. In the 16 bit case, the channel number is double so it can support two 4-D1 streams. If the user set the output port running at 27 MHz, for 8 bit mode, the output data stream will run at 54 MHz and one pin set can output two D1 streams to two CODEC chips. So the output channels are cut in half in 27 MHz mode. Other things needed to know for the user:

- If the associated output ports in a pin set is disabled then number of output channels is cut in half.
- The output rate of the two associated ports must be set to the same value.

8-BIT MODE

This mode basically deals with BT.656 embedded sync-format. It is possible to support 4 output streams running at 108 MHz and output 16 channels using four recording ports or 8 output streams running at 54 MHz (two clock multiplexed method) and output 16 channels using four recording ports, or 8 output streams running at 27 MHz (two clock multiplexed method) and output 8 channels using four recording ports.

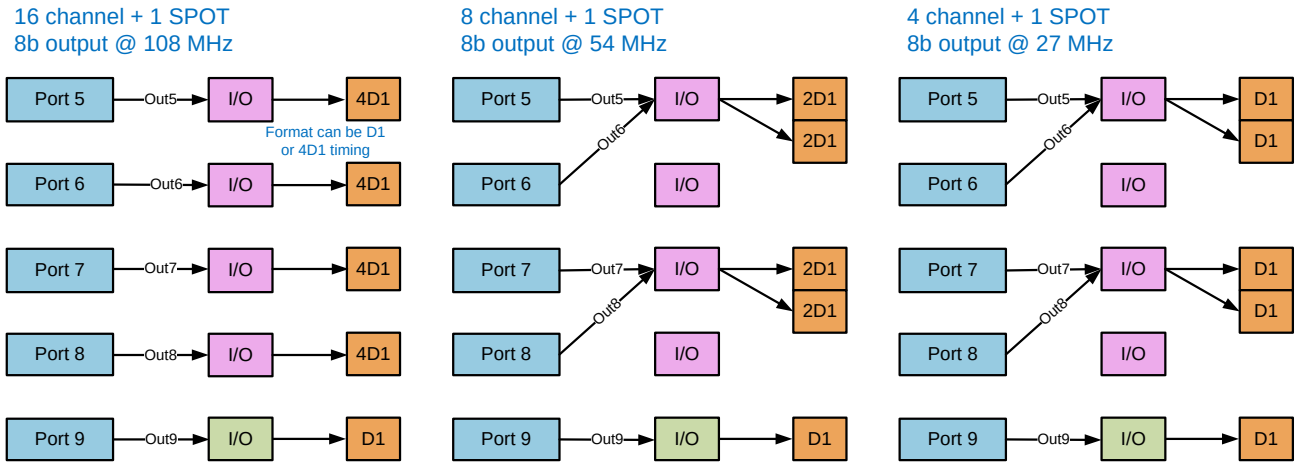


FIGURE 20. EXAMPLE OF 8-BIT MODE OUTPUT PORT CONFIGURATION

16 BIT MODE

TW2828 also support 16 bit output mode where the Y and C data are separated. This setting actually includes support of BT.601 with external sync and BT.1120 with embedded syncs. For setting at 54 MHz, TW2828 can send out two 4 D1 streams into a single CODEC using two ports. The clock and the data arrangement is mostly the same as in the corresponding 8 bit setup.

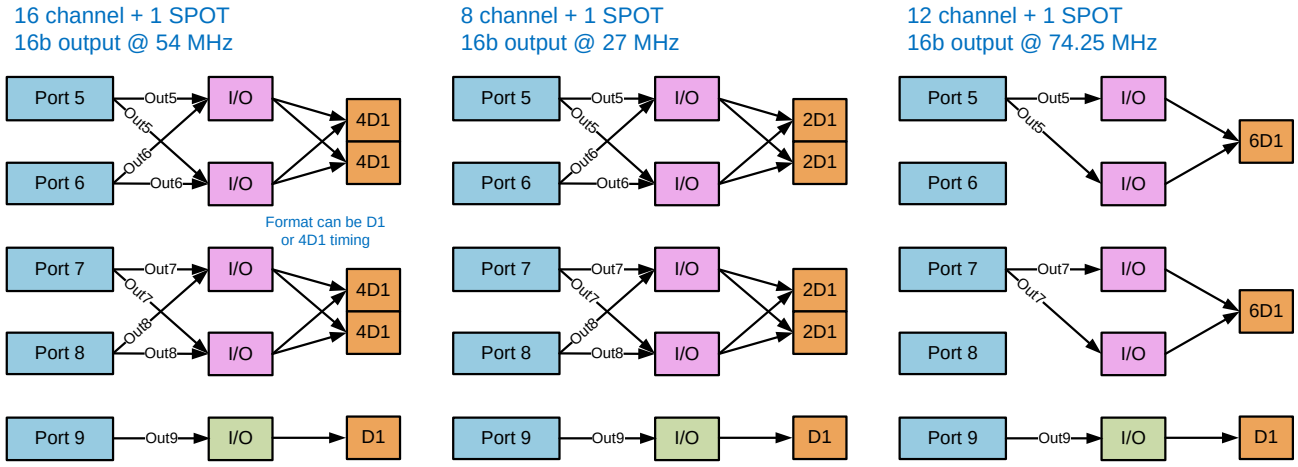


FIGURE 21. EXAMPLE OF 16-BIT MODE OUTPUT PORT CONFIGURATION

16-BIT COMPONENT MODE

In an addition to the traditional 16 bit output mode, there is a new 16 bit mode which is designed specifically fornew generation high speed CODECs. With this mode, if running at 108 MHz, TW2828 can generate 16 bit 8D1 frame or field interleaved video stream. The idea is simple, setup one recording unit the usual way but instead of output 8 bit Y / C component stream sequentially to the outside, it will output both Y / C components at the same clock to the subsequent modules like OSD and embedded sync module.

This means the FIFO output rate doubles as comparison to the normal mode. Because the output speed is clocked at 108 MHz for both component output so 8 D1 channel real time data can be supported. One thing to remember is because the number of output channel is larger than four so the recording unit used is limited to 5, 6, 7, and 8. All four output resolutions are supported but choose BT.1120 will result to a big 8D1 frame (6864x960 for NTSC).

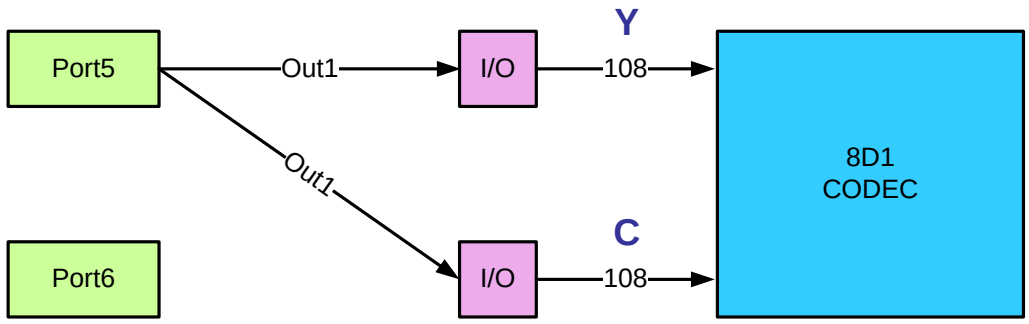


FIGURE 22. BLOCK DIAGRAM OF 16-BIT COMPONENT MODE

To use this mode, after setting the recording buffers and the output options, user needs to set the responsible bits in register 0xCF0 to enable this special component mode and choose the desired video component. As stated before, only two port 5, 6 are needed for output 16 channel D1 real time to the CODEC.

All output resolutions are supported except 6VGA mode, the resulting streams will have different effects based on the resolution. For example, D1 stream will have 8 D1 channel come out before it will repeat itself. NTSC frame interleaved 4D1 mode will have two 1440x960 frame output before repeat itself. Please see the next diagram to understand.

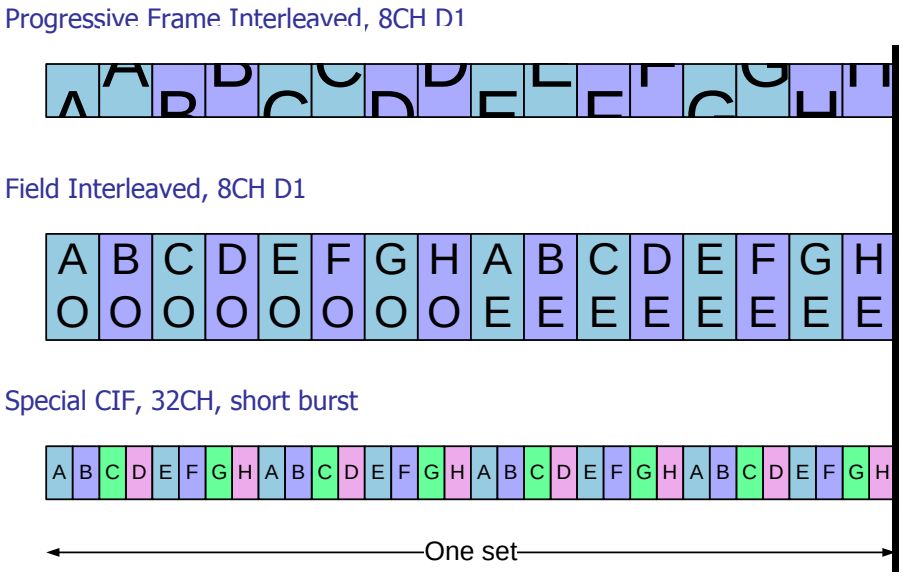


FIGURE 23. RECORD OUTPUT OPTION AT 108 MHZ AND 16-BIT

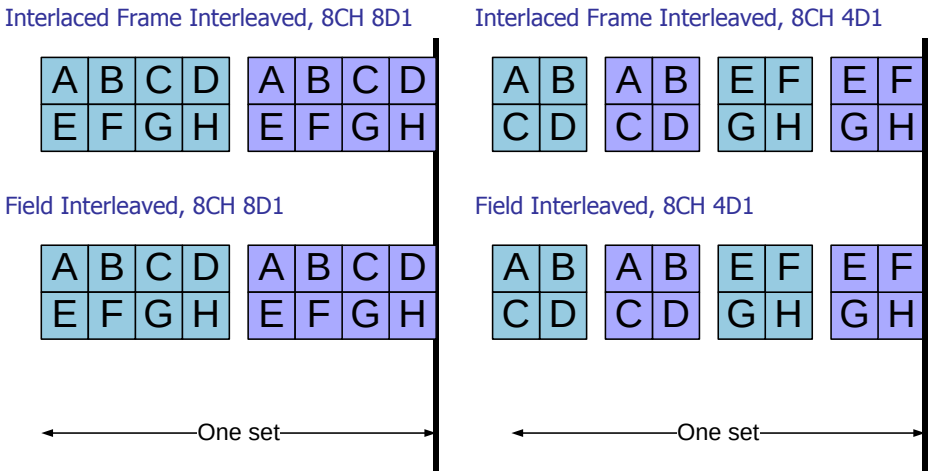


FIGURE 24. RECORD OUTPUT OPTION AT 108 MHZ AND 16-BIT

FIELD SWITCHING MODE

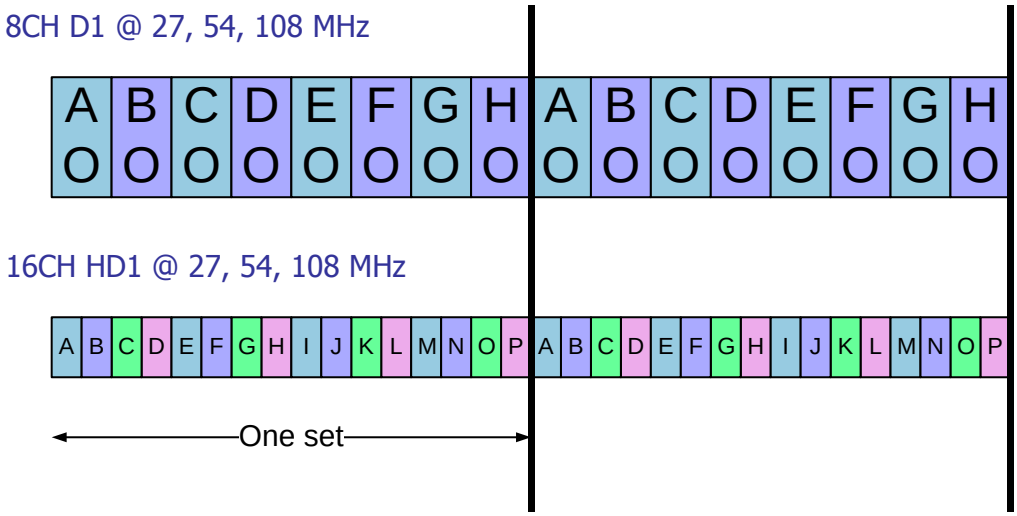


FIGURE 25. FIELD SWITCHING RECORD OUT OPTION

Field switching mode is designed for generating low bit rate stream to cover more channels at half of the normal data rate. To use it, users need to set registers 0xCF1-0xCF4 to determine which buffer is in field switching mode and which field get recorded, the second thing is set the port run at field interleaved mode then the resulting stream will be in field switching mode. D1, half D1 and quad are all legal output format. Another thing to remember is while user still can select output frequency and channel number in a stream, most of the time the resulting stream are non-real time because the channels covered. This is means each field which representing a channel in the resulting stream may come from different input field number.

24 BUFFER MODE

The 16 SPOT buffers can be used by the recording port to increase the total available buffer to 24. This is done by first setting the corresponding bits in SPOT Buffer Control Register 0xCCE – 0xCF to one. Setting these bits are to change the SPOT buffers feedback input in the frame rate control unit. After setting these bits, user will have 24 buffers at their control to create more options. In the buffer naming, 0x0-0xf is the original recording buffers and the 0x10-0x1f is the spot buffers. For example, user can set buffers 0x0-0xf to record D1 resolution and output 16-channel D1 stream while having a special 16CIF video stream to go out using SPOT buffers at the network port. SPOT function is supported if DRAM bandwidth is enough (182 MHz).

OUTPUT PIN SOURCE CONTROL

The source1 and source2 of each output pin set are programmable. The source1 is control by register 0xC4E-0XC51 bit 3 to 0. The source2 is controlled by register 0xCF5-0xCF6. Please see the following diagram, each port can select output from 10 sources. This will make the pair matching in 16 bit mode and byte interleaving in the two CODEC mode easier to program.

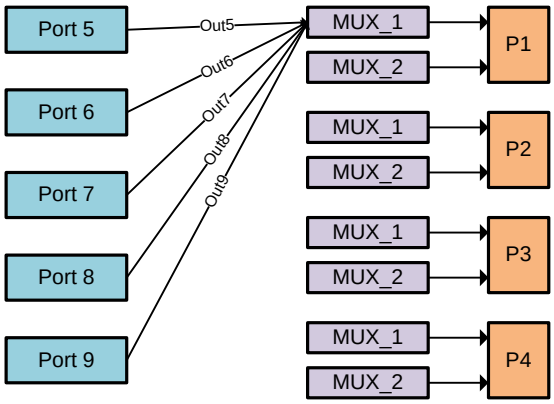


FIGURE 26. EXAMPLE OF OUTPUT PIN SOURCE SELECTION

FIELD SWITCHING QUAD MODE

Based on the field switching mode, a special field switching quad mode is available for use. This mode is created by setting the write buffer side in half D1 field mode and the recording port is in interlaced frame interleaved mode in D1 resolution. To visual result is similar to the normal QUAD mode but has several advantages over the normal mode:

The bandwidth saving is very obvious as one field is dropped.

No need to worry odd / even field reversed because only one field is used.

Image looks sharper because only one low pass filter is used.

This combination can be used in recording output and SPOT output. One thing to remember is you can extend the usage to half D1 mode (except the image is horizontally divided) and divide-by-8 mode.

SYNCHRONIZATION MODE

The table output port 5 to port 9 has a special mode for the TV wall customers. These ports' output can be synchronized together by setting register 0xcf0 bit 0, 2, 4, 6. After setting the corresponding bit the timing of the output port 6, 7, 8, 9 will be controlled by port 5. User can choose any combinations of port to be synchronized together. Another method to synchronize any channels is after setting the output port, do a software reset. After this reset all enabled port will have the same timing if they are configured under the same conditions. By doing this will put a heavy burden on DRAM bandwidth requirement so synchronization is not what you need, after software reset you need to disable and enable the port to scatter the requests.

CONCLUSION

Together with 8 bit mode, TW2828 provides a wide range of connecting options for the backend solutions. One thing to remember is if the new BT.1120 mode is desired, the output will have BT.1120 EAV-SEV syntax output during the sync period.

RECORD OUT AC TIMING

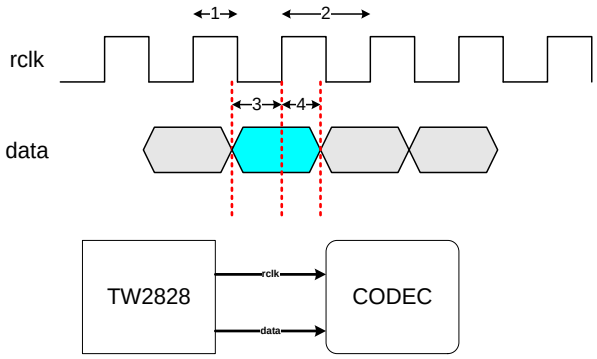
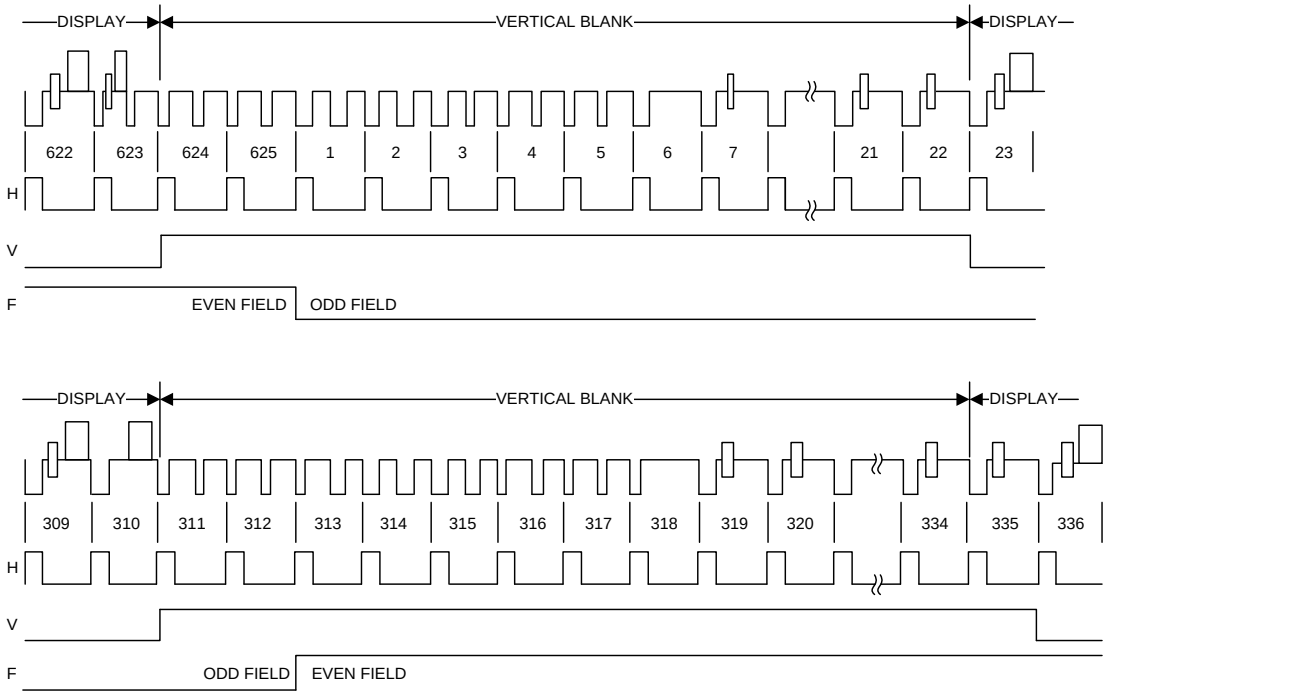


FIGURE 27. TIMING DIAGRAM OF RECORDING OUT AC TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Output Clock Half Period	1		4.62(108) 9.26 (54), 18.52 (27)		ns
Output Clock Period	2		9.25(108) 18.51 (54), 37.03 (27)		ns
Output Data Setup Time	3	3			ns
Output Data Hold Time	4	1.5			ns

TV Encoder

TV Encoder is the module converts all component data from scalar into a standard analog baseband television signal (CVBS) which is compatible with worldwide standards. Follow is the PAL timing.



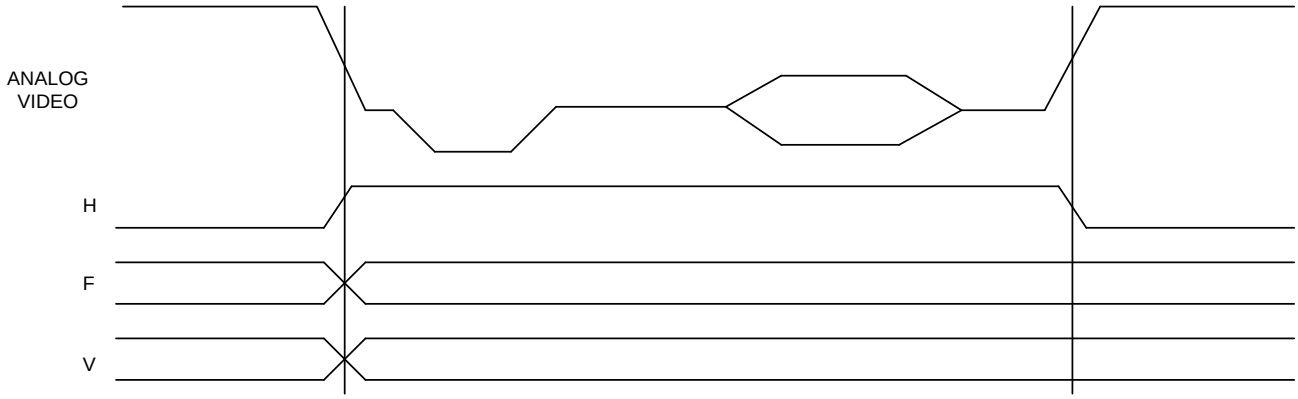


FIGURE 28. TIMING DIAGRAM OF TV ENCODER

Register Table for Recording Path

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xC00	R/W	0	Recording Write Buffer 1 Control Register A [6] Recording format select [5:4] Recording resolution select [3:0] Channel Select
0xC01	R/W	0	Recording Write Buffer 2 Control Register A
0xC02	R/W	0	Recording Write Buffer 3 Control Register A
0xC03	R/W	0	Recording Write Buffer 4 Control Register A
0xC04	R/W	0	Recording Write Buffer 5 Control Register A
0xC05	R/W	0	Recording Write Buffer 6 Control Register A
0xC06	R/W	0	Recording Write Buffer 7 Control Register A
0xC07	R/W	0	Recording Write Buffer 8 Control Register A
0xC08	R/W	0	Recording HD Buffer 1 Control Register A [7] HD Channel Select for OSD [6] Reserved [5:4] Recording resolution select [3:0] Channel Select
0xC09	R/W	0	Recording HD Buffer 2 Control Register A
0xC0A	R/W	0	Recording HD Buffer 3 Control Register A
0xC0B	R/W	0	Recording HD Buffer 4 Control Register A
0xC0C	R/W	0	Recording HD Buffer 5 Control Register A
0xC10	R/W	0	Recording Write Buffer 1 Control Register B [7] Recording buffer enable [6:3] Horizontal position select [2:0] Vertical position select
0xC11	R/W	0	Recording Write Buffer 2 Control Register B
0xC12	R/W	0	Recording Write Buffer 3 Control Register B
0xC13	R/W	0	Recording Write Buffer 4 Control Register B
0xC14	R/W	0	Recording Write Buffer 5 Control Register B
0xC15	R/W	0	Recording Write Buffer 6 Control Register B
0xC16	R/W	0	Recording Write Buffer 7 Control Register B
0xC17	R/W	0	Recording Write Buffer 8 Control Register B
0xC18	R/W	0	Recording HD Buffer 1 Control Register B [7] Recording buffer enable [6:3] Horizontal position select [2:0] Vertical position select
0xC19	R/W	0	Recording HD Buffer 2 Control Register B
0xC1A	R/W	0	Recording HD Buffer 3 Control Register B
0xC1B	R/W	0	Recording HD Buffer 4 Control Register B
0xC1C	R/W	0	Recording HD Buffer 5 Control Register B
0xC32	R/W	0	Record Port 9 Custom Horizontal Control Register
0xC33	R/W	0	Record Port 9 Custom Vertical Control Register
0xC34	R/W	0	Record Port 5 Control Register [7:6] Output resolution select [5] Output port format select [4:3] Reserved [2:1] Output port clock select [0] Output port buffer enable
0xC35	R/W	0	Record port 5 Source Control Address Register[6:0]
0xC36	R/W	0	Record port 5 Source Control Data Register [5] Double table buffer update [4:0] Source buffer select
0xC37	R/W	0	Record port 5 Source Number Register[6:0]
0xC38	R/W	0	Record Port 5 Custom Horizontal Control Register

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xC39	R/W	0	Record Port 6 Custom Vertical Control Register
0xC3A	R/W	0	Record Port 6 Control Register [7:6] Output resolution select [5] Output port format select [4:3] Reserved [2:1] Output port clock select [0] Output port buffer enable
0xC3B	R/W	0	Record port 6 Source Control Address Register[6:0]
0xC3C	R/W	0	Record port 6 Source Control Data Register [5] Double table buffer update [4:0] Source buffer select
0xC3D	R/W	0	Record port 6 Source Number Register[6:0]
0xC3E	R/W	0	Record Port 6 Custom Horizontal Control Register
0xC3F	R/W	0	Record Port 6 Custom Vertical Control Register
0xC40	R/W	0	Record Port 7 Control Register [7:6] Output resolution select [5] Output port format select [4:3] Reserved [2:1] Output port clock select [0] Output port buffer enable
0xC41	R/W	0	Record port 7 Source Control Address Register[6:0]
0xC42	R/W	0	Record port 7 Source Control Data Register [5] Double table buffer update [4:0] Source buffer select
0xC43	R/W	0	Record port 7 Source Number Register[6:0]
0xC44	R/W	0	Record Port 7 Custom Horizontal Control Register
0xC45	R/W	0	Record Port 7 Custom Vertical Control Register
0xC46	R/W	0	Record Port 8 Control Register [7:6] Output resolution select [5] Output port format select [4:3] Reserved [2:1] Output port clock select [0] Output port buffer enable
0xC47	R/W	0	Record port 8 Source Control Address Register[6:0]
0xC48	R/W	0	Record port 8 Source Control Data Register [5] Double table buffer update [4:0] Source buffer select
0xC49	R/W	0	Record port 8 Source Number Register[6:0]
0xC4A	R/W	0	Record Port 8 Custom Horizontal Control Register
0xC4B	R/W	0	Record Port 8 Custom Vertical Control Register
0xC4D	R/W	0	Record Port Operating Mode Select Register [7] ADV[1] [6] ADV[0] [5] Automatic correction [4] BT1120 Select [3] Port 9 Interlaced FMI [2] Record test pattern [1] NTSC_PAL [0] WIN_READ
0xC4E	R/W	0	Output Pin Set 1 Control Register [7:4] Source 1 select [3] Clock polarity [2] Port width select [1:0] Pin clock select

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xC4F	R/W	0x40	Output Pin Set 2 Control Register [7:4] Source 1 select [3] Clock polarity [2] Port width select [1:0] Pin clock select
0xC50	R/W	0x80	Output Pin Set 3 Control Register [7:4] Source 1 select [3] Clock polarity [2] Port width select [1:0] Pin clock select
0xC51	R/W	0xc0	Output Pin Set 4 Control Register [7:4] Source 1 select [3] Clock polarity [2] Port width select [1:0] Pin clock select
0xC52	R/W	0	Port 9 Control Register [7:6] Output resolution select [5] Output port format select [4:3] Reserved [2:1] Output port clock select [0] Output port buffer enable
0xC53	R/W	0	Port 9 Source Control Address Register[6:0]
0xC54	R/W	0	Port 9 Source Control Data Register [5] Double buffer update [4:0] Source buffer select
0xC55	R/W	0	Port 9 Source Number Register [7] Enable free running Port 9 [6:0] Number of source
0xC56	R/W	0	MISC. Control 1 Register [7] Spread read sync option [6] Select different MCLK reset width in FIFO [5] Bottom field low speed update algorithm select [4] Top field low speed update algorithm select [3] Horizontal control override in 6 VGA mode [2:0] Select record side FRSC source
0xC57	R/W	0	HMARGIN[7:0] Register
0xC58	R/W	0xd0	MISC. Control 2 Register [7] Limit record unit start time if using SPOT buffers [6] Limit record unit start time if using record buffers [5:4] Record write buffer request level control [3:0] Enable no video reset frame rate control unit
0xC59	R/W	0x40	MISC. Control 3 Register [7:6] SPOT write buffer request level control [5] SPOT buffer vertical invert line number option [4] Record buffer vertical invert line number option [3:2] SPOT buffer update option select [1:0] Record buffer update option select
0xC5A	R/W	0	HDE selection
0xC5B	R/W	0	VDE selection
0xC5C	R/W	0	Bank Change Mask Control Register [2] Change mask control on/off [1] Reserved [0] Change mask weight
0xC5D	R/W	0	Special OSD Control [7:4] Special OSD type selection for port 5 ~ port 8 [3:0] Special OSD(16-QCIF/9-CH display) on/off control for port 5 ~ port8)

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xC5E	R/W	0	Special OSD Boundary on/off Control for port 5 ~ port 6 [7:4] Boundary on/off control for port 6 [3:0] Boundary on/off control for port 5
0xC5F	R/W	0	Special OSD Boundary on/off Control for port 7 ~ port 8 [7:4] Boundary on/off control for port 8 [3:0] Boundary on/off control for port 7
0xC60	R/W	0	Special OSD Control for port 9 [5] Special OSD type selection for port 9 [4] Special OSD(16-QCIF/9-CH display) on/off control for port 9 [3:0] Boundary on/off control for port 9
0xC61	R/W	0	SPOT OSD on/off Control for port 5(bit 0) ~ port 9(bit 4) [4:0] SPOT on/off control
0xC64	R/W	0	Record Buffer Freeze Control Register A
0xC66	R/W	0	SPOT Buffer Freeze Control Register A
0xC67	R/W	0	SPOT Buffer Freeze Control Register B
0xC68	R/W	0	Custom Clock Control Register [5:4] Window Position Shadow Register Select [3:0] Reserved
0xC69	R/W	0	Interlaced FMI Control Register[7:0]
0xC6A	R/W	0	'wr_page' Reference Selection Control Register A(Write Buffer Index)
0xC6B	R/W	0	'wr_page' Reference Selection Control Register B(Read Port Index) [4] on/off control for separated wr_page [3] Reserved [2:0] wr_page reference selection value
0xC6C	R/W	0	New FRSC control register
0xC6D	R/W	0	PB Ignore Bit on/off Control for Each Port 5 ~ Port 8 and Port 9
0xC6E	R/W	0	1st and 2nd Ignore Bit Value
0xC6F	R/W	0	3rd and 4th Ignore Bit Value
0xC70	R/W	0	Background Color for Cb
0xC71	R/W	0	Background Color for Cr
0xC72	R/W	0	Background Color for Y
0xC73	R/W	0	Background on/off Control for Record Write Buffer 1 ~ Buffer 8
0xC75	R/W	0	Background on/off Control for SPOT Write Buffer 1 ~ Buffer 8
0xC76	R/W	0	Background on/off Control for SPOT Write Buffer 9 ~ Buffer 16
0xC77	R/W	0	New Non-real Time Field Switching Mode for Port 5 ~ Port 9
0xC78	R/W	0	New Field Switching Mode Field Select for Port 5 ~ Port 9
0xC79	R/W	0	Field Interleaved Read Mode with 4 Frames
0xC7A	R/W	0	New Non-real Time Bank Control for Port 5 ~ Port 9
0xC7B	R/W	0xb4	Dram Pitch of SPOT and record(16 pixel unit)
0xC7C	R/W	0	Vertical Start Position of Record Write Buffer Register A
0xC7D	R/W	0	Vertical Start Position of Record Write Buffer Register B
0xC7E	R/W	0	Horizontal Start Position of Record Write Buffer Register A
0xC7F	R/W	0	Vertical Start Position of Record Write Buffer Register B
0xC80	R/W	0	Vertical Start Position of SPOT Write Buffer Register A
0xC81	R/W	0	Vertical Start Position of SPOT Write Buffer Register B
0xC82	R/W	0	Horizontal Start Position of SPOT Write Buffer Register A
0xC83	R/W	0	Vertical Start Position of SPOT Write Buffer Register B
0xC8C	R/W	0	QCIF Mode On/Off Control for SPOT Buffer 1 ~ 8
0xC8D	R/W	0	QCIF Mode On/Off Control for SPOT Buffer 9 ~ 16
0xC8E	R/W	0	QCIF Type Selection for SPOT Buffer 1 ~ 8
0xC8F	R/W	0	QCIF Type Selection for SPOT Buffer 9 ~ 16
0xC90	R/W	0	SPOT Recording Buffer 1 Control Register A [6] Recording format select [5:4] Recording resolution select [3:0] Channel Select

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xC91	R/W	0	SPOT Recording Buffer 2 Control Register A
0xC92	R/W	0	SPOT Recording Buffer 3 Control Register A
0xC93	R/W	0	SPOT Recording Buffer 4 Control Register A
0xC94	R/W	0	SPOT Recording Buffer 5 Control Register A
0xC95	R/W	0	SPOT Recording Buffer 6 Control Register A
0xC96	R/W	0	SPOT Recording Buffer 7 Control Register A
0xC97	R/W	0	SPOT Recording Buffer 8 Control Register A
0xC98	R/W	0	SPOT Recording Buffer 9 Control Register A
0xC99	R/W	0	SPOT Recording Buffer 10 Control Register A
0xC9A	R/W	0	SPOT Recording Buffer 11 Control Register A
0xC9B	R/W	0	SPOT Recording Buffer 12 Control Register A
0xC9C	R/W	0	SPOT Recording Buffer 13 Control Register A
0xC9D	R/W	0	SPOT Recording Buffer 14 Control Register A
0xC9E	R/W	0	SPOT Recording Buffer 15 Control Register A
0xC9F	R/W	0	SPOT Recording Buffer 16 Control Register A
0xCA0	R/W	0	SPOT Recording Buffer 1 Control Register B [7] Recording buffer enable [6:3] Horizontal position select [2:0] Vertical position select
0xCA1	R/W	0	SPOT Recording Buffer 2 Control Register B
0xCA2	R/W	0	SPOT Recording Buffer 3 Control Register B
0xCA3	R/W	0	SPOT Recording Buffer 4 Control Register B
0xCA4	R/W	0	SPOT Recording Buffer 5 Control Register B
0xCA5	R/W	0	SPOT Recording Buffer 6 Control Register B
0xCA6	R/W	0	SPOT Recording Buffer 7 Control Register B
0xCA7	R/W	0	SPOT Recording Buffer 8 Control Register B
0xCA8	R/W	0	SPOT Recording Buffer 9 Control Register B
0xCA9	R/W	0	SPOT Recording Buffer 10 Control Register B
0xCAA	R/W	0	SPOT Recording Buffer 11 Control Register B
0xCAB	R/W	0	SPOT Recording Buffer 12 Control Register B
0xCAC	R/W	0	SPOT Recording Buffer 13 Control Register B
0xCAD	R/W	0	SPOT Recording Buffer 14 Control Register B
0xCAE	R/W	0	SPOT Recording Buffer 15 Control Register B
0xCAF	R/W	0	SPOT Recording Buffer 16 Control Register B
0xCBC	R/W	0	Record OSD register update method selection
0xCBD	R/W	0	Record OSD register sync update on/off control
0xCBE	R/W	0	Record OSD register sync update field selection
0xCC4	R/W	0x01	Read Port Miscellaneous Control Register 1
0xCC8	R/W	0	Background Buffer Indication Register 1
0xCC9	R/W	0	Background Buffer Indication Register 2
0xCCA	R/W	0	Second Record DRAM Buffer Register
0xCCB	R/W	0	Second HD DRAM Buffer Register
0xCCC	R/W	0	Second SPOT DRAM Buffer Register 1
0xCCD	R/W	0	Second SPOT DRAM Buffer Register 2
0xCCE	R/W	0	Record Buffer Alternate Source Register 1
0xCCF	R/W	0	Record Buffer Alternate Source Register 2
0xCD0	R/W	0 0x80	Record/SPOT Buffer Horizontal Offset Control Register 1 PB_PITCH
0xCD1	R/W	0	Record/SPOT Buffer Horizontal Offset Control Register 2 REC_PITCH_SEL
0xCD2	R/W	0	Record/SPOT Buffer Horizontal Offset Control Register 3
0xCD3	R/W	0	Record/SPOT Buffer Horizontal Offset Control Register 4
0xCD4	R/W	0	Record/SPOT Buffer Horizontal Offset Control Register 5
0xCD5	R/W	0	Record/SPOT Buffer Horizontal Offset Control Register 6

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xCD6	R/W	0	Record/SPOT Buffer Horizontal Offset Control Register 7
0xCD7	R/W	0	Record/SPOT Buffer Horizontal Offset Control Register 8
0xCD8	R/W	0	SPOT Buffer Horizontal Offset Control Register 9
0xCD9	R/W	0	SPOT Buffer Horizontal Offset Control Register 10
0xCDA	R/W	0	SPOT Buffer Horizontal Offset Control Register 11
0xCDB	R/W	0	SPOT Buffer Horizontal Offset Control Register 12
0xCDC	R/W	0	SPOT Buffer Horizontal Offset Control Register 13
0xCDD	R/W	0	SPOT Buffer Horizontal Offset Control Register 14
0xCDE	R/W	0	SPOT Buffer Horizontal Offset Control Register 15
0xCDF	R/W	0	SPOT Buffer Horizontal Offset Control Register 16
0xCE0	R/W	0	Record/SPOT Buffer Vertical Offset Control Register 1
0xCE1	R/W	0	Record/SPOT Buffer Vertical Offset Control Register 2
0xCE2	R/W	0	Record/SPOT Buffer Vertical Offset Control Register 3
0xCE3	R/W	0	Record/SPOT Buffer Vertical Offset Control Register 4
0xCE4	R/W	0	Record/SPOT Buffer Vertical Offset Control Register 5
0xCE5	R/W	0	Record/SPOT Buffer Vertical Offset Control Register 6
0xCE6	R/W	0	Record/SPOT Buffer Vertical Offset Control Register 7
0xCE7	R/W	0	Record/SPOT Buffer Vertical Offset Control Register 8
0xCE8	R/W	0	SPOT Buffer Vertical Offset Control Register 9
0xCE9	R/W	0	SPOT Buffer Vertical Offset Control Register 10
0xCEA	R/W	0	SPOT Buffer Vertical Offset Control Register 11
0xCEB	R/W	0	SPOT Buffer Vertical Offset Control Register 12
0xCEC	R/W	0	SPOT Buffer Vertical Offset Control Register 13
0xCED	R/W	0	SPOT Buffer Vertical Offset Control Register 14
0xCEE	R/W	0	SPOT Buffer Vertical Offset Control Register 15
0xCEF	R/W	0	SPOT Buffer Vertical Offset Control Register 16
0xCF0	R/W	0	Special Component Record mode Register
0xCF1	R/W	0	Record Buffer Field Switching Record Mode Register
0xCF3	R/W	0	Record Buffer Field Switching Record Mode Field Select Register
0xCF5	R/W	0x62	Output Pin Set Source 2 Control Register A
0xCF6	R/W	0xea	Output Pin Set Source 2 Control Register B
0xCF7	R/W	0	Frame Rate Controller Update Register
0xCF8	R/W	0	SPOT Buffer Field Switching Record Mode Register 1
0xCF9	R/W	0	SPOT Buffer Field Switching Record Mode Register 2
0xCFA	R/W	0	SPOT Buffer Field Switching Record Mode Field Select Register 1
0xCFB	R/W	0	SPOT Buffer Field Switching Record Mode Field Select Register 2
0xCFC	R/W	0	Write Buffer Control Register
0xCFD	R/W	0	New FRSC Control Register
0xCFE	R/W	0	New Write Buffer Mapping Control Register
0xCFF	R/W	0	PB FRSC connection control

Register Table for SPOT Display

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xF0B	R/W	0x00	SP Frame Rate Control and Vblank Select [7:6] Vblank Select from one of the four SPOT for FRSC [5] SP1 Colorbar Enable [4] RESERVED [3:2] SP1_FLD select 11: use bank0 from the FRSC as the field 10: use bank0 from the FRSC inverse as the filed 0x: use HVCNT generated field [1:0] Reserved
0xF0F	R/W	0x00	SPOT1 Enable Register [7] SP1_FLD_MODE
0xF17	R/W	0x00	SP1_TVE_STD[7:0], SPOT1 TV Standard Register
0xF18	R/W	0x00	SP1_TVE_POL[7:0], SPOT1 TV Sync Polarity Register
0xF19	R/W	0x00	SP1_TVE_FDET[6:0], SPOT1 TV Field Control Register
0xF1A	R/W	0x00	SP1_TVE_HSENC[7:0], SPOT1 TV Encoder Active Pixel delay
0xF1B	R/W	0x00	SP1_TVE_HSENC[9:8], [7:2] Reserved [1:0] SPOT1 TV Encoder Active Pixel delay
0xF1C	R/W	0x00	[7:6] SP1_CVBS_SRC_SEL [5:0] SP1_TVE_VSENC[5:0], SPOT1 TV Encoder Active Line delay
0xF1D	R/W	0x00	SP1_TVE_LINE_OS[4:0], SPOT1 TV Encoder Active Line offset
0xF1E	R/W	0x00	[7;6] SP1_FLD_SW_MODE [5:0] SP1_TVE_PIXEL_OS[5:0], SPOT1 TV Encoder Active Pixel Offset
0xF1F	R/W	0x00	SP1_TVE_FLD_OS[1:0], SPOT1 TV Encoder Active Field offset
0xF20	R/W	0x00	SP1_TVE_FSC_FREE[7], SPOT1 TV Encoder Subcarrier runfree [6:0] RESERVED
0xF6B	R/W	0x00	[7:6] RESERVED [5] SP2_COLORBAR, SPOT2 Color Bar Enable Register [4] RESERVED [3:2] SP2_FLD select 11: use bank0 from the FRSC as the field 10: use bank0 from the FRSC inverse as the filed 0x: use HVCNT generated field [1] SYNC align between record and SPOT [0] Reserved
0xF6F	R/W	0x00	SPOT2 Enable Register [7] SP2_FLD_MODE [6] SP2_2ND_MEM [5] SP2_FRMCNT_EN, SPOT2 Frame Count Enable [4] SP2_ENA, SPOT2 Enable [3:2] SP2_ROT_EN, SPOT2 Rotate Enable [1] SP2_VS_POL, SPOT2 Vsync Polarity Select [0] SP2_HS_POL, SPOT2 Hsync Polarity Select
0xF77	R/W	0x00	SPOT2 TV Encoder Standard Register [7:6] SP2_TVE_FSC_SEL, SPOT2 TV Encoder Fsc Select [5] SP2_TVE_SAT_LMT, SPOT2 TV Saturation Limit [0] SP2_TVE_STD, SPOT2 TV Standard Select

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xF78	R/W	0x00	SPOT2 TV Encoder Standard Register [7] SP2_TVE_VSPOL, SPOT2 TV Encoder Vertical Sync Polarity [6] SP2_TVE_HSPOL, SPOT2 TV Encoder Horiz Sync Polarity [5] SP2_TVE_VSDET, SPOT2 TV Encoder Vsync detect [4] SP2_TVE_PED, SPOT2 TV Encoder Pedestal Enable [3] SP2_TVE_PDRST, SPOT2 TV Encoder Pedestal Reset [2] SP2_TVE_PHALT, SPOT2 TV Encoder Phase Alternated [1] SP2_TVE_F_INV, SPOT2 TV Encoder Field Inverted [0] SP2_TVE_INTL, SPOT2 TV Encoder Interlace Select
0xF79	R/W	0x00	SPOT2 TV Encoder Offset Register [5:4] SP2_TVE_PIX_OS, SPOT2 TV Encoder Pixel Offset [3:2] SP2_TVE_FLD_OS, SPOT2 TV Encoder field Offset [1] SP2_TVE_FLD_POL, SPOT2 TV Encoder Field Polarity [0] SP2_TVE_ FLDDET, SPOT2 Encoder Field Detect
0xF7A	R/W	0x00	SP2_TVE_HSENC[7:0], SPOT2 TV Encoder Active Pixel delay
0xF7B	R/W	0x00	SP2_TVE_HSENC[9:8], [7:2] Reserved [1:0] SPOT2 TV Encoder Active Pixel delay
0xF7C	R/W	0x40	[7:6] SP2_CVBS_SRC_SEL [5:0] SP2_TVE_VSENC[5:0], SPOT2 TV Encoder Active Line delay
0xF7D	R/W	0x00	SP2_TVE_LINE_OS[4:0], SPOT2 TV Encoder Active Line offset
0xF7E	R/W	0x00	[7;6] SP2_FLD_SW_MODE [5:0] SP2_TVE_PIXEL_OS[5:0], SPOT2 TV Encoder Active Pixel offset
0xF7F	R/W	0x00	SP2_TVE_FLD_OS[1:0], SPOT2 TV Encoder Active Field offset
0xF80	R/W	0x00	SP2_TVE_FSC_FREE[7], SPOT2 TV Encoder Subcarrier run free [6:0] RESERVED
0xF9B	R/W	0x00	[7:2] RESERVED [1] SP2_PD_EN [0] SP1_PD_EN
0xF9C	R/W	0x00	SP_USE_BY_REC_NETWK_PORT [7:4] Select REC ports 9-5 to replace SP2 as display port [3:0] Select REC ports 9-5 to replace SP1 as display port

Register Descriptions for Recording Path

RECORDING WRITE BUFFER 1 CONTROL REGISTER A – 0XC00

Bit	R/W	Default	Description
7	R/W	0x0	**Reserved**
6	R/W	0x0	**FLD_INTL** Recording Format Select 0 = Frame Interleaved 1 = Field Interleaved
5:4	R/W	0x0	**REC_RESOL** Recording Resolution Select 00 = D1 01 = Half D1 10 = CIF 11 = Reserved
3:0	R/W	0x0	**CH_NUM** Incoming Channel Select [3:0] = Channel being recorded

NOTE: * SIMILAR ASSIGNMENTS TO OTHER WRITE BUFFERS (2-8) FOLLOW: 0XC01 - 0XC07 RECORDING BUFFER CONTROL REGISTER A.

RECORDING HD BUFFER 1 CONTROL REGISTER A – 0XC08

Bit	R/W	Default	Description
7	R/W	0x0	**HD_SEL** HD Channel Select for OSD 0 = SD channel 1 = HD channel
6	R/W	0x0	**FLD_INTL** **Recording Format Select** 0 = Frame Interleaved 1 = Field Interleaved
5:4	R/W	0x0	**REC_RESOL** **Recording Resolution Select** 00 = D1 01 = Half D1 10 = CIF 11 = Reserved
3:0	R/W	0x0	**CH_NUM** **Incoming Channel Select** [3:0] = Channel being recorded

NOTE: * SIMILAR ASSIGNMENTS TO OTHER HD BUFFERS (2-5) FOLLOW: 0XC09(HD2) - 0XC0C(HD5) RECORDING HD BUFFER CONTROL REGISTER A.

RECORDING WRITE BUFFER 1 CONTROL REGISTER B – 0XC10

Bit	R/W	Default	Description
7	R/W	0x0	**REC_WR_EN** Recording Buffer Enable 0 = Disable (default) 1 = Enable
6:3	R/W	0x0	**H_POS_OFFSET** Horizontal Position Offset Select 0000 = 0 0001 = 320 (6VGA), 360 0010 = 640 (6VGA), 720 0011 = 960 (6VGA), 1080 0100 = 1280 (6VGA), 1440 0101 = 1600 (6VGA), 1800 0110 = 1920 (6VGA), 2160 0111 = 2240 (6VGA), 2520 Other = Reserved Horizontal Position = REC_HSTART*4 + H_POS_OFFSET (REC_HSTART is controlled by setting register '0xc7e' and '0x C7f')
2:0	R/W	0x0	**V_POS_OFFSET** Vertical Position Offset Select 000 = 0 001 = 135 (6VGA), 144 (PAL), 120 (NTSC) 010 = 270 (6VGA), 288 (PAL), 240 (NTSC) 011 = 405 (6VGA), 432 (PAL), 360 (NTSC) 100 = 540 (6VGA), 576 (PAL), 480 (NTSC) 101 = 675 (6VGA), 720 (PAL), 600 (NTSC) 110 = 810 (6VGA), 864 (PAL), 720 (NTSC) 111 = 945 (6VGA), 1008 (PAL), 840 (NTSC) Vertical Position = REC_VSTART + V_POS_OFFSET (REC_VSTART is controlled by setting register '0xc7c' and '0x C7d')

NOTE: * SIMILAR ASSIGNMENTS TO OTHER WRITE BUFFERS (2-8) FOLLOW: 0XC11(BUFFER 2) - 0XC17(BUFFER 8) RECORDING BUFFER CONTROL REGISTER B.

RECORDING HD BUFFER 1 CONTROL REGISTER B – 0XC18

Bit	R/W	Default	Description
7	R/W	0x0	**HD_WR_EN** HD Buffer Enable 0 = Disable (default) 1 = Enable

Bit	R/W	Default	Description
6:3	R/W	0x0	**H_POS_OFFSET** Horizontal Position Offset Select 0000 = 0 0001 = 320 (6VGA), 360 0010 = 640 (6VGA), 720 0011 = 960 (6VGA), 1080 0100 = 1280 (6VGA), 1440 0101 = 1600 (6VGA), 1800 0110 = 1920 (6VGA), 2160 0111 = 2240 (6VGA), 2520 Other = Reserved Horizontal Position = REC_HSTART*4 + H_POS_OFFSET (REC_HSTART is controlled by setting register '0xc7e' and '0x C7f')
2:0	R/W	0x0	**V_POS_OFFSET** Vertical Position Offset Select 000 = 0 001 = 135 (6VGA), 144 (PAL), 120 (NTSC) 010 = 270 (6VGA), 288 (PAL), 240 (NTSC) 011 = 405 (6VGA), 432 (PAL), 360 (NTSC) 100 = 540 (6VGA), 576 (PAL), 480 (NTSC) 101 = 675 (6VGA), 720 (PAL), 600 (NTSC) 110 = 810 (6VGA), 864 (PAL), 720 (NTSC) 111 = 945 (6VGA), 1008 (PAL), 840 (NTSC) Vertical Position = REC_VSTART + V_POS_OFFSET (REC_VSTART is controlled by setting register '0xc7c' and '0x C7d')

NOTE: * SIMILAR ASSIGNMENTS TO OTHER HD BUFFERS (2-5) FOLLOW: 0XC19(HD BUFFER 2) - 0XC1C(HD BUFFER 5) RECORDING HD BUFFER CONTROL REGISTER B.

RECORD PORT 9 CUSTOM HORIZONTAL CONTROL REGISTER – 0XC32

Bit	R/W	Default	Description
7:0	R/W	0x0	HDE[7:0] Times 16

RECORD PORT 9 CUSTOM VERTICAL CONTROL REGISTER – 0XC33

Bit	R/W	Default	Description
7:0	R/W	0x0	VDE[7:0] Times 4

RECORD PORT 5 CONTROL REGISTER – 0XC34

Bit	R/W	Default	Description
7:6	R/W	0x0	**P_REC_RESOL** Output Resolution Select 00 = D1 01 = CIF (short burst special format) 10 = 4D1 (special format) 11 = BT.1120 (1080)
5	R/W	0x0	**P_FLD_INTL** Output Port Format Select 0 = Frame Interleaved 1 = Field Interleaved
4:3	R/W	0x0	**Reserved**
2:1	R/W	0x0	**P_CLK_SEL** Output Port Clock Select 00 = ¼ of record clock 01 = ½ of record clock 10 = full record clock 11 = Reserved
0	R/W	0x0	**ROEN** Output Port Buffer Enable 0 = Disable 1 = Enable record out function

RECORD PORT 5 SOURCE CONTROL ADDRESS REGISTER – 0XC35

Bit	R/W	Default	Description
7	R	0x0	**Reserved**
6:0	R/W	0x0	**R_ADDRI** Address in Source RAM

RECORD PORT 5 SOURCE CONTROL DATA REGISTER – 0XC36

Bit	R/W	Default	Description
7:6	R	0x0	Reserved
5	R/W	0x0	TBL_UPDATE Write 1 to trigger Double Buffer Update
4:0	R/W	0x0	R_MEM Select Source Buffer from the following 29 buffers 0: Record write buffer 1 1: Record write buffer 2 ... 7: Record write buffer 8 8: HD write buffer 1 9: HD write buffer 2 ... 12: HD write buffer 5 13 ~ 15: Not used 16: SPOT write buffer 1 17: SPOT write buffer 2 ... 30: SPOT write buffer 15 31: SPOT write buffer 16

RECORD PORT 5 SOURCE NUMBER REGISTER – 0XC37

Bit	R/W	Default	Description
7	R/W	0x0	Reserved
6:0	R/W	0x0	ROUT_NUM Number of Source in the list (128 is the largest)

RECORD PORT 5 CUSTOM HORIZONTAL CONTROL REGISTER – 0XC38

Bit	R/W	Default	Description
7:0	R/W	0x0	HDE[7:0] Times 16

RECORD PORT 5 CUSTOM VERTICAL CONTROL REGISTER – 0XC39

Bit	R/W	Default	Description
7:0	R/W	0x0	VDE[7:0] Times 4

RECORD PORT 6 CONTROL REGISTER – 0XC3A

Bit	R/W	Default	Description
7	R/W	0x0	**P_REC_RESOL** Output Resolution Select 00 = D1 01 = CIF (short burst special format) 10 = 4D1 (special format) 11 = BT.1120 (1080)
5	R/W	0x0	**P_FLD_INTL** Output Port Format Select 0 = Frame Interleaved 1 = Field Interleaved
4:3	R/W	0x0	**Reserved**
2:1	R/W	0x0	**P_CLK_SEL** Output Port Clock Select 00 = ¼ of record clock 01 = ½ of record clock 10 = full record clock 11 = Reserved
0	R/W	0x0	**ROEN** Output Port Buffer Enable 0 = Disable 1 = Enable record out function

RECORD PORT 6 SOURCE CONTROL ADDRESS REGISTER – 0XC3B

Bit	R/W	Default	Description
7	R	0x0	**Reserved**
6:0	R/W	0x0	**R_ADDRI** Address in Source RAM

RECORD PORT 6 SOURCE CONTROL DATA REGISTER – 0XC3C

Bit	R/W	Default	Description
7:4	R/W	0x0	Reserved
5	R/W	0x0	TBL_UPDATE Write 1 to trigger Double Buffer Update
4:0	R/W	0x0	R_MEM Select Source Buffer from the following 29 buffers 0: Record write buffer 1 1: Record write buffer 2 ... 7: Record write buffer 8 8: HD write buffer 1 9: HD write buffer 2 ... 12: HD write buffer 5 13 ~ 15: Not used 16: SPOT write buffer 1 17: SPOT write buffer 2 ... 30: SPOT write buffer 15 31: SPOT write buffer 16

RECORD PORT 6 SOURCE NUMBER REGISTER – 0XC3D

Bit	R/W	Default	Description
7	R/W	0x0	Reserved
6:0	R/W	0x0	ROUT_NUM Number of Source in the list (128 is the largest)

RECORD PORT 6 CUSTOM HORIZONTAL CONTROL REGISTER – 0XC3E

Bit	R/W	Default	Description
7:0	R/W	0x0	HDE[7:0] Times 16

RECORD PORT 6 CUSTOM VERTICAL CONTROL REGISTER – 0XC3F

Bit	R/W	Default	Description
7:0	R/W	0x0	VDE[7:0] Times 4

RECORD PORT 7 CONTROL REGISTER – 0XC40

Bit	R/W	Default	Description
7:6	R/W	0x0	**P_REC_RESOL** Output Resolution Select 00 = D1 01 = CIF (short burst special format) 10 = 4D1 (special format) 11 = BT.1120 (1080)
5	R/W	0x0	**P_FLD_INTL** Output Port Format Select 0 = Frame Interleaved 1 = Field Interleaved
4:3	R/W	0x0	**Reserved**
2:1	R/W	0x0	**P_CLK_SEL** Output Port Clock Select 00 = ¼ of record clock 01 = ½ of record clock 10 = full record clock 11 = Reserved
0	R/W	0x0	**ROEN** Output Port Buffer Enable 0 = Disable 1 = Enable record out function

RECORD PORT 7 SOURCE CONTROL ADDRESS REGISTER – 0XC41

Bit	R/W	Default	Description
7	R	0x0	**Reserved**
6:0	R/W	0x0	**R_ADDRI** Address in Source RAM

RECORD PORT 7 SOURCE CONTROL DATA REGISTER – 0XC42

Bit	R/W	Default	Description
7:4	R/W	0x0	Reserved
5	R/W	0x0	TBL_UPDATE Write 1 to trigger Double Buffer Update
4:0	R/W	0x0	R_MEM Select Source Buffer from the following 29 buffers 0: Record write buffer 1 1: Record write buffer 2 ... 7: Record write buffer 8 8: HD write buffer 1 9: HD write buffer 2 ... 12: HD write buffer 5 13 ~ 15: Not used 16: SPOT write buffer 1 17: SPOT write buffer 2 ... 30: SPOT write buffer 15 31: SPOT write buffer 16

RECORD PORT 7 SOURCE NUMBER REGISTER – 0XC43

Bit	R/W	Default	Description
7	R/W	0x0	Reserved
6:0	R/W	0x0	ROUT_NUM Number of Source in the list (128 is the largest)

RECORD PORT 7 CUSTOM HORIZONTAL CONTROL REGISTER – 0XC44

Bit	R/W	Default	Description
7:0	R/W	0x0	HDE[7:0] Times 16

RECORD PORT 7 CUSTOM VERTICAL CONTROL REGISTER – 0XC45

Bit	R/W	Default	Description
7:0	R/W	0x0	VDE[7:0] Times 4

RECORD PORT 8 CONTROL REGISTER – 0XC46

Bit	R/W	Default	Description
7:6	R/W	0x0	**P_REC_RESOL** Output Resolution Select 00 = D1 01 = CIF (short burst special format) 10 = 4D1 (special format) 11 = BT.1120 (1080)
5	R/W	0x0	**P_FLD_INTL** Output Port Format Select 0 = Frame Interleaved 1 = Field Interleaved
4:3	R/W	0x0	**Reserved**
2:1	R/W	0x0	**P_CLK_SEL** Output Port Clock Select 00 = ¼ of record clock 01 = ½ of record clock 10 = full record clock 11 = Reserved
0	R/W	0x0	**ROEN** Output Port Buffer Enable 0 = Disable 1 = Enable record out function

RECORD PORT 8 SOURCE CONTROL ADDRESS REGISTER – 0XC47

Bit	R/W	Default	Description
7	R	0x0	**Reserved**
6:0	R/W	0x0	**R_ADDRI** Address in Source RAM

RECORD PORT 8 SOURCE CONTROL DATA REGISTER – 0XC48

Bit	R/W	Default	Description
7:6	R/W	0x0	Reserved
5	R/W	0x0	TBL_UPDATE Write 1 to trigger Double Buffer Update
4:0	R/W	0x0	R_MEM Select Source Buffer from the following 29 buffers 0: Record write buffer 1 1: Record write buffer 2 ... 7: Record write buffer 8 8: HD write buffer 1 9: HD write buffer 2 ... 12: HD write buffer 5 13 ~ 15: Not used 16: SPOT write buffer 1 17: SPOT write buffer 2 ... 30: SPOT write buffer 15 31: SPOT write buffer 16

RECORD PORT 8 SOURCE NUMBER REGISTER – 0XC49

Bit	R/W	Default	Description
7	R/W	0x0	Reserved
6:0	R/W	0x0	ROUT_NUM Number of Source in the list (128 is the largest)

RECORD PORT 8 CUSTOM HORIZONTAL CONTROL REGISTER – 0XC4A

Bit	R/W	Default	Description
7:0	R/W	0x0	HDE[7:0] Times 16

RECORD PORT 8 CUSTOM VERTICAL CONTROL REGISTER – 0XC4B

Bit	R/W	Default	Description
7:0	R/W	0x0	VDE[7:0] Times 4

RECORD PORT OPERATING MODE SELECT REGISTER – 0XC4D

Bit	R/W	Default	Description
7	R/W	0x0	**ADV[1]** Bottom field low speed update algorithm select 1 = 54 /27 MHz, 0 = normal
6	R/W	0x0	**ADV[0]** Top field low speed update algorithm select 1 = 54 /27 MHz, 0 = normal
5	R/W	0x0	**AUTO** Enable field mode automatic correction 0 = disable (default) 1 = enable
4	R/W	0x0	**S56** BT.1120 PAL 50 /60 Hz Selection 0 = 50 Hz (default) 1 = 60 Hz
3	R/W	0x0	**P9_INT_FMI** Port 9 Interlaced FMI Mode Control 0 = Normal (default) 1 = Turn on
2	R/W	0x0	**TST** Record Source Select 0 = Live mode (default) 1 = Internal test pattern mode
1	R/W	0x0	**PALNT** Record Standard Select 0 = NTSC mode (default) 1 = PAL mode
0	R/W	0x0	**SWITCH** Limit Motion Circuitry Read / Write Activity 0 = Disable (default) 1 = Enable

OUTPUT PIN SET 1 CONTROL REGISTER – 0XC4E

Bit	R/W	Default	Description
7:4	R/W	0x0	PIN_SRC_SEL Source 1 Select 1111 = port 8 output high byte 1110 = port 8 output low byte 1101 = port 7 output high byte 1100 = port 7 output low byte 1011 = port 6 output high byte 1010 = port 6 output low byte 1001 = port 5 output high byte 1000 = port 5 output low byte 0111 = port 9 output high byte 0110 = port 9 output low byte Others = pin out is always '0' (default)
3	R/W	0x0	PIN_CLK_POL_SEL Clock Polarity Select 0 = normal, 1 = inverted
2	R/W	0x0	PIN_WIDTH Port width Select 0 = 8 bit, 1 = 16 bit
1:0	R/W	0x0	PIN_CLK_SEL Pin Clock Select 00 = ¼ of record clock 01 = ½ of record clock 10 = full record clock 11 = Reserved

OUTPUT PIN SET 2 CONTROL REGISTER – 0XC4F

Bit	R/W	Default	Description
7:4	R/W	0x4	PIN_SRC_SEL Source 1 Select[3:0] 1111 = port 8 output high byte 1110 = port 8 output low byte 1101 = port 7 output high byte 1100 = port 7 output low byte 1011 = port 6 output high byte 1010 = port 6 output low byte 1001 = port 5 output high byte 1000 = port 5 output low byte 0111 = port 9 output high byte 0110 = port 9 output low byte Others = pin out is always '0' (default)

Bit	R/W	Default	Description
3	R/W	0x0	**PIN_CLK_POL_SEL** Clock Polarity Select 0 = normal, 1 = inverted
2	R/W	0x0	**PIN_WIDTH** Port width Select 0 = 8 bit, 1 = 16 bit
1:0	R/W	0x0	**PIN_CLK_SEL** Pin Clock Select 00 = ¼ of record clock 01 = ½ of record clock 10 = full record clock 11 = Select main display Hsync, Vsync

OUTPUT PIN SET 3 CONTROL REGISTER – 0XC50

Bit	R/W	Default	Description
7	R/W	0x8	**PIN_SRC_SEL** Source 1 Select[3:0] 1111 = port 8 output high byte 1110 = port 8 output low byte 1101 = port 7 output high byte 1100 = port 7 output low byte 1011 = port 6 output high byte 1010 = port 6 output low byte 1001 = port 5 output high byte 1000 = port 5 output low byte (default) 0111 = port 9 output high byte 0110 = port 9 output low byte Others = pin out is always '0'
3	R/W	0x0	**PIN_CLK_POL_SEL** Clock Polarity Select 0 = normal, 1 = inverted
2	R/W	0x0	**PIN_WIDTH** Port width Select 0 = 8 bit, 1 = 16 bit
1:0	R/W	0x0	**PIN_CLK_SEL** Pin Clock Select 00 = ¼ of record clock 01 = ½ of record clock 10 = full record clock 11 = Reserved

OUTPUT PIN SET 4 CONTROL REGISTER – 0XC51

Bit	R/W	Default	Description
7	R/W	0xc	**PIN_SRC_SEL** Source 1 Select[3:0] 1111 = port 8 output high byte 1110 = port 8 output low byte 1101 = port 7 output high byte 1100 = port 7 output low byte (default) 1011 = port 6 output high byte 1010 = port 6 output low byte 1001 = port 5 output high byte 1000 = port 5 output low byte 0111 = port 9 output high byte 0110 = port 9 output low byte
3	R/W	0x0	**PIN_CLK_POL_SEL** Clock Polarity Select 0 = normal, 1 = inverted
2	R/W	0x0	**PIN_WIDTH** Port width Select 0 = 8 bit, 1 = 16 bit
1:0	R/W	0x0	**PIN_CLK_SEL** Pin Clock Select 00 = ¼ of record clock 01 = ½ of record clock 10 = full record clock 11 = Reserved

PORT 9 CONTROL REGISTER – 0XC52

Bit	R/W	Default	Description
7:6	R/W	0x0	**P_REC_RESOL** Output Resolution Select 00 = D1 01 = CIF (short burst special format) 10 = 4D1 (special format) 11 = BT.1120 (1080)
5	R/W	0x0	**P_FLD_INTL** Output Port Format Select 0 = Frame Interleaved 1 = Field Interleaved
4:3	R/W	0x0	**Reserved**

Bit	R/W	Default	Description
2:1	R/W	0x0	P_CLK_SEL Output Port Clock Select 00 = ¼ of record clock 01 = ½ of record clock 10 = full record clock 11 = Reserved
0	R/W	0x0	ROEN Output Port Buffer Enable 0 = Disable 1 = Enable record out function

PORT 9 CONTROL ADDRESS REGISTER – 0XC53

Bit	R/W	Default	Description
7	R	0x0	Reserved
6:0	R/W	0x0	R_ADDRI Address in Source RAM

PORT 9 CONTROL DATA REGISTER – 0XC54

Bit	R/W	Default	Description
7:6	R/W	0x0	Reserved
5	R/W	0x0	TBL_UPDATE Write 1 to trigger Double Buffer Update
4:0	R/W	0x0	R_MEM Select Source Buffer from the following 29 buffers 0: Record write buffer 1 1: Record write buffer 2 … 7: Record write buffer 8 8: HD write buffer 1 9: HD write buffer 2 … 12: HD write buffer 5 13 ~ 15: Not used 16: SPOT write buffer 1 17: SPOT write buffer 2 … 30: SPOT write buffer 15 31: SPOT write buffer 16

PORT 9 SOURCE NUMBER REGISTER – 0XC55

Bit	R/W	Default	Description
7	R/W	0x0	**NET_FREE** Enable Free Running Port 9 1 = enable, 0 = normal mode
6:0	R/W	0x0	**ROUT_NUM** Number of Source in the list (128 is the largest)

MISC. CONTROL REGISTER 1 – 0XC56

Bit	R/W	Default	Description
7	R/W	0x0	**SPREAD** Spread read sync option 1 = spread read sync, 0 = no spread
6	R/W	0x0	**RST_SEL** Select different MCLK reset width in FIFO 1 = Different reset, 0 = Same reset
5	R/W	0x0	**SADV[1]** Bottom field low speed update algorithm select 1 = 54 /27 MHz, 0 = normal ADV[1] for SPOT
4	R/W	0x0	**SADV[0]** Top field low speed update algorithm select 1 = 54 /27 MHz, 0 = normal ADV[0] for SPOT
3	R/W	0x0	**HOVER** Horizontal Control Override in 6 VGA mode
2:0	R/W	0x0	**FRSC_SEL** Select record side FRSC source 0 = Port 5, 1 = Port 6, 2 = Port 7 , 3 = Port 8 , 4 = Port 9 , Others = Port 5

4D1 AND QUAD 2ND WRITE HORIZONTAL MARGIN REGISTER – 0XC57

Bit	R/W	Default	Description
7:0	R/W	0x0	**HMARGIN[7:0]** Unit is hcnt. Increase the 2nd write hblank by this number

MISC. CONTROL REGISTER 2 – 0XC58

Bit	R/W	Default	Description
7	R/W	0x0	**WINOK_ENA[1]** Limit Record unit start time if using SPOT buffers 1 = disable (default) 0 = enable
6	R/W	0x0	**WINOK_ENA[0]** 1 = Limit Record unit start time if using record buffers 1 = disable (default) 0 = enable
5:4	R/W	0x0	**WQL** Record Write Buffer Request Level Control (default = 1)
3:0	R/W	0x0	**DIS4** Enable no video reset frame rate control unit Bit 0: Reserved Bit 1: ROUT5 – ROUT6 Bit 2: ROUT7 – ROUT8 Bit 3: ROUT9

MISC. CONTROL REGISTER 3 – 0XC59

Bit	R/W	Default	Description
7:6	R/W	0x0	**OPT[7:6]** SPOT Write Buffer Request Level Control (default = 1)
5	R/W	0x0	**OPT[5]** SPOT Buffer Vertical Invert Line Number Option
4	R/W	0x0	**OPT[4]** Record Buffer Vertical Invert Line Number Option
3:2	R/W	0x0	**OPT[3:2]** SPOT Buffer Update Option Select
1:0	R/W	0x0	**OPT[1:0]** Record Buffer Update Option Select

RECORD HDE CONTROL REGISTER – 0XC5A

Bit	R/W	Default	Description
7:3	R/W	0x0	**SEL_HDE** HDE selection for Port 9(bit 0) and Port 5(bit 1) ~ Port 8(bit 4) 0: Use normal HDE value 1: Use custom HDE value(0xc32: Port 9, 0xc38: Port 5, 0xc3e: Port 6, 0xc44: Port 7, 0xc4a: Port 8)
2:0	R/W	0x0	**Reserved**

RECORD VDE CONTROL REGISTER – 0XC5B

Bit	R/W	Default	Description
7:3	R/W	0x0	**SEL_VDE** VDE selection for Port 9(bit 0) and Port 5(bit 1) ~ Port 8(bit 4) 0: Use normal VDE value 1: Use custom VDE value(0xc33: Port 9, 0xc39: Port 5, 0xc3f: Port 6, 0xc45: Port 7, 0xc4b: Port 8)
2:0	R/W	0x0	**Reserved**

SPECIAL OSD CONTROL REGISTER – 0XC5C

Bit	R/W	Default	Description
7:3	R	0x0	**Reserved**
2	R/W	0x0	**CHG_MSK_ON** Change mask on, off control. If this bit is '1', some write buffer bank numbers are ignored when those write buffers have longer frame rate than normal one. 0: Normal 0: Bank number is ignored when frame rate is longer than normal
1	R/W	0x0	**Reserved**
0	R/W	0x0	**CHG_MSK_WEIGHT** Longer frame is defined by the this field 1: More than 2-frame period 0: More than 1-frame period

SPECIAL OSD CONTROL REGISTER – 0XC5D

Bit	R/W	Default	Description
7:4	R/W	0x0	**CH9_OSD** 16 QCIF OSD type selection for Port 5(bit 0) ~ Port 8(bit 3) 0: 16 QCIF, 1: 9-channel display 0: 16 QCIF, 1: 9-channel display
3:0	R/W	0x0	**QCIF_OSD_ON** Special OSD(16 QCIF/9-CH display) on/off control for Port 5(bit 0) ~ Port 8(bit 3) 0: Normal OSD, 1: Special OSD 0: Normal OSD, 1: Special OSD

SPECIAL OSD BOUNDARY ON/OFF CONTROL FOR PORT 5 ~ PORT 6 – 0XC5E

Bit	R/W	Default	Description
7:4	R/W	0x0	**OSD_SEP_OFF_P6** Boundary on/off control for port 6 Bit 0: Left-top boundary on/off(0: on, 1: off) Bit 1: Right-top boundary on/off(0: on, 1: off) Bit 2: Left-bottom boundary on/off(0: on, 1: off) Bit 3: Right-bottom boundary on/off(0: on, 1: off)

Bit	R/W	Default	Description
3:0	R/W	0x0	**OSD_SEP_OFF_P5** Boundary on/off control for port 5 Bit 0: Left-top boundary on/off(0: on, 1: off) Bit 1: Right-top boundary on/off(0: on, 1: off) Bit 2: Left-bottom boundary on/off(0: on, 1: off) Bit 3: Right-bottom boundary on/off(0: on, 1: off)

SPECIAL OSD BOUNDARY ON/OFF CONTROL FOR PORT 7 ~ PORT 8 – 0XC5F

Bit	R/W	Default	Description
7:4	R/W	0x0	**OSD_SEP_OFF_P8** Boundary on/off control for port 6 Bit 0: Left-top boundary on/off(0: on, 1: off) Bit 1: Right-top boundary on/off(0: on, 1: off) Bit 2: Left-bottom boundary on/off(0: on, 1: off) Bit 3: Right-bottom boundary on/off(0: on, 1: off)
3:0	R/W	0x0	**OSD_SEP_OFF_P7** Boundary on/off control for port 5 Bit 0: Left-top boundary on/off(0: on, 1: off) Bit 1: Right-top boundary on/off(0: on, 1: off) Bit 2: Left-bottom boundary on/off(0: on, 1: off) Bit 3: Right-bottom boundary on/off(0: on, 1: off)

SPECIAL OSD CONTROL REGISTER FOR PORT 9 – 0XC60

Bit	R/W	Default	Description
7:6	R/W	0x0	**Reserved**
5	R/W	0x0	**CH9_OSD** 16 QCIF OSD type selection for Port 9 0: 16 QCIF, 1: 9-channel display 0: 16 QCIF, 1: 9-channel display
4	R/W	0x0	**QCIF_OSD_ON** Special OSD(16 QCIF/9-CH display) on/off control for Port 9 0: Normal OSD, 1: Special OSD 0: Normal OSD, 1: Special OSD
3:0	R/W	0x0	**OSD_SEP_OFF_P9** Boundary on/off control for port 5 Bit 0: Left-top boundary on/off(0: on, 1: off) Bit 1: Right-top boundary on/off(0: on, 1: off) Bit 2: Left-bottom boundary on/off(0: on, 1: off) Bit 3: Right-bottom boundary on/off(0: on, 1: off)

SPOT OSD ON/OFF CONTROL REGISTER – 0XC61

Bit	R/W	Default	Description
7:5	R/W	0x0	Reserved
4:0	R/W	0x0	SPOT_OSD_ON SPOT OSD on/off control for port 5(bit 0) ~ port 9(bit 4) 0: Record OSD, 1: SPOT OSD If SPOT OSD is on, time is displayed only one place

RECORD BUFFER FREEZE CONTROL REGISTER A – 0XC64

Bit	R/W	Default	Description
7:0	R/W	0x0	REC_FREEZE[7:0] Freeze control for record buffer 1(bit 0) ~ record buffer 8(bit 7) 1 = Channel Freeze 0 = Normal

SPOT BUFFER FREEZE CONTROL REGISTER A – 0XC66

Bit	R/W	Default	Description
7:0	R/W	0x0	SPOT_FREEZE[7:0] Freeze control for SPOT buffer 1(bit 0) ~ SPOT buffer 8(bit 7) 1 = Channel Freeze 0 = Normal

SPOT BUFFER FREEZE CONTROL REGISTER B – 0XC67

Bit	R/W	Default	Description
7:0	R/W	0x0	SPOT_FREEZE[15:8] Freeze control for SPOT buffer 9(bit 0) ~ SPOT buffer 16(bit 7) 1 = Channel Freeze 0 = Normal

CUSTOM CLOCK CONTROL REGISTER – 0XC68

Bit	R/W	Default	Description
7:6	R	0x0	Reserved
5:4	R/W	0x0	SHADOW Window Position Shadow Register Select 0 = recording, 1 = SPOT, 2 = Miscellaneous
3:0	R/W	0x0	Reserved

INTERLACED FRAME OUTPUT MODE CONTROL REGISTER – 0XC69

Bit	R/W	Default	Description
7:4	R/W	0x0	**INT_FMI** Interlaced Frame Control Port 5(bit 0) to Port 8(bit 3) 0 = Progressive Frame (default) 1 = Interlaced Frame
3:0	R/W	0x0	**Reserved**

'WR_PAGE' REFERENCE SELECTION CONTROL REGISTER A(WRITE BUFFER INDEX) – 0XC6A

Bit	R/W	Default	Description
7:6	R	0x0	**Reserved**
5:0	R/W	0x0	**WR_BUF_ADDR** wr_buffer index for selecting 'wr_page' reference from read port 0 ~ 7 : recording write buffer 0 ~ 7 8 ~ 23 : SPOT write buffer 0 ~ 15 24 ~ 28 : PB write buffer 0 ~ 4

'WR_PAGE' REFERENCE SELECTION CONTROL REGISTER B(READ PORT INDEX) – 0XC6B

Bit	R/W	Default	Description
7:5	R	0x0	**Reserved**
4	R/W	0x0	**WR_PAGE_SEP** 0 = Use one wr_page reference 1 = Use separated wr_page reference according to the write buffer
3	R	0x0	**Reserved**
2:0	R/W	0x0	**WR_PAGE_SEL** wr_page reference selection value 0 = port5 wr_page reference 1 = port6 wr_page reference 2 = port7 wr_page reference 3 = port8 wr_page reference 4 = Port 9 wr_page reference the others = port5 wr_page reference

NEW FRSC CONTROL REGISTER B – 0XC6C

Bit	R/W	Default	Description
7	R/W	0x0	**Reserved**
6	R/W	0x0	**FLD_HVCNT_SEL** Field generation option in the hvcnt_rout 0 = Old one 1 = New one

Bit	R/W	Default	Description
5	R/W	0x0	**FLD_CCIR_SEL** Field generation option in the ccir_out_fmt 0 = Old one 1 = New one
4	R/W	0x0	**WR_BUF_FLI_STOP** Write buffer stop control selection between frame and field stop 0 = Frame stop 1 = Field stop
3	R/W	0x0	**WR_BUF_STOP** Read bank repeat option when write buffer is stop in the 4-frame field mode 0 = Repeat one field 1 = Repeat one frame
2	R/W	0x0	**FLI_RD_STOP** Read bank repeat option when bank stop condition is occurred in the 4-frame field mode 0 = Repeat one field 1 = Repeat one frame
1	R/W	0x0	**Reserved**
0	R/W	0x0	**RD_FRSC_FLI_EN** Read side frame rate control enable for field mode 0 = Original frame rate control(bank is increased without checking relation between read and write bank values) 1 = New frame rate control in read side(bank is increased if some condition is met between read and write bank values)

PB IGNORE BIT CONTROL REGISTER – 0XC6D

Bit	R/W	Default	Description
7:0	R/W	0x0	**PB_IGNORE** PB ignore bit on/off control for each port 5(bit 0) ~ port 8(bit 3) 0 = Ignore bit disable 1 = Ignore bit enable
3:0	R/W	0x0	**Reserved**

PB IGNORE VALUE REGISTER 1 – 0XC6E

Bit	R/W	Default	Description
7:4	R/W	0x0	**PB_IG_DATA1** 2nd PB ignore bit value
3:0	R/W	0x0	**PB_IG_DATA0** 1st PB ignore bit value

PB IGNORE VALUE REGISTER 2 – 0XC6F

Bit	R/W	Default	Description
7:4	R/W	0x0	**PB_IG_DATA3** 4th PB ignore bit value
3:0	R/W	0x0	**PB_IG_DATA2** 3rd PB ignore bit value

BACKGROUND COLOR FOR CB – 0XC70

Bit	R/W	Default	Description
7:0	R/W	0x0	**BG_CB** Background color of Cb

BACKGROUND COLOR FOR CR – 0XC71

Bit	R/W	Default	Description
7:0	R/W	0x0	**BG_CR** Background color of Cr

BACKGROUND COLOR FOR Y – 0XC72

Bit	R/W	Default	Description
7:0	R/W	0x0	**BG_Y** Background color of Y

BACKGROUND ON/OFF CONTROL 1 FOR RECORD WRITE BUFFER – 0XC73

Bit	R/W	Default	Description
7:0	R/W	0x0	**BG_ON_REC[7:0]** Background on/off control for record write buffer 1(bit 0) ~ buffer 8(bit 7)

BACKGROUND ON/OFF CONTROL 1 FOR SPOT WRITE BUFFER – 0XC75

Bit	R/W	Default	Description
7:0	R/W	0x0	**BG_ON_SPOT[7:0]** Background on/off control for SPOT write buffer 1(bit 0) ~ buffer 8(bit 7)

BACKGROUND ON/OFF CONTROL 2 FOR SPOT WRITE BUFFER – 0XC76

Bit	R/W	Default	Description
7:0	R/W	0x0	**BG_ON_SPOT[15:8]** Background on/off control for SPOT write buffer 9(bit 0) ~ buffer 16(bit 7)

NEW NON-REAL TIME FIELD SWITCHING MODE FOR PORT 5 ~ PORT 9 – 0XC77

Bit	R/W	Default	Description
7:5	R/W	0x0	Reserved
4:0	R/W	0x0	NEW_FLI_SW New field switching mode for port 5(bit 0) ~ port 9(bit 4) 0 = Original 1 = New field switching

NEW FIELD SWITCHING MODE FIELD SELECT FOR PORT 5 ~ PORT 9 – 0XC78

Bit	R/W	Default	Description
7:5	R/W	0x0	Reserved
4:0	R/W	0x0	NEW_FLI_SW_SEL Field selection of new field switching mode for port 5(bit 0) ~ port 9(bit 4) 0 = Even 1 = Odd

4-FRAME FIELD INTERLEAVED READ MODE FOR PORT 1 ~ PORT 8 – 0XC79

Bit	R/W	Default	Description
7:4	R/W	0x0	FLI_RD Field interleaved read mode with 4 frames for port 5(bit 0) ~ port 8(bit 3) 0 = 2 frames 1 = 4 frames
3:0	R/W	0x0	Reserved

NEW NON-REAL TIME BANK CONTROL FOR PORT 5 ~ PORT 9 – 0XC7A

Bit	R/W	Default	Description
7:5	R/W	0x0	Reserved
4:0	R/W	0x0	FLD_BANK_INC Read bank number control in the field mode for port 5(bit 0) ~ port 9(bit 4) 0 = Original 1 = Bank is increased with real time frame rate

DRAM PITCH OF SPOT DISPLAY – 0XC7B

Bit	R/W	Default	Description
7:0	R/W	0xB4	REC_PITCH DRAM pitch of SPOT display (16 pixel unit)

VERTICAL START POSITION OF RECORD WRITE BUFFER REGISTER A – 0XC7C

Bit	R/W	Default	Description
7:0	R/W	0x0	REC_VSTART[7:0] LSB of vertical start line

VERTICAL START POSITION OF RECORD WRITE BUFFER REGISTER B – 0XC7D

Bit	R/W	Default	Description
7:4	R/W	0x0	Reserved
3:0	R/W	0x0	REC_VSTART[11:8] MSB of vertical start line

HORIZONTAL START POSITION OF RECORD WRITE BUFFER REGISTER A – 0XC7E

Bit	R/W	Default	Description
7:0	R/W	0x0	REC_HSTART[7:0] LSB of horizontal start pixel (4 pixel unit)

HORIZONTAL START POSITION OF RECORD WRITE BUFFER REGISTER B – 0XC7F

Bit	R/W	Default	Description
7:2	R/W	0x0	Reserved
1:0	R/W	0x0	REC_HSTART[9:8] MSB of horizontal start pixel (4 pixel unit)

VERTICAL START POSITION OF SPOT WRITE BUFFER REGISTER A – 0XC80

Bit	R/W	Default	Description
7:0	R/W	0x0	SPOT_VSTART[7:0] LSB of vertical start line

VERTICAL START POSITION OF SPOT WRITE BUFFER REGISTER B – 0XC81

Bit	R/W	Default	Description
7:4	R/W	0x0	Reserved
3:0	R/W	0x0	SPOT_VSTART[11:8] LSB of vertical start line

HORIZONTAL START POSITION OF SPOT WRITE BUFFER REGISTER A – 0XC82

Bit	R/W	Default	Description
7:0	R/W	0x0	SPOT_HSTART[7:0] LSB of horizontal start pixel (4 pixel unit)

HORIZONTAL START POSITION OF SPOT WRITE BUFFER REGISTER B – 0XC83

Bit	R/W	Default	Description
7:2	R/W	0x0	Reserved
1:0	R/W	0x0	SPOT_HSTART[9:8] MSB of horizontal start pixel (4 pixel unit)

QCIF MODE ON/OFF CONTROL REGISTER FOR SPOT WRITE BUFFER 1 ~ 8 – 0XC8C

Bit	R/W	Default	Description
7:0	R/W	0x0	**QCIF_MODE[7:0]** QCIF/9-CH mode on/off control for SPOT write buffer 1(bit 0) ~ 8(bit 7) 0 = Normal mode 1 = QCIF/9-CH mode

QCIF MODE ON/OFF CONTROL REGISTER FOR SPOT WRITE BUFFER 9 ~ 16 – 0XC8D

Bit	R/W	Default	Description
7:0	R/W	0x0	**QCIF_MODE[15:8]** QCIF/9-CH mode on/off control for SPOT write buffer 9(bit 0) ~ 16(bit 7) 0 = Normal mode 1 = QCIF/9-CH mode

QCIF TYPE SELECTION REGISTER FOR SPOT WRITE BUFFER 1 ~ 8 – 0XC8E

Bit	R/W	Default	Description
7:0	R/W	0x0	**CH9_MODE[7:0]** Selection between 16 QCIF and 9-channel display for SPOT write buffer 1(bit 0) ~ 8(bit 7) 0 = 16 QCIF 1 = 9-channel display

QCIF TYPE SELECTION REGISTER FOR SPOT WRITE BUFFER 9 ~ 16 – 0XC8F

Bit	R/W	Default	Description
7:0	R/W	0x0	**CH9_MODE[15:8]** Selection between 16 QCIF and 9-channel display for SPOT write buffer 9(bit 0) ~ 16(bit 7) 0 = 16 QCIF 1 = 9-channel display

SPOT RECORDING WRITE BUFFER 1 CONTROL REGISTER A – 0XC90

Bit	R/W	Default	Description
7	R	0x0	**Reserved**
6	R/W	0x0	**FLD_INTL** Recording Format Select 0 = Frame Interleaved 1 = Field Interleaved

Bit	R/W	Default	Description
5:4	R/W	0x0	REC_RESOL Recording Resolution Select 00 = D1 01 = Half D1 10 = CIF 11 = VGA (640)
3:0	R/W	0x0	CH_NUM Incoming Channel Select [3:0] = Channel being recorded

NOTE: * SIMILAR ASSIGNMENTS TO OTHER WRITE BUFFERS (2-16) FOLLOW: 0XC91 - 0XC9F SPOT RECORDING BUFFER CONTROL REGISTER A.

SPOT RECORDING WRITE BUFFER 1 CONTROL REGISTER B – 0XCA0

Bit	R/W	Default	Description
7	R/W	0x0	REC_WR_EN Recording Buffer Enable 0 = Disable (default) 1 = Enable
6:3	R/W	0x0	H_POS_OFFSET Horizontal Position Offset Select 0000 = 0 0001 = 360(D1, QAUD and CIF), 240(9-CH), 180(QCIF) 0010 = 720(D1, QAUD and CIF), 480(9-CH), 360(QCIF) 0011 = 1080(D1, QAUD and CIF), 720(9-CH), 540(QCIF) 0100 = 1440(D1, QAUD and CIF), 960(9-CH), 720(QCIF) 0101 = 1800(D1, QAUD and CIF), 1200(9-CH), 900(QCIF) 0110 = 2160(D1, QAUD and CIF), 1440(9-CH), 1080(QCIF) 0111 = 2520(D1, QAUD and CIF), 1680(9-CH), 1260(QCIF) Other = Reserved Horizontal Position = SPOT_HSTART*4 + H_POS_OFFSET (SPOT_HSTART is controlled by setting register ‘0xc82’ and ‘0x C83’)

Bit	R/W	Default	Description
2:0	R/W	0x0	V_POS_OFFSET Vertical Position Offset Select 000 = 0 001 = 144 (PAL), 120 (NTSC), 192(PAL 9-CH), 144(PAL QCIF), 160(NTSC 9-CH), 120(NTSC QCIF) 010 = 288 (PAL), 240 (NTSC) 384(PAL 9-CH), 288(PAL QCIF), 320(NTSC 9-CH), 240(NTSC QCIF) 011 = 432 (PAL), 360 (NTSC) 576(PAL 9-CH), 432(PAL QCIF), 480(NTSC 9-CH), 360(NTSC QCIF) 100 = 576 (PAL), 480 (FMI and NTSC) 768(PAL 9-CH), 576(PAL QCIF), 640(NTSC 9-CH), 480(NTSC QCIF) 101 = 720 (PAL), 600 (NTSC) 960(PAL 9-CH), 720(PAL QCIF), 800(NTSC 9-CH), 600(NTSC QCIF) 110 = 1152 (PAL), 960 (NTSC) 1152(PAL 9-CH), 864(PAL QCIF), 960(NTSC 9-CH), 720(NTSC QCIF) 111 = 1296 (PAL), 1080 (NTSC) 1344(PAL 9-CH), 1008(PAL QCIF), 1120(NTSC 9-CH), 840(NTSC QCIF) Vertical Position = SPOT_VSTART + V_POS_OFFSET (SPOT_VSTART is controlled by setting register '0xc80' and '0x C81')

NOTE: * SIMILAR ASSIGNMENTS TO OTHER WRITE BUFFERS (2-16) FOLLOW: 0XCA1 - 0XCAF SPOT RECORDING BUFFER CONTROL REGISTER B.

READ PORT MISCELLANEOUS CONTROL REGISTER– 0XCBC

Bit	R/W	Default	Description
7:5	R	0x0	Reserved
4:0	R/W	0x0	update_sel Record OSD register update method selection for port 5(bit 0) ~ port 9(bit 4) 0 = update register when register is written 1 = update registers in the sync period if update_act(0xCBD) is on

READ PORT MISCELLANEOUS CONTROL REGISTER– 0XCBD

Bit	R/W	Default	Description
7:5	R	0x0	Reserved
4:0	R/W	0x0	update_act Record OSD register sync update on/off control for port 5(bit 0) ~ port 9(bit 4) 0 = sync register update off 1 = sync register update on

READ PORT MISCELLANEOUS CONTROL REGISTER– 0XCBE

Bit	R/W	Default	Description
7:5	R	0x0	Reserved
4:0	R/W	0x0	update_fld_sel Record OSD register sync update field selection for port 5(bit 0) ~ port 9(bit 4) 0 = even field 1 = odd field

READ PORT MISCELLANEOUS CONTROL REGISTER– 0XCC4

Bit	R/W	Default	Description
7:1	R	0x0	Reserved
0	R/W	0x1	FIRST_LINE_CLR First line clear option in the Quad mode 0 = original 1 = Line increase is cleared by quad start line indication signal

BACKGROUND BUFFER INDICATION REGISTER 1 – 0XCC8

Bit	R/W	Default	Description
7:0	R/W	0x0	REC_EN[7:0] Background buffer indication for record buffer 1(bit 0) ~ buffer 8(bit 1) 0 = disable 1 = enable

BACKGROUND BUFFER INDICATION REGISTER 2 – 0XCC9

Bit	R/W	Default	Description
7:5	R/W	0x0	Reserved
4:0	R/W	0x0	HD_EN[4:0] Background buffer indication for HD buffer 1(bit 0) ~ buffer 5(bit 4) 0 = disable 1 = enable

SECOND RECORD BUFFER DRAM CONTROL REGISTER 1 – 0XCCA

Bit	R/W	Default	Description
7:0	R/W	0x0	REC_2ND[7:0] Second record DRAM buffer enable for record write buffer 1(bit 0) ~ buffer 8(bit 7) 0 = disable 1 = enable

SECOND HD BUFFER DRAM CONTROL REGISTER 2 – 0XCCB

Bit	R/W	Default	Description
7:5	R/W	0x0	Reserved
4:0	R/W	0x0	HD_2ND[7:0] Second record DRAM buffer enable for HD write buffer 1(bit 0) ~ buffer 5(bit 4) 0 = disable 1 = enable

SECOND SPOT DRAM BUFFER CONTROL REGISTER 1 – 0XCCC

Bit	R/W	Default	Description
7:0	R/W	0x0	SPOT_2ND[7:0] Second record DRAM buffer enable for SPOT write buffer 1(bit 0) ~ buffer 8(bit 7) 0 = disable 1 = enable

SECOND SPOT DRAM BUFFER CONTROL REGISTER 2 – 0XCCD

Bit	R/W	Default	Description
7:0	R/W	0x0	SPOT_2ND[15:8] Second record DRAM buffer enable for SPOT write buffer 9(bit 0) ~ buffer 16(bit 7) 0 = disable 1 = enable

RECORD BUFFER ALTERNATE SOURCE CONTROL REGISTER 1 – 0XCCE

Bit	R/W	Default	Description
7:0	R/W	0x0	ALTM[7:0] Use SPOT buffer as record buffer. This register is for SPOT buffer 1(bit 0) ~ SPOT buffer 8(bit 7) 0 = disable 1 = enable

RECORD BUFFER ALTERNATE SOURCE CONTROL REGISTER 2 – 0XCCF

Bit	R/W	Default	Description
7:0	R/W	0x0	ALTM[15:8] Use SPOT buffer as record buffer. This register is for SPOT buffer 9(bit 0) ~ SPOT buffer 16(bit 7) 0 = disable 1 = enable

RECORD BUFFER HORIZONTAL OFFSET CONTROL REGISTER – 0XCD0-D7

Bit	R/W	Default	Description
7:0	R/W	0x0	HSTART0(0xCD0) ~ HSTART7(0xCD7) Horizontal starting position to record write buffer 1(0xCD0) ~ buffer 8(0xCD7) Unit is 4 pixel

NOTE: * THIS ADDRESS IS SHARED WITH OTHER CONTROL REGISTER. REGISTER SELECTION IS CONTROLLED BY 'SHADOW'(0XC68[5:4]). FOR THIS PURPOSE, SHADOW NEED TO SET '0'.

RECORD BUFFER VERTICAL OFFSET CONTROL REGISTER – 0XCE0-E7

Bit	R/W	Default	Description
7:0	R/W	0x0	VSTART0(0xCE0) ~ VSTART7(0xCE7) Vertical starting position to record write buffer 1(0xCE0) ~ buffer 8(0xCE7) Unit is line

NOTE: * THIS ADDRESS IS SHARED WITH OTHER CONTROL REGISTER. REGISTER SELECTION IS CONTROLLED BY 'SHADOW'(0XC68[5:4]). FOR THIS PURPOSE, SHADOW NEED TO SET '0'.

SPOT BUFFER HORIZONTAL OFFSET CONTROL REGISTER – 0XCD0-DF

Bit	R/W	Default	Description
7:0	R/W	0x0	HSTART0_SP(0xCD0) ~ HSTART7_SP(0xCDF) Horizontal starting position to SPOT write buffer 1(0xCD0) ~ buffer 16(0xCDF) Unit is 4 pixel

NOTE: * THIS ADDRESS IS SHARED WITH OTHER CONTROL REGISTER. REGISTER SELECTION IS CONTROLLED BY 'SHADOW'(0XC68[5:4]). FOR THIS PURPOSE, SHADOW NEED TO SET '1'.

SPOT BUFFER VERTICAL OFFSET CONTROL REGISTER – 0XCE0-EF

Bit	R/W	Default	Description
7:0	R/W	0x0	VSTART0_SP(0xCE0) ~ VSTART7_SP(0xCEF) Vertical starting position to SPOT write buffer 1(0xCE0) ~ buffer 8(0xCEF) Unit is line

NOTE: * THIS ADDRESS IS SHARED WITH OTHER CONTROL REGISTER. REGISTER SELECTION IS CONTROLLED BY 'SHADOW'(0XC68[5:4]). FOR THIS PURPOSE, SHADOW NEED TO SET '1'.

DRAM PITCH OF PB TO SPOT DISPLAY – 0XCD0

Bit	R/W	Default	Description
7:0	R/W	0x80	PB_PITCH DRAM pitch of PB to SPOT display (16 pixels unit)

NOTE: * THIS ADDRESS IS SHARED WITH OTHER CONTROL REGISTER. REGISTER SELECTION IS CONTROLLED BY 'SHADOW'(0XC68[5:4]). FOR THIS PURPOSE, SHADOW NEED TO SET '2'.

RECORD PITCH SELECTION FOR READ PORT 5 ~ PORT 9 – 0XCD1

Bit	R/W	Default	Description
7:5	R	0x0	Reserved
4:0	R/W	0x0	REC_PITCH_SEL DRAM pitch selection for port 5(Bit 0) ~ port 9(Bit 4) 0: REC_PITCH, 1: PB_PITCH

NOTE: * THIS ADDRESS IS SHARED WITH OTHER CONTROL REGISTER. REGISTER SELECTION IS CONTROLLED BY 'SHADOW'(0XC68[5:4]). FOR THIS PURPOSE, SHADOW NEED TO SET '2'.

SPECIAL COMPONENT RECORD MODE REGISTER – 0XCF0

Bit	R/W	Default	Description
7	R/W	0x0	SP4[7] Single element fetching mode for record port 8 (8D1 possible) 1 = enable, 0 = normal mode
6	R/W	0x0	SP4[6] Synchronized output enable select for record port 9 1 = synchronize with ROUT5, 0 = normal
5	R/W	0x0	SP4[5] Single element fetching mode for record port 7 (8D1 possible) 1 = enable, 0 = normal mode
4	R/W	0x0	SP4[4] Synchronized output enable select for record port 8 1 = synchronize with ROUT5, 0 = normal
3	R/W	0x0	SP4[3] Single element fetching mode for record port 6 (8D1 possible) 1 = enable, 0 = normal mode
2	R/W	0x0	SP4[2] Synchronized output enable select for record port 7 1 = synchronize with ROUT5, 0 = normal
1	R/W	0x0	SP4[1] Single element fetching mode for record port 5 (8D1 possible) 1 = enable, 0 = normal mode
0	R/W	0x0	SP4[0] Synchronized output enable select for record port 6 1 = synchronize with ROUT5, 0 = normal

RECORD BUFFER FIELD SWITCHING RECORD MODE REGISTER – 0XCF1

Bit	R/W	Default	Description
7:0	R/W	0x0	FSWITCH[7:0] Field switching mode on/off control for recording buffer 1(bit 0) ~ buffer 8(bit 7) 1 = enable, 0 = normal mode

RECORD BUFFER FIELD SWITCHING RECORD MODE FIELD SELECT REGISTER – 0XCF3

Bit	R/W	Default	Description
7:0	R/W	0x0	SEL_EVEN[7:0] Field switching mode field type selection control for recording buffer 1(bit 0) ~ buffer 8(bit 7) 1 = even field, 0 = odd field

OUTPUT PIN SET SOURCE 2 CONTROL REGISTER A – 0XCF5

Bit	R/W	Default	Description
7:4	R	0x6	P2SRC2 Pin Set 2 Source 2 Select[3:0] 1111 = port 8 output high byte 1110 = port 8 output low byte 1101 = port 7 output high byte 1100 = port 7 output low byte 1011 = port 6 output high byte 1010 = port 6 output low byte 1001 = port 5 output high byte 1000 = port 5 output low byte 0111 = port 9 output high byte 0110 = port 9 output low byte (default) Others = pin out is always '0'
3:0	R/W	0x2	P2SRC2 Pin Set 1 Source 2 Select[3:0] 1111 = port 8 output high byte 1110 = port 8 output low byte 1101 = port 7 output high byte 1100 = port 7 output low byte 1011 = port 6 output high byte 1010 = port 6 output low byte 1001 = port 5 output high byte 1000 = port 5 output low byte 0111 = port 9 output high byte 0110 = port 9 output low byte Others = pin out is always '0' (default)

OUTPUT PIN SET SOURCE 2 CONTROL REGISTER B – 0XCF6

Bit	R/W	Default	Description
7:4	R	0xe	**P4SRC2** Pin Set 4 Source 2 Select[3:0] 1111 = port 8 output high byte 1110 = port 8 output low byte (default) 1101 = port 7 output high byte 1100 = port 7 output low byte 1011 = port 6 output high byte 1010 = port 6 output low byte 1001 = port 5 output high byte 1000 = port 5 output low byte 0111 = port 9 output high byte 0110 = port 9 output low byte Others = pin out is always '0'
3:0	R/W	0xa	**P3SRC2** Pin Set 3 Source 2 Select[3:0] 1111 = port 8 output high byte 1110 = port 8 output low byte 1101 = port 7 output high byte 1100 = port 7 output low byte 1011 = port 6 output high byte 1010 = port 6 output low byte (default) 1001 = port 5 output high byte 1000 = port 5 output low byte 0111 = port 9 output high byte 0110 = port 9 output low byte Others = pin out is always '0'

FRAME RATE CONTROLLER UPDATE REGISTER – 0XCF7

Bit	R/W	Default	Description
7:0	R/W	0x0	**CH_ENA** Enable free running recording for port 7 ~ port 0 1 = enable, 0 = normal mode

SPOT BUFFER FIELD SWITCHING RECORD MODE REGISTER I – 0XCF8

Bit	R/W	Default	Description
7:0	R/W	0x0	**SFSWITCH[7:0]** Field switching mode on/off control for SPOT buffer 1(bit 0) ~ buffer 8(bit 7) 1 = enable, 0 = normal mode

SPOT BUFFER FIELD SWITCHING RECORD MODE REGISTER 2 – 0XCF9

Bit	R/W	Default	Description
7:0	R/W	0x0	**SFSWITCH[15:8]** Field switching mode on/off control for SPOT buffer 9(bit 0) ~ buffer 16(bit 7) 1 = enable, 0 = normal mode

SPOT BUFFER FIELD SWITCHING RECORD MODE FIELD SELECT REGISTER I – 0XCFA

Bit	R/W	Default	Description
7:0	R/W	0x0	**SEL_EVEN[7:0]** Field switching mode field type selection control for SPOT buffer 1(bit 0) ~ buffer 8(bit 7) 1 = even field, 0 = odd field

SPOT BUFFER FIELD SWITCHING RECORD MODE FIELD SELECT REGISTER 2 – 0XCFB

Bit	R/W	Default	Description
7:0	R/W	0x0	**SSEL_EVEN[15:8]** Field switching mode field type selection control for SPOT buffer 9(bit 0) ~ buffer 16(bit 7) 1 = even field, 0 = odd field

WRITE BUFFER CONTROL REGISTER – 0XCFC

Bit	R/W	Default	Description
7	R/W	0x0	**LINE_BIGGER_EN** Recording / SPOT buffers write control enable 0 = disable, 1= enable
6:5	R/W	0x0	**Reserved**
4	R/W	0x0	**SPOT_MEM** In the SPOT write buffer, buffer write scheme selection control 0 = Use secondary memory area 1 = Use left side memory area for 256 Mb memory
3:2	R/W	0x0	**SSKIP_SEL** SPOT buffer source skip select 00 = No skip (default) 01 = skip every 5 frames (fields) 10 = skip every 6 frames (fields) 11 = skip every 7 frames (fields)
1:0	R/W	0x0	**SKIP_SEL** Recording buffer source skip select 00 = No skip (default) 01 = skip every 5 frames (fields) 10 = skip every 6 frames (fields) 11 = skip every 7 frames (fields)

NEW FRSC CONTROL REGISTER A – 0XCFD

Bit	R/W	Default	Description
7:6	R/W	0x0	**FLD_FRSC** New frame rate control method by using field signal 0x = original frame rate control 10 = new frame rate control, wr_page[0] = field 11 = new frame rate control, wr_page[0] = ~field
5	R/W	0x0	**NEW_EN** New method for mapping wr_buffers to read ports 00 = original mapping 01 = new mapping, each read port selects write buffers by setting register 0xCFD[4:0] and 0xCFE[7:0]
4:0	R/W	0x0	**EN_ADDRI** Read port index 0 = port5, recording write buffer 0 ~ 7 selection 1 = port5, SPOT write buffer 0 ~ 7 selection 2 = port5, SPOT write buffer 8 ~ 15 selection 3 = port6, recording write buffer 0 ~ 7 selection 4 = port6, SPOT write buffer 0 ~ 7 selection 5 = port6, SPOT write buffer 8 ~ 15 selection 6 = port7, recording write buffer 0 ~ 7 selection 7 = port7, SPOT write buffer 0 ~ 7 selection 8 = port7, SPOT write buffer 8 ~ 15 selection 9 = port8, recording write buffer 0 ~ 7 selection 10 = port8, SPOT write buffer 0 ~ 7 selection 11 = port8, SPOT write buffer 8 ~ 15 selection 12 = port9, recording write buffer 0 ~ 7 selection 13 = port9, SPOT write buffer 0 ~ 7 selection 14 = port9, SPOT write buffer 8 ~ 15 selection 15 = port5, pb write buffer 0 ~ 4 selection 16 = port6, pb write buffer 0 ~ 4 selection 17 = port7, pb write buffer 0 ~ 4 selection 18 = port8, pb write buffer 0 ~ 4 selection 19 = port9, pb write buffer 0 ~ 4 selection

NEW WRITE BUFFER MAPPING CONTROL REGISTER– 0XCFE

Bit	R/W	Default	Description
7:0	R/W	0x0	**EN_DATA** New write buffer mapping control data According to the value of EN_ADDRI(0xCFD[4:0]), this value select write buffer for each read port 0 = disable, 1= enable

PB FRSC CONNECTION CONTROL REGISTER– 0XCFF

Bit	R/W	Default	Description
7:5	R	0x0	Reserved
4:0	R/W	0x0	PB_FRSC_REC_ON PB FRSC connection control for PB0(Bit 0) ~ PB 4(Bit 4) 0 = disable, 1= enable

Register Descriptions for SPOT Display

SPOT1 CONTROL REGISTER– 0XF0B

Bit	R/W	Default	Description
7:6	RW	0	Reserved
5	RW	0	SP1 COLOR BAR ENA
4	RW	0	SP1_SWITCH_EN 0: Background enable 1: Background display disable
3:0	RW	0	Reserved

SPOT1 CONTROL REGISTER – 0XF0F

Bit	R/W	Default	Description
7	N/A	1	SP1_Field Mode Select 1: Field mode 0: Frame mode
6:0	RW	0	Reserved

SPOT1 CONTROL REGISTER– 0XF17

Bit	R/W	Default	Description
7:6	RW	0	TVENC_FSC_MODE, SPOT1 TV FSCSEL This register determines the TV modulation frequency standard select. 00 - NTSC M 01 - PAL B, D, G, H, I 10 - PAL M 11 - PAL N
5	RW	0	TVENC_SAT_LMT, SPOT1 TV video saturation limit Control the data range of the ITU-R BT.656 output 0 - Not limit 1 – Data range is limited to 1 – 254 range
4:1	RW	0	Reserved
0	RW	0	TVENC_PALNT, SPOT1 TV PAL or NTSC select This register determines the CVBS output Standard. 0: NSTC mode 1: PAL mode.

SPOT1 CONTROL REGISTER– 0XF18

Bit	R/W	Default	Description
7	RW	0	**SP1_TVENC_VSPOL, SPOT1 TVENC Vertical sync polarity** 0: Active Low 1: Active High
6	RW	0	**SP1_TVENC_HSPOL, SPOT1 TV Encoder Horizontal Sync Polarity** 0: Active Low 1: Active High
5	RW	0	**SP1_TVENC_VSDET, SPOT1 TV Encoder Vsync Det.**
4	RW	0	**SP1_TVENC_PED, SPOT1 TV Encoder Pedestal Enable** Enable Pedestal for video output 0: 0 IRE for pedestal 1: 7.5 IRE pedestal level
3	RW	0	**SP1_TVENC_PDRST, SPOT1 TV Encoder Pedestal Reset** Subcarrier Phase Alternation reset every 8 field in PAL system 0: Constant relationship, reset every 8 field 1: Free running
2	RW	0	**SP1_TVENC_PHALT, SPOT1 TV Encoder Phase Alternation** 0: Disable phase alternation for line by line. Use in NTSC 1: Enable phase alternation for line by line. Use in PAL
1	RW	0	**SP1_TVENC_F_INV, SPOT1 TV Encoder Field Output Invert** This register bit inverts the field output level if set.
0	RW	0	**SP1_TVENC_INTERLACE, SPOT1 TVENC Interlace Select** This register bit determines the TV Standard in Interlace timing mode. 0 - Progressive 1 - Interlace

SPOT1 CONTROL REGISTER– 0XF19

Bit	R/W	Default	Description
7:6	N/A		Reserved
5:4	RW	0	**SP1_TVENC_YC_OS[1:0], SPOT1 TV Encoder Active Pixel Offset delay** 00: No Active offset 01: Active pixel offset for 1/4 pixel unit 10: Active pixel offset for 1/2 pixel unit 11: Active pixel offset for 3/4 pixel unit
3:2	RW	0	**SP1_TVENC_OSENC[1:0], SPOT1 TV Encoder Field Offset for the first video line** 00: Apply same ENC_VDSEL for odd and even field 01: Apply same ENC_VDSEL for odd and odd field 10: Apply TVENC_VSDEL for odd field and TVENC_VSDEL+1 for even field 11: Apply TVENC_VSDEL for odd field and TVENC_VSDEL+2 for even field

Bit	R/W	Default	Description
1	RW	0	**SP1_TVENC_FLDENCP, SPOT1 TV Encoder Field Polarity** This Register control the field polarity 0: Even field is high 1: Odd field is high
0	RW	0	**SP1_TVENC_FLDDET, SPOT1 TV Encoder Field Detect**

SPOT1 CONTROL REGISTER– 0XF1A

Bit	R/W	Default	Description
7:0	RW	0	**SP1_TVENC_HSENC[7:0], SPOT1 TV Encoder Active pixel delay** Lower 8 bit of the pixel delay from active video by ½ pixel per step

SPOT1 CONTROL REGISTER– 0XF1B

Bit	R/W	Default	Description
7:2	N/A	0	**Reserved**
1:0	RW	0	**SP1_TVENC_HSENC[9:8], SPOT1 TV Encoder Active pixel delay** Upper 2 bit of the pixel delay from active video by ½ pixel per step

SPOT1 CONTROL REGISTER– 0XF1C

Bit	R/W	Default	Description
7:6	N/A	0	**SP1_CVBS_SEL** 11 : SP1 CVBS output is coming from SP4 10 : SP1 CVBS output is coming from SP3 01 : SP1 CVBS output is coming from SP2 00 : SP1 CVBS output is coming from SP1
5:0	RW	0	**SP1_TVENC_VSENC, SPOT1 TV Encoder Active line delay** 6 bit of the line delay from active video by line per step

SPOT1 CONTROL REGISTER– 0XF1D

Bit	R/W	Default	Description
7:6	N/A		Reserved
4:0	RW	0	**SP1_TVENC_LINE_OS, SPOT1 TV Encoder Active line offset** 5 bit of the line offset

SPOT1 CONTROL REGISTER– 0XF1E

Bit	R/W	Default	Description
7:6	N/A	0	[7;6] SP1_FLD_SW_MODE [7] Field Switching Mode enable [6] Field Switch Mode image height is 240 lines Enable
5:0	RW	0	SP1_TVENC_PIXEL_OS, SPOT1 TV Encoder Active Pixel offset 6 bit of the pixel offset

SPOT1 CONTROL REGISTER– 0XF1F

Bit	R/W	Default	Description
7	N/A		Reserved
6	RW	0	SP1_TVENC_C_OFF_D, SPOT1 TV Encoder C Off Set the Color Off if set
5:4	RW	0	SP1_TVENC_CBW_D, SPOT1 TV Encoder CBCR delay 2 bit of the CbCr delay
3:2	RW	0	SP1_TVENC_YBW_D, SPOT1 TV Encoder Luma delay 2 bit of the Luminous delay
1:0	RW	0	SP1_TVENC_FLD_OS, SPOT1 TV Encoder Active Field offset 2 bit of the field offset

SPOT1 CONTROL REGISTER– 0XF20

Bit	R/W	Default	Description
7	RW	0	SP1_TVENC_TST_FSC_FREE, SPOT1 TV Encoder Sub-Carrier is set to free run
6	RW	0	SP1_TVENC_T_CCIR_TIM, SPOT1 TV Encoder CCOR Timing 2 bit of the CbCr delay
5	RW	0	SP1_TVENC_T_656_STD, SPOT1 TV Encoder 656 Standard 2 bit of the Luminous delay
4:0	RW	0	SP1_TVENC_VIS_LINE_OS, SPOT1 TV Encoder line offset 5 bit Line offset

SPOT2 CONTROL REGISTER – 0XF6B

Bit	R/W	Default	Description
7:6	RW	0	Reserved
5	RW	0	SP2 COLOR BAR ENA
4	RW	0	Reserved

Bit	R/W	Default	Description
3:2	RW	0	SP2_FLD select 11: use bank0 from the FRSC as the field 10: use bank0 from the FRSC inverse as the filed 0x: use HVCNT generated field
1	RW	0	Reserved
0	RW	0	SYNC_ALIGN 0: Original 1: Use delayed enable signal to align between sync and data

SPOT2 CONTROL REGISTER – 0XF6F

Bit	R/W	Default	Description
7	R/W	1	SP2_ Field Mode Select 1: Field mode 0: Frame mode
6	RW	0	SP2_2ND_MEM Enable
5	RW	0	SP2_FRMCNT_EN SPOT2 Frame Count Enable
4	RW	0	SP2_ENA SPOT2 Enable
3:2	RW	0	SP2_ROT Rotation Enable
1	RW	0	SP2_VSPOL SPOT2 Vertical Polarity Control
0	RW	0	SP2_HSPOL SPOT2 Horizontal Polarity Control

SPOT2 CONTROL REGISTER – 0XF77

Bit	R/W	Default	Description
7:6	RW	0	SP2_TVENC_FSC_MODE, SPOT2 TV FSCSEL This register determines the TV modulation frequency standard select. 00 - NTSC M 01 - PAL B, D, G, H, I 10 - PAL M 11 - PAL N
5	RW	0	SP2_TVENC_SAT_LMT, SPOT2 TV video saturation limit Control the data range of the ITU-R BT.656 output 0 - Not limit 1 – Data range is limited to 1 – 254 range
4:1	N/A	0	Reserved
0	RW	0	SP2_TV PAL or NTSC select This register determines the CVBS output Standard. 0: NSTC mode 1: PAL mode.

SPOT2 CONTROL REGISTER – 0XF78

Bit	R/W	Default	Description
7	RW	0	**SP2_TVENC_VSPOL, SPOT2 TVENC Vertical sync polarity** 0: Active Low 1: Active High
6	RW	0	**SP2_TVENC_HSPOL, SPOT2 TV Encoder Horizontal Sync Polarity** 0: Active Low 1: Active High
5	RW	0	**SP2_TVENC_VSDET, SPOT1 TV Encoder Vsync Det.**
4	RW	0	**SP2_TVENC_PED, SPOT2 TV Encoder Pedestal Enable** Enable Pedestal for video output 0: 0 IRE for pedestal 1: 7.5 IRE pedestal level
3	RW	0	**SP2_TVENC_PDRST, SPOT2 TV Encoder Pedestal Reset** Subcarrier Phase Alternation reset every 8 field in PAL system 0: Constant relationship, reset every 8 field 1: Free running
2	RW	0	**SP2_TVENC_PHALT, SPOT2 TV Encoder Phase Alternation** 0: Disable phase alternation for line by line 1: Enable phase alternation for line by line
1	RW	0	**SP2_TVENC_F_INV, SPOT2 TV Encoder Field Output Invert** This register bit inverts the field output level if set.
0	RW	0	**SP2_TVENC_INTERLACE, SPOT2 TVENC Interlace Select** This register bit determines the TV Standard in Interlace timing mode. 0 - Progressive 1 - Interlace

SPOT2 CONTROL REGISTER – 0XF79

Bit	R/W	Default	Description
7:6	N/A		Reserved
5:4	RW	0	**SP2_TVENC_YC_OS[1:0], SPOT2 TV Encoder Active Pixel Offset delay** 00: No Active offset 01: Active pixel offset for 1/4 pixel unit 10: Active pixel offset for 1/2 pixel unit 11: Active pixel offset for 3/4 pixel unit
3:2	RW	0	**SP2_TVENC_OSENC[1:0], SPOT2 TV Encoder Field Offset for the first video line** 00: Apply same ENC_VDSEL for odd and even field 01: Apply same ENC_VDSEL for odd and odd field 10: Apply TVENC_VSDEL for odd field and TVENC_VSDEL+1 for even field 11: Apply TVENC_VSDEL for odd field and TVENC_VSDEL+2 for even field

Bit	R/W	Default	Description
1	RW	0	SP2_TVENC_FLDENCP, SPOT2 TV Encoder Field Polarity This Register control the field polarity 0: Even field is high 1: Odd field is high
0	RW	0	SP2_TVENC_FLDDET, SPOT2 TV Encoder Field Detect

SPOT2 CONTROL REGISTER – 0XF7A

Bit	R/W	Default	Description
7:0	RW	0	SP2_TVENC_HSENC[7:0], SPOT2 TV Encoder Active pixel delay Lower 8 bit of the pixel delay from active video by ½ pixel per step

SPOT2 CONTROL REGISTER – 0XF7B

Bit	R/W	Default	Description
7:2	N/A	0	Reserved
1:0	RW	0	SP2_TVENC_HSENC[9:8], SPOT2 TV Encoder Active pixel delay Upper 2 bit of the pixel delay from active video by ½ pixel per step

SPOT2 CONTROL REGISTER – 0XF7C

Bit	R/W	Default	Description
7:6	N/A	1	SP2_CVBS_SEL Others : SP2 CVBS output is coming from SP2 00 : SP2 CVBS output is coming from SP1
5:0	RW	0	SP2_TVENC_VSENC, SPOT2 TV Encoder Active line delay 6 bit of the line delay from active video by line per step

SPOT2 CONTROL REGISTER – 0XF7D

Bit	R/W	Default	Description
7:5	N/A		Reserved
4:0	RW	0	SP2_TVENC_LINE_OS, SPOT2 TV Encoder Active line offset 5 bit of the line offset

SPOT2 CONTROL REGISTER – 0XF7E

Bit	R/W	Default	Description
7:6	N/A	0	[7;6] SP2_FLD_SW_MODE [7] Field Switching Mode enable [6] Field Switch Mode image height is 240 lines Enable
5:0	RW	0	SP2_TVENC_PIXEL_OS, SPOT2 TV Encoder Active Pixel offset 6 bit of the pixel offset

SPOT2 CONTROL REGISTER – 0XF7F

Bit	R/W	Default	Description
7	N/A		Reserved
6	RW	0	SP2_TVENC_C_OFF_D, SPOT2 TV Encoder C Off Set the Color Off if set
5:4	RW	0	SP2_TVENC_CBW_D, SPOT2 TV Encoder CBCR delay 2 bit of the CbCr delay
3:2	RW	0	SP2_TVENC_YBW_D, SPOT2 TV Encoder Luma delay 2 bit of the Luminous delay
1:0	RW	0	SP2_TVENC_FLD_OS, SPOT2 TV Encoder Active Field offset 2 bit of the field offset

SPOT2 CONTROL REGISTER – 0XF80

Bit	R/W	Default	Description
7	RW	0	SP2_TVENC_TST_FSC_FREE, SPOT2 TV Encoder Sub-Carrier is set to free run
6	RW	0	SP2_TVENC_T_CCIR_TIM, SPOT2 TV Encoder CCOR Timing 2 bit of the CbCr delay
5	RW	0	SP2_TVENC_T_656_STD, SPOT2 TV Encoder 656 Standard 2 bit of the Luminous delay
4:0	RW	0	SP2_TVENC_VIS_LINE_OS, SPOT2 TV Encoder line offset 5 bit Line offset

SPOT3 CONTROL REGISTER – 0XF9B

Bit	R/W	Default	Description
7:2	RW	0	Reserved
1:0	RW	0	SPOT_POWER_DOWN_EN [1] SP2 PD enable when 0 [0] SP1 PD enable when 0

SPOT3 CONTROL REGISTER – 0XF9C

Bit	R/W	Default	Description
7:4	RW	0	**REC, Port 9 use SP1 as the display** [7] = 1, select Port 9 to display on SP1 = 0, [6:4] selects REC PORT 5 - 8 display on SP1 [6:4] = Others, selects REC PORT9 [6:4] = 4, selects REC PORT5 [6:4] = 5, selects REC PORT6 [6:4] = 6, selects REC PORT7 [6:4] = 7, selects REC PORT8
3:0	RW	0	**REC, Port 9 use SP2 as the display** [7] = 1, select Port 9 to display on SP2 = 0, [6:4] selects REC PORT 1 - 8 display on SP2 [6:4] = Others, selects REC PORT9 [6:4] = 4, selects REC PORT5 [6:4] = 5, selects REC PORT6 [6:4] = 6, selects REC PORT7 [6:4] = 7, selects REC PORT8

OSD for Recording Path

Introduction

TW2828 recording OSD controller displays channel information for each channel. There are 5 recording ports supported. It is a font based design. All font tables are stored in local SRAM. Channel information includes 32 characters date/time, 16 characters title and 16 characters status. There are totally 64 fonts saved in SRAM. Font width can be selected linearly from 8 ~22. Font height can be selected linearly from 8 ~ 22. These fonts can be repeated and size can be doubled up to 44. Channel information is also saved in local SRAM. Besides channel information layer, there are background layer and channel boundary layer.

Features

- 5 OSD engines for 5 recording ports
- 64 fonts table saved in SRAM
- Channel information table saved in SRAM
- Three lines channel information
- 32 characters date/time
- 16 characters channel title for each channel
- 16 characters channel status for each channel
- Font size can be changed
- Channel Boundary
- Background
- Color Bar

Description

LAYERS

There are four layers including video. The bottom layer is background. Background is a pure color under video layer. Background color can be programmed. It is shown up when this channel of video is not enabled. Boundary layer is a boundary for each channel. Boundary width and color can be programmed. The top layer is channel information.

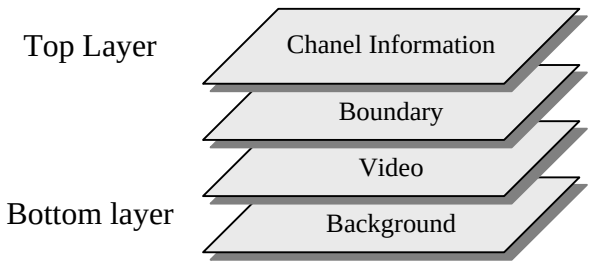
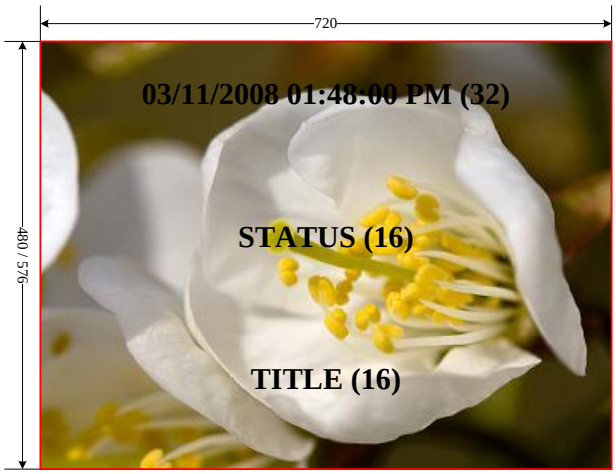


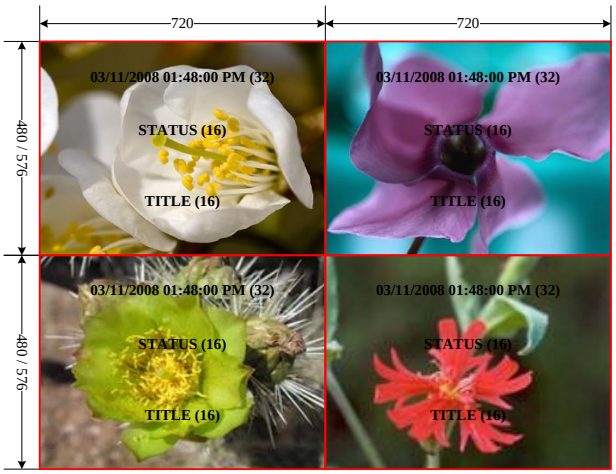
FIGURE 29. RECORD OSD LAYERS

RESOLUTIONS

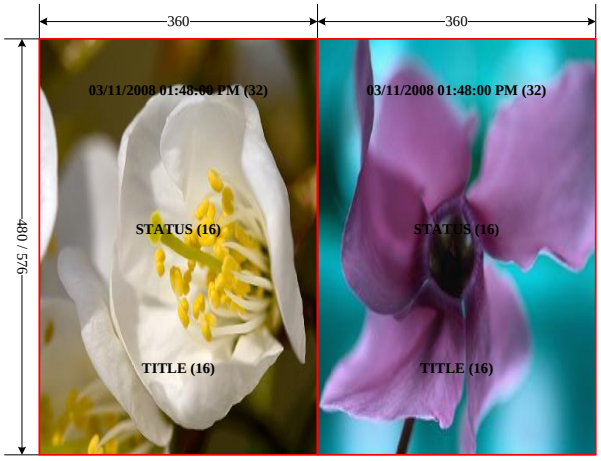
The following resolutions are supported: D1 (720x480 or 720x576),CIF (352x240 or 352x288), 4D1 (1440x960 or 1440x1152) and BT1120 (1920x1080). In D1 case, it can be full D1 picture or two half D1 pictures or four quad pictures or 16 QCIF pictures or nine 1/3D1 pictures. In 4D1 case, it has 4 D1 pictures in one frame. In BT1120, it has 6 VGA pictures in one frame. Channel information picture is shown below. For each resolution, font size can be programmed.



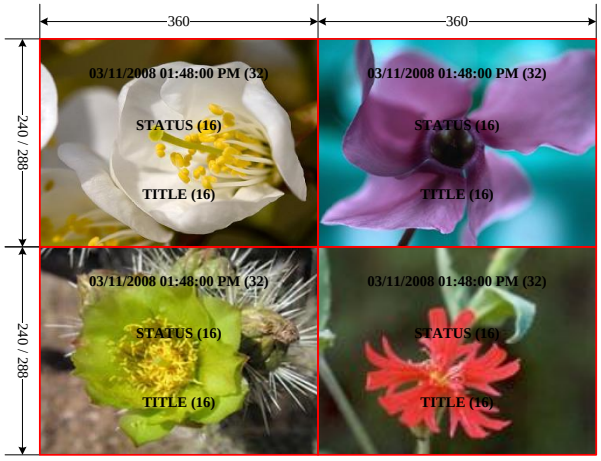
D1



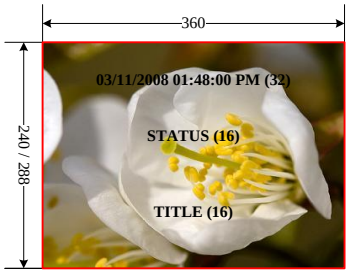
4D1



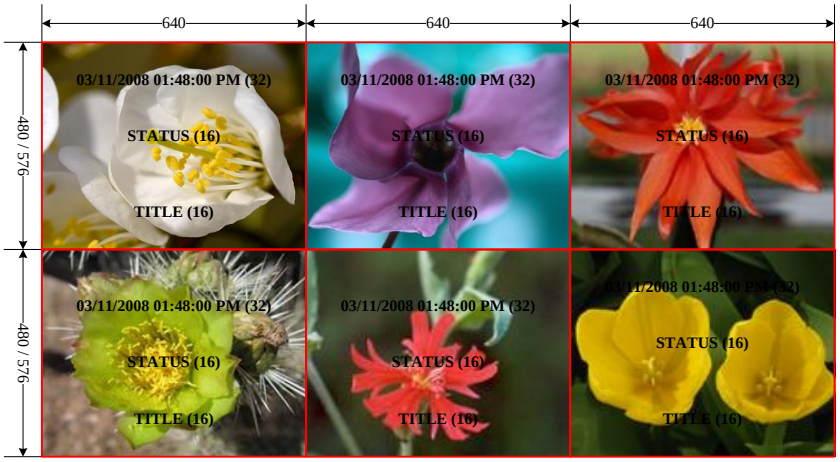
Half D1



Quad



CIF



BT1120

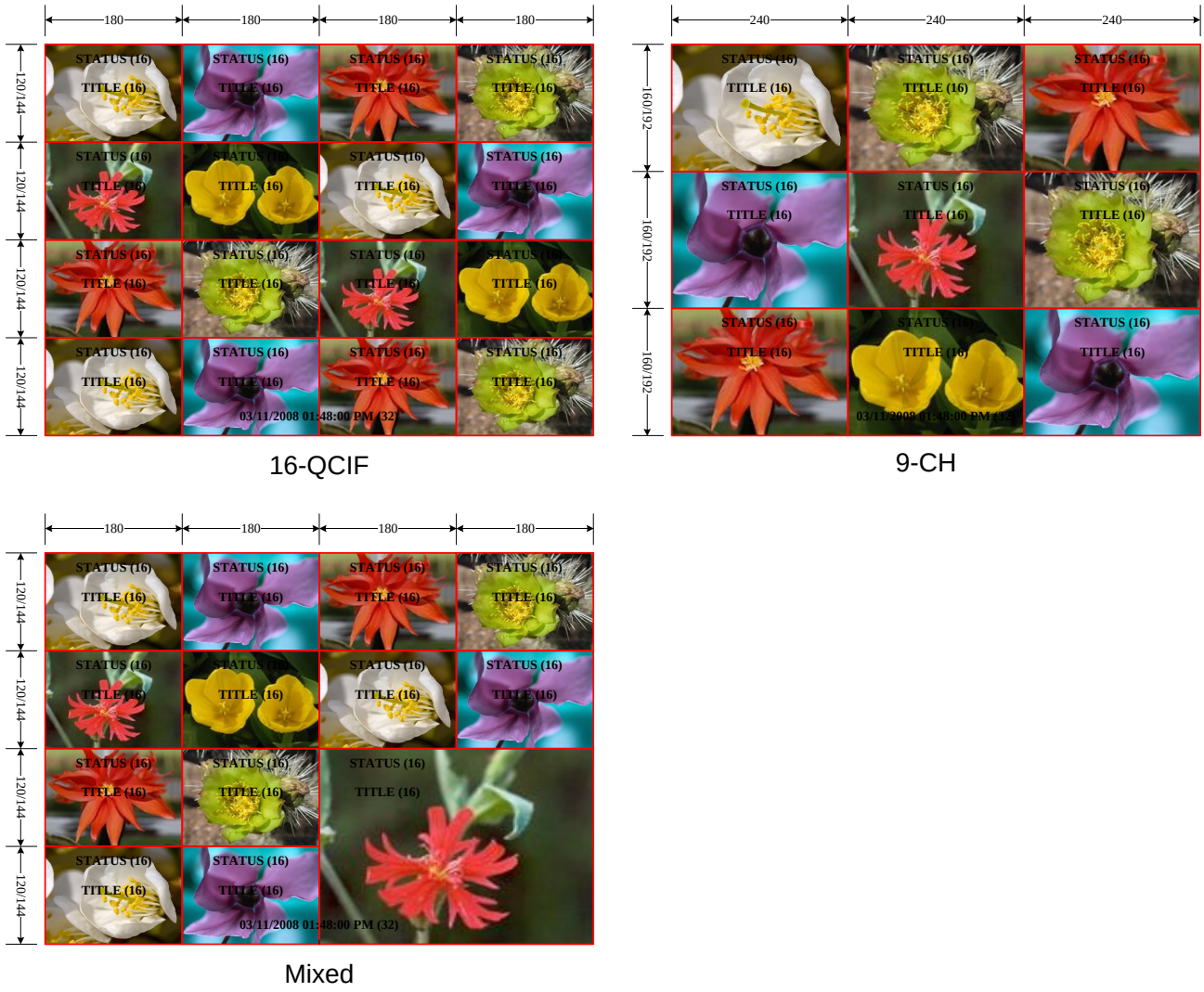


FIGURE 30. EXAMPLE OF OSD ACCORDING TO OUTPUT RESOLUTION

Timing Diagram

Vertical timing:

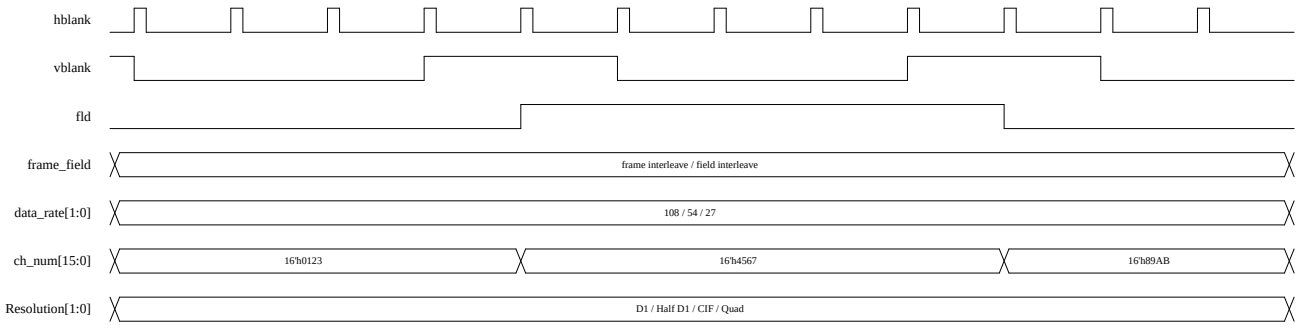


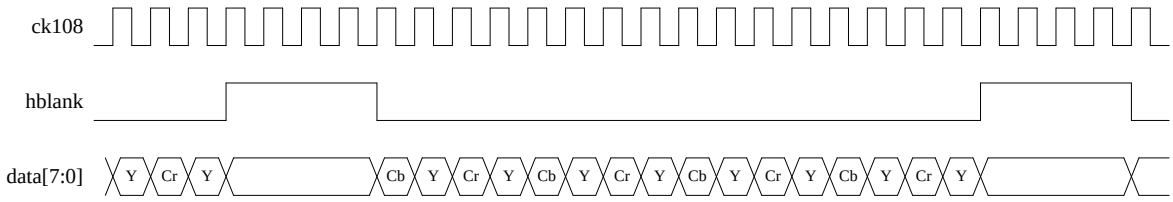
FIGURE 31. VERTICAL TIMING OF RECORDING OSD

"fld" signal has different means between frame interleave and field interleave. In frame interleave, "fld" is selection for top half frame and bottom half frame. In field interleave, "fld" is selection for odd field and even field.

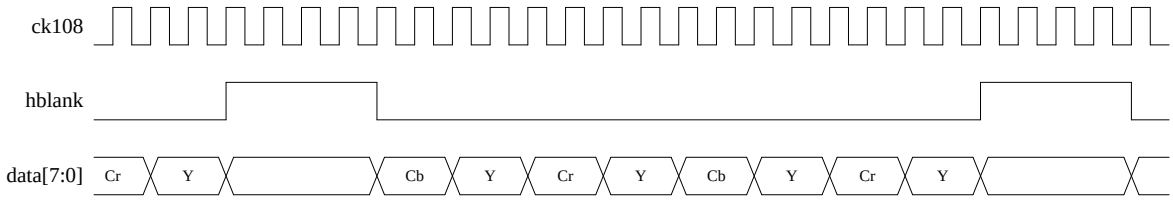
Channel number is 16 bits. If Quad mode is used, total 16 bits are used. [15:12] is for top left channel, [11:8] is for top right channel, [7:4] is for bottom left channel, and [3:0] is for bottom right channel. If D1 or CIF mode is selected, only bit [15:12] is used. If Half D1 mode is selected, bit [15:8] is used. [15:12] is for left channel and [11:8] is for right channel.

Resolution can be selected different size of each channel. D1, Half D1 and Quad have same timing, but the contents in active area are different. In D1 mode, there is only one channel data. In Half D1 mode, there is two channels data. In Quad mode, there is four channels data. In CIF mode, there is only one channel but size is 1/4 of D1.

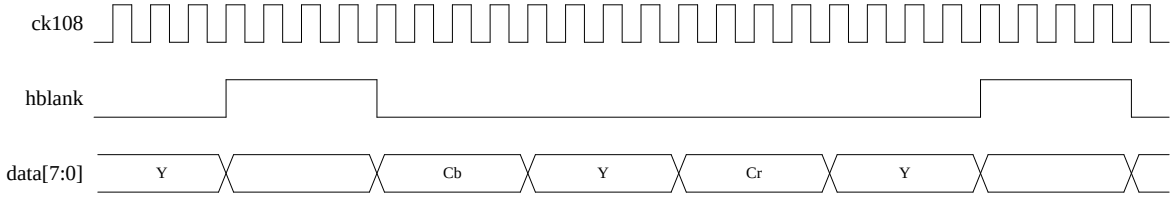
Horizontal timing:



Horizontal Timing (108M)



Horizontal Timing (54M)



Horizontal Timing (27M)

FIGURE 32. HORIZONTAL TIMING OF RECORD OSD ACCORDING TO OUTPUT CLOCK

Input clock is always 108MHz. But data rate can be select from 108MHz, 54MHz and 27MHz. Input and output data are 8 bits.

Font

There are totally 64 fonts which can be saved in SRAM. The font size saved in SRAM is fixed to 22x22. But displayed font size can be changed. Horizontal can display various sizes: 8 ~ 22. Font can be repeated and font size becomes double to 16 ~ 44. Vertical can also display various sizes: 8 ~ 22. Font can be doubled to 16 ~ 44. According to the font size, fonts saved in SRAM must have same size. The following picture shows SRAM data.

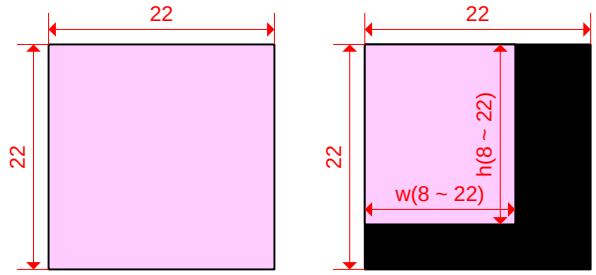


FIGURE 33. FONT SIZE OF RECORDING OSD

There are 2 bits for each pixel color. 00 means transparent, color 01, 10 and 11 can be set by registers: ROSD_FONT_R1 (G1, B1), ROSD_FONT_R2 (G2, B2) and ROSD_FONT_R3 (G3, B3).

Data saved in SRAM is shown below. There are totally 64x22x22*2=1408x44 bits in SRAM. Data are saved font by font. For each font, data is saved line by line. Pixel data in each line is in big endian.

Different size font is used for different resolution. For example, 16x20 can be used for D1, 8x10 can be use for CIF and Quad, and 8x20 can be use for Half D1.

The font size can be changed according to register ROSD_FONT_HSIZE_* and ROSD_FONT_VSIZE_*. But remember the fonts saved in memory are always 22x22. If double size is selected, just repeat every pixel twice.

ROSD_FONT_HSIZE_FULL is for D1 mode. ROSD_FONT_HSIZE_HALF is for Half D1 and Quad and CIF mode. ROSD_FONT_VSIZE_FULL is for D1 and Half D1 mode. ROSD_FONT_VSIZE_HALF is for Quad and CIF mode.

Font size can be controlled by setting the register, 0xE4C and 0xE4D, ROSD_FONT_*SIZE_ADD_*. Font size is as the following formula.

8 + ROSD_FONT_*SIZE_ADD* (no repeat)

16 + 2XROSD_FONT_*SIZE_ADD* (repeat)

Display Channel Information

DATE AND TIME

There are totally 32 fonts can be displayed including space. Date and time are same for each channel. The position for date and time can be programmed for different resolutions, not for channels. Each font is selected from 64-font table. So index for each font is 6 bit. Time and date can be enabled by setting register ROSD_TIME_EN and ROSD_EN to high. It can be mixed with video data by setting register ROSD_TIME_MIX to high. Mix percentage is 50% video plus 50% channel number. The font index is saved in display SRAM. It needs 32x6 bits.

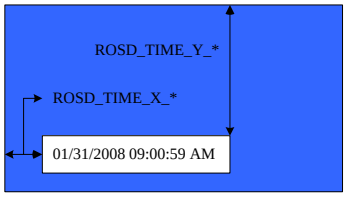


FIGURE 34. POSITION OF TIME IN THE D1 MODE

ROSD_TIME_Y_* defines vertical start position. There are three different vertical positions. ROSD_TIME_Y_FULL is for D1 and Half D1, ROSD_TIME_Y_TOP is for Quad top channels or CIF, and ROSD_TIME_Y_BOTTOM is for Quad bottom channels. All the number is based on (0, 0) of whole image.

ROSD_TIME_X_* defines horizontal start position. There are three different horizontal positions. ROSD_TIME_X_FULL is for D1, ROSD_TIME_X_LEFT is for Quad left channels or CIF, and ROSD_TIME_X_RIGHT is for Quad right channels. All the number is based on (0, 0) of whole image.

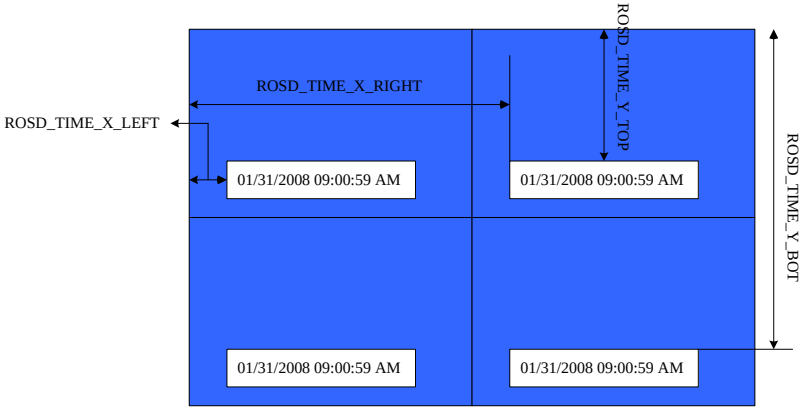


FIGURE 35. POSITION OF TIME IN THE QUAD MODE

TITLE

For each channel, there is 16-font title information. Each font is selected from 64-font table. So index for each font is 6 bit. Title can be enabled by setting register ROSD_TITLE_EN and ROSD_EN to high. Title can be mixed with video data by setting register ROSD_TITLE_MIX to high. Mix percentage is 50% video plus 50% channel number. The position for date and time can be programmed for different resolutions, not for channels.

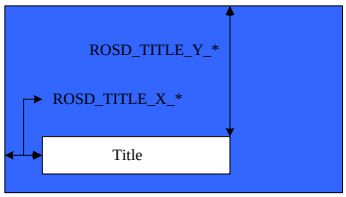


FIGURE 36. POSITION OF TITLE IN THE D1 MODE

ROSD_TITLE_Y_* defines vertical start position. There are three different vertical positions. ROSD_TITLE_Y_FULL is for D1 and Half D1, ROSD_TITLE_Y_TOP is for Quad top channels or CIF, and ROSD_TITLE_Y_BOTTOM is for Quad bottom channels.

ROSD_TITLE_X_* defines horizontal start position. There are three different horizontal positions. ROSD_TITLE_X_FULL is for D1, ROSD_TITLE_X_LEFT is for Quad left channels or CIF, and ROSD_TITLE_X_RIGHT is for Quad right channels.

If channel number information has less than 16 fonts, you can set the remaining font to space. So you need to put space font in the 64-font table.

Channel information for display is saved in display SRAM. It contains 16x6x(16 + 5) =336x6. There are 16 channel informations for live input and there are 5 channel informations for HD input. The sequence is channel by channel. In each channel, the sequence is font by font.

STATUS

Status is same as title. It has 16 fonts. It needs 16x6x16 bit SRAM size.

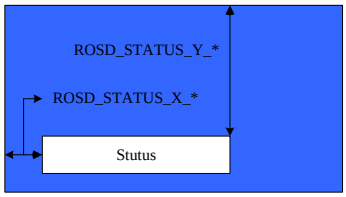


FIGURE 37. POSITION OF STATUS IN THE D1 MODE

SRAM Allocation

There are two SRAM blocks in this design. One is for font. The other is for display information.

FONT SRAM

Fonts are saved in one SRAM block. Font SRAM size is 1408x44 bits.

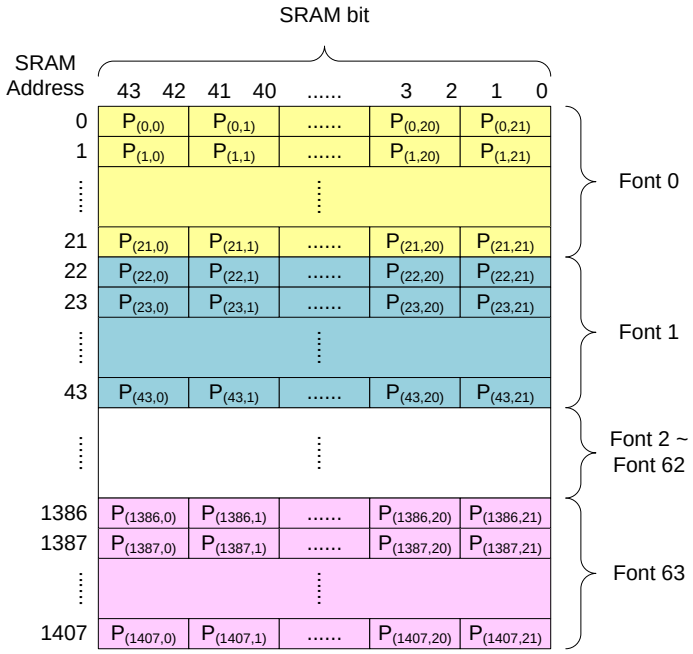


FIGURE 38. STRUCTURE OF FONT SRAM

During system initialization, host need to write font data in this SRAM. The write sequence is:

1. ROSD_FRAM_ADDR[7:0] , 0xEE0 [7:0]
2. ROSD_FRAM_ADDR[10:8] , 0xEE1 [2:0]
3. ROSD_FRAM_DATA[7:0] , 0xEE2 [7:0]
4. ROSD_FRAM_DATA[15:8], , 0xEE3 [7:0]
5. ROSD_FRAM_DATA[23:16], , 0xEE4 [7:0]
6. ROSD_FRAM_DATA[31:24], , 0xEE5 [7:0]
7. ROSD_FRAM_DATA[39:32], , 0xEE6 [7:0]
8. ROSD_FRAM_DATA[43:40], , 0xEE7 [3:0]

ROSD_FRAM_DATA[43:40] must be the last one.

DISPLAY SRAM

Display SRAM includes time and date, channel title and status. Time and date needs 32x6 bits, channel title needs 256x6 bits, and channel status needs 256x16 bits also. So the total SRAM size is 544x6 bits.

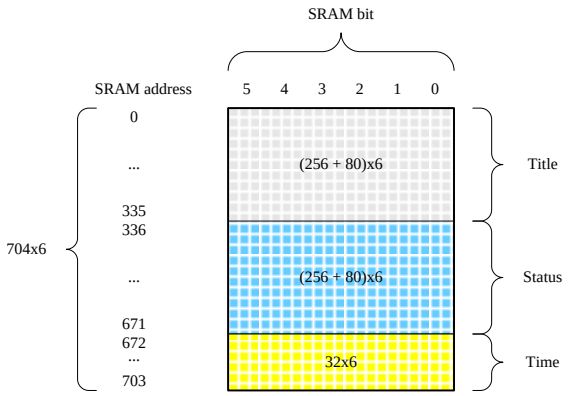


FIGURE 39. STRUCTURE OF DISPLAY SRAM

During display, host need to write index data in this SRAM. The write sequence is:

Set ROSD_DRAM_ADDR, and then set ROSD_DRAM_DATA.

1. ROSD_DRAM_ADDR[7:0] , 0xEE8 [7:0]

2. ROSD_DRAM_ADDR[9:8] , 0xEE9 [1:0]

3. ROSD_DRAM_DATA[5:0] , 0xEEA [5:0]

ROSD_DRAM_DATA[5:0] must be the last one.

Registers Table

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xE00	R/W	0	[7]: ROSD_EN8 [6]: ROSD_EN7 [5]: ROSD_EN6 [4]: ROSD_EN5 [3:0]: Reserved
0xE01	R/W	0	[7]: ROSD_TIME_EN8 [6]: ROSD_TIME_EN7 [5]: ROSD_TIME_EN6 [4]: ROSD_TIME_EN5 [3:0]: Reserved
0xE02	R/W	0	[7]: ROSD_TITLE_EN8 [6]: ROSD_TITLE_EN7 [5]: ROSD_TITLE_EN6 [4]: ROSD_TITLE_EN5 [3:0]: Reserved
0xE03	R/W	0	[7]: ROSD_STATUS_EN8 [6]: ROSD_STATUS_EN7 [5]: ROSD_STATUS_EN6 [4]: ROSD_STATUS_EN5 [3:0]: Reserved
0xE04	R/W	0	[7]: ROSD_BNDRY_EN8 [6]: ROSD_BNDRY_EN7 [5]: ROSD_BNDRY_EN6 [4]: ROSD_BNDRY_EN5 [3:0]: Reserved
0xE05	R/W	0	[7]: ROSD_BGND_EN8 [6]: ROSD_BGND_EN7 [5]: ROSD_BGND_EN6 [4]: ROSD_BGND_EN5 [3:0]: Reserved
0xE06	R/W	0	[7]: ROSD_MIX_8 [6]: ROSD_MIX_7 [5]: ROSD_MIX_6 [4]: ROSD_MIX_5 [3:0]: Reserved
0xE07	R/W	0x2	[3:0]: ROSD_BNDRY_WIDTH[3:0]
0xE08	R/W	0x77	[7:6]: ROSD_FONT_VSIZE_HALF [5:4]: ROSD_FONT_VSIZE_FULL [3:2]: ROSD_FONT_HSIZE_HALF [1:0]: ROSD_FONT_HSIZE_FULL
0xE09	R/W	0	ROSD_TIME_X_FULL[7:0]
0xE0A	R/W	0	ROSD_TIME_X_FULL[9:8]
0xE0B	R/W	0	ROSD_TIME_X_LEFT[7:0]
0xE0C	R/W	0	ROSD_TIME_X_LEFT[9:8]
0xE0D	R/W	0	ROSD_TIME_X_RIGHT[7:0]
0xE0E	R/W	0	ROSD_TIME_X_RIGHT[9:8]
0xE0F	R/W	0	ROSD_TIME_Y_FULL[7:0]
0xE10	R/W	0	ROSD_TIME_Y_FULL[9:8]
0xE11	R/W	0	ROSD_TIME_Y_TOP[7:0]
0xE12	R/W	0	ROSD_TIME_Y_TOP[9:8]
0xE13	R/W	0	ROSD_TIME_Y_BOTTOM[7:0]
0xE14	R/W	0	ROSD_TIME_Y_BOTTOM[9:8]
0xE15	R/W	0	ROSD_TITLE_X_FULL[7:0]
0xE16	R/W	0	ROSD_TITLE_X_FULL[9:8]

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xE17	R/W	0	ROSD_TITLE_X_LEFT[7:0]
0xE18	R/W	0	ROSD_TITLE_X_LEFT[9:8]
0xE19	R/W	0	ROSD_TITLE_X_RIGHT[7:0]
0xE1A	R/W	0	ROSD_TITLE_X_RIGHT[9:8]
0xE1B	R/W	0	ROSD_TITLE_Y_FULL[7:0]
0xE1C	R/W	0	ROSD_TITLE_Y_FULL[9:8]
0xE1D	R/W	0	ROSD_TITLE_Y_TOP[7:0]
0xE1E	R/W	0	ROSD_TITLE_Y_TOP[9:8]
0xE1F	R/W	0	ROSD_TITLE_Y_BOTTOM[7:0]
0xE20	R/W	0	ROSD_TITLE_Y_BOTTOM[9:8]
0xE21	R/W	0	ROSD_STATUS_X_FULL[7:0]
0xE22	R/W	0	ROSD_STATUS_X_FULL[9:8]
0xE23	R/W	0	ROSD_STATUS_X_LEFT[7:0]
0xE24	R/W	0	ROSD_STATUS_X_LEFT[9:8]
0xE25	R/W	0	ROSD_STATUS_X_RIGHT[7:0]
0xE26	R/W	0	ROSD_STATUS_X_RIGHT[9:8]
0xE27	R/W	0	ROSD_STATUS_Y_FULL[7:0]
0xE28	R/W	0	ROSD_STATUS_Y_FULL[9:8]
0xE29	R/W	0	ROSD_STATUS_Y_TOP[7:0]
0xE2A	R/W	0	ROSD_STATUS_Y_TOP[9:8]
0xE2B	R/W	0	ROSD_STATUS_Y_BOTTOM[7:0]
0xE2C	R/W	0	ROSD_STATUS_Y_BOTTOM[9:8]
0xE2D	R/W	0x10	ROSD_FONT_Y1[7:0]
0xE2E	R/W	0x80	ROSD_FONT_CB1[7:0]
0xE2F	R/W	0x80	ROSD_FONT_CR1[7:0]
0xE30	R/W	0x10	ROSD_FONT_Y2[7:0]
0xE31	R/W	0x80	ROSD_FONT_CB2[7:0]
0xE32	R/W	0x80	ROSD_FONT_CR2[7:0]
0xE33	R/W	0x10	ROSD_FONT_Y3[7:0]
0xE34	R/W	0x80	ROSD_FONT_CB3[7:0]
0xE35	R/W	0x80	ROSD_FONT_CR3[7:0]
0xE36	R/W	0x10	ROSD_BGND_Y[7:0]
0xE37	R/W	0x80	ROSD_BGND_CB[7:0]
0xE38	R/W	0x80	ROSD_BGND_CR[7:0]
0xE39	R/W	0x10	ROSD_BNDRY_Y[7:0]
0xE3A	R/W	0x80	ROSD_BNDRY_CB[7:0]
0xE3B	R/W	0x80	ROSD_BNDRY_CR[7:0]
0xE43	R/W	0	[7]: ROSD_COLBAR_EN8 [6]: ROSD_COLBAR_EN7 [5]: ROSD_COLBAR_EN6 [4]: ROSD_COLBAR_EN 5 [3:0]: Reserved
0xE44	R/W	0	[7]: ROSD_COLBAR_EN9 [6]: ROSD_MIX_9 [5]: ROSD_BGND_EN9 [4]: ROSD_BNDRY_EN9 [3]: ROSD_STATUS_EN9 [2]: ROSD_TITLE_EN9 [1]: ROSD_TIME_EN9 [0]: ROSD_EN9
0xE45	R/W	0	ROSD_COLBAR_VPOS[7:0]
0xE46	R/W	0	[4:0]: ROSD_FSWITCH

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xE4C	R/W	0	[7:4]: ROSD_FONT_VSIZE_ADD_FULL [3:0]: ROSD_FONT_HSIZE_ADD_FULL
0xE4D	R/W	0	[7:4]: ROSD_FONT_VSIZE_ADD_HALF [3:0]: ROSD_FONT_HSIZE_ADD_HALF
0xE50	R/W	0	ROSD_TITLE_OFF_P5[7:0]
0xE51	R/W	0	ROSD_TITLE_OFF_P5[15:8]
0xE52	R/W	0	ROSD_STATUS_OFF_P5[7:0]
0xE53	R/W	0	ROSD_STATUS_OFF_P5[15:8]
0xE54	R/W	0	ROSD_TITLE_OFF_P6[7:0]
0xE55	R/W	0	ROSD_TITLE_OFF_P6[15:8]
0xE56	R/W	0	ROSD_STATUS_OFF_P6[7:0]
0xE57	R/W	0	ROSD_STATUS_OFF_P6[15:8]
0xE58	R/W	0	ROSD_TITLE_OFF_P7[7:0]
0xE59	R/W	0	ROSD_TITLE_OFF_P7[15:8]
0xE5A	R/W	0	ROSD_STATUS_OFF_P7[7:0]
0xE5B	R/W	0	ROSD_STATUS_OFF_P7[15:8]
0xE5C	R/W	0	ROSD_TITLE_OFF_P8[7:0]
0xE5D	R/W	0	ROSD_TITLE_OFF_P8[15:8]
0xE5E	R/W	0	ROSD_STATUS_OFF_P8[7:0]
0xE5F	R/W	0	ROSD_STATUS_OFF_P8[15:8]
0xE60	R/W	0	ROSD_TITLE_OFF_P9[7:0]
0xE61	R/W	0	ROSD_TITLE_OFF_P9[15:8]
0xE62	R/W	0	ROSD_STATUS_OFF_P9[7:0]

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xE63	R/W	0	ROSD_STATUS_OFF_P9[15:8]
0xE70	R/W	0	ROSD_MSK_TOP1_W_P5
0xE71	R/W	0	ROSD_MSK_TOP2_W_P5
0xE72	R/W	0	ROSD_MSK_MID1_W_P5
0xE73	R/W	0	ROSD_MSK_MID2_W_P5
0xE74	R/W	0	ROSD_MSK_MID3_W_P5
0xE75	R/W	0	ROSD_MSK_MID4_W_P5
0xE76	R/W	0	ROSD_MSK_BOT1_W_P5
0xE77	R/W	0	ROSD_MSK_BOT2_W_P5
0xE79	R/W	0	ROSD_MSK_ON_P5
0xE7A	R/W	0	[7:4] : ROSD_VMSK_L2_W_P5 [3:0] : ROSD_VMSK_L1_W_P5
0xE7B	R/W	0	[7:4] : ROSD_VMSK_M2_W_P5 [3:0] : ROSD_VMSK_M1_W_P5
0xE7C	R/W	0	[7:4] : ROSD_VMSK_M4_W_P5 [3:0] : ROSD_VMSK_M3_W_P5
0xE7D	R/W	0	[7:4] : ROSD_VMSK_R2_W_P5 [3:0] : ROSD_VMSK_R1_W_P5
0xE7E	R/W	0	ROSD_VMSK_ON_P5
0xE80	R/W	0	ROSD_MSK_TOP1_W_P6
0xE81	R/W	0	ROSD_MSK_TOP2_W_P6
0xE82	R/W	0	ROSD_MSK_MID1_W_P6
0xE83	R/W	0	ROSD_MSK_MID2_W_P6
0xE84	R/W	0	ROSD_MSK_MID3_W_P6

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xE85	R/W	0	ROSD_MSK_MID4_W_P6
0xE86	R/W	0	ROSD_MSK_BOT1_W_P6
0xE87	R/W	0	ROSD_MSK_BOT2_W_P6
0xE89	R/W	0	ROSD_MSK_ON_P6
0xE8A	R/W	0	[7:4] : ROSD_VMSK_L2_W_P6 [3:0] : ROSD_VMSK_L1_W_P6
0xE8B	R/W	0	[7:4] : ROSD_VMSK_M2_W_P6 [3:0] : ROSD_VMSK_M1_W_P6
0xE8C	R/W	0	[7:4] : ROSD_VMSK_M4_W_P6 [3:0] : ROSD_VMSK_M3_W_P6
0xE8D	R/W	0	[7:4] : ROSD_VMSK_R2_W_P6 [3:0] : ROSD_VMSK_R1_W_P6
0xE8E	R/W	0	ROSD_VMSK_ON_P6
0xE90	R/W	0	ROSD_MSK_TOP1_W_P7
0xE91	R/W	0	ROSD_MSK_TOP2_W_P7
0xE92	R/W	0	ROSD_MSK_MID1_W_P7
0xE93	R/W	0	ROSD_MSK_MID2_W_P7
0xE94	R/W	0	ROSD_MSK_MID3_W_P7
0xE95	R/W	0	ROSD_MSK_MID4_W_P7
0xE96	R/W	0	ROSD_MSK_BOT1_W_P7
0xE97	R/W	0	ROSD_MSK_BOT2_W_P7
0xE99	R/W	0	ROSD_MSK_ON_P7
0xE9A	R/W	0	[7:4] : ROSD_VMSK_L2_W_P7 [3:0] : ROSD_VMSK_L1_W_P7

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xE9B	R/W	0	[7:4] : ROSD_VMSK_M2_W_P7 [3:0] : ROSD_VMSK_M1_W_P7
0xE9C	R/W	0	[7:4] : ROSD_VMSK_M4_W_P7 [3:0] : ROSD_VMSK_M3_W_P7
0xE9D	R/W	0	[7:4] : ROSD_VMSK_R2_W_P7 [3:0] : ROSD_VMSK_R1_W_P7
0xE9E	R/W	0	ROSD_VMSK_ON_P7
0xEA0	R/W	0	ROSD_MSK_TOP1_W_P8
0xEA1	R/W	0	ROSD_MSK_TOP2_W_P8
0xEA2	R/W	0	ROSD_MSK_MID1_W_P8
0xEA3	R/W	0	ROSD_MSK_MID2_W_P8
0xEA4	R/W	0	ROSD_MSK_MID3_W_P8
0xEA5	R/W	0	ROSD_MSK_MID4_W_P8
0xEA6	R/W	0	ROSD_MSK_BOT1_W_P8
0xEA7	R/W	0	ROSD_MSK_BOT2_W_P8
0xEA9	R/W	0	ROSD_MSK_ON_P8
0xEAA	R/W	0	[7:4] : ROSD_VMSK_L2_W_P8 [3:0] : ROSD_VMSK_L1_W_P8
0xEAB	R/W	0	[7:4] : ROSD_VMSK_M2_W_P8 [3:0] : ROSD_VMSK_M1_W_P8
0xEAC	R/W	0	[7:4] : ROSD_VMSK_M4_W_P8 [3:0] : ROSD_VMSK_M3_W_P8
0xEAD	R/W	0	[7:4] : ROSD_VMSK_R2_W_P8 [3:0] : ROSD_VMSK_R1_W_P8

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xEAE	R/W	0	ROSD_VMSK_ON_P8
0xEB0	R/W	0	ROSD_MSK_TOP1_W_P9
0xEB1	R/W	0	ROSD_MSK_TOP2_W_P9
0xEB2	R/W	0	ROSD_MSK_MID1_W_P9
0xEB3	R/W	0	ROSD_MSK_MID2_W_P9
0xEB4	R/W	0	ROSD_MSK_MID3_W_P9
0xEB5	R/W	0	ROSD_MSK_MID4_W_P9
0xEB6	R/W	0	ROSD_MSK_BOT1_W_P9
0xEB7	R/W	0	ROSD_MSK_BOT2_W_P9
0xEB9	R/W	0	ROSD_MSK_ON_P9
0xEBA	R/W	0	[7:4] : ROSD_VMSK_L2_W_P9 [3:0] : ROSD_VMSK_L1_W_P9
0xEBB	R/W	0	[7:4] : ROSD_VMSK_M2_W_P9 [3:0] : ROSD_VMSK_M1_W_P9
0xEBC	R/W	0	[7:4] : ROSD_VMSK_M4_W_P9 [3:0] : ROSD_VMSK_M3_W_P9
0xEBD	R/W	0	[7:4] : ROSD_VMSK_R2_W_P9 [3:0] : ROSD_VMSK_R1_W_P9
0xEBE	R/W	0	ROSD_VMSK_ON_P9
0xEC0	R/W	0	ROSD_MSK_Y
0xEC1	R/W	0	ROSD_MSK_CB
0xEC2	R/W	0	ROSD_MSK_CR
0xED0	R/W	0	OSD_V_OFF_P5[7:0]

ADDRESS	R/W	DEFAULT	DESCRIPTION
0xED1	R/W	0	[7:4]: OSD_H_OFF_P5[11:8] [3:0]: OSD_V_OFF_P5[11:8]
0xED2	R/W	0	OSD_H_OFF_P5[7:0]
0xED3	R/W	0	OSD_V_OFF_P6[7:0]
0xED4	R/W	0	[7:4]: OSD_H_OFF_P6[11:8] [3:0]: OSD_V_OFF_P6[11:8]
0xED5	R/W	0	OSD_H_OFF_P6[7:0]
0xED6	R/W	0	OSD_V_OFF_P7[7:0]
0xED7	R/W	0	[7:4]: OSD_H_OFF_P7[11:8] [3:0]: OSD_V_OFF_P7[11:8]
0xED8	R/W	0	OSD_H_OFF_P7[7:0]
0xED9	R/W	0	OSD_V_OFF_P8[7:0]
0xEDA	R/W	0	[7:4]: OSD_H_OFF_P8[11:8] [3:0]: OSD_V_OFF_P8[11:8]
0xEDB	R/W	0	OSD_H_OFF_P8[7:0]
0xEDC	R/W	0	OSD_V_OFF_P9[7:0]
0xEDD	R/W	0	[7:4]: OSD_H_OFF_P9[11:8] [3:0]: OSD_V_OFF_P9[11:8]
0xEDE	R/W	0	OSD_H_OFF_P9[7:0]
0xEE0	W	0	ROSD_FRAM_ADDR[7:0]
0xEE1	W	0	ROSD_FRAM_ADDR[9:8]
0xEE2	W	0	ROSD_FRAM_DATA[7:0]
0xEE3	W	0	ROSD_FRAM_DATA[15:8]
0xEE4	W	0	ROSD_FRAM_DATA[23:16]
0xEE5	W	0	ROSD_FRAM_DATA[31:24]
0xEE6	W	0	ROSD_FRAM_DATA[39:32]
0xEE7	W	0	[3:0]: ROSD_FRAM_DATA[43:40]
0xEE8	W	0	ROSD_DRAM_ADDR[7:0]
0xEE9	W	0	ROSD_DRAM_ADDR[9:8]
0xEEA	W	0	ROSD_DRAM_DATA[5:0]
0xEEA	W	0	ROSD_DRAM_DATA[5:0]

Register Descriptions

ROSD ENABLE REGISTER – 0XE00

Bit	R/W	Default	Description
7:4	RW	0	ROSD_EN [7]: ROSD_EN8 [6]: ROSD_EN7 [5]: ROSD_EN6 [4]: ROSD_EN5 Recording port n (5 to 8) OSD enable or disable. If this register is set to 1, OSD is enabled. But you need to set ROSD_TIME_EN or ROSD_TITLE_EN or ROSD_STATUS_EN if needed. If ROSD_EN is set to 0, all ROSD display is disabled.
3:0	RW	0	Reserved

ROSD TIME AND DATE ENABLE REGISTER – 0XE01

Bit	R/W	Default	Description
7:4	RW	0	ROSD_TIME_EN [7]: ROSD_TIME_EN8 [6]: ROSD_TIME_EN7 [5]: ROSD_TIME_EN6 [4]: ROSD_TIME_EN5 Recording port n (5 to 8) time and date enable or disable. To enable time and date, you need to set ROSD_EN and ROSD_TIME_EN.
3:0	RW	0	Reserved

ROSD TITLE ENABLE REGISTER – 0XE02

Bit	R/W	Default	Description
7:4	RW	0	ROSD_TITLE_EN [7]: ROSD_TITLE_EN8 [6]: ROSD_TITLE_EN7 [5]: ROSD_TITLE_EN6 [4]: ROSD_TITLE_EN5 Recording port n (5 to 8) title enable or disable. To enable title, you need to set ROSD_EN and ROSD_TITLE_EN.
3:0	RW	0	Reserved

ROSD STATUS ENABLE REGISTER – 0XE03

Bit	R/W	Default	Description
7:4	RW	0	ROSD_STATUS_EN [7]: ROSD_STATUS_EN8 [6]: ROSD_STATUS_EN7 [5]: ROSD_STATUS_EN6 [4]: ROSD_STATUS_EN5 Recording port n (5 to 8) status enable or disable. To enable status, you need to set ROSD_EN and ROSD_STATUS_EN.
3:0	RW	0	Reserved

ROSD BOUNDARY ENABLE REGISTER – 0XE04

Bit	R/W	Default	Description
7:4	RW	0	ROSD_BNDRY_EN [7]: ROSD_BNDRY_EN8 [6]: ROSD_BNDRY_EN7 [5]: ROSD_BNDRY_EN6 [4]: ROSD_BNDRY_EN5 Recording port n (5 to 8) boundary enable or disable. To enable boundary, you need to set ROSD_EN and ROSD_BNDRY_EN.
3:0	RW	0	Reserved

ROSD BACKGROUND ENABLE REGISTER – 0XE05

Bit	R/W	Default	Description
7:4	RW	0	ROSD_BGND_EN [7]: ROSD_BGND_EN8 [6]: ROSD_BGND_EN7 [5]: ROSD_BGND_EN6 [4]: ROSD_BGND_EN5 Recording port n (5 to 8) back ground enable or disable. To enable back ground, you need to set ROSD_EN and ROSD_BGND_EN.
3:0	RW	0	Reserved

ROSD MIX CONTROL ENABLE REGISTER – 0XE06

Bit	R/W	Default	Description
7:4	RW	0	ROSD_MIX [7]: ROSD_MIX_8 [6]: ROSD_MIX_7 [5]: ROSD_MIX_6 [4]: ROSD_MIX_5 Display font mix enable bit. If set to 1, font data will be 50% blending with video 1: enable 0: disable
3:0	RW	0	Reserved

ROSD BOUNDARY WIDTH REGISTER – 0XE07

Bit	R/W	Default	Description
3:0	RW	2	ROSD_BNDRY_WIDTH Boundary width from 0 to 15. Unit is 2 pixels. Only Quad has boundary.

ROSD FONT SIZE REGISTER – 0XE08

Bit	R/W	Default	Description
7:6	RW	1	ROSD_FONT_VSIZE_HALF Font vertical size for Quad and CIF mode. There are four choices. 00: 8 + ROSD_FONT_VSIZE_ADD_HALF 01: 24 + ROSD_FONT_VSIZE_ADD_HALF 10: 16 + 2X ROSD_FONT_VSIZE_ADD_HALF (font repeat 2 times) 11: 48 + ROSD_FONT_VSIZE_ADD_HALF
5:4	RW	3	ROSD_FONT_VSIZE_FULL Font vertical size for D1 and half D1 mode. There are four choices. 00: 8 + ROSD_FONT_VSIZE_ADD_FULL 01: 24 + ROSD_FONT_VSIZE_ADD_FULL 10: 16 + 2X ROSD_FONT_VSIZE_ADD_FULL (font repeat 2 times) 11: 48 + ROSD_FONT_VSIZE_ADD_FULL
3:2	RW	1	ROSD_FONT_HSIZE_HALF Font horizontal size for Quad, half D1 and CIF mode. There are four choices. 00: 8 + ROSD_FONT_HSIZE_ADD_HALF 01: 24 + ROSD_FONT_HSIZE_ADD_HALF 10: 16 + 2X ROSD_FONT_HSIZE_ADD_HALF (font repeat 2 times) 11: 48 + ROSD_FONT_HSIZE_ADD_HALF
1:0	RW	1	ROSD_FONT_HSIZE_FULL Font horizontal size for D1 mode. There are four choices. 00: 8 + ROSD_FONT_HSIZE_ADD_FULL 01: 24 + ROSD_FONT_HSIZE_ADD_FULL 10: 16 + 2X ROSD_FONT_HSIZE_ADD_FULL (font repeat 2 times) 11: 48 + ROSD_FONT_HSIZE_ADD_FULL

ROSD TIME HORIZONTAL POSTION FOR FULL MODE LOW BYTE REGISTER – 0XE09

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TIME_X_FULL[7:0] Time and Date horizontal position for D1 mode. Unit is 1 pixel

ROSD TIME HORIZONTAL POSTION FOR FULL MODE HIGH BYTE REGISTER – 0XE0A

Bit	R/W	Default	Description
1:0	RW	0	ROSD_TIME_X_FULL[9:8] Time and Date horizontal position for D1 mode. Unit is 1 pixel

ROSD TIME HORIZONTAL LEFT POSTION FOR HALF MODE LOW BYTE REGISTER – 0XE0B

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TIME_X_LEFT[7:0] Time and Date horizontal left position for half D1, Quad and CIF mode. Unit is 1 pixel

ROSD TIME HORIZONTAL LEFT POSTION FOR HALF MODE HIGH BYTE REGISTER – 0XE0C

Bit	R/W	Default	Description
1:0	RW	0	ROSD_TIME_X_LEFT[9:8] Time and Date horizontal left position for half D1, Quad and CIF mode. Unit is 1 pixel

ROSD TIME HORIZONTAL RIGHT POSTION FOR HALF MODE LOW BYTE REGISTER – 0XE0D

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TIME_X_RIGHT[7:0] Time and Date horizontal right position for half D1, Quad and CIF mode. Unit is 1 pixel

ROSD TIME HORIZONTAL RIGHT POSTION FOR HALF MODE HIGH BYTE REGISTER – 0XE0E

Bit	R/W	Default	Description
1:0	RW	0	ROSD_TIME_X_RIGHT[9:8] Time and Date horizontal right position for half D1, Quad and CIF mode. Unit is 1 pixel

ROSD TIME VERTICAL POSTION FOR FULL MODE LOW BYTE REGISTER – 0XE0F

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TIME_Y_FULL[7:0] Time and Date vertical position for D1 and half D1 mode. Unit is 1 pixel

ROSD TIME VERTICAL POSTION FOR FULL MODE HIGH BYTE REGISTER – 0XE10

Bit	R/W	Default	Description
1:0	RW	0	ROSD_TIME_Y_FULL[9:8] Time and Date vertical position for D1 and half D1 mode. Unit is 1 pixel

ROSD TIME VERTICAL TOP POSTION FOR HALF MODE LOW BYTE REGISTER – 0XE11

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TIME_Y_TOP[7:0] Time and Date vertical top position for Quad and CIF mode. Unit is 1 pixel

ROSD TIME VERTICAL TOP POSTION FOR HALF MODE HIGH BYTE REGISTER – 0XE12

Bit	R/W	Default	Description
1:0	RW	0	ROSD_TIME_Y_TOP[9:8] Time and Date vertical top position for Quad and CIF mode. Unit is 1 pixel

ROSD TIME VERTICAL BOTTOM POSTION FOR HALF MODE LOW BYTE REGISTER – 0XE13

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TIME_Y_BOTTOM[7:0] Time and Date vertical bottom position for Quad and CIF mode. Unit is 1 pixel

ROSD TIME VERTICAL BOTTOM POSTION FOR HALF MODE HIGH BYTE REGISTER – 0XE14

Bit	R/W	Default	Description
1:0	RW	0	ROSD_TIME_Y_BOTTOM[9:8] Time and Date vertical bottom position for Quad and CIF mode. Unit is 1 pixel

ROSD TITLE HORIZONTAL POSTION FOR FULL MODE LOW BYTE REGISTER – 0XE15

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_X_FULL[7:0] Title horizontal position for D1 mode. Unit is 1 pixel

ROSD TITLE HORIZONTAL POSTION FOR FULL MODE HIGH BYTE REGISTER – 0XE16

Bit	R/W	Default	Description
1:0	RW	0	ROSD_TITLE_X_FULL[9:8] Title horizontal position for D1 mode. Unit is 1 pixel

ROSD TITLE HORIZONTAL LEFT POSTION FOR HALF MODE LOW BYTE REGISTER – 0XE17

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_X_LEFT[7:0] Title horizontal left position for half D1, Quad and CIF mode. Unit is 1 pixel

ROSD TITLE HORIZONTAL LEFT POSTION FOR HALF MODE HIGH BYTE REGISTER – 0XE18

Bit	R/W	Default	Description
1:0	RW	0	ROSD_TITLE_X_LEFT[9:8] Title horizontal left position for half D1, Quad and CIF mode. Unit is 1 pixel

ROSD TITLE HORIZONTAL RIGHT POSTION FOR HALF MODE LOW BYTE REGISTER – 0XE19

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_X_RIGHT[7:0] Title horizontal right position for half D1, Quad and CIF mode. Unit is 1 pixel

ROSD TITLE HORIZONTAL RIGHT POSTION FOR HALF MODE HIGH BYTE REGISTER – 0XE1A

Bit	R/W	Default	Description
1:0	RW	0	ROSD_TITLE_X_RIGHT[9:8] Title horizontal right position for half D1, Quad and CIF mode. Unit is 1 pixel

ROSD TITLE VERTICAL POSTION FOR FULL MODE LOW BYTE REGISTER – 0XE1B

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_Y_FULL[7:0] Title vertical position for D1 and half D1 mode. Unit is 1 pixel

ROSD TITLE VERTICAL POSTION FOR FULL MODE HIGH BYTE REGISTER – 0XE1C

Bit	R/W	Default	Description
1:0	RW	0	ROSD_TITLE_Y_FULL[9:8] Title vertical position for D1 and half D1 mode. Unit is 1 pixel

ROSD TITLE VERTICAL TOP POSTION FOR HALF MODE LOW BYTE REGISTER – 0XE1D

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_Y_TOP[7:0] Title vertical top position for Quad and CIF mode. Unit is 1 pixel

ROSD TITLE VERTICAL TOP POSTION FOR HALF MODE HIGH BYTE REGISTER – 0XE1E

Bit	R/W	Default	Description
1:0	RW	0	ROSD_TITLE_Y_TOP[9:8] Title vertical top position for Quad and CIF mode. Unit is 1 pixel

ROSD TITLE VERTICAL BOTTOM POSTION FOR HALF MODE LOW BYTE REGISTER – 0XE1F

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_Y_BOTTOM[7:0] Title vertical bottom position for Quad and CIF mode. Unit is 1 pixel

ROSD TITLE VERTICAL BOTTOM POSTION FOR HALF MODE HIGH BYTE REGISTER – 0XE20

Bit	R/W	Default	Description
1:0	RW	0	ROSD_TITLE_Y_BOTTOM[9:8] Title vertical bottom position for Quad and CIF mode. Unit is 1 pixel

ROSD STATUS HORIZONTAL POSTION FOR FULL MODE LOW BYTE REGISTER – 0XE21

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_X_FULL[7:0] Status horizontal position for D1 mode. Unit is 1 pixel

ROSD STATUS HORIZONTAL POSTION FOR FULL MODE HIGH BYTE REGISTER – 0XE22

Bit	R/W	Default	Description
1:0	RW	0	ROSD_STATUS_X_FULL[9:8] Status horizontal position for D1 mode. Unit is 1 pixel

ROSD STATUS HORIZONTAL LEFT POSTION FOR HALF MODE LOW BYTE REGISTER – 0XE23

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_X_LEFT[7:0] Status horizontal left position for half D1, Quad and CIF mode. Unit is 1 pixel

ROSD STATUS HORIZONTAL LEFT POSTION FOR HALF MODE HIGH BYTE REGISTER – 0XE24

Bit	R/W	Default	Description
1:0	RW	0	ROSD_STATUS_X_LEFT[9:8] Status horizontal left position for half D1, Quad and CIF mode. Unit is 1 pixel

ROSD STATUS HORIZONTAL RIGHT POSTION FOR HALF MODE LOW BYTE REGISTER – 0XE25

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_X_RIGHT[7:0] Status horizontal right position for half D1, Quad and CIF mode. Unit is 1 pixel

ROSD STATUS HORIZONTAL RIGHT POSTION FOR HALF MODE HIGH BYTE REGISTER – 0XE26

Bit	R/W	Default	Description
1:0	RW	0	ROSD_STATUS_X_RIGHT[9:8] Status horizontal right position for half D1, Quad and CIF mode. Unit is 1 pixel

ROSD STATUS VERTICAL POSTION FOR FULL MODE LOW BYTE REGISTER – 0XE27

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_Y_FULL[7:0] Status vertical position for D1 and half D1 mode. Unit is 1 pixel

ROSD STATUS VERTICAL POSTION FOR FULL MODE HIGH BYTE REGISTER – 0XE28

Bit	R/W	Default	Description
1:0	RW	0	ROSD_STATUS_Y_FULL[9:8] Status vertical position for D1 and half D1 mode. Unit is 1 pixel

ROSD STATUS VERTICAL TOP POSTION FOR HALF MODE LOW BYTE REGISTER – 0XE29

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_Y_TOP[7:0] Status vertical top position for Quad and CIF mode. Unit is 1 pixel

ROSD STATUS VERTICAL TOP POSTION FOR HALF MODE HIGH BYTE REGISTER – 0XE2A

Bit	R/W	Default	Description
1:0	RW	0	ROSD_STATUS_Y_TOP[9:8] Status vertical top position for Quad and CIF mode. Unit is 1 pixel

ROSD STATUS VERTICAL BOTTOM POSTION FOR HALF MODE LOW BYTE REGISTER – 0XE2B

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_Y_BOTTOM[7:0] Status vertical bottom position for Quad and CIF mode. Unit is 1 pixel

ROSD STATUS VERTICAL BOTTOM POSTION FOR HALF MODE HIGH BYTE REGISTER – 0XE2C

Bit	R/W	Default	Description
1:0	RW	0	ROSD_STATUS_Y_BOTTOM[9:8] Status vertical bottom position for Quad and CIF mode. Unit is 1 pixel

ROSD FONT Y COLOR 1 REGISTER – 0XE2D

Bit	R/W	Default	Description
7:0	RW	0x10	ROSD_FONT_Y1[7:0] Font color Y for index 1

ROSD FONT CB COLOR 1 REGISTER – 0XE2E

Bit	R/W	Default	Description
7:0	RW	0x80	ROSD_FONT_CB1[7:0] Font color Cb for index 1

ROSD FONT CR COLOR 1 REGISTER – 0XE2F

Bit	R/W	Default	Description
7:0	RW	0x80	ROSD_FONT_CR1[7:0] Font color Cr for index 1

ROSD FONT Y COLOR 2 REGISTER – 0XE30

Bit	R/W	Default	Description
7:0	RW	0x10	ROSD_FONT_Y2[7:0] Font color Y for index 2

ROSD FONT CB COLOR 2 REGISTER – 0XE31

Bit	R/W	Default	Description
7:0	RW	0x80	ROSD_FONT_CB2[7:0] Font color Cb for index 2

ROSD FONT CR COLOR 2 REGISTER – 0XE32

Bit	R/W	Default	Description
7:0	RW	0x80	ROSD_FONT_CR2[7:0] Font color Cr for index 2

ROSD FONT Y COLOR 3 REGISTER – 0XE33

Bit	R/W	Default	Description
7:0	RW	0x10	ROSD_FONT_Y3[7:0] Font color Y for index 3

ROSD FONT CB COLOR 3 REGISTER – 0XE34

Bit	R/W	Default	Description
7:0	RW	0x80	ROSD_FONT_CB3[7:0] Font color Cb for index 3

ROSD FONT CR COLOR 3 REGISTER – 0XE35

Bit	R/W	Default	Description
7:0	RW	0x80	ROSD_FONT_CR3[7:0] Font color Cr for index 3

ROSD BACKGROUND Y COLOR REGISTER – 0XE36

Bit	R/W	Default	Description
7:0	RW	0x10	ROSD_BGND_Y [7:0] Background color Y

ROSD BACKGROUND CB COLOR REGISTER – 0XE37

Bit	R/W	Default	Description
7:0	RW	0x80	ROSD_BGND_CB[7:0] Background color Cb

ROSD BACKGROUND CR COLOR REGISTER – 0XE38

Bit	R/W	Default	Description
7:0	RW	0x80	ROSD_BGND_CR[7:0] Background color Cr

ROSD BOUNDARY Y COLOR REGISTER – 0XE39

Bit	R/W	Default	Description
7:0	RW	0x10	ROSD_BNDRY_Y[7:0] Boundary color Y

ROSD BOUNDARY CB COLOR REGISTER – 0XE3A

Bit	R/W	Default	Description
7:0	RW	0x80	ROSD_BNDRY_CB[7:0] Boundary color Cb

ROSD BOUNDARY CR COLOR REGISTER – 0XE3B

Bit	R/W	Default	Description
7:0	RW	0x80	ROSD_BNDRY_CR[7:0] Boundary color Cr

ROSD COLOR BAR ENABLE REGISTER – 0XE43

Bit	R/W	Default	Description
7:4	RW	0	ROSD_COLBAR_EN [7]: ROSD_COLBAR_EN8 [6]: ROSD_COLBAR _EN7 [5]: ROSD_COLBAR _EN6 [4]: ROSD_COLBAR _EN5 Recording port n (5 to 8) color bar enable or disable.
3:0	RW	0	Reserved

ROSD ENABLE FOR PORT 9 REGISTER – 0XE44

Bit	R/W	Default	Description
7:0	RW	0	[7]: ROSD_COLBAR_EN9 [6]: ROSD_MIX_9 [5]: ROSD_BGND_EN9 [4]: ROSD_BNDRY_EN9 [3]: ROSD_STATUS_EN9 [2]: ROSD_TITLE_EN9 [1]: ROSD_TIME_EN9 [0]: ROSD_EN9

ROSD COLBAR VERITICAL BLACK BAR POSITION REGISTER – 0XE45

Bit	R/W	Default	Description
7:0	RW	0	ROSD_COLBAR_VPOS[7:0] There is a black bar (32 lines) in color bar. This register defines start position for this bar. It is for test purpose.

ROSD FIELD SWITCH REGISTER – 0XE46

Bit	R/W	Default	Description
7:5	RW	0	Reserved
4:0	RW	0	ROSD_FSWITCH Field switch mode for record port 5(Bit 0) to 9(Bit 4) 0: not field switch 1: field switch

ROSD FONT FULL SIZE CONTROL REGISTER – 0XE4C

Bit	R/W	Default	Description
7:4	RW	0	ROSD_FONT_VSIZE_ADD_FULL Add value for controlling rosd font vertical size of full size image
3:0	RW	0	ROSD_FONT_HSIZE_ADD_FULL Add value for controlling rosd font horizontal size of full size image

ROSD FONT HALF SIZE CONTROL REGISTER – 0XE4D

Bit	R/W	Default	Description
7:4	RW	0	ROSD_FONT_VSIZE_ADD_HALF Add value for controlling rosd font vertical size of small size image
3:0	RW	0	ROSD_FONT_HSIZE_ADD_HALF Add value for controlling rosd font horizontal size of small size image

ROSD TITLE ON/OFF CONTROL REGISTER FOR 1ST ~ 8TH CHANNEL OF PORT 5 – 0XE50

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_OFF_P5[7:0] Bit 0 : 1st channel title off(0: On, 1: Off) … Bit 7 : 8th channel title off(0: On, 1: Off)

ROSD TITLE ON/OFF CONTROL REGISTER FOR 9TH ~ 16TH CHANNEL OF PORT 5 – 0XE51

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_OFF_P5[15:8] Bit 0 : 8st channel title off(0: On, 1: Off) … Bit 7 : 16th channel title off(0: On, 1: Off)

ROSD STATUS ON/OFF CONTROL REGISTER FOR 1ST ~ 8TH CHANNEL OF PORT 5 – 0XE52

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_OFF_P5[7:0] Bit 0 : 1st channel status off(0: On, 1: Off) ... Bit 7 : 8th channel status off(0: On, 1: Off)

ROSD STATUS ON/OFF CONTROL REGISTER FOR 9TH ~ 16TH CHANNEL OF PORT 5 – 0XE53

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_OFF_P5[15:8] Bit 0 : 8st channel status off(0: On, 1: Off) ... Bit 7 : 16th channel status off(0: On, 1: Off)

ROSD TITLE ON/OFF CONTROL REGISTER FOR 1ST ~ 8TH CHANNEL OF PORT 6 – 0XE54

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_OFF_P6[7:0] Bit 0 : 1st channel title off(0: On, 1: Off) ... Bit 7 : 8th channel title off(0: On, 1: Off)

ROSD TITLE ON/OFF CONTROL REGISTER FOR 9TH ~ 16TH CHANNEL OF PORT 6 – 0XE55

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_OFF_P6[15:8] Bit 0 : 8st channel title off(0: On, 1: Off) ... Bit 7 : 16th channel title off(0: On, 1: Off)

ROSD STATUS ON/OFF CONTROL REGISTER FOR 1ST ~ 8TH CHANNEL OF PORT 6 – 0XE56

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_OFF_P6[7:0] Bit 0 : 1st channel status off(0: On, 1: Off) ... Bit 7 : 8th channel status off(0: On, 1: Off)

ROSD STATUS ON/OFF CONTROL REGISTER FOR 9TH ~ 16TH CHANNEL OF PORT 6 – 0XE57

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_OFF_P6[15:8] Bit 0 : 8st channel status off(0: On, 1: Off) … Bit 7 : 16th channel status off(0: On, 1: Off)

ROSD TITLE ON/OFF CONTROL REGISTER FOR 1ST ~ 8TH CHANNEL OF PORT 7 – 0XE58

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_OFF_P7[7:0] Bit 0 : 1st channel title off(0: On, 1: Off) … Bit 7 : 8th channel title off(0: On, 1: Off)

ROSD TITLE ON/OFF CONTROL REGISTER FOR 9TH ~ 16TH CHANNEL OF PORT 7 – 0XE59

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_OFF_P7[15:8] Bit 0 : 8st channel title off(0: On, 1: Off) … Bit 7 : 16th channel title off(0: On, 1: Off)

ROSD STATUS ON/OFF CONTROL REGISTER FOR 1ST ~ 8TH CHANNEL OF PORT 7 – 0XE5A

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_OFF_P7[7:0] Bit 0 : 1st channel status off(0: On, 1: Off) … Bit 7 : 8th channel status off(0: On, 1: Off)

ROSD STATUS ON/OFF CONTROL REGISTER FOR 9TH ~ 16TH CHANNEL OF PORT 7 – 0XE5B

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_OFF_P7[15:8] Bit 0 : 8st channel status off(0: On, 1: Off) … Bit 7 : 16th channel status off(0: On, 1: Off)

ROSD TITLE ON/OFF CONTROL REGISTER FOR 1ST ~ 8TH CHANNEL OF PORT 8 – 0XE5C

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_OFF_P8[7:0] Bit 0 : 1st channel title off(0: On, 1: Off) ... Bit 7 : 8th channel title off(0: On, 1: Off)

ROSD TITLE ON/OFF CONTROL REGISTER FOR 9TH ~ 16TH CHANNEL OF PORT 8 – 0XE5D

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_OFF_P8[15:8] Bit 0 : 8st channel title off(0: On, 1: Off) ... Bit 7 : 16th channel title off(0: On, 1: Off)

ROSD STATUS ON/OFF CONTROL REGISTER FOR 1ST ~ 8TH CHANNEL OF PORT 8 – 0XE5E

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_OFF_P8[7:0] Bit 0 : 1st channel status off(0: On, 1: Off) ... Bit 7 : 8th channel status off(0: On, 1: Off)

ROSD STATUS ON/OFF CONTROL REGISTER FOR 9TH ~ 16TH CHANNEL OF PORT 8 – 0XE5F

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_OFF_P8[15:8] Bit 0 : 8st channel status off(0: On, 1: Off) ... Bit 7 : 16th channel status off(0: On, 1: Off)

ROSD TITLE ON/OFF CONTROL REGISTER FOR 1ST ~ 8TH CHANNEL OF PORT 9 – 0XE60

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_OFF_P9[7:0] Bit 0 : 1st channel title off(0: On, 1: Off) ... Bit 7 : 8th channel title off(0: On, 1: Off)

ROSD TITLE ON/OFF CONTROL REGISTER FOR 9TH ~ 16TH CHANNEL OF PORT 9 – 0XE61

Bit	R/W	Default	Description
7:0	RW	0	ROSD_TITLE_OFF_P9[15:8] Bit 0 : 8st channel title off(0: On, 1: Off) ... Bit 7 : 16th channel title off(0: On, 1: Off)

ROSD STATUS ON/OFF CONTROL REGISTER FOR 1ST ~ 8TH CHANNEL OF PORT 9 – 0XE62

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_OFF_P9[7:0] Bit 0 : 1st channel status off(0: On, 1: Off) ... Bit 7 : 8th channel status off(0: On, 1: Off)

ROSD STATUS ON/OFF CONTROL REGISTER FOR 9TH ~ 16TH CHANNEL OF PORT 9 – 0XE63

Bit	R/W	Default	Description
7:0	RW	0	ROSD_STATUS_OFF_P9[15:8] Bit 0 : 8st channel status off(0: On, 1: Off) ... Bit 7 : 16th channel status off(0: On, 1: Off)

ROSD MASK 1ST TOP SIDE WIDTH OF PORT 5 – 0XE70

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_TOP1_W_P5 Line number for masking in the top and left side

ROSD MASK 2ND TOP SIDE WIDTH OF PORT 5 – 0XE71

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_TOP2_W_P5 Line number for masking in the top and right side

ROSD MASK 1ST CENTER SIDE WIDTH OF PORT 5 – 0XE72

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID1_W_P5 Line number for masking in the 1st center and left side

ROSD MASK 2ND CENTER SIDE WIDTH OF PORT 5 – 0XE73

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID2_W_P5 Line number for masking in the 1st center and right side

ROSD MASK 3RD CENTER SIDE WIDTH OF PORT 5 – 0XE74

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID3_W_P5 Line number for masking in the 2nd center and left side

ROSD MASK 4TH CENTER SIDE WIDTH OF PORT 5 – 0XE75

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID4_W_P5 Line number for masking in the 2nd center and right side

ROSD MASK 1ST BOTTOM SIDE WIDTH OF PORT 5 – 0XE76

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_BOT1_W_P5 Line number for masking in the bottom and left side

ROSD MASK 2ND BOTTOM SIDE WIDTH OF PORT 5 – 0XE77

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_BOT2_W_P5 Line number for masking in the top and right side

ROSD MASK POSITION CONTROL OF PORT 5 – 0XE78

Bit	R/W	Default	Description
7:6	R	0	Reserved
5:4	RW	1	ROSD_MSK_VPOS_P5 Vertical position of masking area 00: 1st area among 4 vertical divisions 01: 2nd area among 4 vertical divisions 10: 3rd area among 4 vertical divisions 11: 4th area among 4 vertical divisions
3:2	R	0	Reserved

Bit	R/W	Default	Description
1:0	RW	1	ROSD_MSK_HPOS_P5 Horizontal position of masking area 00: 1st area among 4 horizontal divisions 01: 2nd area among 4 horizontal divisions 10: 3rd area among 4 horizontal divisions 11: 4th area among 4 horizontal divisions

ROSD MASK ON/OFF CONTROL OF PORT 5 – 0XE79

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_ON_P5 ROSD masking on/off control for port 5 (0: off, 1: on) Bit 0 : 1st top Bit 1 : 2nd top Bit 2 : 1st center Bit 3 : 2nd center Bit 4 : 3rd center Bit 5 : 4th center Bit 6 : 1st bottom Bit 7 : 2nd bottom

ROSD MASK 1ST /2ND VERTICAL LEFT SIDE WIDTH OF PORT 5 – 0XE7A

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_L2_W_P5 Pixel number for masking in 2nd vertical left side
7:4	RW	0	ROSD_VMSK_L1_W_P5 Pixel number for masking in 1st vertical left side

ROSD MASK 1ST / 2ND VERTICAL CENTER SIDE WIDTH OF PORT 5 – 0XE7B

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_M2_W_P5 Pixel number for masking in 2nd vertical center side
7:4	RW	0	ROSD_VMSK_M1_W_P5 Pixel number for masking in 1st vertical center side

ROSD MASK 3RD / 4TH VERTICAL CENTER SIDE WIDTH OF PORT 5 – 0XE7C

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_M4_W_P5 Pixel number for masking in 4th vertical center side
7:4	RW	0	ROSD_VMSK_M3_W_P5 Pixel number for masking in 3rd vertical center side

ROSD MASK 1ST / 2ND VERTICAL RIGHT SIDE WIDTH OF PORT 5 – 0XE7D

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_R2_W_P5 Pixel number for masking in 2nd vertical right side
7:4	RW	0	ROSD_VMSK_R1_W_P5 Pixel number for masking in 1st vertical right side

ROSD VERTICAL MASK ON/OFF CONTROL OF PORT 5 – 0XE7E

Bit	R/W	Default	Description
7:0	RW	0	ROSD_VMSK_ON_P5 ROSD vertical masking on/off control for port 5 (0: off, 1: on) Bit 0 : 1st left Bit 1 : 2nd left Bit 2 : 1st center Bit 3 : 2nd center Bit 4 : 3rd center Bit 5 : 4th center Bit 6 : 1st right Bit 7 : 2nd right

ROSD MASK 1ST TOP SIDE WIDTH OF PORT 6 – 0XE80

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_TOP1_W_P6 Line number for masking in the top and left side

ROSD MASK 2ND TOP SIDE WIDTH OF PORT 6 – 0XE81

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_TOP2_W_P6 Line number for masking in the top and right side

ROSD MASK 1ST CENTER SIDE WIDTH OF PORT 6 – 0XE82

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID1_W_P6 Line number for masking in the 1st center and left side

ROSD MASK 2ND CENTER SIDE WIDTH OF PORT 6 – 0XE83

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID2_W_P6 Line number for masking in the 1st center and right side

ROSD MASK 3RD CENTER SIDE WIDTH OF PORT 6 – 0XE84

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID3_W_P6 Line number for masking in the 2nd center and left side

ROSD MASK 4TH CENTER SIDE WIDTH OF PORT 6 – 0XE85

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID4_W_P6 Line number for masking in the 2nd center and right side

ROSD MASK 1ST BOTTOM SIDE WIDTH OF PORT 6 – 0XE86

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_BOT1_W_P6 Line number for masking in the bottom and left side

ROSD MASK 2ND BOTTOM SIDE WIDTH OF PORT 6 – 0XE87

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_BOT2_W_P6 Line number for masking in the top and right side

ROSD MASK POSITION CONTROL OF PORT 6 – 0XE88

Bit	R/W	Default	Description
7:6	R	0	Reserved
5:4	RW	1	ROSD_MSK_VPOS_P6 Vertical position of masking area for port 6 00: 1st area among 4 vertical divisions 01: 2nd area among 4 vertical divisions 10: 3rd area among 4 vertical divisions 11: 4th area among 4 vertical divisions
3:2	R	0	Reserved
1:0	RW	1	ROSD_MSK_HPOS_P6 Horizontal position of masking area for port 6 00: 1st area among 4 horizontal divisions 01: 2nd area among 4 horizontal divisions 10: 3rd area among 4 horizontal divisions 11: 4th area among 4 horizontal divisions

ROSD MASK ON/OFF CONTROL OF PORT 6 – 0XE89

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_ON_P6 ROSD masking on/off control for port 6 (0: off, 1: on) Bit 0 : 1st top Bit 1 : 2nd top Bit 2 : 1st center Bit 3 : 2nd center Bit 4 : 3rd center Bit 5 : 4th center Bit 6 : 1st bottom Bit 7 : 2nd bottom

ROSD MASK 1ST /2ND VERTICAL LEFT SIDE WIDTH OF PORT 6 – 0XE8A

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_L2_W_P6 Pixel number for masking in 2nd vertical left side
7:4	RW	0	ROSD_VMSK_L1_W_P6 Pixel number for masking in 1st vertical left side

ROSD MASK 1ST / 2ND VERTICAL CENTER SIDE WIDTH OF PORT 6 – 0XE8B

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_M2_W_P6 Pixel number for masking in 2nd vertical center side
7:4	RW	0	ROSD_VMSK_M1_W_P6 Pixel number for masking in 1st vertical center side

ROSD MASK 3RD / 4TH VERTICAL CENTER SIDE WIDTH OF PORT 6 – 0XE8C

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_M4_W_P6 Pixel number for masking in 4th vertical center side
7:4	RW	0	ROSD_VMSK_M3_W_P6 Pixel number for masking in 3rd vertical center side

ROSD MASK 1ST / 2ND VERTICAL RIGHT SIDE WIDTH OF PORT 6 – 0XE8D

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_R2_W_P6 Pixel number for masking in 2nd vertical right side
7:4	RW	0	ROSD_VMSK_R1_W_P6 Pixel number for masking in 1st vertical right side

ROSD VERTICAL MASK ON/OFF CONTROL OF PORT 6 – 0XE8E

Bit	R/W	Default	Description
7:0	RW	0	ROSD_VMSK_ON_P6 ROSD vertical masking on/off control for port 6 (0: off, 1: on) Bit 0 : 1st left Bit 1 : 2nd left Bit 2 : 1st center Bit 3 : 2nd center Bit 4 : 3rd center Bit 5 : 4th center Bit 6 : 1st right Bit 7 : 2nd right

ROSD MASK 1ST TOP SIDE WIDTH OF PORT 7 – 0XE90

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_TOP1_W_P7 Line number for masking in the top and left side

ROSD MASK 2ND TOP SIDE WIDTH OF PORT 7 – 0XE91

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_TOP2_W_P7 Line number for masking in the top and right side

ROSD MASK 1ST CENTER SIDE WIDTH OF PORT 7 – 0XE92

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID1_W_P7 Line number for masking in the 1st center and left side

ROSD MASK 2ND CENTER SIDE WIDTH OF PORT 7 – 0XE93

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID2_W_P7 Line number for masking in the 1st center and right side

ROSD MASK 3RD CENTER SIDE WIDTH OF PORT 7 – 0XE94

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID3_W_P7 Line number for masking in the 2nd center and left side

ROSD MASK 4TH CENTER SIDE WIDTH OF PORT 7 – 0XE95

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID4_W_P7 Line number for masking in the 2nd center and right side

ROSD MASK 1ST BOTTOM SIDE WIDTH OF PORT 7 – 0XE96

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_BOT1_W_P7 Line number for masking in the bottom and left side

ROSD MASK 2ND BOTTOM SIDE WIDTH OF PORT 7 – 0XE97

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_BOT2_W_P7 Line number for masking in the top and right side

ROSD MASK POSITION CONTROL OF PORT 7 – 0XE98

Bit	R/W	Default	Description
7:6	R	0	Reserved
5:4	RW	1	ROSD_MSK_VPOS_P7 Vertical position of masking area for port 7 00: 1st area among 4 vertical divisions 01: 2nd area among 4 vertical divisions 10: 3rd area among 4 vertical divisions 11: 4th area among 4 vertical divisions
3:2	R	0	Reserved
1:0	RW	1	ROSD_MSK_HPOS_P7 Horizontal position of masking area for port 7 00: 1st area among 4 horizontal divisions 01: 2nd area among 4 horizontal divisions 10: 3rd area among 4 horizontal divisions 11: 4th area among 4 horizontal divisions

ROSD MASK ON/OFF CONTROL OF PORT 7 – 0XE99

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_ON_P7 ROSD masking on/off control for port 7 (0: off, 1: on) Bit 0 : 1st top Bit 1 : 2nd top Bit 2 : 1st center Bit 3 : 2nd center Bit 4 : 3rd center Bit 5 : 4th center Bit 6 : 1st bottom Bit 7 : 2nd bottom

ROSD MASK 1ST /2ND VERTICAL LEFT SIDE WIDTH OF PORT 7 – 0XE9A

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_L2_W_P7 Pixel number for masking in 2nd vertical left side
3:0	RW	0	ROSD_VMSK_L1_W_P7 Pixel number for masking in 1st vertical left side

ROSD MASK 1ST / 2ND VERTICAL CENTER SIDE WIDTH OF PORT 7 – 0XE9B

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_M2_W_P7 Pixel number for masking in 2nd vertical center side
3:0	RW	0	ROSD_VMSK_M1_W_P7 Pixel number for masking in 1st vertical center side

ROSD MASK 3RD / 4TH VERTICAL CENTER SIDE WIDTH OF PORT 7 – 0XE9C

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_M4_W_P7 Pixel number for masking in 4th vertical center side
3:0	RW	0	ROSD_VMSK_M3_W_P7 Pixel number for masking in 3rd vertical center side

ROSD MASK 1ST / 2ND VERTICAL RIGHT SIDE WIDTH OF PORT 7 – 0XE9D

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_R2_W_P7 Pixel number for masking in 2nd vertical right side
3:0	RW	0	ROSD_VMSK_R1_W_P7 Pixel number for masking in 1st vertical right side

ROSD VERTICAL MASK ON/OFF CONTROL OF PORT 7 – 0XE9E

Bit	R/W	Default	Description
7:0	RW	0	ROSD_VMSK_ON_P7 ROSD vertical masking on/off control for port 7 (0: off, 1: on) Bit 0 : 1st left Bit 1 : 2nd left Bit 2 : 1st center Bit 3 : 2nd center Bit 4 : 3rd center Bit 5 : 4th center Bit 6 : 1st right Bit 7 : 2nd right

ROSD MASK 1ST TOP SIDE WIDTH OF PORT 8 – 0XEA0

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_TOP1_W_P8 Line number for masking in the top and left side

ROSD MASK 2ND TOP SIDE WIDTH OF PORT 8 – 0XEA1

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_TOP2_W_P8 Line number for masking in the top and right side

ROSD MASK 1ST CENTER SIDE WIDTH OF PORT 8 – 0XEA2

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID1_W_P8 Line number for masking in the 1st center and left side

ROSD MASK 2ND CENTER SIDE WIDTH OF PORT 8 – 0XEA3

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID2_W_P8 Line number for masking in the 1st center and right side

ROSD MASK 3RD CENTER SIDE WIDTH OF PORT 8 – 0XEA4

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID3_W_P8 Line number for masking in the 2nd center and left side

ROSD MASK 4TH CENTER SIDE WIDTH OF PORT 8 – 0XEA5

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID4_W_P8 Line number for masking in the 2nd center and right side

ROSD MASK 1ST BOTTOM SIDE WIDTH OF PORT 8 – 0XEA6

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_BOT1_W_P8 Line number for masking in the bottom and left side

ROSD MASK 2ND BOTTOM SIDE WIDTH OF PORT 8 – 0XEA7

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_BOT2_W_P8 Line number for masking in the top and right side

ROSD MASK POSITION CONTROL OF PORT 8 – 0XEA8

Bit	R/W	Default	Description
7:6	R	0	Reserved
5:4	RW	1	ROSD_MSK_VPOS_P8 Vertical position of masking area for port 8 00: 1st area among 4 vertical divisions 01: 2nd area among 4 vertical divisions 10: 3rd area among 4 vertical divisions 11: 4th area among 4 vertical divisions
3:2	R	0	Reserved
1:0	RW	1	ROSD_MSK_HPOS_P8 Horizontal position of masking area for port 8 00: 1st area among 4 horizontal divisions 01: 2nd area among 4 horizontal divisions 10: 3rd area among 4 horizontal divisions 11: 4th area among 4 horizontal divisions

ROSD MASK ON/OFF CONTROL OF PORT 8 – 0XEA9

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_ON_P8 (0: off, 1: on) ROSD masking on/off control for port 8 Bit 0 : 1st top Bit 1 : 2nd top Bit 2 : 1st center Bit 3 : 2nd center Bit 4 : 3rd center Bit 5 : 4th center Bit 6 : 1st bottom Bit 7 : 2nd bottom

ROSD MASK 1ST /2ND VERTICAL LEFT SIDE WIDTH OF PORT 8 – 0XEAA

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_L2_W_P8 Pixel number for masking in 2nd vertical left side
3:0	RW	0	ROSD_VMSK_L1_W_P8 Pixel number for masking in 1st vertical left side

ROSD MASK 1ST / 2ND VERTICAL CENTER SIDE WIDTH OF PORT 8 – 0XEAB

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_M2_W_P8 Pixel number for masking in 2nd vertical center side
3:0	RW	0	ROSD_VMSK_M1_W_P8 Pixel number for masking in 1st vertical center side

ROSD MASK 3RD / 4TH VERTICAL CENTER SIDE WIDTH OF PORT 8 – 0XEAC

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_M4_W_P8 Pixel number for masking in 4th vertical center side
3:0	RW	0	ROSD_VMSK_M3_W_P8 Pixel number for masking in 3rd vertical center side

ROSD MASK 1ST / 2ND VERTICAL RIGHT SIDE WIDTH OF PORT 8 – 0XEAD

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_R2_W_P8 Pixel number for masking in 2nd vertical right side
3:0	RW	0	ROSD_VMSK_R1_W_P8 Pixel number for masking in 1st vertical right side

ROSD VERTICAL MASK ON/OFF CONTROL OF PORT 8 – 0XEAE

Bit	R/W	Default	Description
7:0	RW	0	ROSD_VMSK_ON_P8 ROSD vertical masking on/off control for port 8 (0: off, 1: on) Bit 0 : 1st left Bit 1 : 2nd left Bit 2 : 1st center Bit 3 : 2nd center Bit 4 : 3rd center Bit 5 : 4th center Bit 6 : 1st right Bit 7 : 2nd right

ROSD MASK 1ST TOP SIDE WIDTH OF PORT 9 – 0XEB0

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_TOP1_W_P9 Line number for masking in the top and left side

ROSD MASK 2ND TOP SIDE WIDTH OF PORT 9 – 0XEB1

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_TOP2_W_P9 Line number for masking in the top and right side

ROSD MASK 1ST CENTER SIDE WIDTH OF PORT 9 – 0XEB2

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID1_W_P9 Line number for masking in the 1st center and left side

ROSD MASK 2ND CENTER SIDE WIDTH OF PORT 9 – 0XEB3

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID2_W_P9 Line number for masking in the 1st center and right side

ROSD MASK 3RD CENTER SIDE WIDTH OF PORT 9 – 0XEB4

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID3_W_P9 Line number for masking in the 2nd center and left side

ROSD MASK 4TH CENTER SIDE WIDTH OF PORT 9 – 0XEB5

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_MID4_W_P9 Line number for masking in the 2nd center and right side

ROSD MASK 1ST BOTTOM SIDE WIDTH OF PORT 9 – 0XEB6

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_BOT1_W_P9 Line number for masking in the bottom and left side

ROSD MASK 2ND BOTTOM SIDE WIDTH OF PORT 9 – 0XEB7

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_BOT2_W_P9 Line number for masking in the top and right side

ROSD MASK POSITION CONTROL OF PORT 9 – 0XEB8

Bit	R/W	Default	Description
7:6	R	0	Reserved
5:4	RW	1	ROSD_MSK_VPOS_P9 Vertical position of masking area for port 9 00: 1st area among 4 vertical divisions 01: 2nd area among 4 vertical divisions 10: 3rd area among 4 vertical divisions 11: 4th area among 4 vertical divisions
3:2	R	0	Reserved
1:0	RW	1	ROSD_MSK_HPOS_P9 Horizontal position of masking area for port 9 00: 1st area among 4 horizontal divisions 01: 2nd area among 4 horizontal divisions 10: 3rd area among 4 horizontal divisions 11: 4th area among 4 horizontal divisions

ROSD MASK ON/OFF CONTROL OF PORT 9 – 0XEB9

Bit	R/W	Default	Description
7:0	RW	0	ROSD_MSK_ON_P9 (0: off, 1: on) ROSD masking on/off control for port 9 Bit 0 : 1st top Bit 1 : 2nd top Bit 2 : 1st center Bit 3 : 2nd center Bit 4 : 3rd center Bit 5 : 4th center Bit 6 : 1st bottom Bit 7 : 2nd bottom

ROSD MASK 1ST /2ND VERTICAL LEFT SIDE WIDTH OF PORT 9 – 0XEBA

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_L2_W_P9 Pixel number for masking in 2nd vertical left side
3:0	RW	0	ROSD_VMSK_L1_W_P9 Pixel number for masking in 1st vertical left side

ROSD MASK 1ST / 2ND VERTICAL CENTER SIDE WIDTH OF PORT 9 – 0XEBB

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_M2_W_P9 Pixel number for masking in 2nd vertical center side
3:0	RW	0	ROSD_VMSK_M1_W_P9 Pixel number for masking in 1st vertical center side

ROSD MASK 3RD / 4TH VERTICAL CENTER SIDE WIDTH OF PORT 9 – 0XEBC

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_M4_W_P9 Pixel number for masking in 4th vertical center side
3:0	RW	0	ROSD_VMSK_M3_W_P9 Pixel number for masking in 3rd vertical center side

ROSD MASK 1ST / 2ND VERTICAL RIGHT SIDE WIDTH OF PORT 9 – 0XEBD

Bit	R/W	Default	Description
7:4	RW	0	ROSD_VMSK_R2_W_P9 Pixel number for masking in 2nd vertical right side
3:0	RW	0	ROSD_VMSK_R1_W_P9 Pixel number for masking in 1st vertical right side

ROSD VERTICAL MASK ON/OFF CONTROL OF PORT 9 – 0XEBE

Bit	R/W	Default	Description
7:0	RW	0	ROSD_VMSK_ON_P9 ROSD vertical masking on/off control for port 5 (0: off, 1: on) Bit 0 : 1st left Bit 1 : 2nd left Bit 2 : 1st center Bit 3 : 2nd center Bit 4 : 3rd center Bit 5 : 4th center Bit 6 : 1st right Bit 7 : 2nd right

ROSD MASK Y COLOR REGISTER – 0XEC0

Bit	R/W	Default	Description
7:0	RW	0x10	ROSD_MSK_Y[7:0] Masking color Y

ROSD MASK CB COLOR REGISTER – 0XEC1

Bit	R/W	Default	Description
7:0	RW	0x80	ROSD_ MSK_CB[7:0] Masking color Cb

ROSD MASK CR COLOR REGISTER – 0XEC2

Bit	R/W	Default	Description
7:0	RW	0x80	ROSD_ MSK_CR[7:0] Masking color Cr

ROSD VERTICAL ON/OFF CONTROL REGISTER 1 FOR PORT 5 – 0XED0

Bit	R/W	Default	Description
7:0	RW	0x00	OSD_ V_OFF_P5[7:0] First 8 internal vertical line on/off control(0: On, 1: Off)

ROSD VERTICAL/HORIZONTAL ON/OFF CONTROL REGISTER 2 FOR PORT 5 – 0XED1

Bit	R/W	Default	Description
7:4	RW	0x80	OSD_ H_OFF_P5[11:8] Last 4 internal horizontal line on/off control(0: On, 1: Off)
3:0	RW	0x80	OSD_ V_OFF_P5[11:8] Last 4 internal vertical line on/off control(0: On, 1: Off)

ROSD HORIZONTAL ON/OFF CONTROL REGISTER 1 FOR PORT 5 – 0XED2

Bit	R/W	Default	Description
7:0	RW	0x00	OSD_ H_OFF_P5[7:0] First 8 internal Horizontal line on/off control(0: On, 1: Off)

ROSD VERTICAL ON/OFF CONTROL REGISTER 1 FOR PORT 6 – 0XED3

Bit	R/W	Default	Description
7:0	RW	0x00	OSD_ V_OFF_P6[7:0] First 8 internal vertical line on/off control(0: On, 1: Off)

ROSD VERTICAL/HORIZONTAL ON/OFF CONTROL REGISTER 2 FOR PORT 6 – 0XED4

Bit	R/W	Default	Description
7:4	RW	0x80	OSD_ H_OFF_P6[11:8] Last 4 internal horizontal line on/off control(0: On, 1: Off)
3:0	RW	0x80	OSD_ V_OFF_P6[11:8] Last 4 internal vertical line on/off control(0: On, 1: Off)

ROSD HORIZONTAL ON/OFF CONTROL REGISTER 1 FOR PORT 6 – 0XED5

Bit	R/W	Default	Description
7:0	RW	0x00	OSD_ H_OFF_P6[7:0] First 8 internal Horizontal line on/off control(0: On, 1: Off)

ROSD VERTICAL ON/OFF CONTROL REGISTER 1 FOR PORT 7 – 0XED6

Bit	R/W	Default	Description
7:0	RW	0x00	OSD_ V_OFF_P7[7:0] First 8 internal vertical line on/off control(0: On, 1: Off)

ROSD VERTICAL/HORIZONTAL ON/OFF CONTROL REGISTER 2 FOR PORT 7 – 0XED7

Bit	R/W	Default	Description
7:4	RW	0x80	OSD_ H_OFF_P7[11:8] Last 4 internal horizontal line on/off control(0: On, 1: Off)
3:0	RW	0x80	OSD_ V_OFF_P7[11:8] Last 4 internal vertical line on/off control(0: On, 1: Off)

ROSD HORIZONTAL ON/OFF CONTROL REGISTER 1 FOR PORT 7 – 0XED8

Bit	R/W	Default	Description
7:0	RW	0x00	OSD_ H_OFF_P7[7:0] First 8 internal Horizontal line on/off control(0: On, 1: Off)

ROSD VERTICAL ON/OFF CONTROL REGISTER 1 FOR PORT 8 – 0XED9

Bit	R/W	Default	Description
7:0	RW	0x00	OSD_ V_OFF_P8[7:0] First 8 internal vertical line on/off control(0: On, 1: Off)

ROSD VERTICAL/HORIZONTAL ON/OFF CONTROL REGISTER 2 FOR PORT 8 – 0XEDA

Bit	R/W	Default	Description
7:4	RW	0x80	OSD_ H_OFF_P8[11:8] Last 4 internal horizontal line on/off control(0: On, 1: Off)
3:0	RW	0x80	OSD_ V_OFF_P8[11:8] Last 4 internal vertical line on/off control(0: On, 1: Off)

ROSD HORIZONTAL ON/OFF CONTROL REGISTER 1 FOR PORT 8 – 0XEDB

Bit	R/W	Default	Description
7:0	RW	0x00	OSD_ H_OFF_P8[7:0] First 8 internal Horizontal line on/off control(0: On, 1: Off)

ROSD VERTICAL ON/OFF CONTROL REGISTER 1 FOR PORT 9 – 0XEDC

Bit	R/W	Default	Description
7:0	RW	0x00	OSD_ V_OFF_P9[7:0] First 8 internal vertical line on/off control(0: On, 1: Off)

ROSD VERTICAL/HORIZONTAL ON/OFF CONTROL REGISTER 2 FOR PORT 9 – 0XEDD

Bit	R/W	Default	Description
7:4	RW	0x80	OSD_ H_OFF_P9[11:8] Last 4 internal horizontal line on/off control(0: On, 1: Off)
3:0	RW	0x80	OSD_ V_OFF_P9[11:8] Last 4 internal vertical line on/off control(0: On, 1: Off)

ROSD HORIZONTAL ON/OFF CONTROL REGISTER 1 FOR PORT 9 – 0XEDE

Bit	R/W	Default	Description
7:0	RW	0x00	OSD_ H_OFF_P9[7:0] First 8 internal Horizontal line on/off control(0: On, 1: Off)

ROSD FONT RAM ADDRESS LOW BYTE REGISTER – 0XEE0

Bit	R/W	Default	Description
7:0	RW	0	ROSD_FRAM_ADDR[7:0] Font SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1408x44.

ROSD FONT RAM ADDRESS HIGH BYTE REGISTER – 0XEE1

Bit	R/W	Default	Description
2:0	RW	0	ROSD_FRAM_ADDR[10:8] Font SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1408x44.

ROSD FONT RAM DATA 1ST BYTE REGISTER – 0XEE2

Bit	R/W	Default	Description
7:0	RW	0	ROSD_FRAM_DATA[7:0] Font SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1408x44.

ROSD FONT RAM DATA 2ND BYTE REGISTER – 0XEE3

Bit	R/W	Default	Description
7:0	RW	0	ROSD_FRAM_DATA[15:8] Font SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1408x44.

ROSD FONT RAM DATA 3RD BYTE REGISTER – 0XEE4

Bit	R/W	Default	Description
7:0	RW	0	ROSD_FRAM_DATA[23:16] Font SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1408x44.

ROSD FONT RAM DATA 4TH BYTE REGISTER – 0XEE5

Bit	R/W	Default	Description
7:0	RW	0	ROSD_FRAM_DATA[31:24] Font SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1408x44.

ROSD FONT RAM DATA 5TH BYTE REGISTER – 0XEE6

Bit	R/W	Default	Description
7:0	RW	0	ROSD_FRAM_DATA[39:32] Font SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1408x44.

ROSD FONT RAM DATA 6TH BYTE REGISTER – 0XEE7

Bit	R/W	Default	Description
7:4	RW	0	Reserved
3:0	RW	0	ROSD_FRAM_DATA[43:40] Font SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 1408x44.

ROSD DISPLAY RAM ADDRESS REGISTER – 0XEE8

Bit	R/W	Default	Description
7:0	RW	0	ROSD_DRAM_ADDR[7:0] Display SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 704x6

ROSD DISPLAY RAM ADDRESS REGISTER – 0XEE9

Bit	R/W	Default	Description
7:2	RW	0	Reserved
1:0	RW	0	ROSD_DRAM_ADDR[9:8] Display SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 704x6

ROSD DISPLAY RAM DATA REGISTER – 0XEEA

Bit	R/W	Default	Description
7:0	RW	0	ROSD_DRAM_DATA[5:0] Display SRAM address. When host write data to this SRAM, address is written first and then data. SRAM size is 704x6

Host Interface

Introduction

TW2828 provides two kind of interfaces to meet different needs of the customers. There are serial host interface and parallel host interface. The selection is done by setting HSPB pin high or low. When HSPB is low, the parallel interface is selected. When HSPB pin is set to high, the serial interface is selected. Some of the interface pins served as dual purpose pins depending on the working mode. The pin HCSB and the HDAT[7] in the parallel mode become SCLK and SDAT pins in serial mode and the four hard coded slave addresses are selected by two primary pins. Each interface protocol is shown in the following figures.

Pin Assignments for Serial and Parallel Interface

PIN NAME	SERIAL MODE	PARALLEL MODE	DESCRIPTION
HSPB	HIGH	LOW	Host Interface select
HCSB	SCLK	PCSB	Chip Select
HWRB	Not Used (4.7Kohm Pull up)	PWRB	Write pulse
HRDB	Not Used (4.7Kohm Pull up)	PRDB	Read pulse
HADDR [11:0]	Not Used (Tied ground)	Parallel Address[11:0]	Address
HDAT [6:0]	Not Used (Tied ground)	Parallel Data[6:0]	Data
HDAT [7]	SDAT	Parallel Data[7]	Data

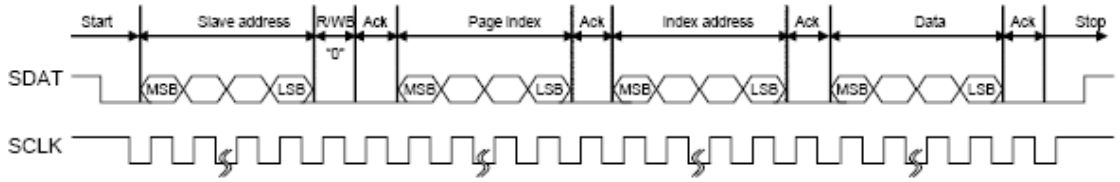
Serial Interface

SLAVE ADDRESS							R/W
1	0	1	1	0	P_I2C_SID2	P_I2C_SID1	1 = Read 0 = Write

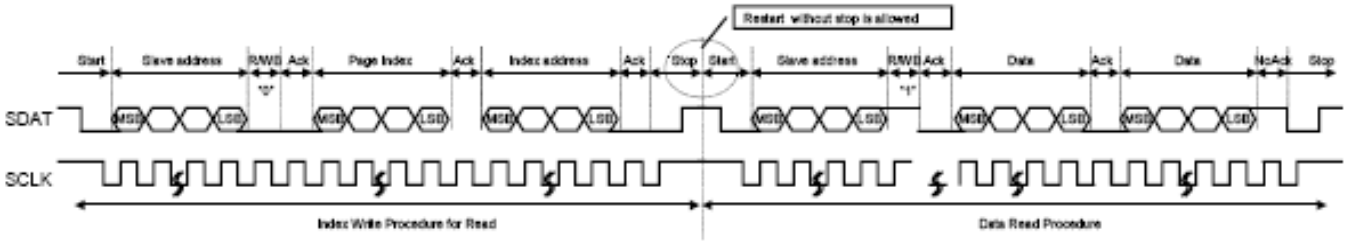
In the Serial Mode, there are two address pins (P_I2C_SID2, P_I2C_SID1) can be assigned to select 4 I²C slave addresses (0x58, 0x59, 0x5a, 0x5b) for full flexibility. The figure below shows an illustration of the serial interface for the case of the slave address set for Read as "0xB1" and Write as "0xB0".

TW2828 has total of 16 pages for registers with each page contains 256 eight bit registers. So that the page index[3:0] is used to select page of registers, Indexed address is used to select the registers in each page. For each page assignment, please refer to the correspondent module. Following is the detail timing diagram.

TW2828 also supports automatic index increment so that it can read or write continuous multi-bytes without restart. Therefore, The host can read or write multiple bytes in sequential order without writing additional slave address, page index and index address. With the automatic index increment function, the data transfer performance is highly improved and transfer rate on the bus is up to 400 kbits per second.



WRITE TIMING OF THE SERIAL INTERFACE



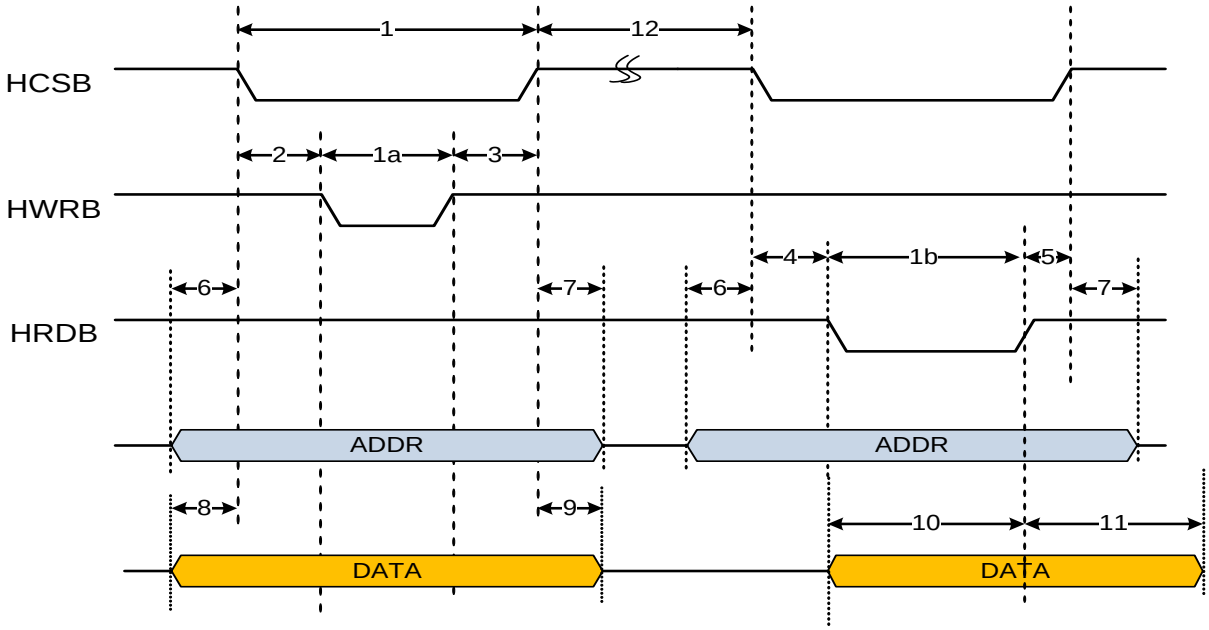
Parallel Interface

The parallel interface consists of 8 bi-directional data pins (HDAT[7:0]), read /write signal (HWRB, HRDB), and chip select signal (HCSB). When parallel interface is the intended interface, the HSPB pin must set to low. All bus transaction cycles are initiated by pulling HCSB is low. For a write cycle, HWRB is pulled low the whole cycle and the HRDB should maintain high, then TW2828 is to set in write mode and is ready to receive data from coming from the HDAT[7:0]. The data latching is done in the beginning of the HWRB pulse. If the HWRB is set to HIGH and HRDB is set to low, the TW2828 is set in read mode and ready to send data through HDAT[7:0] to the host. If reading TW2828's registers, the read data will become valid after a fixed access time when the HRDB pulse go high. If reading TW2828's DDR2 SDRAM content, the access time will depend on the activities on the DRAM and is not a constant.

Address space arrangement in parallel interface mode looks like this: twelve bit address with the upper four bits served as page selector and the lower eight bits served as indexed address. Altoghter there are 16 pages and each with 256 (0x00-0xFF) selections. For all registers definition, please refer to the related module to in the TW2828 specification.

SINGLE TRANSFER

The single transfer throughput of the parallel host port is about 10MB/sec (sustained). This is calculated from the waveform below. One transaction is one HCSB pulse and the waiting time is 70+30 = 100 nS. So 8 bit input is 10 MB/sec.



TIMING PARAMETERS OF THE PARALLEL INTERFACE

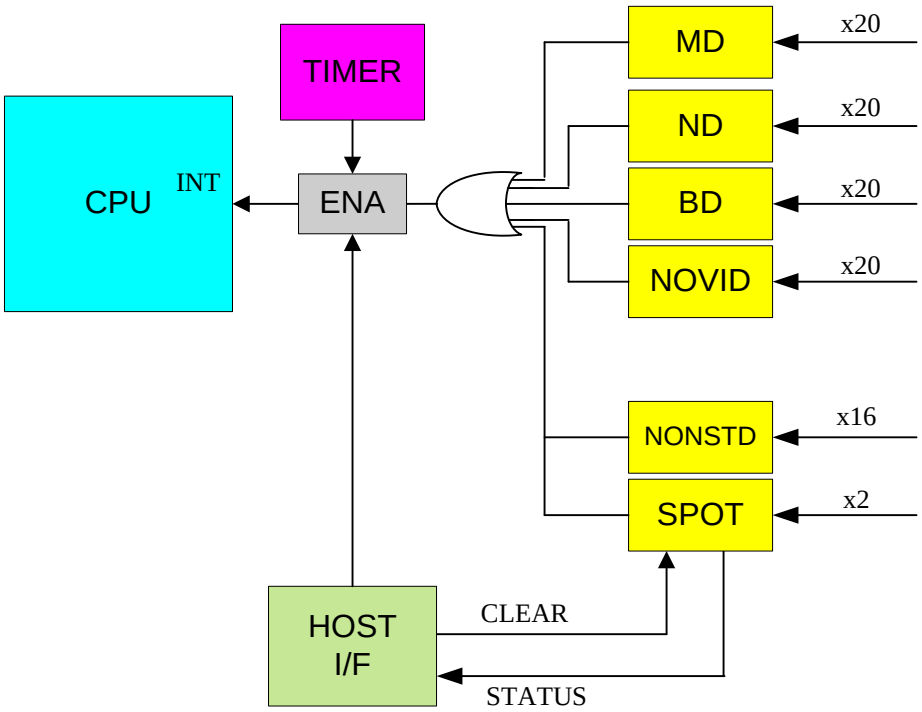
	PARAMETER	SYMBOL	MIN	MAX	UNITS
1, 1a, 1b	HCSB, HWRB, HRDB pulse width Address Data latching time	Tcs	30	N/A	ns
2	HCSB low to HWRB low	Hwrb_tsu	0	N/A	ns
3	HWRB high to HCSB high	Hwrb_th	0	N/A	ns
4	HCSB low to HRDB low	Hrdb_tsu	0	N/A	ns
5	HRDB high to HCSB high	Hrdb_th	0	N/A	ns
6	HADDR setup to HCSB low	Haddr_tsu	2	N/A	ns
7	HADDR hold after HCSB high	Haddr_th	0	N/A	ns
8	HDAT write setup to HCSB low	Hdat_wr_tsu	5	N/A	ns
9	HDAT write hold after HCSB high	Hdat_wr_th	0	N/A	ns
10	HDAT read delay to HRDB inactive	Hdat_trds	10	30	ns
11	HDAT read hold after HRDB inactive	Hdat_trdh	0	60	ns
12	HCSB inactive pulse width	Tcsn	70	-	ns
13	CPU Halt to TW2828 access	TcpuH	30	-	ns
14	Write pulse low to wait signal low	Twait	30	35	ns

External Host to Display Memory access Interface

TW2828 allows the external host get access to the display memory. This feature is provided mainly for debugging purpose because in normal operations user does not need to read or write the content of the DRAM. To use this feature user only need to program the 24 bit linear starting address into the three registers (0x000, 0x001, 0x002), then program the DRAM access control register 0x003 to specify the read or the write operation and the burst length. Once these registers are programmed, for write operations users need to write to port register 0x004 continuesly util the number of bytes written equal to the burst length. For read operation user needs to read the port register continuously to get all the data requested.

Interrupt Interface

The TW2828 provides a very sophisticated interrupt request function for user to inter-react with the host CPU. Any video loss, motion, blind, or night detection in every channel will generate an interrupt request to the host CPU. The polarity of the interrupt is selectable by the user. The user can disable the one single interrupt function for each channel and category. After receiving the interrupt, the host can distinguish which functional unit generated the interrupt by writing to the interrupt status registers. User can choose to read the real time detection status of the all functional units by chaning a bit. The interrupt can be cleared by reading the interrupt clearing registers.



A set of idle and resend counters is incorporated in the interrupt generation process to help easing the burden of the CPU is responding and switching between different interrupt service routines. Once an interrupt is raised and does not get attention of CPU for certain period of time, the interrupt of TW2828 will become inactive for a while and become active again. This is process will go on indefinely until the unit get reset. This function can be disabled by user.

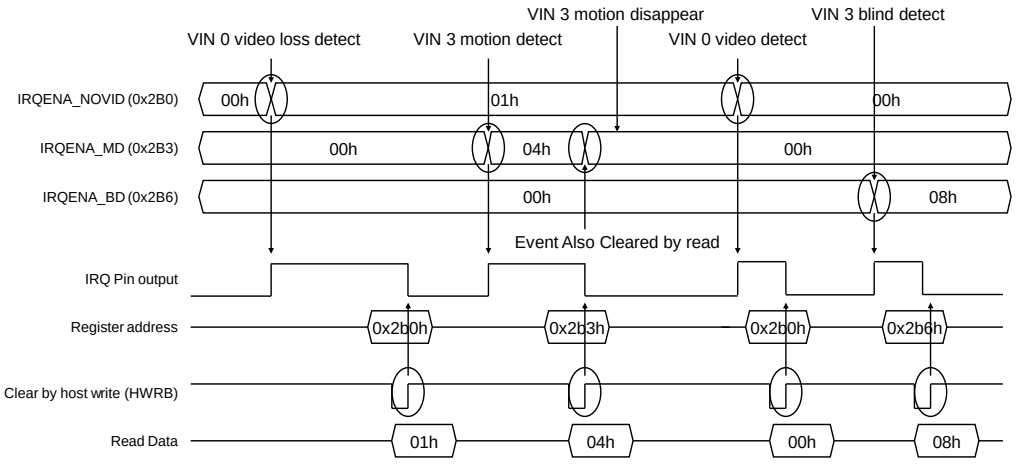


ILLUSTRATION OF THE INTERRUPT GENERATED AND CLEARED SEQUENCE

Register Table

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x2B0	R/W	0x00	No video IRQ Enable Register 1
0x2B1	R/W	0x00	No video IRQ Enable Register 2
0x2B2	R/W	0x00	No video IRQ Enable Register 3
0x2B3	R/W	0x00	Motion Detection IRQ Enable Register 1
0x2B4	R/W	0x00	Motion Detection IRQ Enable Register 2
0x2B5	R/W	0x00	Motion Detection IRQ Enable Register 3
0x2B6	R/W	0x00	Blind Detection IRQ Enable Register 1
0x2B7	R/W	0x00	Blind Detection IRQ Enable Register 2
0x2B8	R/W	0x00	Blind Detection IRQ Enable Register 3
0x2B9	R/W	0x00	Night Detection IRQ Enable Register 1
0x2BA	R/W	0x00	Night Detection IRQ Enable Register 2
0x2BB	R/W	0x00	Night Detection IRQ Enable Register 3
0x2BC	R/W	0x00	No video IRQ Status Register 1
0x2BD	R/W	0x00	No video IRQ Status Register 2
0x2BE	R/W	0x00	No video IRQ Status Register 3
0x2BF	R/W	0x00	Motion Detection IRQ Status Register 1
0x2C0	R/W	0x00	Motion Detection IRQ Status Register 2
0x2C1	R/W	0x00	Motion Detection IRQ Status Register 3
0x2C2	R/W	0x00	Blind Detection IRQ Status Register 1
0x2C3	R/W	0x00	Blind Detection IRQ Status Register 2
0x2C4	R/W	0x00	Blind Detection IRQ Status Register 3
0x2C5	R/W	0x00	Night Detection IRQ Status Register 1
0x2C6	R/W	0x00	Night Detection IRQ Status Register 2
0x2C7	R/W	0x00	Night Detection IRQ Status Register 3
0x2C8	R/W	0x00	IRQ Main Control Register
0x2C9	R/W	0x00	IRQ Spacing Register
0x2CA	R/W	0x00	IRQ Report Counter Register 1
0x2CB	R/W	0x00	IRQ Report Counter Register 2
0x2CC	R/W	0x00	IRQ Report Counter Register 3
0x2D0	R/W	0x00	Field Freeze Enable Register 5

Register Descriptions

NO VIDEO IRQ ENABLE REGISTER 1 – 0X2B0

Bit	R/W	Default	Description
7:0	R/W	0x00	IRQENA_NOVID[7:0] for channel 0 to 7 1: enable 0: disable

NO VIDEO IRQ ENABLE REGISTER 2 – 0X2B1

Bit	R/W	Default	Description
7:0	R/W	0x00	IRQENA_NOVID[15:8] for channel 8 to 15 1: enable 0: disable

NO VIDEO IRQ ENABLE REGISTER 3 – 0X2B2

Bit	R/W	Default	Description
3:0	R/W	0x00	IRQENA_NOVID[19:16] for channel 16 to 19 1: enable 0: disable

MOTION DETECTION IRQ ENABLE REGISTER 1 – 0X2B3

Bit	R/W	Default	Description
7:0	R/W	0x00	IRQENA_MD[7:0] for channel 0 to 7 1: enable 0: disable

MOTION DETECTION IRQ ENABLE REGISTER 2 – 0X2B4

Bit	R/W	Default	Description
7:0	R/W	0x00	IRQENA_MD[15:8] for channel 8 to 15 1: enable 0: disable

MOTION DETECTION IRQ ENABLE REGISTER 3 – 0X2B5

Bit	R/W	Default	Description
3:0	R/W	0x00	IRQENA_MD[19:16] for channel 16 to 19 1: enable 0: disable

BLIND DETECTION IRQ ENABLE REGISTER 1 – 0X2B6

Bit	R/W	Default	Description
7:0	R/W	0x00	IRQENA_BD[7:0] for channel 0 to 7 1: enable 0: disable

BLIND DETECTION IRQ ENABLE REGISTER 2 – 0X2B7

Bit	R/W	Default	Description
7:0	R/W	0x00	IRQENA_BD[15:8] for channel 8 to 15 1: enable 0: disable

BLIND DETECTION IRQ ENABLE REGISTER 3 – 0X2B8

Bit	R/W	Default	Description
3:0	R/W	0	IRQENA_BD[19:16] for channel 16 to 19 1: enable 0: disable

NIGHT DETECTION IRQ ENABLE REGISTER 1 – 0X2B9

Bit	R/W	Default	Description
7:0	R/W	0x00	IRQENA_ND[7:0] for channel 0 to 7 1: enable 0: disable

NIGHT DETECTION IRQ ENABLE REGISTER 2 – 0X2BA

Bit	R/W	Default	Description
7:0	R/W	0x00	IRQENA_ND[15:8] for channel 8 to 15 1: enable 0: disable

NIGHT DETECTION IRQ ENABLE REGISTER 3 – 0X2BB

Bit	R/W	Default	Description
3:0	R/W	0x00	IRQENA_ND[19:16] for channel 16 to 19 1: enable 0: disable

NO VIDEO IRQ STATUS REGISTER 1 – 0X2BC

Bit	R/W	Default	Description
7:0	R	0x00	IRQ_RD_NOVID[7:0] for channel 0 to 7 1: Interrupt 0: idle Status register is cleared by writing "1"

NO VIDEO IRQ STATUS REGISTER 2 – 0X2BD

Bit	R/W	Default	Description
7:0	R	0x00	IRQ_RD_NOVID[15:8] for channel 8 to 15 1: interrupt 0: idle Status register is cleared by writing "1"

NO VIDEO IRQ STATUS REGISTER 3 – 0X2BE

Bit	R/W	Default	Description
3:0	R	0x00	IRQ_RD_NOVID[19:16] for channel 16 to 19 1: interrupt 0: idle Status register is cleared by writing "1"

MOTION DETECTION IRQ STATUS REGISTER 1 – 0X2BF

Bit	R/W	Default	Description
7:0	R	0x00	IRQ_RD_MD[7:0] for channel 0 to 7 1: interrupt 0: idle Status register is cleared by writing "1"

MOTION DETECTION IRQ STATUS REGISTER 2 – 0X2C0

Bit	R/W	Default	Description
7:0	R	0x00	IRQ_RD_MD[15:8] for channel 8 to 15 1: interrupt 0: idle Status register is cleared by writing "1"

MOTION DETECTION IRQ STATUS REGISTER 3 – 0X2C1

Bit	R/W	Default	Description
3:0	R	0x00	IRQ_RD_MD[19:16] for channel 16 to 19 1: interrupt 0: idle Status register is cleared by writing "1"

BLIND DETECTION IRQ STATUS REGISTER 1 – 0X2C2

Bit	R/W	Default	Description
7:0	R	0x00	IRQ_RD_BD[7:0] for channel 0 to 7 1: interrupt 0: idle Status register is cleared by writing "1"

BLIND DETECTION IRQ STATUS REGISTER 2 – 0X2C3

Bit	R/W	Default	Description
7:0	R	0x00	IRQ_RD_BD[15:8] for channel 8 to 15 1: interrupt 0: idle Status register is cleared by writing "1"

BLIND DETECTION IRQ STATUS REGISTER 3 – 0X2C4

Bit	R/W	Default	Description
3:0	R	0x00	IRQ_RD_BD[19:16] for channel 16 to 19 1: interrupt 0: idle Status register is cleared by writing "1"

NIGHT DETECTION IRQ STATUS REGISTER 1 – 0X2C5

Bit	R/W	Default	Description
7:0	R	0x00	IRQ_RD_ND[7:0] for channel 0 to 7 1: interrupt 0: idle Status register is cleared by writing "1"

NIGHT DETECTION IRQ STATUS REGISTER 2 – 0X2C6

Bit	R/W	Default	Description
7:0	R	0x00	IRQ_RD_ND[15:8] for channel 8 to 15 1: interrupt 0: idle Status register is cleared by writing "1"

NIGHT DETECTION IRQ STATUS REGISTER 3 – 0X2C7

Bit	R/W	Default	Description
3:0	R	0x00	IRQ_RD_ND[19:16] for channel 16 to 19 1: interrupt 0: idle Status register is cleared by writing "1"

IRQ MAIN CONTROL REGISTER —OFFSET 0X2C8

Bit	R/W	Default	Description
7	R/W	0	IRQENA_RD_MD 0: normal 1: When read interrupt status line become interrupt enable line
6	R/W	0	Interrupt Polarity Select 0: positive 1: negative
5	R/W	0	Main Interrupt line enable 0: no report 1: report
4	R/W	0	Reserved
3	R/W	0	Control Line Select for Night Detection 0: real detect 1: IRQ register
2	R/W	0	Control Line Select for Blind Detection 0: real detect 1: IRQ register
1	R/W	0	Control Line Select for Motion Detection 0: real detect 1: IRQ register
0	R/W	0	Control Line Select for No video Detection 0: real detect 1: IRQ register

IRQ SPACING REGISTER – 0X2C9

Bit	R/W	Default	Description
7:0	R/W	0x00	IRQ period[7:0]

IRQ REPORT COUNTER REGISTER 1 – 0X2CA

Bit	R/W	Default	Description
7:0	R/W	0x00	IRQ Report Counter[7:0]

IRQ REPORT COUNTER REGISTER 2 – 0X2CB

Bit	R/W	Default	Description
7:0	R/W	0x00	IRQ Report Counter[15:8]

IRQ REPORT COUNTER REGISTER 3 – 0X2CC

Bit	R/W	Default	Description
7:4	R/W	0x0	Reserved
3:0	R/W	0x0	IRQ Report Counter[19:16]

FREEZE CONTROL REGISTER 5 – 0X2D0

Bit	R/W	Default	Description
4:0	R/W	0x00	CH_FIELD_FREEZZE[36:32] for channel 32 to 36 Frame Freeze On/Off 0 : Frame freeze 1 : Field freeze

Register Descriptions

DISPLAY DRAM ADDRESS REGISTER 0 – 0X000

Bit	R/W	Default	Description
7:0	R/W	0	Display Memory Address Low Byte

DISPLAY DRAM ADDRESS REGISTER 1– 0X001

Bit	R/W	Default	Description
7:0	R/W	0	Display Memory Address Middle Byte

DISPLAY DRAM ADDRESS REGISTER 2– 0X002

Bit	R/W	Default	Description
7:0	R/W	0	Display Memory Address High Byte

DISPLAY DRAM ACCESS CONTROL REGISTER — 0X003

Bit	R/W	Default	Description
7:6	R/W	0	**Display DRAM read / write enable** 00 = Reserved 01 = Enable read access 10 = Reserved 11 = Enable write access
5:0	R/W	0	**Burst Width** Numbers of bytes to be written or read from memory

DISPLAY DRAM DATA PORT REGISTER– 0X004

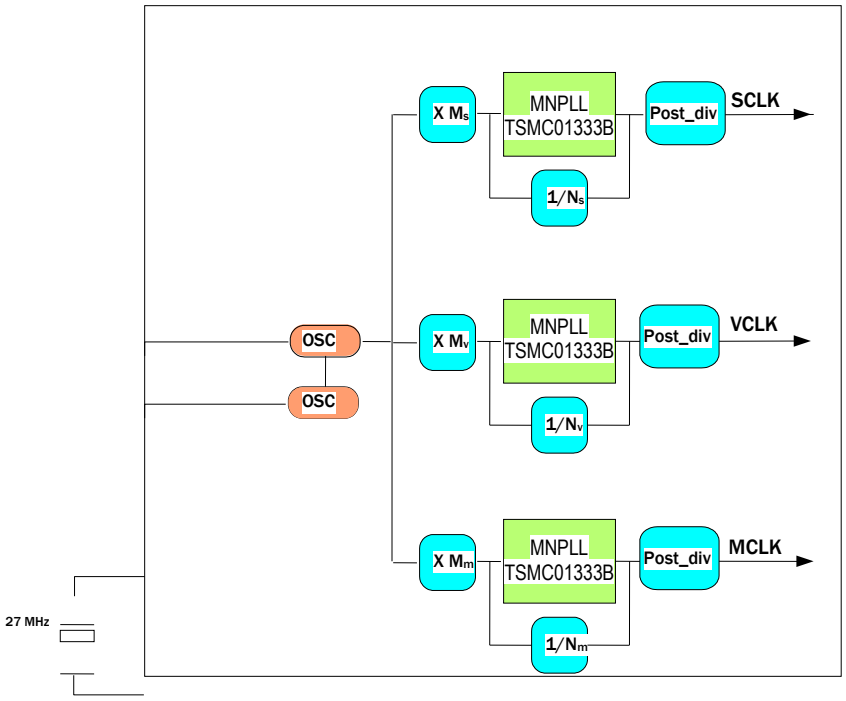
Bit	R/W	Default	Description
7:0	R/W	0	Display Memory Data[7:0]

Clock Synthesizer and Pin MUX

Introduction

TW2828 has an integrated PLL system to generate all the clocks that are needed for the chip operations. As showed from the following block diagram, the 27 MHz crystal is the only external component are needed by all internal PLLs. The crystal and the on-chip oscillator supply the base frequency to the on-chip PLL system. The base frequency is fed into three PLLs: One for generating a fixed system clock at 108 MHz, The second one is the DDR2 MCLK generation and the last one for generating display clock for the display unit. Users can changed the frequencies by applying different values to the following formula below, the clock output frequencies on each clock domain can be derived by provide the proper values of M, N and P.

$$CLK\_OUT = \frac{27\ MHz}{(N+1)} \times \frac{(M+1)}{2^P}$$



BLOCK DIAGRAM OF THE PLL AND CLOCK GENERATION LOGIC

PARAMETER	SYM	CONDITION	MIN TYP	MAX	UNIT
Input Clock Frequency [2]	FIN = 27 MHz		5	400	MHz
Comparison Frequency	FREF = 27 /(NR+1)	High-band	10	50	MHz
		Middle-band	10	50	
		Low-band	5	50	
VCO Operating Range	FVCO = FREF * (MR+1)	High-band	500	1000	MHz
		Middle-band	300	600	
		Low-band	100	300	
Output Clock Frequency	FOUT = FVCO /2^{OD}	High-band	62.5	1000	MHz
		Middle-band	37.5	600	
		Low-band	12.5	300	

Output Clock Examples

In the table below, the M, N, P values are used for illustration purpose.

FROM	FREQUENCY	DUTY CYCLE	JITTER	SKEW (FROM RISING EDGE OF REFERENCE CLOCK)	REMARK
OSC	27 MHz	50%			
SCLK	108 MHz	50%		TBD	M= 7 N= 1 P= 1
VCLK	27 MHz	50%	250ps	TBD	M= 7 N= 7 P= 1
	108 MHz	50%	250ps	TBD	M= 7 N= 1 P= 1
	121.5 MHz	50%	250ps	TBD	M= 8 N= 1 P= 1
	148.5 MHz	50%	250ps	TBD	M= 10 N= 1 P= 1
MCLK	324 MHz	50%	250ps	TBD	M=23 N=1 P=0
	277 MHz	50%	250ps	TBD	M=19 N=1 P=0

Initial Conditions and Changing PLL Values

The 108 MHz clock is used as system clock. It will control all the registers access and most of the down scaling, recording and CPU related blocks. The frequency of this clock will not get changed during the normal operation. The other two PLLs has initial setting and frequencies when power up, their frequencies will get changed on the fly during subsequent operations. The dividers of these two PLLs are changed through registers programming.

The formula used to calculate the frequency MPLL, VPLL and SPLL is:

$F = [27 * (M+1)] / [(N+1) * (2^P)]$

M is the multiplier in the range [10:0]

N is the divider in the range [5:0]

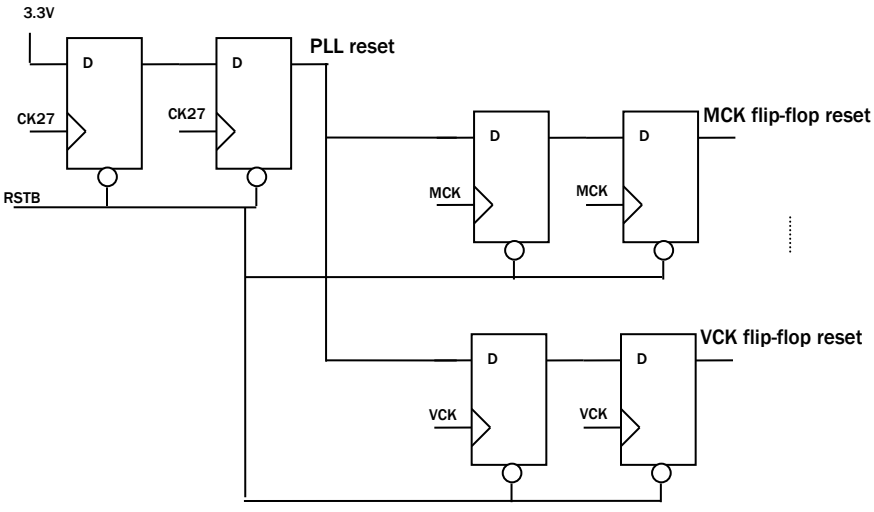
P is the post divider in the range [1:0]

Depends on band select, The PLL will function properly as long as the $100 < [27 * (M+1)] < 1000$ MHZ

RESET Logic

TW2828's reset source comes from an external reset signal running asynchronously for at least 10 uS. This signal reset the whole chip logic by resets a pair of master reset flips-flops, which in turn drive the master reset signal asynchronously through the reset buffer tree to the rest of the flip-flops in the design. The entire chip will be asynchronously reset.

To come out of reset mode we need to de-assert the reset signal pin. Which then permits the d-input of the first master reset flip-flop to be clocked through a reset synchronizer. It takes two rising edges after the reset removal to synchronize removal of the master reset. TW2828 has individual reset control to all the major functioning blocks and is controlled by users through register programming.



Multi-Clock reset de-assertion logic diagram

Playback Pin Mux

TW2828's playback port can support two kinds of input formats: BT.656 and BT.1120. It is controlled by register 0x371[3:0] for PB4-1 and 0x356[1] for PB5. If set to 0 the ports are used as BT.656 ports and set to one will let these ports become a 16 bit BT.1120 port. Most of the popular BT.1120 standards are supported.

Live Video Pin Mux

TW2828's live video ports support either at 74.24, 108 or 144 MHz mode for standard 656 format, 960H format or HD format. When register 0x201 bit 2 set to 1, the port 5, 6 and REC port1 are defined as output pins and is used to output digital RGB of the main display.

Register Table

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x200	R/W	0x00	Reserved
0x201	R/W	0x00	MISC. Control Register
0x202	R/W	0x00	MPLL Multiplier Register (MPLL_MR)
0x203	R/W	0x00	Reserved
0x204	R/W	0x00	MPLL Divider Register (MPLL_NR)
0x205	R/W	0x00	VPLL Multiplier Register (VPLL_MR)
0x206	R/W	0x00	Reserved
0x207	R/W	0x00	VPLL Divider Register (VPLL_NR)
0x208	R/W	0x00	SPLL Multiplier Register (SPLL_MR)
0x209	R/W	0x00	Reserved
0x20A	R/W	0x00	SPLL Divider Register (SPLL_NR)
0x20B	R/W	0x00	Digital Block Reset Control Register 1
0x20C	R/W	0x00	Digital Block Reset Control Register 2
0x20D	R/W	0x00	Digital Block Reset Control Register 3
0x20E	R/W	0x00	Digital Block Reset Control Register 4
0x20F	R/W	0x00	Digital Block Reset Control Register 5
0x210	R/W	0x00	LCD Display Pitch Register
0x211	R/W	0x00	Display DRAM Controller Configuration Register
0x213	R/W	0x00	PLL Post Divider Register
0x215	R/W	0x00	Chip ID Register: 0x79
0x216	R/W	0x00	Chip ID Register: 0x6E
0x217	R/W	0x00	PLL Soft Reset Control Register
0x218	R/W	0x00	REC Output Clock Phase Control Register 1
0x219	R/W	0x00	REC Output Clock Phase Control Register 2
0x21A	R/W	0x00	TV Decoder Output Clock Select Register
0x21B	R/W	0x00	IN Rate Select Register
0x21C	R/W	0x00	Live Input Clock Phase Select Register
0x21F	R/W	0x00	Misc. Control 5 Register
0x220	R/W	0x00	MPLL Control Register 1 Register
0x221	R/W	0x00	MPLL Control Register 2 Register
0x222	R/W	0x00	MPLL Control Register 3 Register
0x223	R/W	0x00	Reserved
0x224	R/W	0x48	LP_CON1 x Control Register
0x225	R/W	0x5a	LP_CON2 x Control Register
0x226	R/W	0x6c	LP_CON3 x Control Register
0x227	R/W	0x7e	LP_CON4 x Control Register
0x228	R/W	0x00	SPLL Control Register 1 Register
0x229	R/W	0x00	SPLL Control Register 2 Register
0x22A	R/W	0x00	SPLL Control Register 3 Register
0x22B	R/W	0x00	DEC Display Pitch Register 1
0x22C	R/W	0x00	DEC Display Pitch Register 2
0x22D	R/W	0x00	VPLL Control Register 1 Register
0x22E	R/W	0x00	VPLL Control Register 2 Register
0x22F	R/W	0x00	VPLL Control Register 3 Register
0x230	R/W	0x00	Display DRAM Source Vertical Position LSB Register
0x231	R/W	0x00	Display DRAM Source Vertical Position MSB Register
0x232	R/W	0x00	Display DRAM Destination Vertical Position LSB Register
0x233	R/W	0x00	Display DRAM Destination Vertical Position MSB Register
0x234	R/W	0x00	Display DRAM Vertical Transfer Size LSB Register
0x235	R/W	0x00	Display DRAM Vertical Transfer Size MSB Register
0x236	R/W	0x00	Display DRAM Source Horizontal Position LSB Register
0x237	R/W	0x00	Display DRAM Source Horizontal Position MSB Register

ADDRESS	R/W	DEFAULT	DESCRIPTION
0x238	R/W	0x00	Display DRAM Destination Hori. Position LSB Register
0x239	R/W	0x00	Display DRAM Destination Hori. Position MSB Register
0x23A	R/W	0x00	Display DRAM Horizontal Transfer Size LSB Register
0x23B	R/W	0x00	Display DRAM Horizontal Transfer Size MSB Register
0x23C	R/W	0x00	Display DRAM DMA Enable Register
0x23D	R/W	0x00	LP_CON5 x Control Register
0x23E	R/W	0x00	[7:4]: P_SEL[3:0] [1:0]: GPIO Output Select Register
0x23F	R/W	0x00	Reversed
0x240	R/W	0x00	Field Freeze Enable Register 1
0x241	R/W	0x00	Field Freeze Enable Register 2
0x242	R/W	0x00	Field Freeze Enable Register 3
0x243	R/W	0x00	Field Freeze Enable Register 4
0x244	R/W	0x00	GPIO Interrupt Mode Select Register 1
0x245	R/W	0x00	GPIO Interrupt Mode Select Register 2
0x246	R/W	0x00	GPIO Level Select Register 1
0x247	R/W	0x00	GPIO Level Select Register 2
0x248	R/W	0x00	GPIO Edge Select Register 1
0x249	R/W	0x00	GPIO Edge Select Register 2
0x24A	R/W	0x00	GPIO Interrupt Masking Register 1
0x24B	R/W	0x00	GPIO Interrupt Masking Register 2
0x24C	R/W	0x00	GPIO Pin Direction Control Register 1
0x24D	R/W	0x00	GPIO Pin Direction Control Register 2
0x24E	R/W	0x00	GPIO Output Data Register 1
0x24F	R/W	0x00	GPIO Output Data Register 2
0x250	R/W	0x00	Record DRAM Source Vertical Position LSB Register
0x251	R/W	0x00	Record DRAM Source Vertical Position MSB Register
0x252	R/W	0x00	Record DRAM Destination Vertical Position LSB Register
0x253	R/W	0x00	Record DRAM Destination Vertical Position MSB Register
0x254	R/W	0x00	Record DRAM Vertical Transfer Size LSB Register
0x255	R/W	0x00	Record DRAM Vertical Transfer Size MSB Register
0x256	R/W	0x00	Record DRAM Source Horizontal Position LSB Register
0x257	R/W	0x00	Record DRAM Source Horizontal Position MSB Register
0x258	R/W	0x00	Record DRAM Destination Horizontal Position LSB Register
0x259	R/W	0x00	Record DRAM Destination Horizontal Position MSB Register
0x25A	R/W	0x00	Record DRAM Horizontal Transfer Size LSB Register
0x25B	R/W	0x00	Record DRAM Horizontal Transfer Size MSB Register
0x25C	R/W	0x00	Record DRAM DMA Enable Register
0x25D	R/W	0x00	Record DRAM DMA Pitch Register
0x260	R/W	0x00	PB Horizontal X2 Register 1
0x261	R/W	0x00	PB Horizontal X2 Register 2
0x262	R/W	0x00	PB Automatic CHID Insertion Control Register
0x263	R/W	0x00	PB T/B Frame Count Control Register
0x264	R/W	0x00	PB T/B Frame Count Control Register
0x267	R/W	0x00	PB T/B Frame Count Control Register
0x268	R/W	0x00	Period3 Register

Registers Description

MISC. CONTROL REGISTER — 0X201

Bit	R/W	Default	Description
7	R/W	0	**Special cascade mode enable** 0: normal operation, PB5 output go to PB FIFOs 1: special operation, PB5 output go to Live FIFOs.
6:4	RO	0	**Reserved**
3	R/W	0	**REC_ENC_OEN** 0: REC output enable 1: REC output off
2	R/W	0	**External_RGB24_OEN** 0: Vin port 5,6,7 is set as inputs 1: RGB24 output enable control, P_GPIO[9] as clock source
1	R/W	0	**Reserved**
0	R/W	0	**LCD display power down** 0: Enable analog VGA display 1: VGA display power off

MPLL MULTIPLIER REGISTER (MPLLMR) — 0X202

Bit	R/W	Default	Description
7:0	R/W	0x17	**MPLL M Multiplier Register MR[7:0]** Default value: MPLL = $27 * (23+1)/(0+1) * 2^0 = 648$ MHz The MPLL frequency will be divided by 2 with another internal divider to generate 324 MHz **MCLK = MPLL / 2 = 324 MHz**

MPLL MULTIPLER REGISTER (MPLLMR) — 0X203

Bit	R/W	Default	Description
7:3	RO	0	**Reserved**
2:0	R/W	0x0	**MPLL M Multiplier Register MR[10:8]** Upper three bits of the MPLL Multiplier Register[10:8] The default values set the MPLL frequency equals 324 Mhz

MPLL DIVIDER REGISTER (MPLLNR) — 0X204

Bit	R/W	Default	Description
7:6	R/W	0	**MPLL Output Divider OD[1:0]**
5	RO	0	**Reserved**
4:0	R/W	0x0	**MPLL NR Divider Register[4:0]**

VPLL MULTIPLIER REGISTER (VPLLMR) — 0X205

Bit	R/W	Default	Description
7:0	R/W	0x20	**VPLL M Multiplier Register MR[7:0]** Default value: VPLL = 27* (32+1)/(0+1)*2^0 = 891 Mhz The VPLL frequency will be divided by 6 with another internal divider to generate 148.5 Mhz **VCLK = VPLL / 6 = 148.5 Mhz**

VPLL MULTIPLER REGISTER (VPLLMR) — 0X206

Bit	R/W	Default	Description
7:3	RO	0	**Reserved**
2:0	R/W	0x0	**VPLL M Multiplier Register MR[10:8]** Upper three bits of the VPLL Multiplier Register[10:8] The default values set the VPLL frequency equals VCLK = 27* (296+1)/(53+1)*2^0 = 148.5 MHZ

VPLL DIVIDER REGISTER (VPLLNR) — 0X207

Bit	R/W	Default	Description
7:6	R/W	0	**VPLL Output Divider OD[1:0]**
5	RO	0	**Reserved**
4:0	R/W	0x0	**VPLL Divider Register NR[4:0]**

SPLL MULTIPLIER REGISTER (SPLLMR) — 0X208

Bit	R/W	Default	Description
7:0	R/W	0x1F	**SPLL M Multiplier Register MR[7:0]** Default value: SPLL = 27* (31+1)/(0+1)*2^0 = 864 Mhz The SPLL frequency will be divided by 8 with another internal divider to generate 108 Mhz and divided by 6 to generate the 144 Mhz for the 960H video format. **SCLK = SPLL / 8 = 108 Mhz**

SPLL MULTIPLER REGISTER (SPLLMR) — 0X209

Bit	R/W	Default	Description
7:3	RO	0	**Reserved**
2:0	R/W	0x0	**SPLL M Multiplier Register MR[10:8]** Upper three bits of the SPLL Multiplier Register[10:8]

SPLL DIVIDER REGISTER (SPLLNR) — 0X20A

Bit	R/W	Default	Description
7:6	R/W	0	SPLL Output Divider OD[1:0]
5	RO	0	Reserved
4:0	R/W	0x0	SPLL Divider Register[4:0]

DIGITAL BLOCK RESET CONTROL REGISTER 1 —OFFSET 0X20B

Bit	R/W	Default	Description
7:2	RO	00	Reserved
1	R/W	0	Soft Reset Control PB in RGB controller 0: normal operation 1: reset PB in RGB controller
0	R/W	0	Soft Reset Control in RGB interface controller 0: normal operation 1: reset RGB controller

DIGITAL BLOCK RESET CONTROL REGISTER 2 — 0X20C

Bit	R/W	Default	Description
7:3	-	-	Reserved
3	R/W	0	Soft Reset LCD FRSC controller 0: normal operation 1: reset LCD FRSC controller
2	R/W	0	Soft Reset 2D de-interlace controller 0: normal operation 1: reset 2D de-interlace controller
1	R/W	0	Soft Reset LCD Dram controller 0: normal operation 1: reset LCD Dram controller
0	R/W	0	Soft Reset the whole LCD controller 0: normal operation 1: reset LCD controller

DIGITAL BLOCK RESET CONTROL REGISTER 3 — 0X20D

Bit	R/W	Default	Description
7	R/W	0	Reserved
6	R/W	-	Soft Reset the Freeze control 0: normal operation 1: Soft reset on
5:3	RO	0	Reserved
2	R/W	0	Soft Reset the SPOT controller MCLK domain 0: normal operation 1: Soft reset spot for MCLK domain logic
1:0	RO	0	Reserved

DIGITAL BLOCK RESET CONTROL REGISTER 4 — 0X20E

Bit	R/W	Default	Description
7	RO	0	**Soft Reset REC FRSC controller** 0 normal operation 1 reset REC FRSC controller
6	R/W	0	**Soft Reset IRQ controller** 0 normal operation 1 reset IRQ controller
5	R/W	0	**Soft Reset MD controller SCLK domain** 0 normal operation 1 reset MD ck108 control modules
4	R/W	0	**Soft Reset MD controller MCLK domain** 0 normal operation 1 reset MD MCLK control modules
3	R/W	0	**Soft Reset Encoder controller SCLK domain** 0 normal operation 1 reset ENC ck108 control modules
2	R/W	0	**Soft Reset Encoder controller MCLK domain** 0 normal operation 1 reset ENC MCLK control modules
1	R/W	0	**Soft Reset Decoder controller SCLK domain** 0 normal operation 1 reset DEC ck108 control modules
0	R/W	0	**Soft Reset Decoder Controller MCLK Domain** 0 normal operation 1 reset DEC MCLK control modules

DIGITAL BLOCK RESET CONTROL REGISTER 5 — 0X20F

Bit	R/W	Default	Description
7	RO	-	**Reserved**
6	R/W	0	**Soft Reset Host to DDR2 PHY** 0 normal operation 1 reset DDR2 PHY
5	R/W	0	**Soft Reset Host to Memory Controller** 0 normal operation 1 reset Host to Memory controller
4	R/W	0	**Soft Reset DCM Controller** 0 normal operation 1 reset DCM controller
3	R/W	0	**Soft Reset Down Scale Controller SCLK Domains** 0 normal operation 1 reset Down Scale in SCK control modules
2	R/W	0	**Soft Reset Down Scale Controller PB Channels** 0 normal operation 1 reset Down Scale in PBCLK control modules
1	R/W	0	**Soft Reset Down Scale Controller CK27VIN Domains**

Bit	R/W	Default	Description
			0 normal operation 1 reset Down Scale in CK27VIN control modules
0	R/W	0	**Soft Reset the Down Scale Controller** 0 normal operation 1 reset all Down Scale controllers

LCD DISPLAY PITCH REGISTER — 0X210

Bit	R/W	Default	Description
7:0	R/W	0x80	**Horizontal Display Pitch for LCD** This register is used to calculate the SDRAM horizontal size. The unit is 16 pixels / 32 bytes. Default is 2048/16 =128. If 2x128Mbit SDRAM, one page of SDRAM can be mapped to 2048x2048 pixels logic size. There are four pages in one SDRAM.

DISPLAY DRAM CONTROLLER CONFIGURATION REGISTER — 0X211

Bit	R/W	Default	Description
7:4	R/W	0x0	**Reserved**
3	R/W	1	**Frame Freeze On/Off** **0 = Frame freeze** **1 = Field freeze**
2:1	R/W	1	**Display DRAM Type Select** **00 = 128 MBIT** **01 = 256 MBIT** **10 = 512 MBIT** **11 = 1 GBIT**
0	R/W	1	**DRAM Data Width Select** **0 = not support** **1 = 16 bits**

PLL POST DIVIDER REGISTER — 0X213

Bit	R/W	Default	Description
7:6	RO	0	Reserved
5:4	R/W	0	MCLK PLL Post divider P [1:0] The value is used to further divide the MPLL frequency by 2^p
3:2	R/W	0	VCLK PLL Post divider P [1:0] The value is used to further divide the VPLL frequency by 2^p
1:0	R/W	0	SCLK PLL Post divider P [1:0] The value is used to further divide the SPLL frequency by 2^p

CHIP ID REGISTER1 — 0X215

Bit	RO	Default	Description
7:0	RO	0x28	TW2828 Series ID Chip ID = 2828_h

CHIP ID REGISTER2 — 0X216

Bit	RO	Default	Description
7:0	RO	0x28	TW2828 Series ID Chip ID = 2828_h

PLL SOFT RESET CONTROL REGISTER — 0X217

Bit	R/W	Default	Description
7:3	RO	0	Reserved
2	R/W	0	Soft reset VCK PLL 1: reset active 0: Normal
1	R/W	0	Soft reset MCK PLL 1: reset active 0: Normal
0	R/W	0	Soft reset SCK PLL 1: reset active 0: Normal

REC CLOCK CONTROL REGISTER — 0X218

Bit	R/W	Default	Description
7:2	RO	0	Reserved

1:0	R/W	0	**Select RCLK Source to generate record output port clock** 11: SCLK 10: VCLK with different phase 01: VCLK 00: SCLK

REC OUTPUT CLOCK PHASE CONTROL REGISTER — 0X219

Bit	R/W	Default	Description
7:6	R/W	0	**Rec4_clkn , Rec4_clkp phase control when SCLK is the source** 11: 270 degree phase shift 10: 180 degree phase shift 01: 90 degree phase shift 00: No phase shift
5:4		0	**Rec3_clkn, Rec3_clkp phase control when SCLK is the source** 11: 270 degree phase shift 10: 180 degree phase shift 01: 90 degree phase shift 00: No phase shift
3:2	R/W	0	**Rec2_clkn, Rec2_clkp phase control when SCLK is the source** 11: 270 degree phase shift 10: 180 degree phase shift 01: 90 degree phase shift 00: No phase shift
1:0	R/W	0	**Rec1_clkn, Rec1_clkp phase control when SCLK is the source** 11: 270 degree phase shift 10: 180 degree phase shift 01: 90 degree phase shift 00: No phase shift

IN RATE SELECT REGISTER — 0X21B

Bit	R/W	Default	Description
7:2	-	-	Reserved
1:0	R/W	0	Input data frequency selection 00: live video input is set to 108/144 MHz 01: live video input is set to 54/72 MHz 1X: Live video input is set at 27/36 MHz

LIVE INPUT CLOCK PHASE SELECT REGISTER — 0X21C

Bit	R/W	Default	Description
7	R/W	0	CK27PB4 input phase Select 1: Inverts the input clock phase 0: Normal, no phase invert
6	R/W	0	CK27PB3 input phase Select 1: Inverts the input clock phase 0: Normal, no phase invert
5	R/W	0	CK27PB2 input phase Select 1: Inverts the input clock phase 0: Normal, no phase invert
4	R/W	0	CK27PB1 input phase Select 1: Inverts the input clock phase 0: Normal, no phase invert
3	R/W	0	ckvin4 input phase Select 1: Inverts the input clock phase 0: Normal, no phase invert
2	R/W	0	ckvin3 input phase Select 1: Inverts the input clock phase 0: Normal, no phase invert
1	R/W	0	ckvin2 input phase Select 1: Inverts the input clock phase 0: Normal, no phase invert
0	R/W	0	ckvin1 input phase Select 1: Inverts the input clock phase 0: Normal, no phase invert

MISC CONTROL REGISTER 5 — 0X21F

Bit	R/W	Default	Description
7	R/W	0	**Record Port 1, 2 Source Select** 1: Select record output (D and C) 0: Select display output (D and C) output is controlled by 0x201.2
6	R/W	0	**Record Port 3 Source Select** 1: Select record output (D and C) 0: Select GPIO output (D and C)
5	R/W	0	**Record Port 4 Source Select** 1: Select record output (D and C) 0: Select GPIO output (D and C)
4:1	R/W	0	**Reserved**
0	R/W	0	**DAC Output Select** 1: Select display output 0: Select SPOT (default)

MPLL CONTROL REGISTER 1 — 0X220

Bit	R/W	Default	Description
7:6	R/W	0	**MPLL Clock Output Selection** 1x: Select VPLL default frequency (891Mhz)/5=178.2Mhz as MCLK 01: Select SPLL default frequency (864Mhz)/5=172.8Mhz as MCLK 00: Select MPLL output as MCLK
5:0	R/W	0	**Reserved**

MPLL CONTROL REGISTER 2 — 0X221

Bit	R/W	Default	Description
7:6	R/W	10	**MPLL Bank Select[1:0]** 11: NA 10: high-Band 01: Middle-Band 00: Low-Band
5	R/W	0	**MPLL Bypass Control** Bypass the MPLL and used the 27 Mhz input as the output frequency
4	R/W	0	**MPLL Analog Power Down Control** 1 : Power down the PLL 0 : Normal operation
3:0	R/W	0	**Reserved**

MPLL CONTROL REGISTER 3 — 0X222

Bit	R/W	Default	Description
7:6	R/W	0	**MPLL Loop Resistor Value Select** 11 : 1.1 KOHM 10 : 2.2 KOHM 01 : 6.6 KOHM 00 : 38.5 KOHM
5:4	R/W	0x3	**MPLL VCO Frequency Range Selection** 11 : 270 - 700 MHz 10 : 110 - 320 MHz 01 : 50 - 140 MHz 00 : 5 - 75 MHz
3:1	R/W	0x1	**MPLL Charge Pump Current Selection** 3'h7 : 319 uA 3'h6 : 159 uA 3'h5 : 79 uA 3'h4 : 39 uA 3'h3 : 19 uA 3'h2 : 9 uA 3'h1 : 4 uA 3'h0 : 1.5 uA
0	R/W	0	**MPLL Current Generator Control** 1 : more current generated 0 : Normal Operation

LP_CON1 X CONTROL REGISTER — 0X224

Bit	R/W	Default	Description
7:4	R/W	000	When PB1 port are used for HD purpose (0x371[0] = 1'b1), PB1 data is from: Others: **Reserved** 0110: rec4_data, rec3_data 0101: rec_data[15:0] (display) 0100: pb5_data 0011: pb4_data 0010: pb3_data 0001: pb2_data 0000: pb1_data When PB1 port are used for SD purpose (0x371[0] = 1'b0), PB1 data is from: Others: **Reserved** 0111: pb5_data 0111: rec4_data 0110: rec3_data 0101: rec2_data 0100: rec1_data 0011: pb4_data 0010: pb3_data 0001: pb2_data 0000: pb1_data
3:0	R/W	0000	When PB1 port are used for HD purpose (0x371[0] = 1'b1) PB1 clock is from: 1111: **Reserved**

Bit	R/W	Default	Description
			1110: rec3_clkn 1101: rec1_clkn 1100: pb5_clk invert 1011: pb4_clk invert 1010: pb3_clk invert 1001: pb2_clk invert 1000: pb1_clk invert 0111: **Reserved** 0110: rec3_clkp 0101: rec1_clkp 0100: pb5_clk 0011: pb4_clk 0010: pb3_clk 0001: pb2_clk 0000: pb1_clk When PB1 port are used for SD purpose (0x371[0] = 1'b0) PB1 port clock is coming from: 1111: rec4_clkn 1110: rec4_clkp 1101: rec3_clkn 1100: rec3_clkp 1011: rec2_clkn 1010: rec2_clkp 1001: rec1_clkn 1000: rec1_clkp 0111: pb4_clk invert when 0x23e[0] = 0, pb5_clk invert when 0x23e[0] = 1 0110: pb3_clk invert 0101: pb2_clk invert 0100: pb1_clk invert 0011: pb4_clk when 0x23e[0] = 0, pb5_clk when 0x23e[0] = 1 0010: pb3_clk 0001: pb2_clk 0000: pb1_clk

LP_CON2 X CONTROL REGISTER — 0X225

Bit	R/W	Default	Description
7:4	R/W	000	When PB2 port are used for HD purpose (0x371[1] = 1'b1), PB2 data is from: Others: **Reserved** 0110: rec4_data, rec3_data 0101: rec_data[15:0] (display) 0100: pb5_data 0011: pb4_data 0010: pb3_data 0001: pb2_data 0000: pb1_data When PB2 port are used for SD purpose (0x371[1] = 1'b0), PB2 data is from: Others: **Reserved** 1000: pb5_data 0111: rec4_data 0110: rec3_data 0101: rec2_data 0100: rec1_data 0011: pb4_data 0010: pb3_data

Bit	R/W	Default	Description
			0001: pb2_data 0000: pb1_data
3:0	R/W	0000	When PB2 port are used for HD purpose (0x371[1] = 1'b1) PB2 clock is from: 1111: **Reserved** 1110: rec3_clkn 1101: rec1_clkn 1100: pb5_clk invert 1011: pb4_clk invert 1010: pb3_clk invert 1001: pb2_clk invert 1000: pb1_clk invert 0111: **Reserved** 0110: rec3_clkp 0101: rec1_clkp 0100: pb5_clk 0011: pb4_clk 0010: pb3_clk 0001: pb2_clk 0000: pb1_clk When PB2 port are used for SD purpose (0x371[1] = 1'b0) PB2 port clock is coming from: 1111: rec4_clkn 1110: rec4_clkp 1101: rec3_clkn 1100: rec3_clkp 1011: rec2_clkn 1010: rec2_clkp 1001: rec1_clkn 1000: rec1_clkp 0111: pb4_clk invert when 0x23e[1] = 0, pb5_clk invert when 0x23e[1] = 1 0110: pb3_clk invert 0101: pb2_clk invert 0100: pb1_clk invert 0011: pb4_clk when 0x23e[1] = 0, pb5_clk when 0x23e[1] = 1 0010: pb3_clk 0001: pb2_clk 0000: pb1_clk

LP_CON3 X CONTROL REGISTER — 0X226

Bit	R/W	Default	Description
7:4	R/W	000	When PB3 port are used for HD purpose (0x371[2] = 1'b1), PB3 data is from: Others: **Reserved** 0110: rec4_data, rec3_data 0101: rec_data[15:0] (display) 0100: pb5_data 0011: pb4_data 0010: pb3_data 0001: pb2_data 0000: pb1_data When PB3 port are used for SD purpose (0x371[2] = 1'b0), PB3 data is from: Others: **Reserved**

Bit	R/W	Default	Description
			1000: pb5_data 0111: rec4_data 0110: rec3_data 0101: rec2_data 0100: rec1_data 0011: pb4_data 0010: pb3_data 0001: pb2_data 0000: pb1_data
3:0	R/W	0000	When PB3 port are used for HD purpose (0x371[2] = 1'b1) PB3 clock is from: 1111: **Reserved** 1110: rec3_clkn 1101: rec1_clkn 1100: pb5_clk invert 1011: pb4_clk invert 1010: pb3_clk invert 1001: pb2_clk invert 1000: pb1_clk invert 0111: **Reserved** 0110: rec3_clkp 0101: rec1_clkp 0100: pb5_clk 0011: pb4_clk 0010: pb3_clk 0001: pb2_clk 0000: pb1_clk When PB3 port are used for SD purpose (0x371[2] = 1'b0) PB3 port clock is coming from: 1111: rec4_clkn 1110: rec4_clkp 1101: rec3_clkn 1100: rec3_clkp 1011: rec2_clkn 1010: rec2_clkp 1001: rec1_clkn 1000: rec1_clkp 0111: pb4_clk invert when 0x23e[2] = 0, pb5_clk invert when 0x23e[2] = 1 0110: pb3_clk invert 0101: pb2_clk invert 0100: pb1_clk invert 0011: pb4_clk when 0x23e[2] = 0, pb5_clk when 0x23e[2] = 1 0010: pb3_clk 0001: pb2_clk 0000: pb1_clk

LP_CON4 X CONTROL REGISTER — 0X227

Bit	R/W	Default	Description
7:4	R/W	000	When PB4 port are used for HD purpose (0x371[3] = 1'b1), PB4 data is from: Others: **Reserved** 0110: rec4_data, rec3_data 0101: rec_data[15:0] (display) 0100: pb5_data 0011: pb4_data 0010: pb3_data

Bit	R/W	Default	Description
			0001: pb2_data 0000: pb1_data When PB4 port are used for SD purpose (0x371[3] = 1'b0), PB4 data is from: Others: **Reserved** 1000: pb5_data 0111: rec4_data 0110: rec3_data 0101: rec2_data 0100: rec1_data 0011: pb4_data 0010: pb3_data 0001: pb2_data 0000: pb1_data
3:0	R/W	0000	When PB4 port are used for HD purpose (0x371[3] = 1'b1) PB4 clock is from: 1111: **Reserved** 1110: rec3_clkn 1101: rec1_clkn 1100: pb5_clk invert 1011: pb4_clk invert 1010: pb3_clk invert 1001: pb2_clk invert 1000: pb1_clk invert 0111: **Reserved** 0110: rec3_clkp 0101: rec1_clkp 0100: pb5_clk 0011: pb4_clk 0010: pb3_clk 0001: pb2_clk 0000: pb1_clk When PB4 port are used for SD purpose (0x371[3] = 1'b0) PB4 port clock is coming from: 1111: rec4_clkn 1110: rec4_clkp 1101: rec3_clkn 1100: rec3_clkp 1011: rec2_clkn 1010: rec2_clkp 1001: rec1_clkn 1000: rec1_clkp 0111: pb4_clk invert when 0x23e[3] = 0, pb5_clk invert when 0x23e[3] = 1 0110: pb3_clk invert 0101: pb2_clk invert 0100: pb1_clk invert 0011: pb4_clk when 0x23e[3] = 0, pb5_clk when 0x23e[3] = 1 0010: pb3_clk 0001: pb2_clk 0000: pb1_clk

SPLL CONTROL REGISTER 1 — 0X228

Bit	R/W	Default	Description
7	R/W	0	**SPLL Clock Output Frequency Select** 1: 144 MHz 0: 108 MHz
6	R/W	0	**Clock Output 13.5 MHz Inverts** 1: Inverts the PLL 13.5 MHz output 0: No Inversion
5	R/W	0	**Clock Output 27 MHz Inverts** 1: Inverts the PLL 27 MHz output 0: No Inversion
4	R/W	0	**Clock Output 54 MHz Inverts** 1: Inverts the PLL 54 MHz output 0: No Inversion
3	R/W	0	**SPLL Clock Output Inverts** 1: Inverts the PLL output 0: No Inversion
2:0	R/W	0	**SPLL Clock Output Delay Control** **Each Increment will delay the clock output by 45º** … 11: 135º phase shift 10: 90º phase shift 01: 45º phase shift 00: No phase shift

SPLL CONTROL REGISTER 2 — 0X229

Bit	R/W	Default	Description
7:6	R/W	10	**SPLL Bank Select[1:0]** 11: NA 10: high-Band 01 : Middle-Band 00: Low-Band
5	R/W	0	**SPLL Bypass Control** Bypass the SPLL and used the 27 Mhz input as the output frequency
4	R/W	0	**SPLL Analog Power Down Control** 1 : Power down the SPLL 0 : Normal operation
3:1	R/W	0	**Reserved**
0	R/W	0	**Output to TVDEC frequency Select** 1: Output frequency is 36 MHz when send to TV decoder in 960 Format 0: Output frequency is 108 MHz when send to TV decoder in SD Format

SPLL CONTROL REGISTER 3 — 0X22A

Bit	R/W	Default	Description
7:0	R/W	0	**Reserved**

DEC DISPLAY PITCH REGISTER 1— 0X22B

Bit	R/W	Default	Description
7:0	R/W	0x80	**DEC Horizontal Display Pitch[7:0]** This is use in calculate SDRAM horizontal size. The unit is 16 pixels / 32 bytes. Default is 2048/16=128. If 2x128Mbit SDRAM, one page SDRAM can be mapped to 2048x2048 pixels logic size. There are four pages in one SDRAM.

DEC DISPLAY PITCH REGISTER 2— 0X22C

Bit	R/W	Default	Description
7	R/W	1	**DEC Horizontal Display Pitch[8]** This is use in calculate SDRAM horizontal size. The unit is 16 pixels / 32 bytes. Default is 2048/16=128. If 2x128Mbit SDRAM, one page SDRAM can be mapped to 2048x2048 pixels logic size. There are four pages in one SDRAM.
6:0			**Reserved**

VPLL CONTROL REGISTER 1 — 0X22D

Bit	R/W	Default	Description
7:4	R/W	0010	**VCLK1 Output Frequency Selection** **When reg_22F[7:6]=00, the VCLK1 uses the internal divider to divide the VPLL frequency by this programmed registers** 0000: divides by 4 0001: divides by 4 and invert 0010: divides by 6 0011: divides by 6 and invert 0100: divides by 7 0101: divides by 7 and invert 0100: divides by 8 0101: divides by 8 and invert 1000: divides by 10 1001: divides by 10 and invert 1010: divides by 12 1011: divides by 12 and invert 1100: divides by 28 1101: divides by 28 and invert 1110: divides by 16 1111: divides by 16 and invert When reg_22F[7:6]=01, VCLK1 = 13.5 Mhz When reg_22F[7:6]=10, VCLK1 = 27.0 Mhz When reg_22F[7:6]=11, VCLK1 = 108 Mhz
3:0	R/W	2	**VCLK Output Frequency Selection** **When reg_22F[5:4]=00, the VCLK uses the internal divider to divide the VPLL frequency by this programmed registers** 0000: divides by 4 0001: divides by 4 and invert 0010: divides by 6 0011: divides by 6 and invert 0100: divides by 7 0101: divides by 7 and invert 0100: divides by 8 0101: divides by 8 and invert 1000: divides by 10 1001: divides by 10 and invert

Bit	R/W	Default	Description
			1010: divides by 12 1011: divides by 12 and invert 1100: divides by 28 1101: divides by 28 and invert 1110: divides by 16 1111: divides by 16 and invert When reg_22F[5:4]=01, VCLK = 13.5 Mhz When reg_22F[5:4]=10, VCLK = 27.0 Mhz When reg_22F[5:4]=11, VCLK = 108 Mhz

VPLL CONTROL REGISTER 2 — 0X22E

Bit	R/W	Default	Description
7:6	R/W	10	**VPLL Bank Select BS[1:0]** 11: NA 10: high-Band 01 : Middle-Band 00: Low-Band
5	R/W	0	**VPLL Bypass Control** Bypass the VPLL and used the 27 Mhz input as the output frequency
4	R/W	0	**VPLL Analog Power Down Control** 1 : Power down the VPLL 0 : Normal operation
3:2	R/W	0	**Reserved**
1:0	R/W	0	**VCLK internal divider phase Selection** 11: 135^0 shift 10: 90^0 shift 01 : 45^0 shift 0 0: no shift

VPLL CONTROL REGISTER 3 — 0X22F

Bit	R/W	Default	Description
7:6	R/W	0	**VCLK1 Output Frequency Selection** Refers to register 0x22D for the VCLK1 Frequency selection
5:4	R/W	0	**VCLK Output Frequency Selection** Refers to register 0x22D for the VCLK Frequency selection
3:0	R/W	0	**Reserved**

DISPLAY DRAM SOURCE VERTICAL POSITION LSB REGISTER – 0X230

Bit	R/W	Default	Description
7:0	W	0	**Source vertical position[7:0] (a line)**

DISPLAY DRAM SOURCE VERTICAL POSITION MSB REGISTER – 0X231

Bit	R/W	Default	Description
7:6	W	0	Reserved
5:4	W	0	Source bank
3:0	W	0	Source vertical position[11:8]

DISPLAY DRAM DESTINATION VERTICAL POSITION LSB REGISTER – 0X232

Bit	R/W	Default	Description
7:0	W	0	Destination vertical position[7:0] (a line)

DISPLAY DRAM DESTINATION VERTICAL POSITION MSB REGISTER – 0X233

Bit	R/W	Default	Description
7:6	W	0	Reserved
5:4	W	0	Destination bank
3:0	W	0	Destination vertical position[11:8]

DISPLAY DRAM VERTICAL TRANSFER SIZE LSB REGISTER – 0X234

Bit	R/W	Default	Description
7:0	W	0	Vertical transfer size[7:0] (a line)

DISPLAY DRAM VERTICAL TRANSFER SIZE MSB REGISTER – 0X235

Bit	R/W	Default	Description
7:3	W	0	Reserved
2:0	W	0	Vertical transfer size [10:8]

DISPLAY DRAM SOURCE HORIZONTAL POSITION LSB REGISTER – 0X236

Bit	R/W	Default	Description
7:0	W	0	Source horizontal position[7:0] (4 pixels)

DISPLAY DRAM SOURCE HORIZONTAL POSITION MSB REGISTER – 0X237

Bit	R/W	Default	Description
7:2	W	0	Reserved
1:0	W	0	Source vertical position[9:8]

DISPLAY DRAM DESTINATION HORIZONTAL POSITION LSB REGISTER – 0X238

Bit	R/W	Default	Description
7:0	W	0	Destination horizontal position[7:0] (4 pixels)

DISPLAY DRAM DESTINATION HORIZONTAL POSITION MSB REGISTER – 0X239

Bit	R/W	Default	Description
7:2	W	0	Reserved
1:0	W	0	Destination horizontal position[9:8]

DISPLAY DRAM HORIZONTAL TRANSFER SIZE LSB REGISTER – 0X23A

Bit	R/W	Default	Description
7:0	W	0	Horizontal transfer size[7:0] (4 pixels)

DISPLAY DRAM HORIZONTAL TRANSFER SIZE MSB REGISTER – 0X23B

Bit	R/W	Default	Description
7	R	0	Reserved
6	W	0	1 = PB_CLK5 clock reversed
5:1	R	0	Reserved
0	W	0	Horizontal transfer size [8]

DISPLAY DRAM DMA ENABLE REGISTER – 0X23C

Bit	R/W	Default	Description
7:1	W	0	Reserved
0	W	0	Display DRAM DMA enable

LP_CON5 X CONTROL REGISTER — 0X23D

Bit	R/W	Default	Description
7:4	R/W	000	PB5 HD data is from: 111: **Reserved** 110: REC data 101: din5 & din6 ports 100: din3 & din4 ports 011: din1 & din2 ports 010: PB5 & PB6 ports 001: PB3 & PB4 ports 000: PB1 & PB2 ports
3:0	R/W	0000	PB5 port clock is coming from: 1111: **Reserved** 1110: RCLK 1101: ckvin56 invert 1100: ckvin34 invert 1011: ckvin12 invert 1010: pb5_clk invert 1001: pb3_clk invert 1000: pb1_clk invert 0111: **Reserved** 0110: RCLK 0101: ckvin56 0100: ckvin34 0011: ckvin12

Bit	R/W	Default	Description
			0010: pb5_clk 0001: pb3_clk 0000: pb1_clk

GPIO OUTPUT SELECT REGISTER — 0X23E

Bit	R/W	Default	Description
7:4	R	0	**PSEL[3:0]:** Loop back 5 phase control
3:2	R	0	**Reserved**
1:0	R/W	0	GPIO output source select: bit 1 controls high byte, bit 0 controls low byte. 00: from Record Port 01: Connected Record Port[15:8](high byte) and GPIO[7:0](low byte) 10: Connected GPIO[15:8] for high byte and Record Port[7:0](low byte) 11: Connected GPIO[15:0]

FIELD FREEZE ENABLE REGISTER 1 – 0X240

Bit	R/W	Default	Description
7:0	R/W	0	**CH_FIELD_FREEZE[7:0] for field freezing of live channel 0 to 7** 1: enable 0: disable

FIELD FREEZE ENABLE REGISTER 2 – 0X241

Bit	R/W	Default	Description
7:0	R/W	0	**CH_FIELD_FREEZE[15:8] for field freezing of live channel 8 to 15** 1: enable 0: disable

FIELD FREEZE ENABLE REGISTER 3 – 0X242

Bit	R/W	Default	Description
7:0	R/W	0	**CH_FIELD_FREEZE[23:16] for field freezing of PB channel 0 to 7** 1: enable 0: disable

FIELD FREEZE ENABLE REGISTER 4 – 0X243

Bit	R/W	Default	Description
7:0	R/W	0	**CH_FIELD_FREEZE[31:24] for field freezing of PB channel 8 to 15** 1: enable 0: disable

GPIO INTERRUPT MODE SELECT REGISTER 1 – 0X244

Bit	R/W	Default	Description
7:0	R/W	0	**MODE[7:0] for GPIO[7:0]** 1: edge-triggered interrupt mode 0: level-triggered interrupt mode

GPIO INTERRUPT MODE SELECT REGISTER 2 – 0X245

Bit	R/W	Default	Description
7:0	R/W	0	**MODE[15:8] for GPIO[15:8]** 1: edge-triggered interrupt mode 0: level-triggered interrupt mode

GPIO LEVEL SELECT REGISTER 1 – 0X246

Bit	R/W	Default	Description
7:0	R/W	0	**LEVEL[7:0] for GPIO[7:0]** 1: high level-triggered interrupt 0: low level-triggered interrupt

GPIO LEVEL SELECT REGISTER 2 – 0X247

Bit	R/W	Default	Description
7:0	R/W	0	**LEVEL[15:8] for GPIO[15:8]** 1: high level-triggered interrupt 0: low level-triggered interrupt

GPIO EDGE SELECT REGISTER 1 – 0X248

Bit	R/W	Default	Description
7:0	R/W	0	**EDGE[7:0] for GPIO[7:0]** 1: rising edge interrupt 0: falling edge interrupt

GPIO EDGE SELECT REGISTER 2 – 0X249

Bit	R/W	Default	Description
7:0	R/W	0	**EDGE[15:8] for GPIO[15:8]** 1: rising edge interrupt 0: falling edge interrupt

GPIO INTERRUPT MASKING REGISTER 1 – 0X24A

Bit	R/W	Default	Description
7:0	R/W	FF	MASK[7:0] for GPIO[7:0] 1: interrupt mask enable 0: normal operation

GPIO INTERRUPT MASKING REGISTER 2 – 0X24B

Bit	R/W	Default	Description
7:0	R/W	0xFF	MASK[15:8] for GPIO[15:8] 1: interrupt mask enable 0: normal operation

GPIO PIN DIRECTION CONTROL REGISTER 1 – 0X24C

Bit	R/W	Default	Description
7:0	R/W	0x00	DIR[7:0] for GPIO[7:0] 1: output mode 0: input mode

GPIO PIN DIRECTION CONTROL REGISTER 2 – 0X24D

Bit	R/W	Default	Description
7:0	R/W	0x00	DIR[15:8] for GPIO[15:8] 1: output mode 0: input mode

GPIO OUTPUT DATA REGISTER 1 – 0X24E

Bit	R/W	Default	Description
7:0	R/W	0x00	OUT[7:0] for GPIO[7:0] data

GPIO OUTPUT DATA REGISTER 2 – 0X24F

Bit	R/W	Default	Description
7:0	R/W	0x00	OUT[15:8] for GPIO[15:8] data

RECORD DRAM SOURCE VERTICAL POSITION LSB REGISTER – 0X250

Bit	R/W	Default	Description
7:0	W	0x00	Source vertical position[7:0] (a line)

RECORD DRAM SOURCE VERTICAL POSITION MSB REGISTER – 0X251

Bit	R/W	Default	Description
7:6	W	0	Reserved
5:4	W	0	Source bank
3:0	W	0	Source vertical position[11:8]

RECORD DRAM DESTINATION VERTICAL POSITION LSB REGISTER – 0X252

Bit	R/W	Default	Description
7:0	W	0x00	Destination vertical position[7:0] (a line)

RECORD DRAM DESTINATION VERTICAL POSITION MSB REGISTER – 0X253

Bit	R/W	Default	Description
7:6	W	0	Reserved
5:4	W	0	Destination bank
3:0	W	0	Destination vertical position[11:8]

RECORD DRAM VERTICAL TRANSFER SIZE LSB REGISTER – 0X254

Bit	R/W	Default	Description
7:0	W	0x00	Vertical transfer size[7:0] (a line)

RECORD DRAM VERTICAL TRANSFER SIZE MSB REGISTER – 0X255

Bit	R/W	Default	Description
7:3	W	0	Reserved
2:0	W	0	Vertical transfer size [10:8]

RECORD DRAM SOURCE HORIZONTAL POSITION LSB REGISTER – 0X256

Bit	R/W	Default	Description
7:0	W	0x00	Source horizontal position[7:0] (4 pixels)

RECORD DRAM SOURCE HORIZONTAL POSITION MSB REGISTER – 0X257

Bit	R/W	Default	Description
7:2	W	0	Reserved
1:0	W	0	Source horizontal position[9:8]

RECORD DRAM DESTINATION HORIZONTAL POSITION LSB REGISTER – 0X258

Bit	R/W	Default	Description
7:0	W	0x00	Destination horizontal position[7:0] (4 pixels)

RECORD DRAM DESTINATION HORIZONTAL POSITION MSB REGISTER – 0X259

Bit	R/W	Default	Description
7:2	W	0	Reserved
1:0	W	0	Destination horizontal position[9:8]

RECORD DRAM HORIZONTAL TRANSFER SIZE LSB REGISTER – 0X25A

Bit	R/W	Default	Description
7:0	W	0x00	Horizontal transfer size[7:0] (4 pixels)

RECORD DRAM HORIZONTAL TRANSFER SIZE MSB REGISTER – 0X25B

Bit	R/W	Default	Description
7:1	R	0	Reserved
0	W	0	Horizontal transfer size [8]

RECORD DRAM DMA ENABLE REGISTER – 0X25C

Bit	R/W	Default	Description
7:1	W	0	Reserved
0	W	0	Copy DMA enable

RECORD DMA PITCH REGISTER – 0X25D

Bit	R/W	Default	Description
7:0	W	0x00	Pitch[7:0]

PB HORIZONTAL X2 CONTROL REGISTER 1 — 0X260

Bit	R/W	Default	Description
7-5			Reserved
4	R/W	0	ENAX2_PB4 for PB5 horizontal size x2 upscale enable/disable control 0: disable 1: enable
3	R/W	0	ENAX2_PB[4:0] for horizontal size x2 upscale enable/disable control 0: disable 1: enable
2	R/W	0	ENAX2_PB[4:0] for horizontal size x2 upscale enable/disable control 0: disable 1: enable
1	R/W	0	ENAX2_PB[4:0] for horizontal size x2 upscale enable/disable control 0: disable 1: enable
0	R/W	0	ENAX2_PB[4:0] for horizontal size x2 upscale enable/disable control 0: disable 1: enable

PB HORIZONTAL X2 CONTROL REGISTER 2 — 0X261

Bit	R/W	Default	Description
7-5			Reserved
4	R/W	0	PBX2_MODE4 for mode selection of PB5 Horizontal size x2 upscale 0: always enable 1: control by auto channel ID bit 34(1 = enable)
3	R/W	0	PBX2_MODE3 for mode selection of PB4 Horizontal size x2 upscale 0: always enable 1: control by auto channel ID bit 34(1 = enable)
2	R/W	0	PBX2_MODE2 for mode selection of PB3 Horizontal size x2 upscale 0: always enable 1: control by auto channel ID bit 34(1 = enable)
1	R/W	0	PBX2_MODE1 for mode selection of PB2 Horizontal size x2 upscale 0: always enable 1: control by auto channel ID bit 34(1 = enable)
0	R/W	0	PBX2_MODE0 for mode selection of PB1 Horizontal size x2 upscale 0: always enable 1: control by auto channel ID bit 34(1 = enable)

PB AUTOMATIC CHID INSERTION CONTROL REGISTER — 0X262

Bit	R/W	Default	Description
7-5			Reserved
4	R/W	0	CHID_SEL4 for PB5 automatic channel ID insertion 0: normal 1: CHID is inserted by TW2828
3	R/W	0	CHID_SEL3 for PB4 automatic channel ID insertion 0: normal 1: CHID is inserted by TW2828
2	R/W	0	CHID_SEL2 for PB3 automatic channel ID insertion 0: normal 1: CHID is inserted by TW2828
1	R/W	0	CHID_SEL1 for PB2 automatic channel ID insertion 0: normal 1: CHID is inserted by TW2828
0	R/W	0	CHID_SEL0 for PB1 automatic channel ID insertion 0: normal 1: CHID is inserted by TW2828

PB T/B FRAME COUNT CONTROL REGISTER — 0X263

Bit	R/W	Default	Description
7:4	R/W	0	FRM_SEL1[3:0]: T/B field toggle frame count for PB2
3:0	R/W	0	FRM_SEL0[3:0]: T/B field toggle frame count for PB1

PB T/B FRAME COUNT CONTROL REGISTER — 0X264

Bit	R/W	Default	Description
7:4	R/W	0	**FRM_SEL3[3:0]:** T/B field toggle frame count for PB4
3:0	R/W	0	**FRM_SEL2[3:0]:** T/B field toggle frame count for PB3

PB T/B FRAME COUNT CONTROL REGISTER — 0X267

Bit	R/W	Default	Description
7:4	R/W	0	**Reserved**
3:0	R/W	0	**FRM_SEL4[3:0]:** T/B field toggle frame count for PB5

PERIOD3 REGISTER – 0X268

Bit	R/W	Default	Description
7:0	R/W	0x00	**Period3[7:0] for PB1 to 5**

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION #	CHANGE
March 27, 2013	FN8291.1	Initial release.

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