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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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MOS FIELD EFFECT TRANSISTOR

μ PA2354

DUAL N-CHANNEL MOSFET

DESCRIPTION

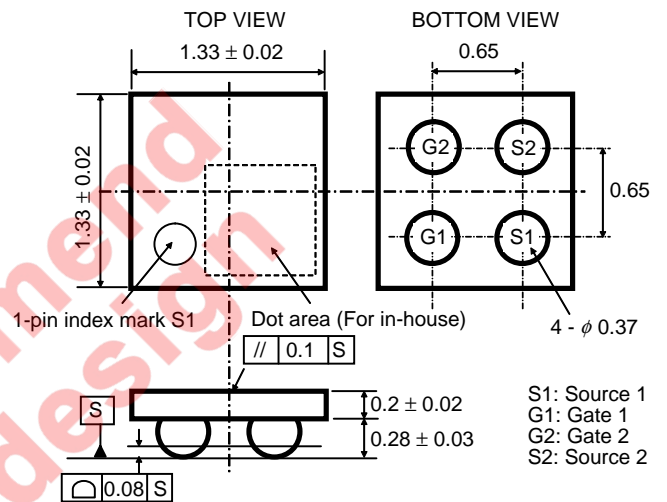
The μ PA2354 is a Dual N-channel MOSFET designed for Lithium-Ion battery protection circuit.

Ecologically Flip chip MOSFET for Lithium-Ion battery Protection (EFLIP).

FEATURES

- Monolithic Dual MOSFET
Connecting the Drains on the circuit board is not required because the Drains of the FET1 and the FET2 are internally connected.
- 1.8 V drive available and low on-state resistance
 $R_{SS(on)1} = 42.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_S = 2.0 \text{ A)}$
 $R_{SS(on)2} = 49.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 3.1 \text{ V, } I_S = 2.0 \text{ A)}$
 $R_{SS(on)3} = 57.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 2.5 \text{ V, } I_S = 2.0 \text{ A)}$
 $R_{SS(on)4} = 99.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 1.8 \text{ V, } I_S = 2.0 \text{ A)}$
- Built-in G-S protection diode against ESD
- Pb-free Bump

OUTLINE DRAWING (Unit: mm)



ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA2354T1G-E4-A ^{Note}	4-pin EFLIP

Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

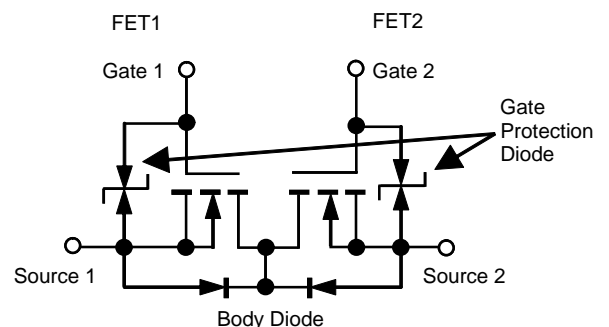
Remark "-E4" indicates the unit orientation (E4 only).

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Source to Source Voltage (V _{GS} = 0 V)	V _{SSS}	24	V
Gate to Source Voltage (V _{SS} = 0 V)	V _{GSS}	±8	V
Source Current (DC) ^{Note1}	I _{S(DC)}	±4.0	A
Source Current (pulse) ^{Note2}	I _{S(pulse)}	±33	A
Total Power Dissipation (2 units) ^{Note1}	P _T	0.75	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

- Notes** 1. Mounted on BT resin board of 40.5 mm x 25 mm x 1.5 mm
 2. PW ≤ 100 μs, Duty Cycle ≤ 1%

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

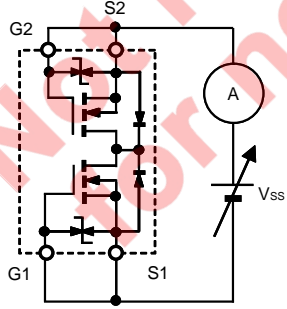
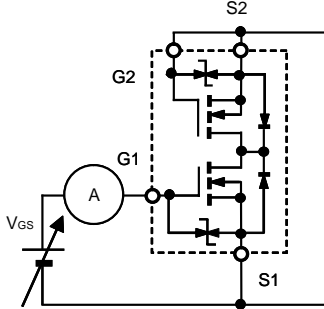
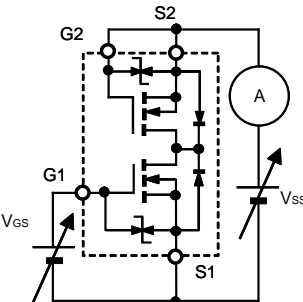
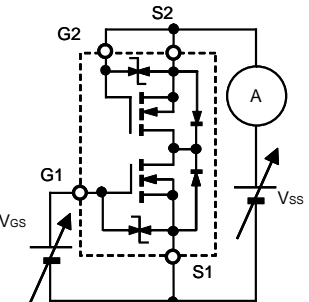
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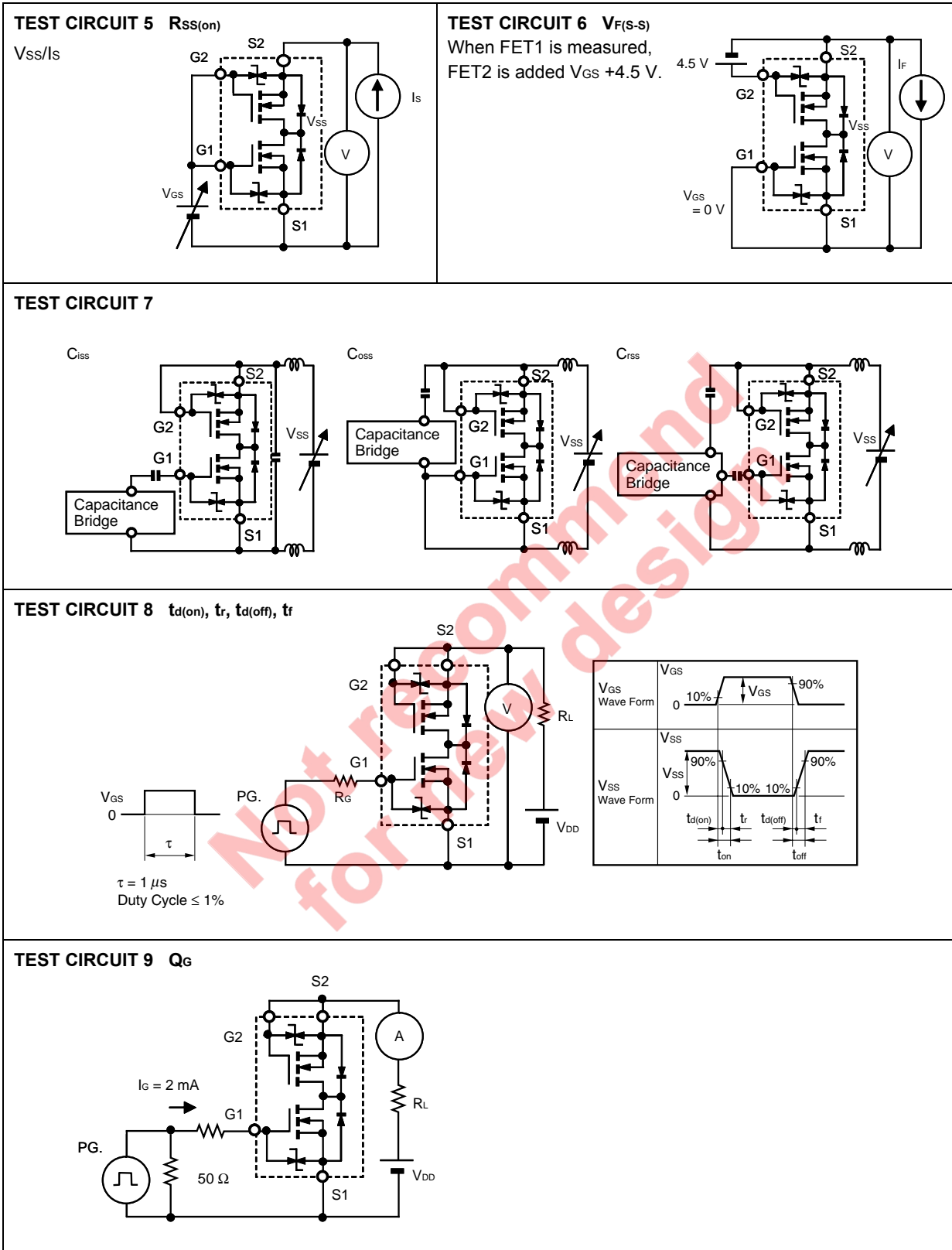
ELECTRICAL CHARACTERISTICS (TA = 25°C) These are common to FET1 and FET2.

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Source Current	I_{SSS}	$V_{SS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$, TEST CIRCUIT 1			10	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 12\text{ V}$, $V_{SS} = 0\text{ V}$, TEST CIRCUIT 2			±10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	$V_{SS} = 10.0\text{ V}$, $I_S = 1.0\text{ mA}$, TEST CIRCUIT 3	0.4	0.7	1.2	V
Forward Transfer Admittance ^{Note}	$ y_{fs} $	$V_{SS} = 10.0\text{ V}$, $I_S = 2.0\text{ A}$, TEST CIRCUIT 4	2.2			S
Source to Source On-state Resistance ^{Note}	$R_{SS(on)1}$	$V_{GS} = 4.5\text{ V}$, $I_S = 2.0\text{ A}$, TEST CIRCUIT 5	23.0	35.0	42.0	mΩ
	$R_{SS(on)2}$	$V_{GS} = 3.1\text{ V}$, $I_S = 2.0\text{ A}$, TEST CIRCUIT 5	26.5	40.0	49.0	mΩ
	$R_{SS(on)3}$	$V_{GS} = 2.5\text{ V}$, $I_S = 2.0\text{ A}$, TEST CIRCUIT 5	29.0	43.0	57.0	mΩ
	$R_{SS(on)4}$	$V_{GS} = 1.8\text{ V}$, $I_S = 2.0\text{ A}$, TEST CIRCUIT 5	32.0	57.0	99.0	mΩ
Input Capacitance	C_{iss}	$V_{SS} = 10.0\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$		720		pF
Output Capacitance	C_{oss}	TEST CIRCUIT 7		130		pF
Reverse Transfer Capacitance	C_{rss}			80		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 20.0\text{ V}$, $I_S = 4.0\text{ A}$,		2.2		μs
Rise Time	t_r	$V_{GS} = 4.0\text{ V}$, $R_G = 6.0\text{ Ω}$,		4.4		μs
Turn-off Delay Time	$t_{d(off)}$	TEST CIRCUIT 8		9.2		μs
Fall Time	t_f			9.7		μs
Total Gate Charge	Q_G	$V_{DD} = 16\text{ V}$, $V_{G1S1} = 4.0\text{ V}$, $I_S = 4.0\text{ A}$, TEST CIRCUIT 9		6.0		nC
Body Diode Forward Voltage ^{Note}	$V_{F(S-S)}$	$I_F = 4.0\text{ A}$, $V_{GS} = 0\text{ V}$, TEST CIRCUIT 6		0.9		V

Note Pulsed

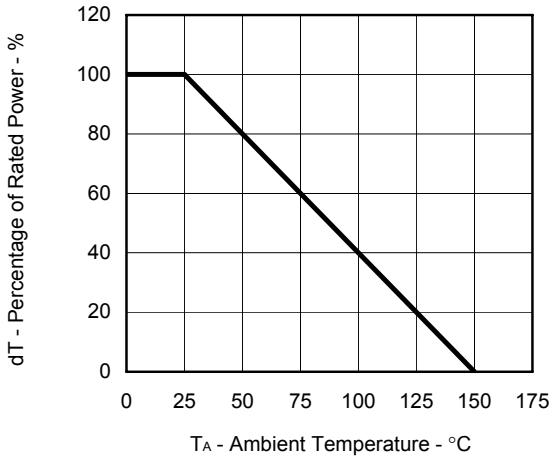
Both the FET1 and the FET2 are measured. Test circuits are example of measuring the FET1 side.

<p>TEST CIRCUIT 1 I_{SSS}</p> 	<p>TEST CIRCUIT 2 I_{GSS}</p> <p>When FET1 is measured, between GATE and SOURCE of FET2 are shorted.</p> 
<p>TEST CIRCUIT 3 $V_{GS(off)}$</p> <p>When FET1 is measured, between GATE and SOURCE of FET2 are shorted.</p> 	<p>TEST CIRCUIT 4 y_{fs}</p> <p>$\Delta I_S / \Delta V_{GS}$</p> 

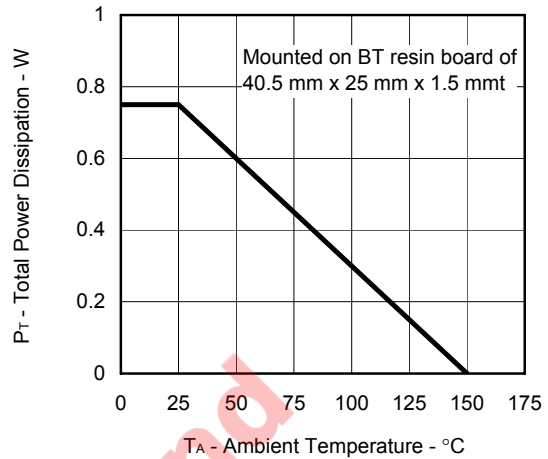


TYPICAL CHARACTERISTICS (T_A = 25°C)

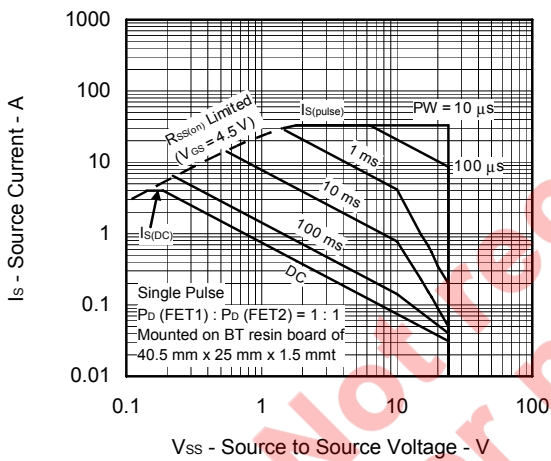
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



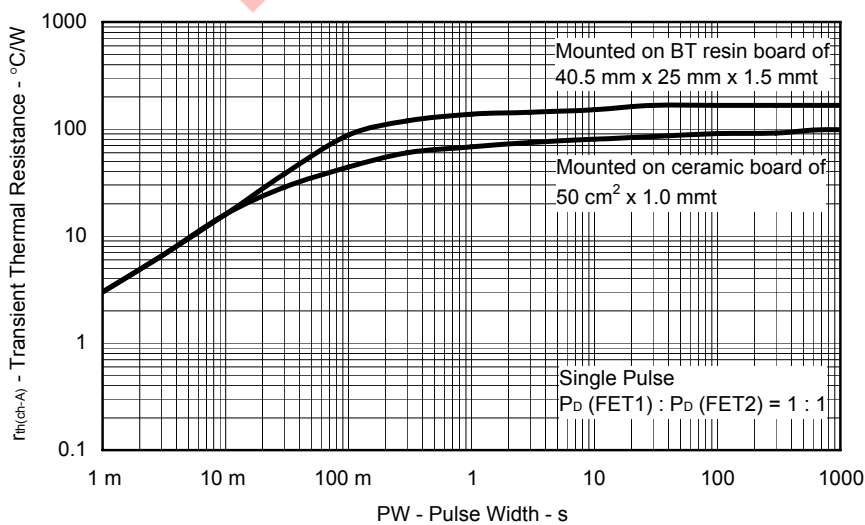
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



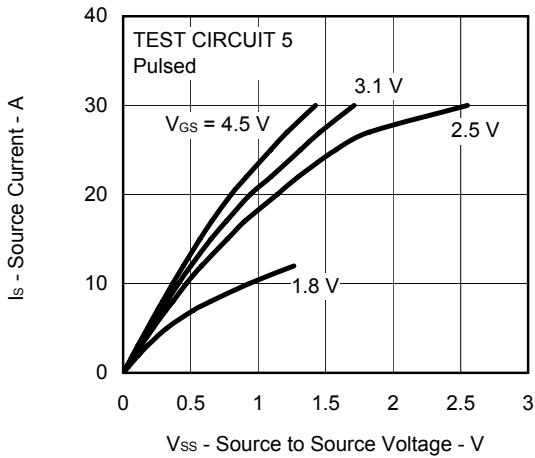
FORWARD BIAS SAFE OPERATING AREA



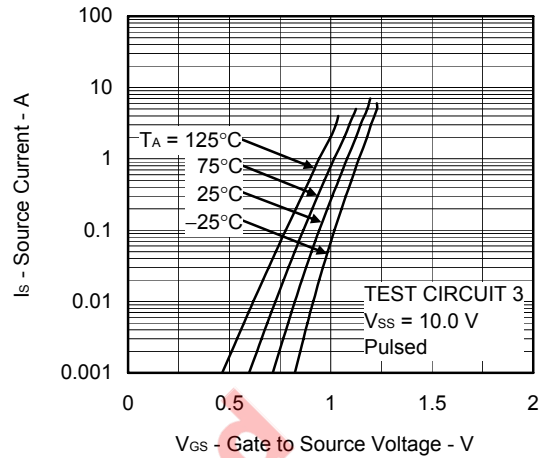
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



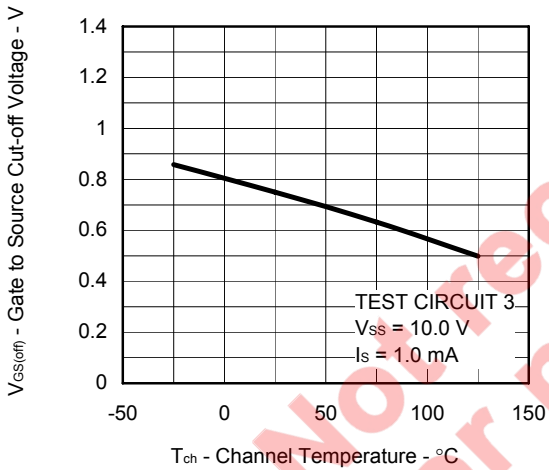
SOURCE CURRENT vs. SOURCE TO SOURCE VOLTAGE



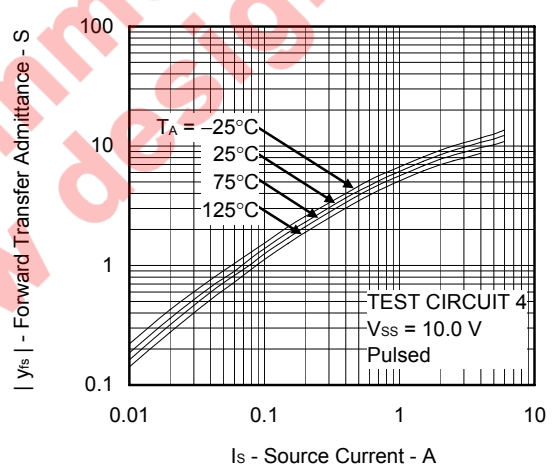
FORWARD TRANSFER CHARACTERISTICS



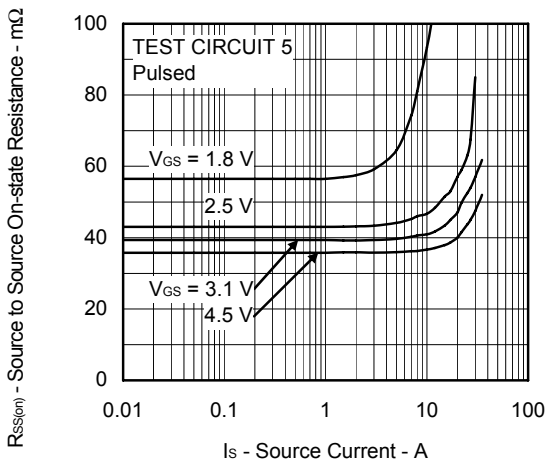
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



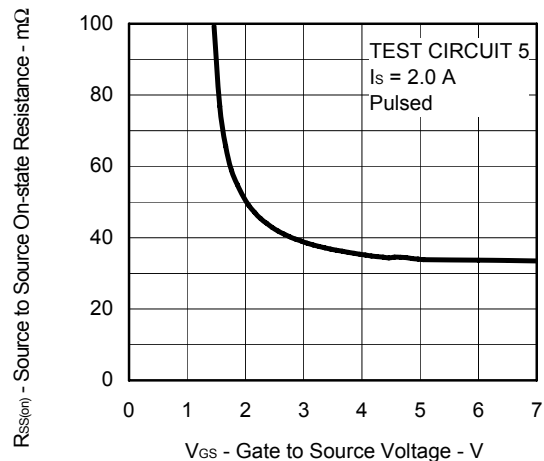
FORWARD TRANSFER ADMITTANCE vs. SOURCE CURRENT



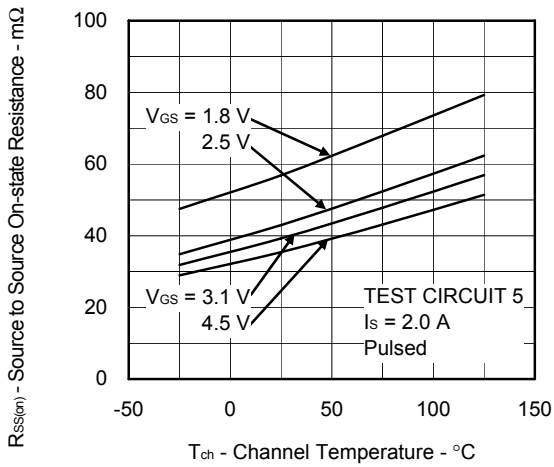
SOURCE TO SOURCE ON-STATE RESISTANCE vs. SOURCE CURRENT



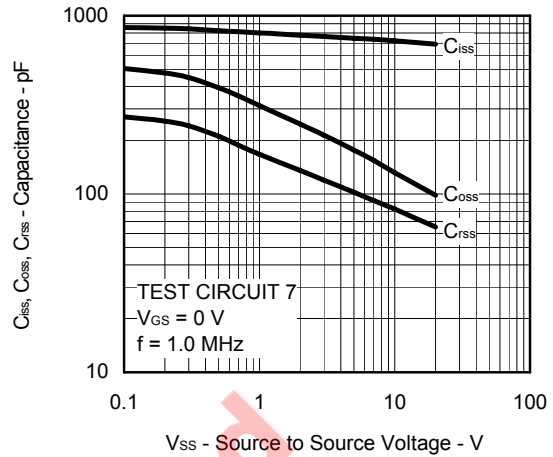
SOURCE TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



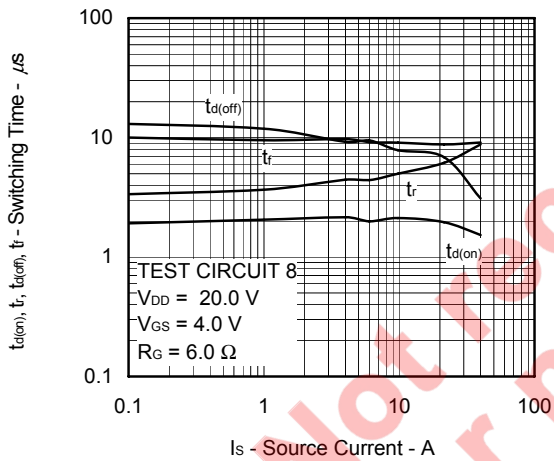
SOURCE TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



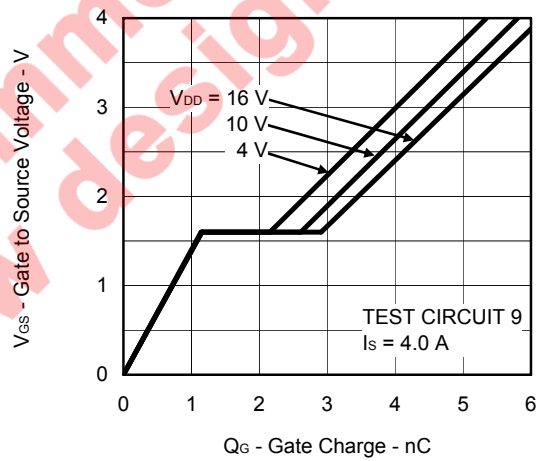
CAPACITANCE vs. SOURCE TO SOURCE VOLTAGE



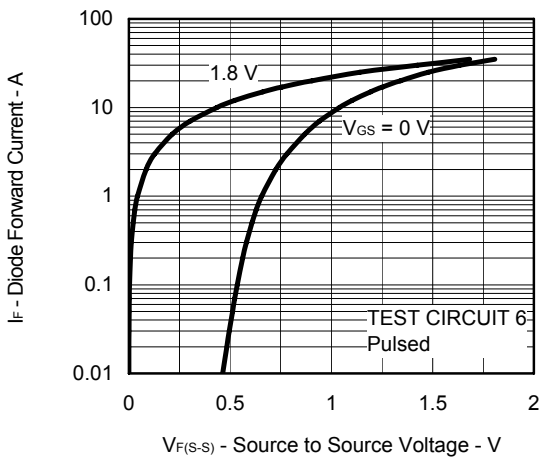
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS



SOURCE TO SOURCE DIODE FORWARD VOLTAGE



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