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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR μ PA2722UT1A

SWITCHING N-CHANNEL POWER MOSFET

DESCRIPTION

The μ PA2722UT1A is N-channel MOSFET designed for DC/DC converter applications.

FEATURES

Low on-state resistance

 $R_{DS(on)1} = 3.3 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 15 \text{ A})$

 $R_{DS(on)2} = 4.6 \text{ m}\Omega \text{ MAX}. \text{ (Vgs} = 4.5 \text{ V, Ip} = 15 \text{ A)}$

- Thin type surface mount package with heat spreader (8-pin HVSON)
- RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (V _{GS} = 0 V)	Voss	30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC)	I _{D(DC)}	±29	Α
Drain Current (pulse) Note1	ID(pulse)	±170	Α
Total Power Dissipation Note2	P _{T1}	1.5	W
Total Power Dissipation (PW =10 sec) Note2	P _{T2}	4.6	W
Channel Temperature	Tch	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current Note3	las	29	Α
Single Avalanche Energy Note3	Eas	84	mJ

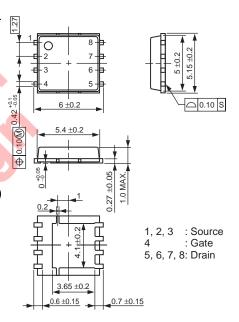
THERMAL RESISTANCE

Channel to Ambient Thermal Resistance Note2	Rth(ch-A)	83.3	°C/W
Channel to Case (Drain) Thermal Resistance	Rth(ch-C)	1.5	°C/W

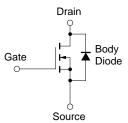
Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

- 2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm
- 3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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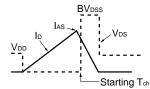
ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

	1	1			1	1
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 30 V, V _{GS} = 0 V			10	μΑ
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0		2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 15 A	13			S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10 V, I _D = 15 A		2.4	3.3	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 15 A		3.4	4.6	mΩ
Input Capacitance	Ciss	V _{DS} = 15 V,		6200		pF
Output Capacitance	Coss	V _{GS} = 0 V,		800		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		410		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 15 A,		31		ns
Rise Time	tr	V _{GS} = 10 V,		20		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		129		ns
Fall Time	tf			40		ns
Total Gate Charge	Q _G	V _{DD} = 15 V,		46		nC
Gate to Source Charge	Qgs	V _{GS} = 5 V,		17		nC
Gate to Drain Charge	Q _{GD}	I _D = 29 A		18		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 29 A, V _{GS} = 0 V		0.8		V
Reverse Recovery Time	trr	I _F = 29 A, V _{GS} = 0 V,		44		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		44		nC
Gate Resistance	Rg	f = 1 MHz		1.4		Ω

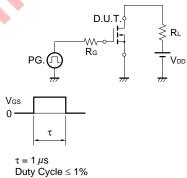
Note Pulsed

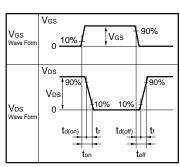
TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c} \text{D.U.T.} \\ \text{Rg} = 25 \ \Omega \\ \text{VGS} = 20 \rightarrow 0 \ \text{V} \end{array}$



TEST CIRCUIT 2 SWITCHING TIME



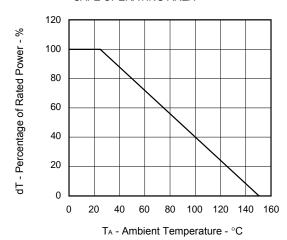


TEST CIRCUIT 3 GATE CHARGE

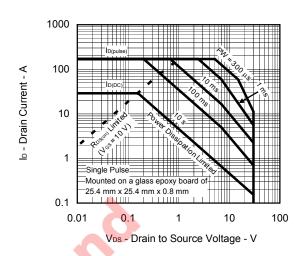
$$\begin{array}{c|c} D.U.T. \\ \hline \\ I_G = 2 \text{ mA} \\ \hline \\ \hline \\ \hline \\ \hline \\ \end{array} \begin{array}{c} R_L \\ \hline \\ V_{DD} \end{array}$$

<R> TYPICAL CHARACTERISTICS (TA = 25°C)

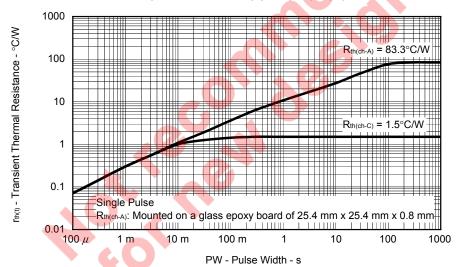
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



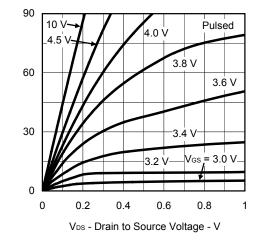
FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

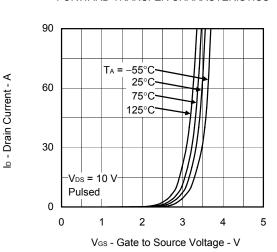


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

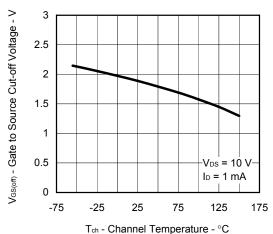


lo - Drain Current - A

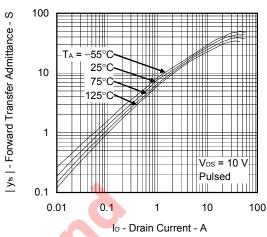
FORWARD TRANSFER CHARACTERISTICS



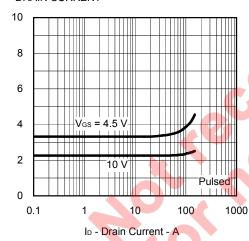
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



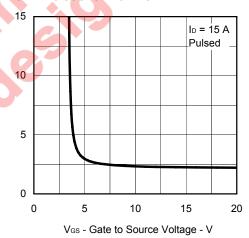
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



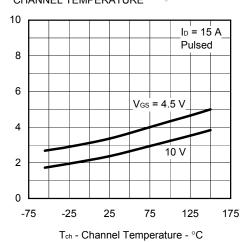
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



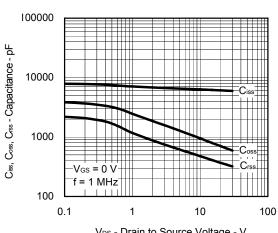
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



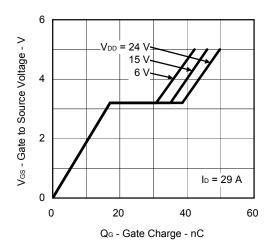
VDS - Drain to Source Voltage - V

R_{DS(on)} - Drain to Source On-state Resistance - mΩ

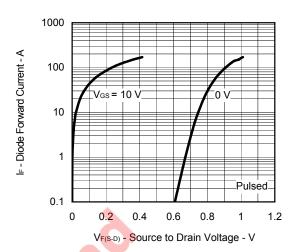
 $\mathsf{R}_{\mathsf{DS}(\varpi)}$ - Drain to Source On-state Resistance - $m\Omega$

RDS(on) - Drain to Source On-state Resistance - mΩ

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μPA2722UT1A-E1-AZ Note	Co. Di		
μPA2722UT1A-E2-AZ Note	Sn-Bi	Tana 2000 n/mal	8-pin HVSON
μPA2722UT1A-E1-AY Note	Dura Ca	Tape 3000 p/reel	0.10 g TYP.
μPA2722UT1A-E2-AY Note	Pure Sn		

Note Pb-free (This product does not contain Pb in the external electrode.)

 μ PA2722UT1A

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