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# MOS FIELD EFFECT TRANSISTOR $\mu$ PA2723UT1A

# SWITCHING N-CHANNEL POWER MOSFET

#### **DESCRIPTION**

The  $\mu$ PA2723UT1A is N-channel MOSFET designed for low side device of synchronous rectifier DC/DC converter.

#### **FEATURES**

• Low on-state resistance

 $R_{DS(on)1}$  = 2.5  $m\Omega$  MAX. (Vgs = 10 V, Ip = 17 A)

 $R_{DS(on)2} = 3.5 \text{ m}\Omega \text{ MAX.} \text{ (V}_{GS} = 4.5 \text{ V}, I_{D} = 17 \text{ A})$ 

- Thin type surface mount package with heat spreader (8-pin HVSON)
- RoHS Compliant

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

| Drain to Source Voltage (V <sub>GS</sub> = 0 V) | VDSS               | 30          | V  |
|---|--------------------|-------------|----|
| Gate to Source Voltage (V <sub>DS</sub> = 0 V)  | Vgss               | ±20         | V  |
| Drain Current (DC)                              | I <sub>D(DC)</sub> | ±33         | Α  |
| Drain Current (pulse) Note1                     | D(pulse)           | ±200        | Α  |
| Total Power Dissipation Note2                   | P <sub>T1</sub>    | 1.5         | W  |
| Total Power Dissipation (PW =10 sec) Note2      | P <sub>T2</sub>    | 4.6         | W  |
| Channel Temperature                             | Tch                | 150         | °C |
| Storage Temperature                             | Tstg               | -55 to +150 | °C |
| Single Avalanche Current Note3                  | las                | 33          | Α  |
| Single Avalanche Energy Note3                   | Eas                | 109         | mJ |
|   |                    |             |    |

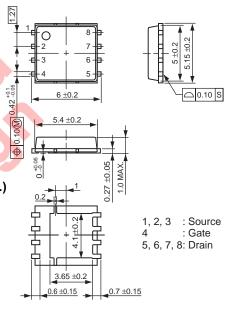
#### THERMAL RESISTANCE

| Channel to Ambient Thermal Resistance Note2 | Rth(ch-A) | 83.3 | °C/W |
|---|-----------|------|------|
| Channel to Case (Drain) Thermal Resistance  | Rth(ch-C) | 1.5  | °C/W |

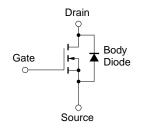
**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

- 2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm
- 3. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 15 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V, L = 100  $\mu$ H

#### PACKAGE DRAWING (Unit: mm)



#### **EQUIVALENT CIRCUIT**



**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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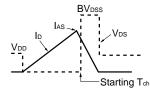
#### **ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)**

| CHARACTERISTICS                          | SYMBOL               | TEST CONDITIONS                                   | MIN. | TYP. | MAX. | UNIT |
|--|----------------------|---|------|------|------|------|
| Zero Gate Voltage Drain Current          | IDSS                 | V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V     |      |      | 10   | μA   |
| Gate Leakage Current                     | Igss                 | $V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$ |      |      | ±100 | nA   |
| Gate to Source Cut-off Voltage           | V <sub>GS(off)</sub> | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA     | 1.0  |      | 2.5  | V    |
| Forward Transfer Admittance Note         | yfs                  | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 17 A     | 17   |      |      | S    |
| Drain to Source On-state Resistance Note | RDS(on)1             | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 17 A     |      | 1.9  | 2.5  | mΩ   |
|  | RDS(on)2             | V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 17 A    |      | 2.6  | 3.5  | mΩ   |
| Input Capacitance                        | Ciss                 | V <sub>DS</sub> = 10 V,                           |      | 8100 |      | pF   |
| Output Capacitance                       | Coss                 | V <sub>GS</sub> = 0 V,                            |      | 1290 |      | pF   |
| Reverse Transfer Capacitance             | Crss                 | f = 1 MHz   |      | 610  |      | pF   |
| Turn-on Delay Time                       | t <sub>d(on)</sub>   | V <sub>DD</sub> = 15 V, I <sub>D</sub> = 17 A,    |      | 30   |      | ns   |
| Rise Time                                | <b>t</b> r           | V <sub>GS</sub> = 10 V,                           |      | 40   |      | ns   |
| Turn-off Delay Time                      | t <sub>d(off)</sub>  | R <sub>G</sub> = 10 Ω                             |      | 160  |      | ns   |
| Fall Time                                | t <sub>f</sub>       |   |      | 55   |      | ns   |
| Total Gate Charge                        | Q <sub>G</sub>       | V <sub>DD</sub> = 15 V,                           |      | 64   |      | nC   |
| Gate to Source Charge                    | QGS                  | V <sub>GS</sub> = 5 V,                            |      | 19   |      | nC   |
| Gate to Drain Charge                     | Q <sub>GD</sub>      | ID = 33 A   |      | 24   |      | nC   |
| Body Diode Forward Voltage Note          | V <sub>F(S-D)</sub>  | I <sub>F</sub> = 33 A, V <sub>GS</sub> = 0 V      |      | 0.76 |      | V    |
| Reverse Recovery Time                    | trr                  | I <sub>F</sub> = 33 A, V <sub>GS</sub> = 0 V,     |      | 55   |      | ns   |
| Reverse Recovery Charge                  | Qrr                  | di/dt = 100 A/μs                                  |      | 66   |      | nC   |
| Gate Resistance                          | RG                   | f = 1 MHz   |      | 1.4  |      | Ω    |

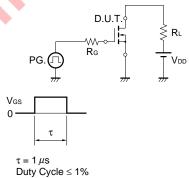
Note Pulsed

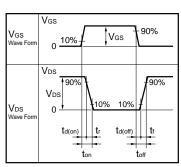
#### TEST CIRCUIT 1 AVALANCHE CAPABILITY

# $\begin{array}{c|c} D.U.T. \\ \hline RG = 25 \ \Omega \\ \hline VOD \\ \hline VOS = 20 \rightarrow 0 \ V \end{array}$



#### TEST CIRCUIT 2 SWITCHING TIME



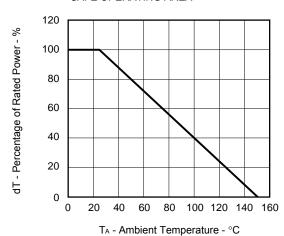


#### **TEST CIRCUIT 3 GATE CHARGE**

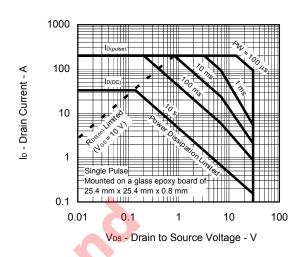
$$\begin{array}{c|c} D.U.T. \\ \hline \\ I_G = 2 \text{ mA} \\ \hline \\ \hline \\ \hline \\ \hline \\ \end{array} \begin{array}{c} R_L \\ \hline \\ V_{DD} \end{array}$$

#### TYPICAL CHARACTERISTICS (TA = 25°C)

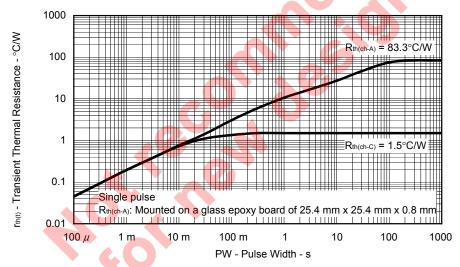
#### DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



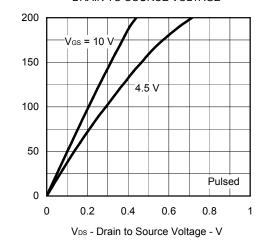
#### FORWARD BIAS SAFE OPERATING AREA



#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

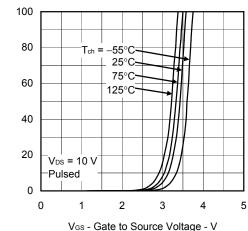


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



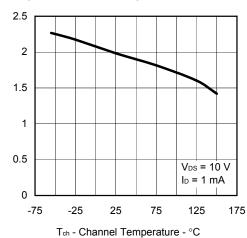
lo - Drain Current - A

#### FORWARD TRANSFER CHARACTERISTICS

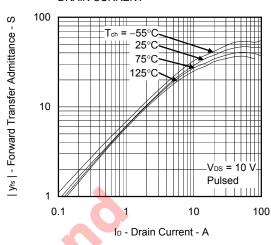


VGS(off) - Gate to Source Cut-off Voltage - V

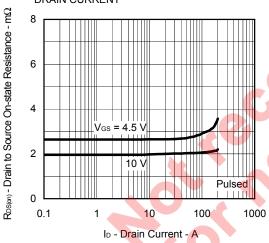
# GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



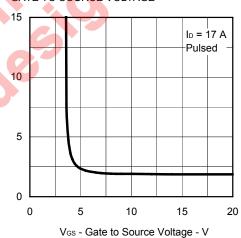
# FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



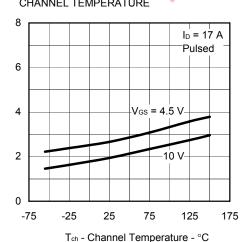
## DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



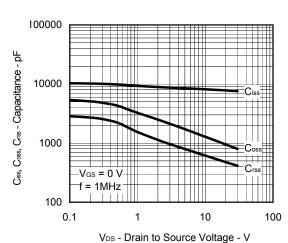
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



# DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



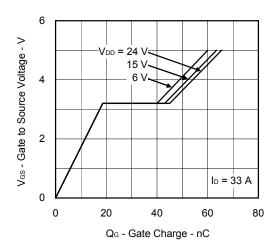
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



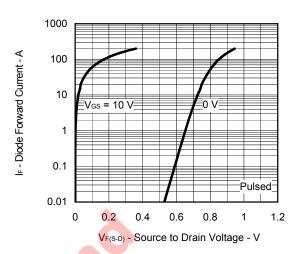
RDS(cn) - Drain to Source On-state Resistance - m\Omega

RDS(on) - Drain to Source On-state Resistance - m

#### DYNAMIC INPUT/OUTPUT CHARACTERISTICS



#### SOURCE TO DRAIN DIODE FORWARD VOLTAGE



#### **ORDERING INFORMATION**

| PART NUMBER            | LEAD PLATING | PACKING          | PACKAGE     |
|------------------------|--------------|------------------|-------------|
| μPA2723UT1A-E1-AZ Note | C- D:        |                  |             |
| μPA2723UT1A-E2-AZ Note | Sn-Bi        | Tana 2000 n/masl | 8-pin HVSON |
| μPA2723UT1A-E1-AY Note | D O.         | Tape 3000 p/reel | 0.10 g TYP. |
| μPA2723UT1A-E2-AY Note | Pure Sn      | 0                |             |

Note Pb-free (This product does not contain Pb in the external electrode.)

 $\mu$ PA2723UT1A

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