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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended
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MOS FIELD EFFECT TRANSISTOR
 μ PA2724UT1A

SWITCHING
 N-CHANNEL POWER MOSFET

DESCRIPTION

The μ PA2724UT1A is N-channel MOSFET designed for DC/DC converter applications.

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 3.3 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 15 \text{ A)}$
 $R_{DS(on)2} = 5.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 15 \text{ A)}$
- Low input capacitance
 $C_{iss} = 4400 \text{ pF TYP. (} V_{DS} = 15 \text{ V, } V_{GS} = 0 \text{ V)}$
- Thin type surface mount package with heat spreader (8-pin HVSON)
- RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 29	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 170	A
Total Power Dissipation ^{Note2}	P_{T1}	1.5	W
Total Power Dissipation ($PW = 10 \text{ sec}$) ^{Note2}	P_{T2}	4.6	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	29	A
Single Avalanche Energy ^{Note3}	E_{AS}	84	mJ

THERMAL RESISTANCE

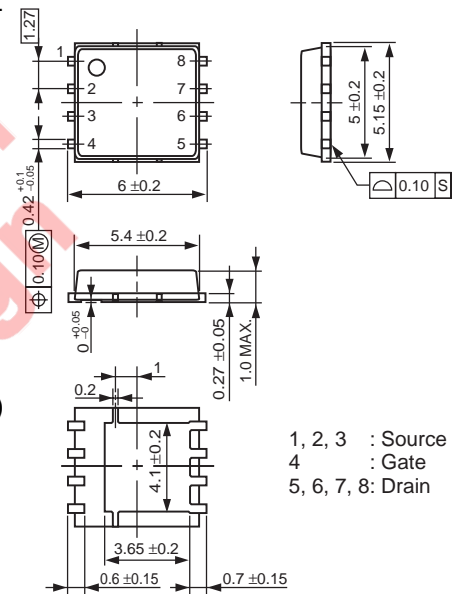
Channel to Ambient Thermal Resistance ^{Note2}	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$
Channel to Case (Drain) Thermal Resistance	$R_{th(ch-C)}$	1.5	$^\circ\text{C/W}$

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm
3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 15 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$, $L = 100 \mu\text{H}$

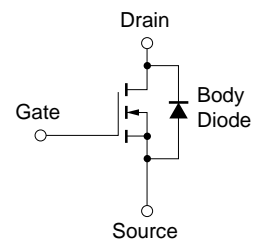
Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

PACKAGE DRAWING (Unit: mm)



1, 2, 3 : Source
 4 : Gate
 5, 6, 7, 8: Drain

EQUIVALENT CIRCUIT



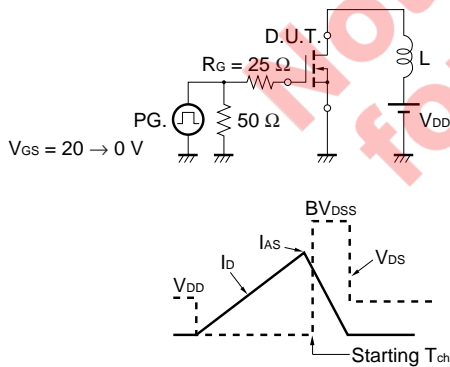
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ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

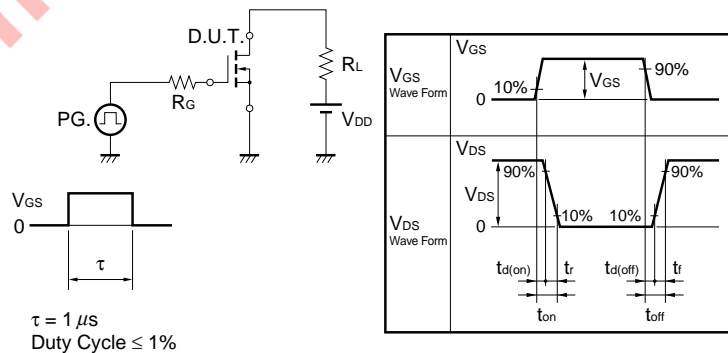
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			10	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			±100	nA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	1.5		2.5	V
Forward Transfer Admittance ^{Note}	$ y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 15\text{ A}$	13			S
Drain to Source On-state Resistance ^{Note}	$R_{DS(on)1}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		2.7	3.3	mΩ
	$R_{DS(on)2}$	$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$		3.7	5.0	mΩ
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V},$		4400		pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V},$		835		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1\text{ MHz}$		310		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, I_D = 15\text{ A},$		26		ns
Rise Time	t_r	$V_{GS} = 10\text{ V},$		9.4		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 10\ \Omega$		109		ns
Fall Time	t_f			28		ns
Total Gate Charge	Q_G	$V_{DD} = 15\text{ V},$		35		nC
Gate to Source Charge	Q_{GS}	$V_{GS} = 5\text{ V},$		13		nC
Gate to Drain Charge	Q_{GD}	$I_D = 29\text{ A}$		12		nC
Body Diode Forward Voltage ^{Note}	$V_{F(S-D)}$	$I_F = 29\text{ A}, V_{GS} = 0\text{ V}$		0.8		V
Reverse Recovery Time	t_{rr}	$I_F = 29\text{ A}, V_{GS} = 0\text{ V},$		42		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{ A}/\mu\text{s}$		43		nC
Gate Resistance	R_G	$f = 1\text{ MHz}$		1.8		Ω

Note Pulsed

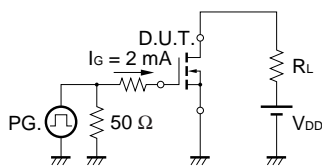
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

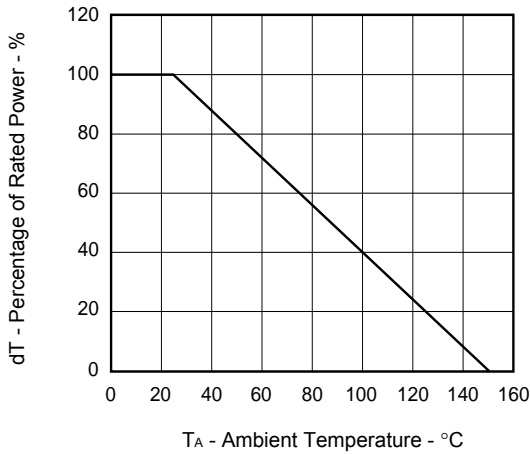


TEST CIRCUIT 3 GATE CHARGE

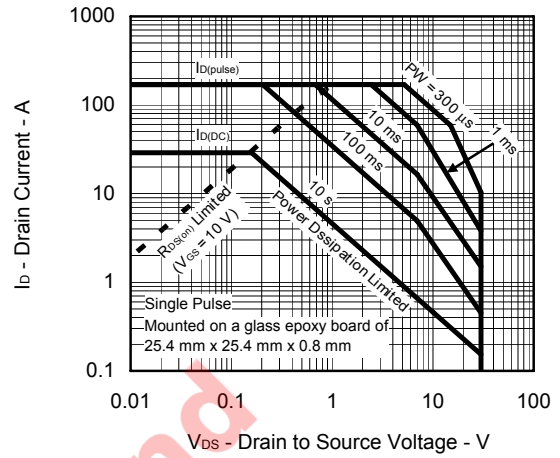


TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

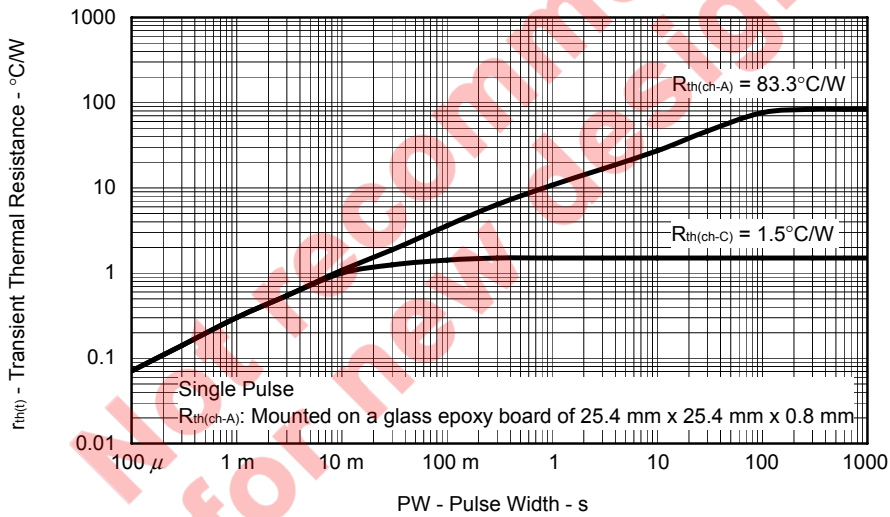
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



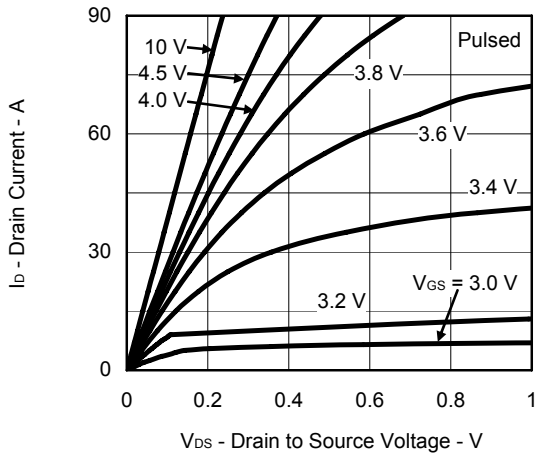
FORWARD BIAS SAFE OPERATING AREA



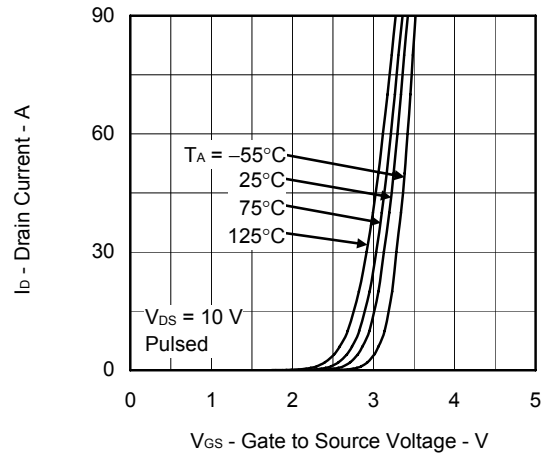
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

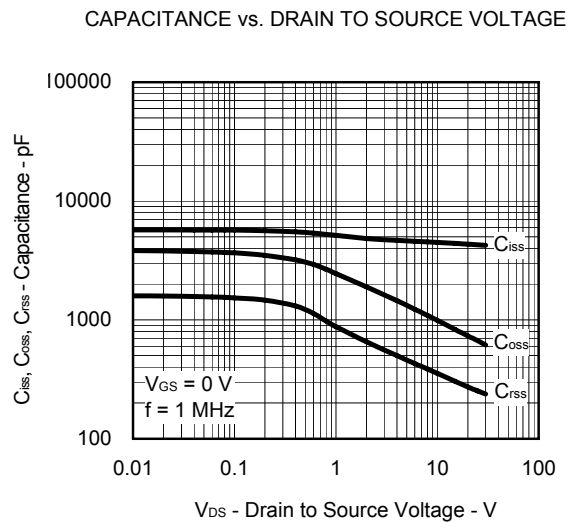
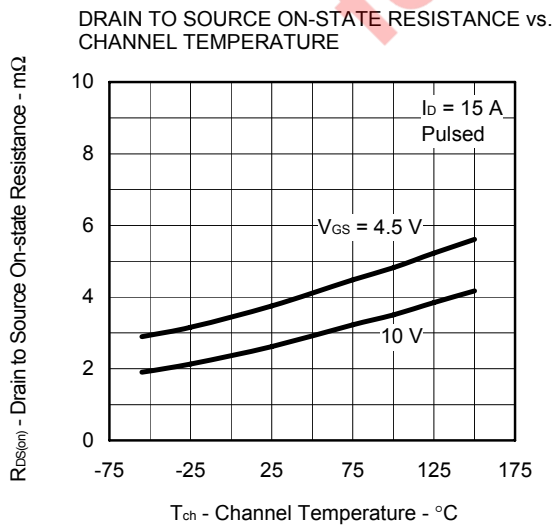
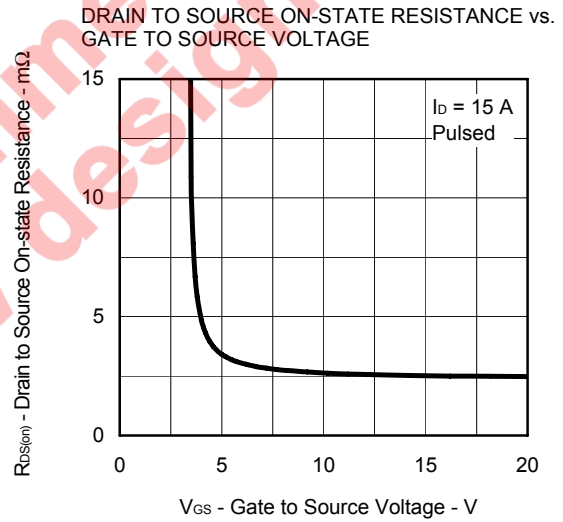
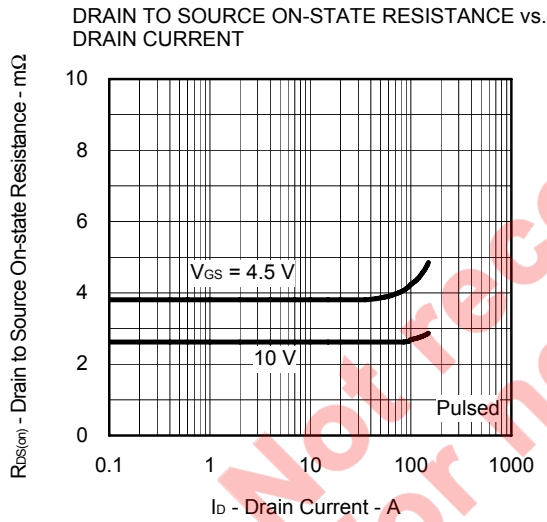
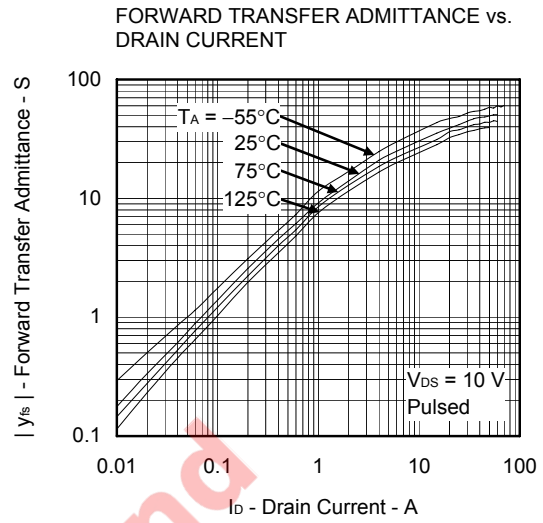
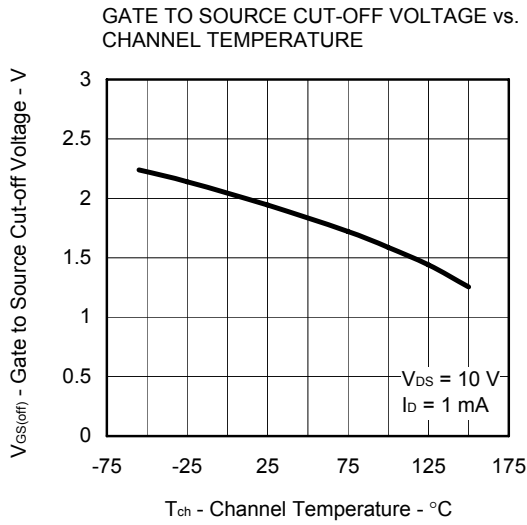


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

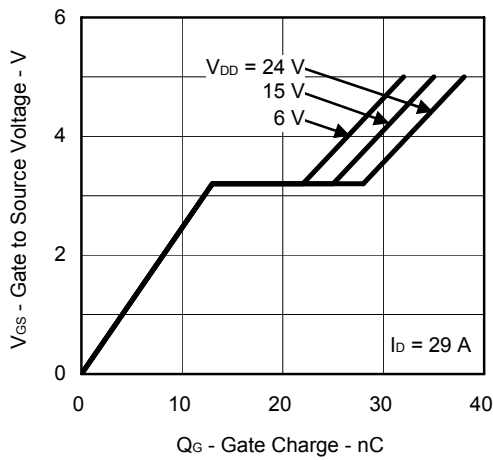


FORWARD TRANSFER CHARACTERISTICS

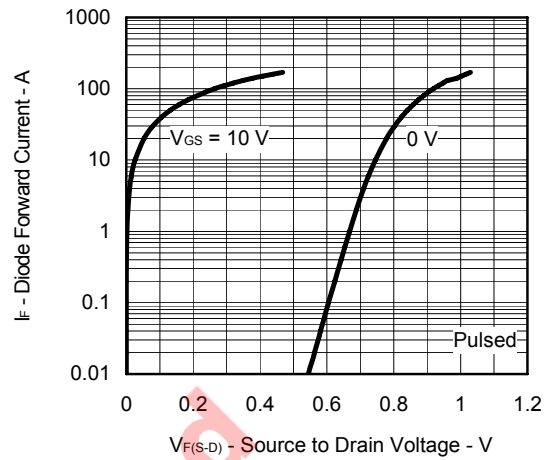




DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μ PA2724UT1A-E1-AZ <small>Note</small>	Sn-Bi	Tape 3000 p/reel	8-pin HVSON 0.10 g TYP.
μ PA2724UT1A-E2-AZ <small>Note</small>			
μ PA2724UT1A-E1-AY <small>Note</small>	Pure Sn		
μ PA2724UT1A-E2-AY <small>Note</small>			

Note Pb-free (This product does not contain Pb in the external electrode.)

Not recommended for new design

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