To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET

MOS FIELD EFFECT TRANSISTOR

μPA2725UT1A

SWITCHING
N-CHANNEL POWER MOSFET

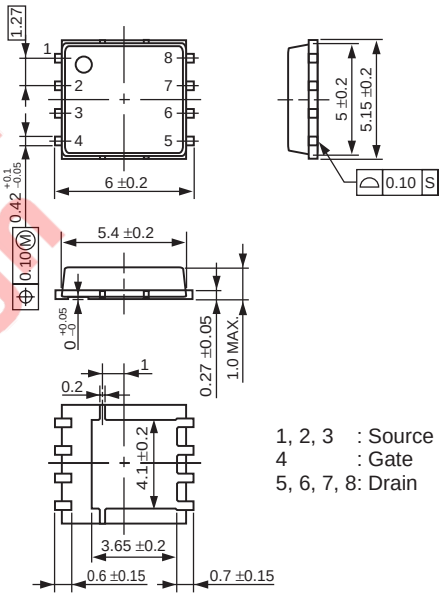
DESCRIPTION

The μPA2725UT1A is N-channel MOSFET designed for DC/DC converter applications.

FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 5.0 mΩ MAX. (V_{GS} = 10 V, I_D = 13 A)
  $R_{DS(on)2}$ = 7.5 mΩ MAX. (V_{GS} = 4.5 V, I_D = 13 A)
- Low input capacitance
  C_{iss} = 2580 pF TYP. (V_{DS} = 15 V, V_{GS} = 0 V)
- Thin type surface mount package with heat spreader (8-pin HVSON)
- RoHS Compliant

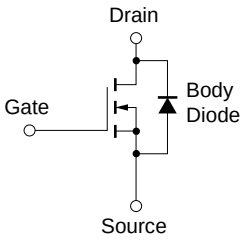
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±25	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±150	A
Total Power Dissipation Note2	P_{T1}	1.5	W
Total Power Dissipation (PW =10 sec) Note2	P_{T2}	4.6	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Single Avalanche Current Note3	I_{AS}	25	A
Single Avalanche Energy Note3	E_{AS}	62	mJ

EQUIVALENT CIRCUIT



THERMAL RESISTANCE

Channel to Ambient Thermal Resistance Note2	$R_{th(ch-A)}$	83.3	°C/W
Channel to Case (Drain) Thermal Resistance	$R_{th(ch-C)}$	1.5	°C/W

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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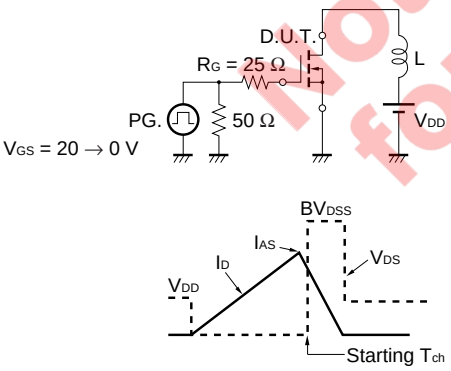
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

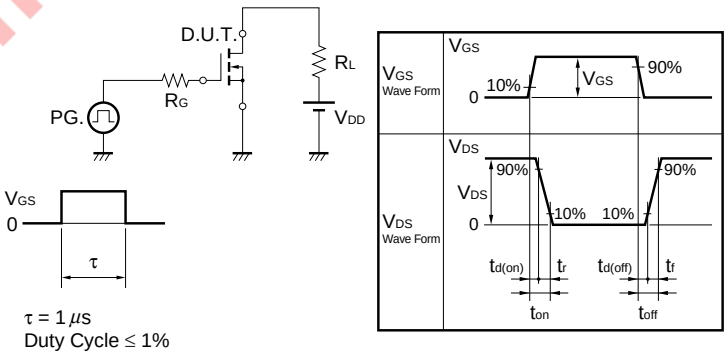
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5		2.5	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 13 A	9			S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 13 A		3.8	5.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 13 A		5.5	7.5	mΩ
Input Capacitance	C_{iss}	V_{DS} = 15 V,		2580		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		510		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		200		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 13 A,		17		ns
Rise Time	t_r	V_{GS} = 10 V,		13		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		74		ns
Fall Time	t_f			17		ns
Total Gate Charge	Q_G	V_{DD} = 15 V,		22		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 5 V,		7.3		nC
Gate to Drain Charge	Q_{GD}	I_D = 25 A		7.1		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 25 A, V_{GS} = 0 V		0.81		V
Reverse Recovery Time	t_{rr}	I_F = 25 A, V_{GS} = 0 V,		35		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		35		nC
Gate Resistance	R_G	f = 1 MHz		2.2		Ω

Note Pulsed

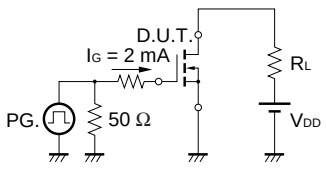
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

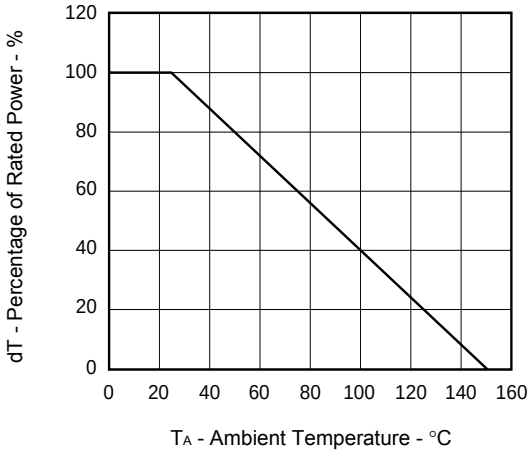


TEST CIRCUIT 3 GATE CHARGE

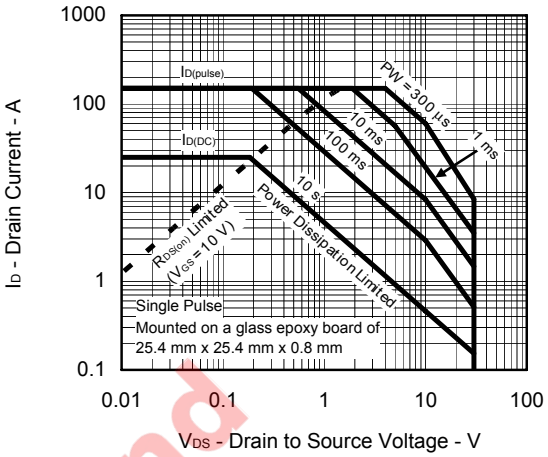


TYPICAL CHARACTERISTICS (T_A = 25°C)

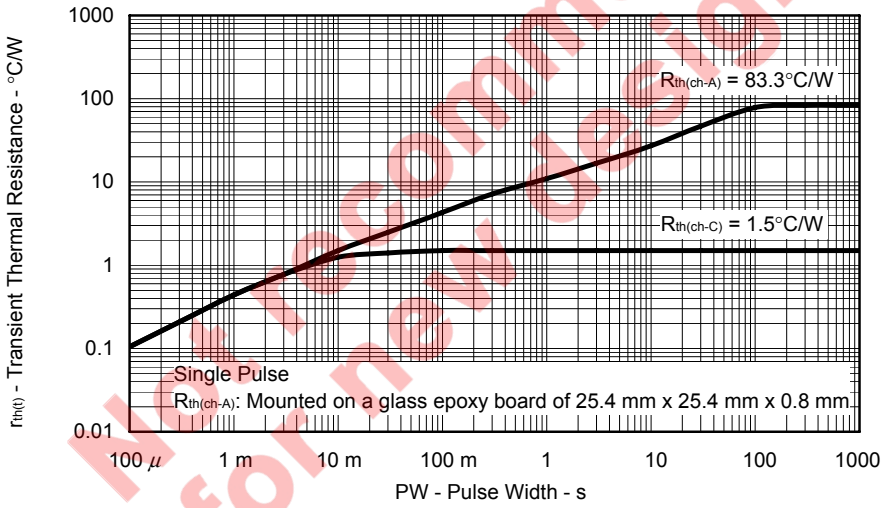
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



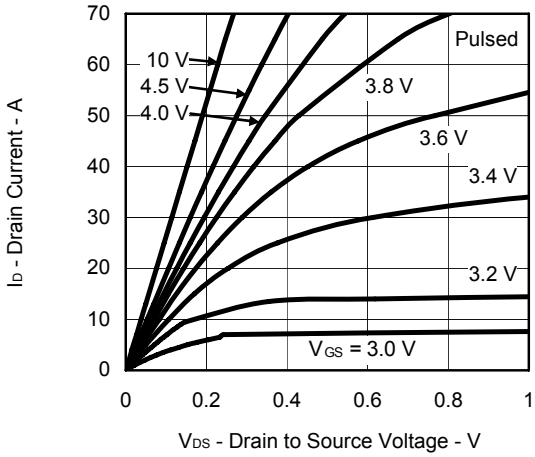
FORWARD BIAS SAFE OPERATING AREA



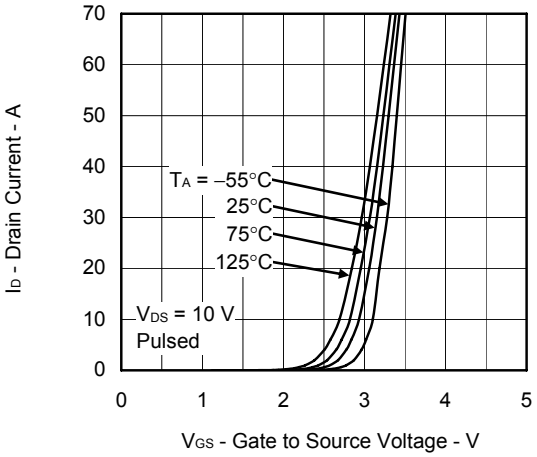
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



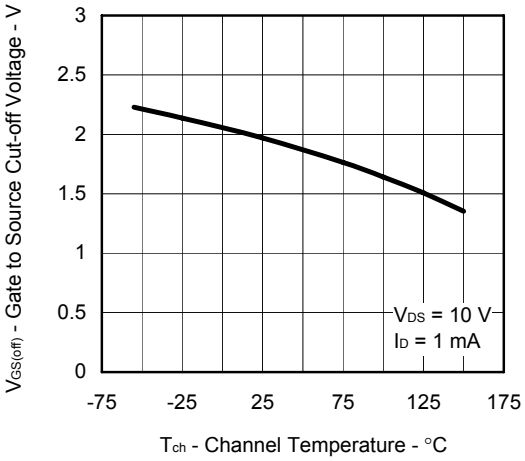
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



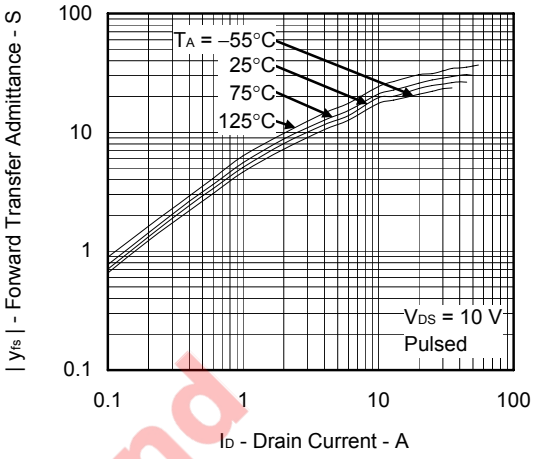
FORWARD TRANSFER CHARACTERISTICS



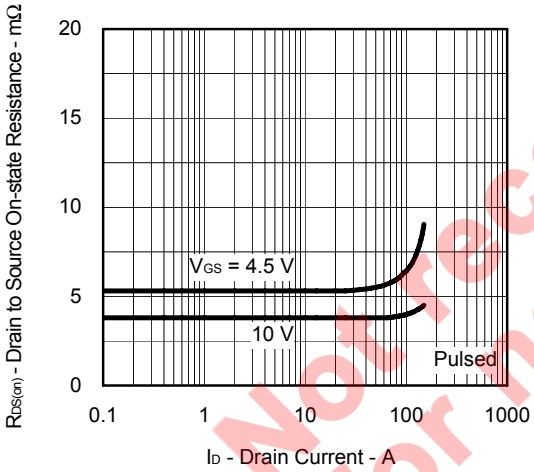
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



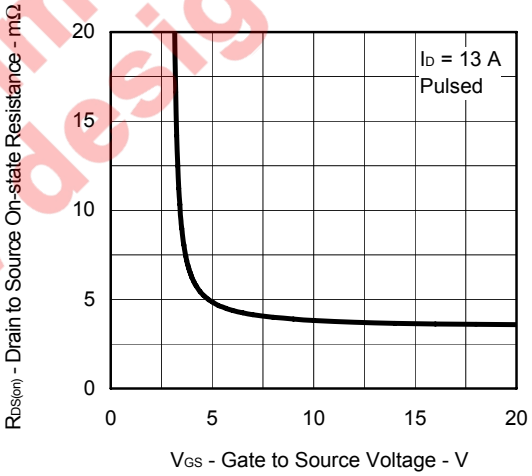
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



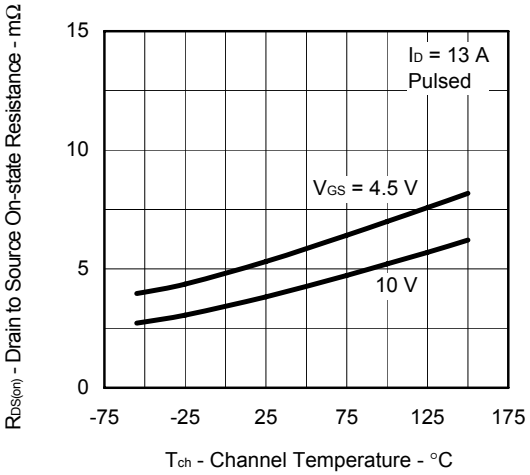
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



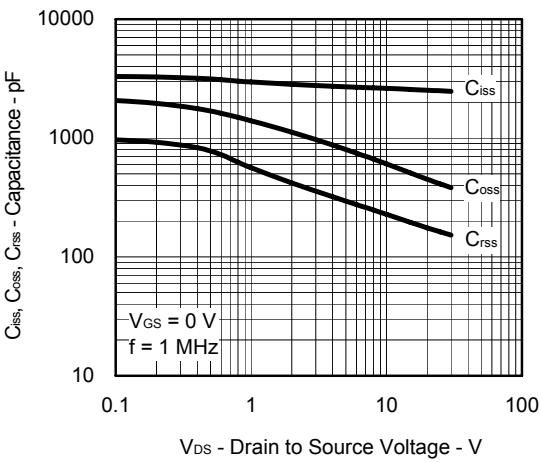
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



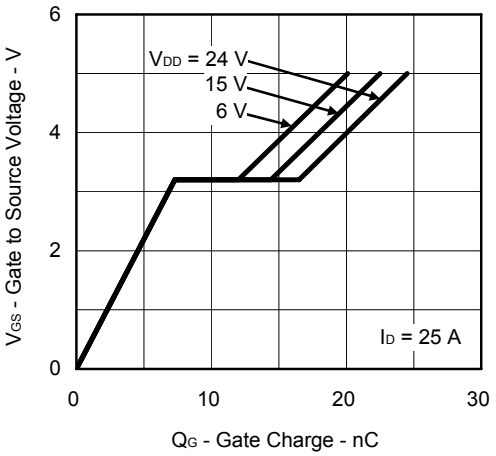
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



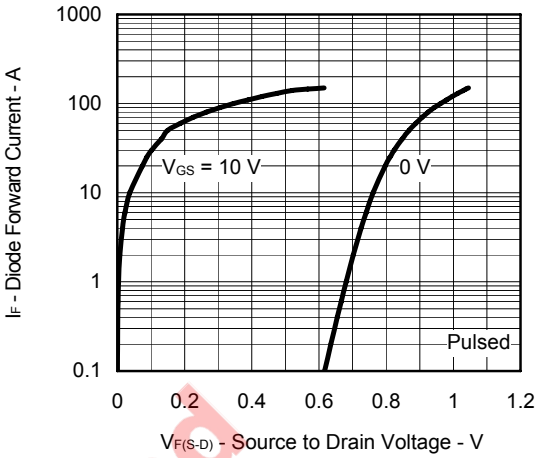
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μPA2725UT1A-E1-AZ Note	Sn-Bi	Tape 3000 p/reel	8-pin HVSON 0.10 g TYP.
μPA2725UT1A-E2-AZ Note			
μPA2725UT1A-E1-AY Note	Pure Sn		
μPA2725UT1A-E2-AY Note			

Note Pb-free (This product does not contain Pb in the external electrode.)

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