

# μ PA2762UGR

## MOS FIELD EFFECT TRANSISTOR

R07DS0011EJ0100

Rev.1.00

Jun 01, 2010

### Description

The μ PA2762UGR is N-Channel MOS Field Effect Transistor designed for power management applications of a notebook computer.

### Features

- Low on-state resistance
  - $R_{DS(on)1} = 13.5 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$ )
  - $R_{DS(on)2} = 22 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$ )
- Low Ciss:  $C_{iss} = 710 \text{ pF TYP.}$  ( $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}$ )
- Small and surface mount package (Power SOP8)
- RoHS Compliant

### Ordering Information

Part No.	LEAD PLATING	PACKING	Package
μ PA2762UGR-E1-AT *1	Pure Sn (Tin)	Tape 2500 p/reel	Power SOP8 0.08 g TYP.
μ PA2762UGR-E2-AT *1			

Note: \*1. Pb-free (This product does not contain Pb in external electrode and other parts.)

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ , All terminals are connected)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	30	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	±20	V
Drain Current (DC)	$I_{D(DC)}$	±12	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±50	A
Total Power Dissipation *2	$P_{T1}$	1.1	W
Total Power Dissipation (PW = 10 sec) *2	$P_{T2}$	2.5	W
Channel Temperature	$T_{ch}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C
Single Avalanche Current *3	$I_{AS}$	12	A
Single Avalanche Energy *3	$E_{AS}$	14.4	mJ

Notes: \*1.  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

\*2. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

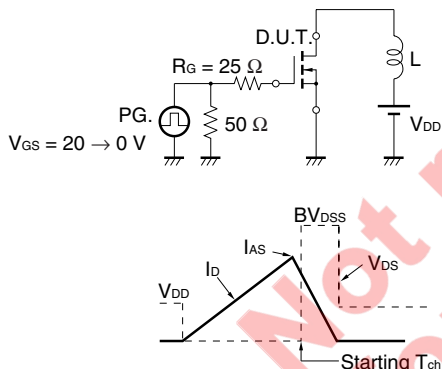
\*3. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 17.5 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$ ,  $L = 100 \mu\text{H}$

**Electrical Characteristics (T<sub>A</sub> = 25°C, All terminals are connected)**

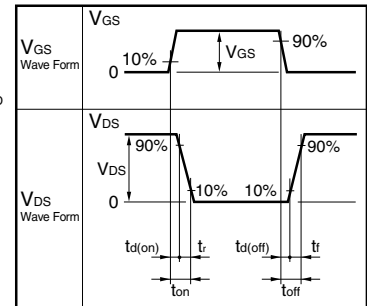
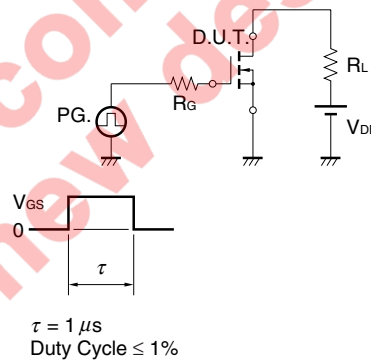
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μA	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>			±100	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V
Gate Cut-off Voltage	V <sub>GS(off)</sub>	1.0		2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance *1	y <sub>fs</sub>	3.5			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 6 A
Drain to Source On-state Resistance *1	R <sub>DS(on)1</sub>		11.0	13.5	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A
	R <sub>DS(on)2</sub>		15.8	22	mΩ	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A
Input Capacitance	C <sub>iss</sub>		710		pF	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz
Output Capacitance	C <sub>oss</sub>		120		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		71		pF	
Turn-on Delay Time	t <sub>d(on)</sub>		8.3		ns	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 6 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 10 Ω
Rise Time	t <sub>r</sub>		3.9		ns	
Turn-off Delay Time	t <sub>d(off)</sub>		28		ns	
Fall Time	t <sub>f</sub>		5.5		ns	
Total Gate Charge	Q <sub>G</sub>		6.2		nC	V <sub>DD</sub> = 15 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 12 A
Gate to Source Charge	Q <sub>GS</sub>		2.5		nC	
Gate to Drain Charge	Q <sub>GD</sub>		3.0		nC	
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>			1.2	V	I <sub>F</sub> = 12 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>		22		ns	I <sub>F</sub> = 12 A, V <sub>GS</sub> = 0 V,
Reverse Recovery Charge	Q <sub>rr</sub>		15		nC	di/dt = 100 A/μs

Note: \*1. Pulsed

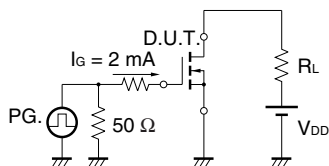
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

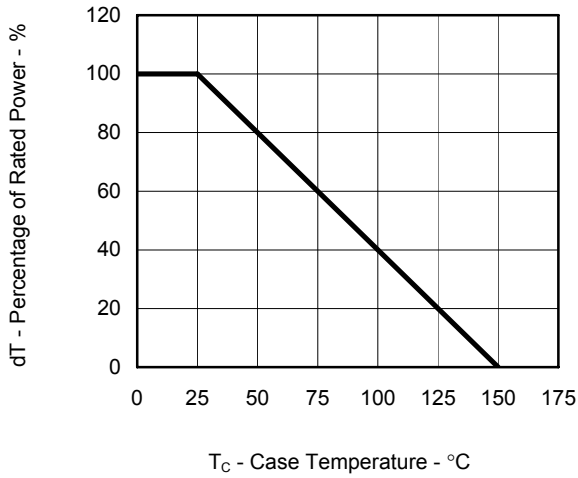


**TEST CIRCUIT 3 GATE CHARGE**

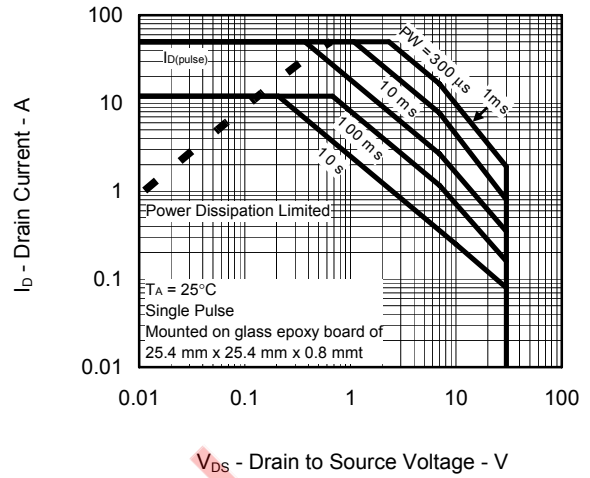


Typical Characteristics (T<sub>A</sub> = 25°C)

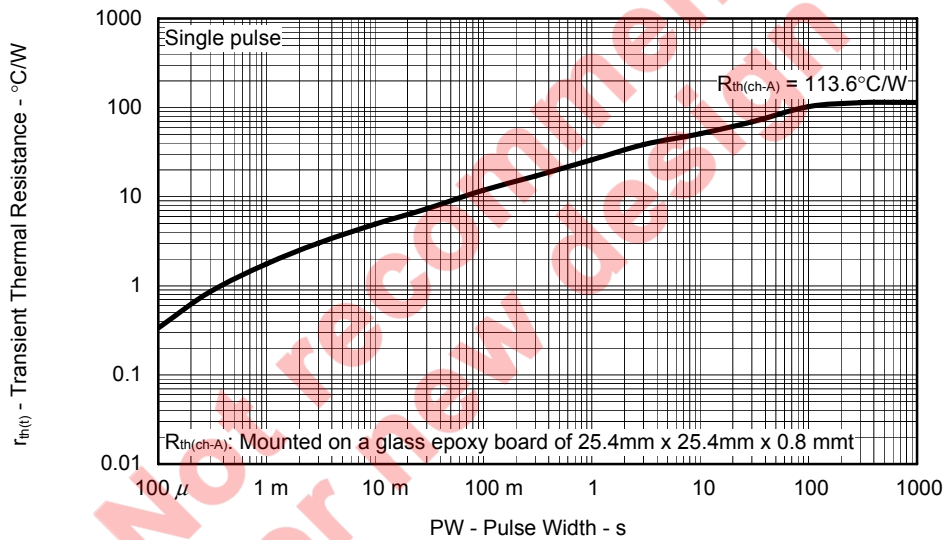
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



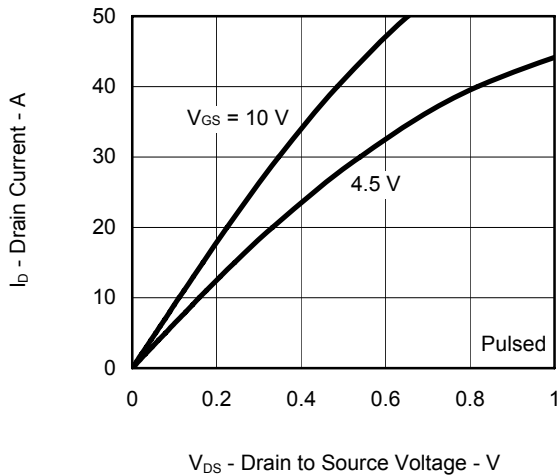
FORWARD BIAS SAFE OPERATING AREA



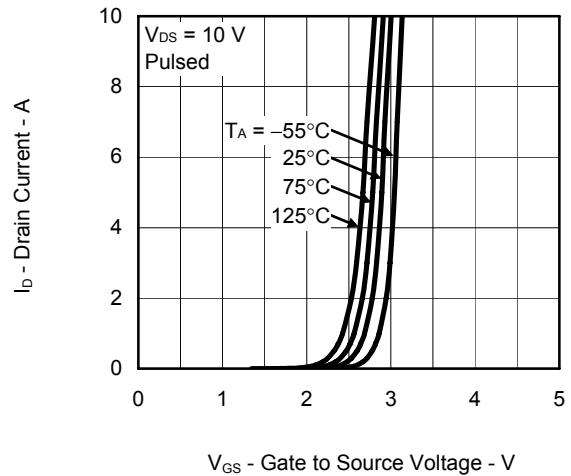
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



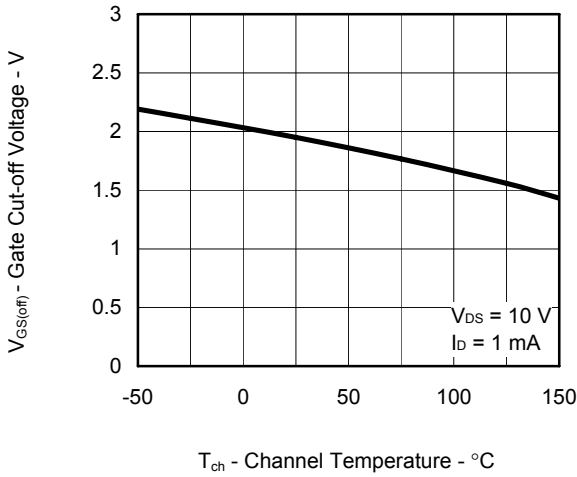
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



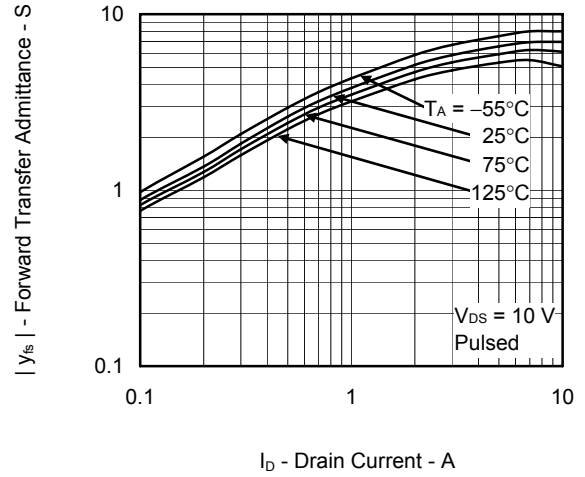
FORWARD TRANSFER CHARACTERISTICS



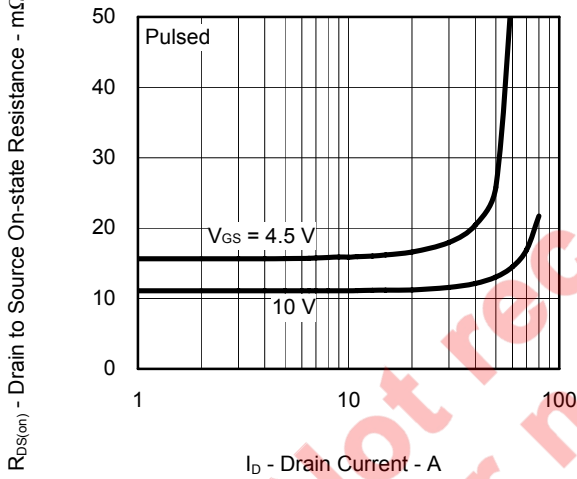
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



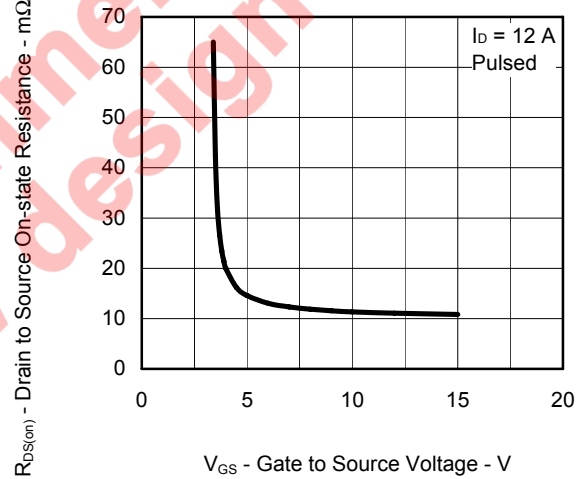
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



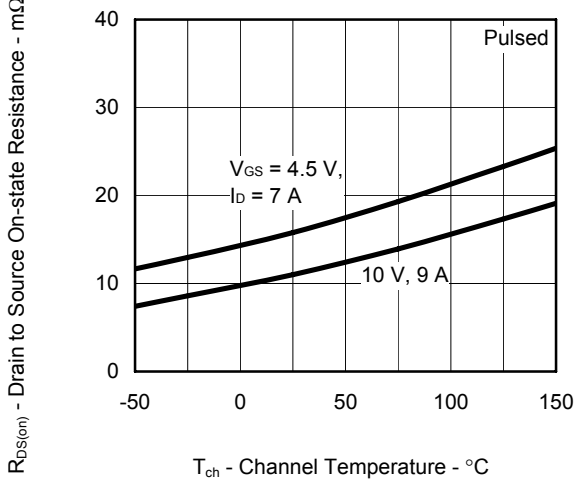
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



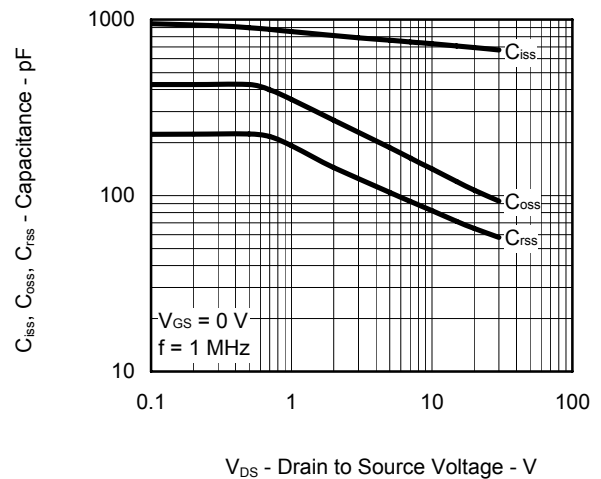
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



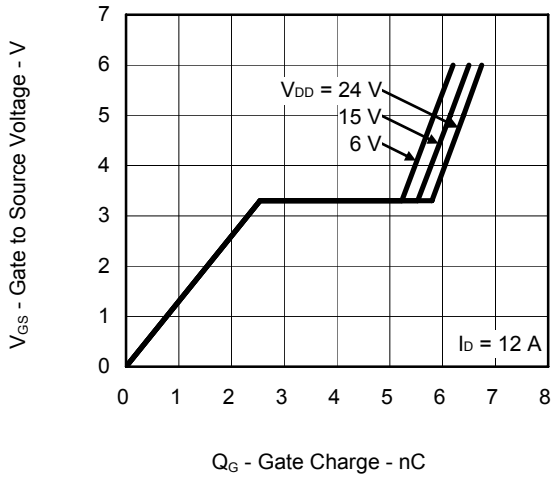
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



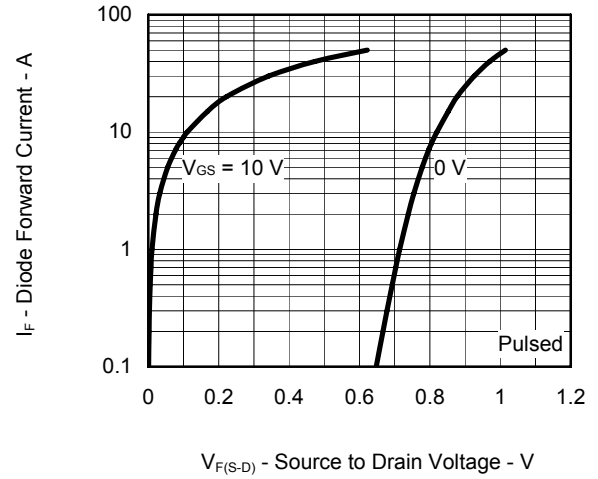
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT CHARACTERISTICS



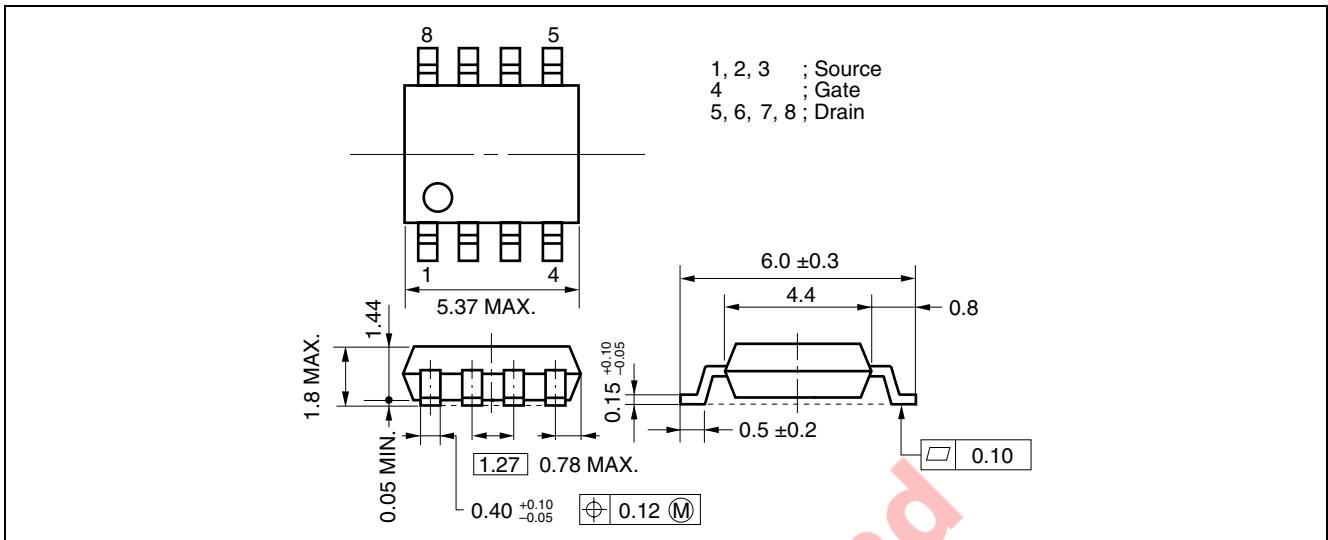
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



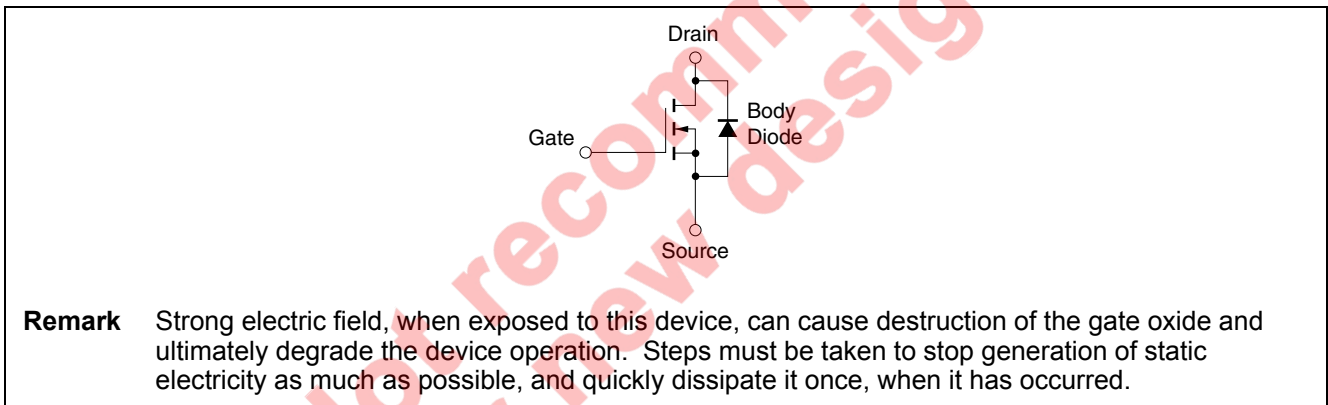
Not recommend  
for new design

### Package Drawings (Unit: mm)

#### Power SOP8



### Equivalent Circuit



<b>Revision History</b>	<b>μPA2762UGR</b>
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Rev.	Date	Description	
		Page	Summary
1.00	June 01, 2010	–	First Eddition Issued

**Not recommend  
for new design**

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