Product part number: SLG46400

Active SLG46400 Errata List

ISSUE 1: PIN2 Pull up

If the pull up on PIN 2 is used the input will be pulled to VDD only for 50-70% of VDD voltage (PIN is floating, depending on VDD value), while other PINs show up to 98% of VDD voltage.

Workaround:

- Use external pull up resistor on this PIN
- Use another input PIN

ISSUE 2: ACMP Low Bandwidth

ACMP Low Bandwidth function does not operate at VDD > 1.8 V

Workaround:

- There is no possible workaround for this issue. The chip needs to be supplied with not more than 1.8 V to make this option operational.
- Use SLG46400 Rev. B chips.

ISSUE 3: Internal RC OSC frequency variation

For higher internal RC OSC frequency options the frequency variation from chip to chip and per PVT can be bigger than 25%.

Workaround:

- Use SLG46400 Rev. B chips.

ISSUE 4: Internal RC OSC frequency difference

The SLG46400 Rev. B chips have difference in internal RC OSC frequency options. For example, reg<586:583> = 0000b option will set the RC OSC to 28.93kHz at VDD=3.3V in SLG46400 Rev. B chips and 27.74kHz in SLG46400 Rev. A chips, reg<586:583> = 0011b option will set the RC OSC to 122.3kHz at VDD=3.3V in SLG46400 Rev. B chips and 308.27kHz in SLG46400 Rev. A chips.

Workaround:

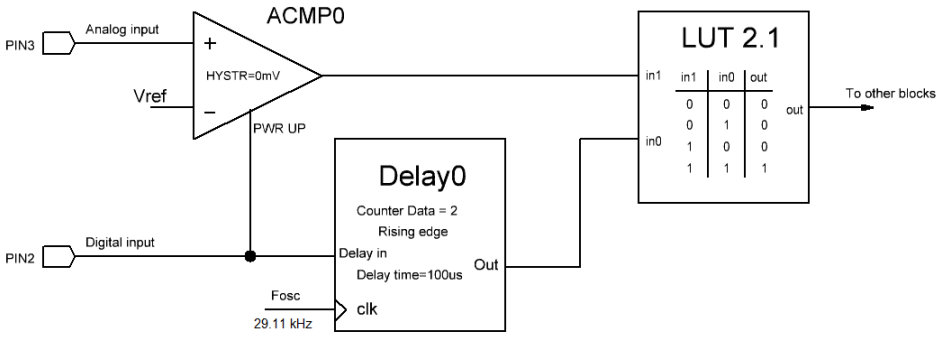
- Recalculate Counter Data for Counter/Delay blocks.
- Choose another frequency option from the list.

ISSUE 5: ACMP dynamic on/off glitches

ACMP will have glitches on its output after being turned on during 100us maximum.

Workaround:

- Use 100us Deglitch Delay on the ACMP output (typically 100us both edges delay) or make a system of 100us rising edge Delay block and LUT to reject the ACMP output for 100us after its power up (See example below)



ISSUE 6: Glitches on ACMP output on VDD fluctuation

Glitches on the ACMP output can appear when the difference between IN+ and IN- is less than 50mV, auto power detector power control mode is used and VDD value passes the internal Power Detector threshold with slew rate bigger than 0.5V/ms.

Workaround:

- Change VDD ramp slew rate to be less than 0.5V/ms in combination with SLG46400 Rev. B chips.

ISSUE 7: Improper use of PGA output as ACMP0 input

PGA output cannot be used as ACMP input for input voltage bigger than 1V due to the ADC PGA limitation. If the input voltage is bigger than 1V, the ACMP output can have glitches during the ADC turn on.

Workaround:

- Apply voltage less than 1V.
- Use SLG46400 Rev. B chips with ACMP input from PGA input option.

ISSUE 8: Incorrect first ADC sample.

In some cases the first ADC sample can be incorrect.

Workaround:

- Rejection of the first ADC sample after it is turned on is recommended. If the internal RC OSC is used to clock ADC, the Delay block configured to have Counter Data > 1024 together with logical blocks can be used to reject the first ADC sample.

ISSUE 9: Delay block switch output without delay

Delay blocks can switch its output without delay if the input is pulse shorter than 30ns.

Workaround:

- Avoid using very short pulses.
- Use two delays in series, where first delay time is very small compared to the second delay. The second delay will never fail because the first delay will filter short pulses.

ISSUE 10: Incorrect ADC serial data

In some cases the ADC serial data can be incorrect for 1 out of 10000 samples in previous silicon revisions.

Workaround:

- Use up to date silicon

ISSUE 11: ADC data can’t reach 255

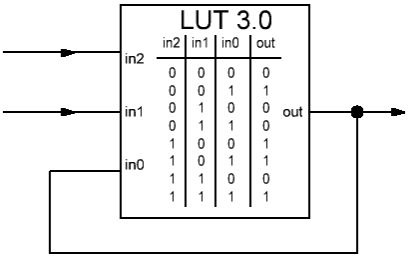
For VDD<2V and PGA Bypass to ADC mode the ADC data can’t reach 255 value

Workaround:

- Use external divider to shift the input voltage range, so the maximal voltage is less than 800mV.

ISSUE 12: LUT starts with output high when the feedback from its output to IN0 is used.

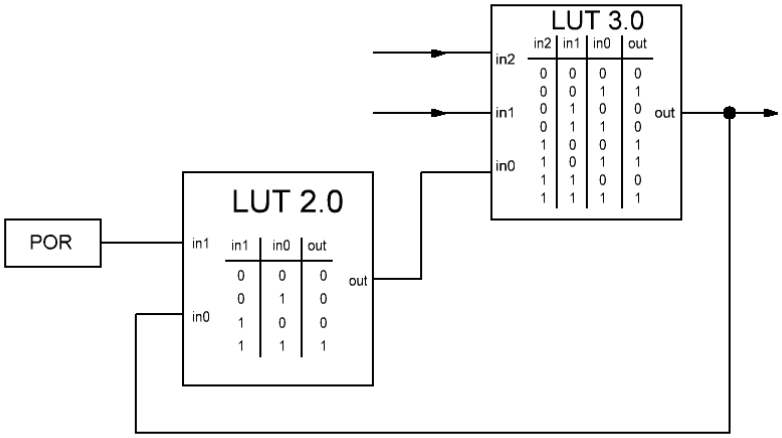
LUTs configured to have a feedback from its OUT to IN0 and truth table contains the situation, for 2-bit LUT IN1=0, IN0=1, OUT=1, for 3-bit LUT IN2=0, IN1=0, IN0=1, OUT=1, for 4-bit LUT IN3=0, IN2=0, IN1=0, IN0=1, OUT=1 can start with OUT HIGH (see example below).



- Incorrect

Workaround:

- Use another input for LUT, or add AND cell with POR as one of its inputs (see below).



ISSUE 13: Chip's operation is incorrect after startup

Chip can halt or configure improperly if the VDD low voltage is higher than 40mV.

Workaround:

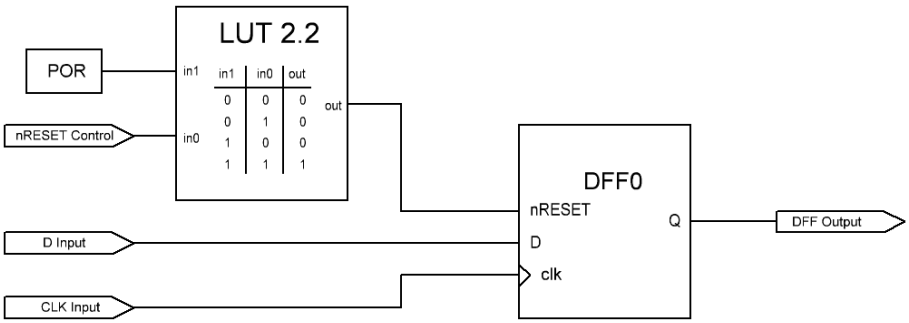
- Make sure the VDD rail should be discharged slower than 0.5V/ms before ramping back up.

ISSUE 14: DFF incorrect startup

DFFs with nREST/nSET can start (initialize) with different output states.

Workaround:

- Set DFF initial state before POR signal appears. Use similar connections as shown below



ISSUE 15: Can't detect 0V level using ADC

PGA unit on input of ADC has up to 20mV of internal offset. This does not allow to detect voltage lower than 20mV.

Workaround:

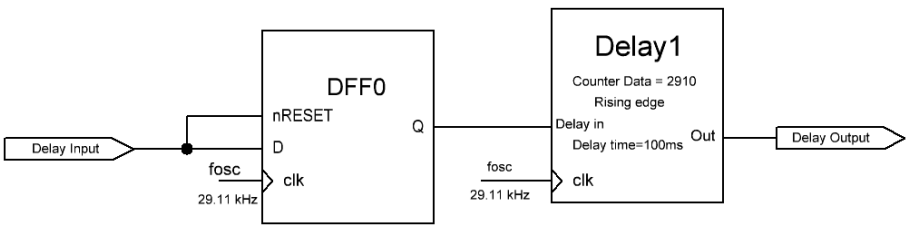
- Currently there is no workaround. Please do not use ADC for detection of voltages lower than 20mV.

ISSUE 16: Incorrect Delay time

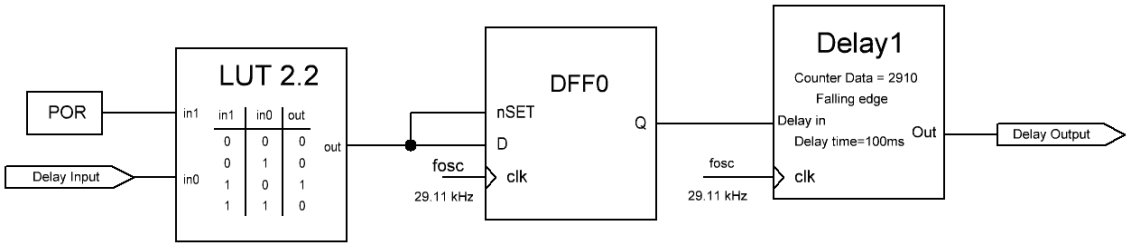
If the input edge of the Delay (or reset of Counter) is very close (<1ns) to the rising edge of the sourced clocking signal (RC OSC is Forced Power On or operating because another blocks request) the Counter/Delay cell might have incorrect Counter Data loaded.

Workaround:

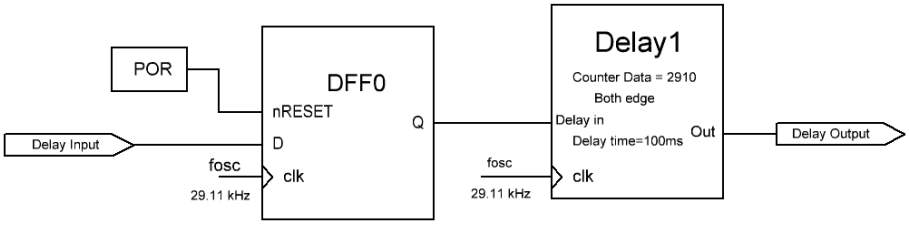
- Use synchronization block on the Counter/Delay input, similar to that shown below.
  In case of Rising Edge Delay:



In case of Falling Edge Delay:



In case of Both Edges Delay:



- Use two Delays in series, where the first delay has a much shorter delay time. In this case the second delay will never have this issue. The first delay time should be very small compared to the second one. It will not influence the total time much in case the first delay has loaded incorrect counter data.

ISSUE 17: LATCH0 and LATCH1 nSET or nRESET operation is incorrect

The nSET or nRESET functions of LATCH units operate incorrect. LATCH unit operates only when nSET/nRESET node is sourced with HIGH level signal.

Workaround:

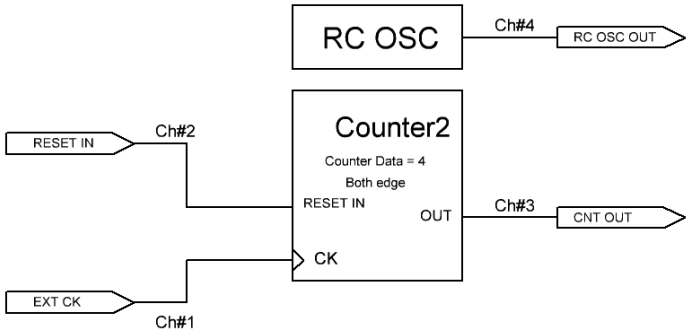
- Currently there is no workaround. Please see the truth tables of LATCH blocks below:

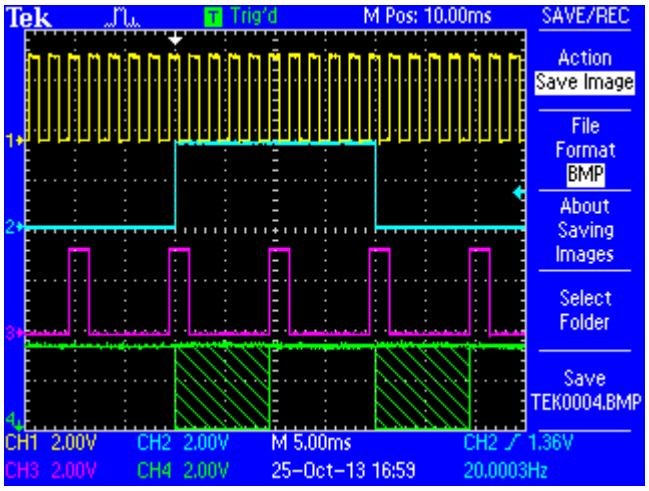
D	CK	nRESET	Q	nQ
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

D	CK	nSET	Q	nQ
0	0	0	1	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

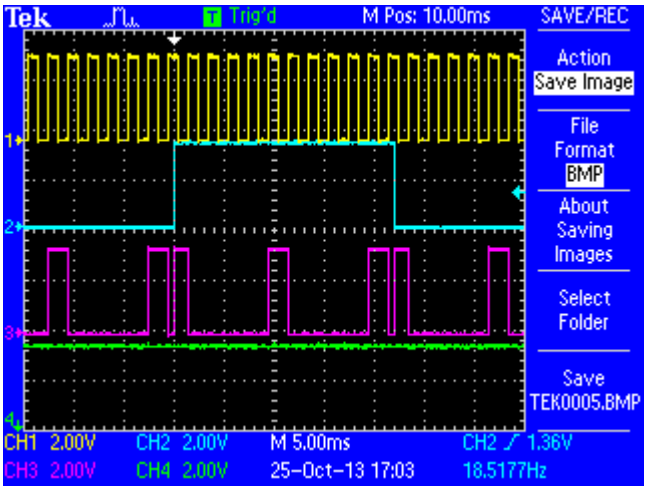
ISSUE 18: Counter with external clock starts internal RC OSC operation when reset

CNT2 and CNT3 (FSM0 and FSM1) have a possibility to be sourced from external RC OSC signal and have RESET signal at the same time. While block is in a reset state (when finished counting cycle and output is logic HIGH) and the defined RESET edge appears the internal RC OSC will start its operation until counter enters the next reset state.





Reset Edges came up with Reset state



Reset Edges and Reset state are at a different time

Workaround:

- Currently there is no universal workaround. If the RSC should be powered down all the time its Shared Power Down can be set to be controlled from matrix and SHARED PD input connected to HIGH level source.

ISSUE 19: ADC PGA 2X-16X gain options are not operational

ADC PGA gain options 2X up to 16X are not operational in the ADC signle-ended mode. Selection of these options will leave PGA with 1X gain. This issue applies to all LOTs of rev.B chips.

Workaround:

- Use rev.A chips if ADC PGA with 2X-16X option should be used in the design.
- Power up ADC, switch ADC mode to pseudo-differential. Configure PIN8 as Analog Input and use it as an input. Configure PIN9 as Analog Input and connect it to GND (this PIN will not be available in the design).
- Power up ADC, switch ADC mode to differential. Configure PIN8 as Analog Input and use it as an input. Configure PIN9 as Analog Input and connect it to GND (this PIN will not be available in the design).

NOTE: in pseudo-differential mode the ADC PGA input offset will be multiplied and added as well. For example: ACMP0 IN+ source is sourced from ADC PGA, PGA Gain is 2X, ADC input offset is 20mV, voltage applied to PIN8 is 100mV. Voltage applied to ACMP0 IN+ will be 240mV (2X · (100mV + 20mV)).

NOTE: using differential mode will add ADC Vref/2 to the PGA output voltage. For example: ACMP0 IN+ source is sourced from ADC PGA, ADC Vref is Bandgap 1V, PGA Gain option is 2X. Applying 100mV to PIN8 will lead to applying 700mV (2X · 100mV + 500mV) to ACMP0 IN+.

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