Interface IP for the PCI Express/USB3.0/SATA

Combo PHY for TSMC 28nm HPM

Overview

This IP is based on the PHY Interface for the PCI Express, USB3.0 Architecture Version 3.00 and Serial ATA Revision 3.1 . Both PCIe and USB3.0 make connection with a MAC layer through PIPE I/F. SATA make connection with a Link layer through SAPIS-like interface .
This IP include that Renesas Combo SerDes PHY is useful analog transceiver hard macro for various high speed serial interface PHY layer of TSMC 28nm HPM process. This macro is designed for PCI Express 2.1 / USB3.0 SuperSpeed / Serial ATA Revision 3.1 and can be used for each interface as “Combo” without GDS replace.
A customer can realize Low Power and Low cost easily.

Combo SerDes PHY Key Features

- Renesas Combo PHY can be used for analog transceiver of following interface.
  - PCI Express 2.1 (compliant with “PCI-Express Base Specification Revision 2.1”)
  - USB3.0 SuperSpeed (compliant with “Universal Serial Bus 3.0 Specification Revision 1.0 “)
  - Serial ATA Revision 3.1 (compliant with “Serial ATA Revision 3.1”)
- This macro can also be used for OBSAI/CPRI/SGMII/QSGMII/JESD204/CEI-6G/1000BASE-KX standards. (*1)
- Multi-lane support for PCI Express 2.1 (1 / 2 / 4 / 8 lanes available).
- Technology is TSMC 28nm HPM/HPC 1p10M / 1p9M .
- Supply voltage is 1.8V (min 1.62V max. 1.98V) / 0.995V (min. 0.935V max. 1.08V) .
- Selectable 10bit / 20bit for parallel side interface.
- 2Tap FIR filter for Tx equalizer / Tunable peaking amplifier for Rx equalizer.
- Built-in differential input buffer for clean reference clock.
- Power shut off mode can be used for avoiding leakage current of power/GND node.

*1 There are some restrictions for use case of these standards. Please contact and consult to Renesas Electronics for detail information before purchasing product.

PCIe PIPE Function Specification

- Based on PCI Express 2.1 (Gen2: 5.0Gbps) and PCI Express 1.1 (Gen1:2.5Gbps)
- Based on PIPE Spec3.0 for MAC layer interface
- Support to the Root Complex, Endpoint, Dual Mode and Switch, Bridge
- Multi-lane support: 1 / 2 / 4 / 8 lanes available
- Reference Clock 100MHz, Core Clock (PCLK) 62.5MHz/125MHz/250MHz
  - When use 62.5MHz, PIPE Data Bus width is 32bit (Gen1).
  - When use 125MHz, PIPE Data Bus width is 32bit (Gen2) or 16bit (Gen1).
  - When use 250MHz, PIPE Data Bus width is 16bit (Gen2) or 8bit (Gen1).
- Control of Driver Emphasis Level and Receiver equalizer is possible by an Internal Register.
- Support L1.1 (L1 PM sub-state: Stop reference clock on L1 state)

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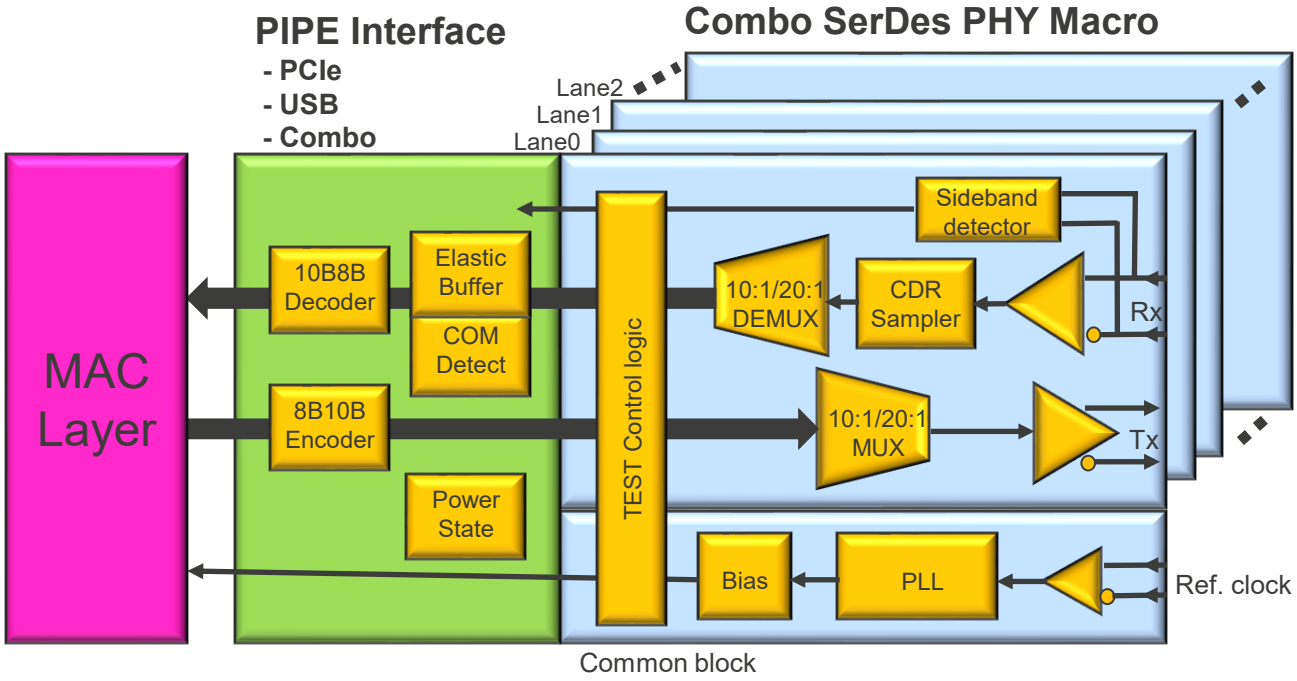
USB PIPE Function Specification

- Based on USB3.0 Super Speed (5.0Gbps)
- Based on PIPE Spec3.0 for MAC layer interface
- Select of Reference Clock is possible to 20/24/30/40/48MHz.
- Driver Emphasis Level setting value change circuit.
- LFPS(Low Frequency Periodic Signaling) transmission

Combo PIPE (PCIe/USB)

- Operation is possible as the PCI Express or USB by input terminal (PHYMODE) setting.
  00: PCI Express, 01: USB
- Key Feature shows above each sentence

Block Diagram (PCIe /USB/Combo PIPE)



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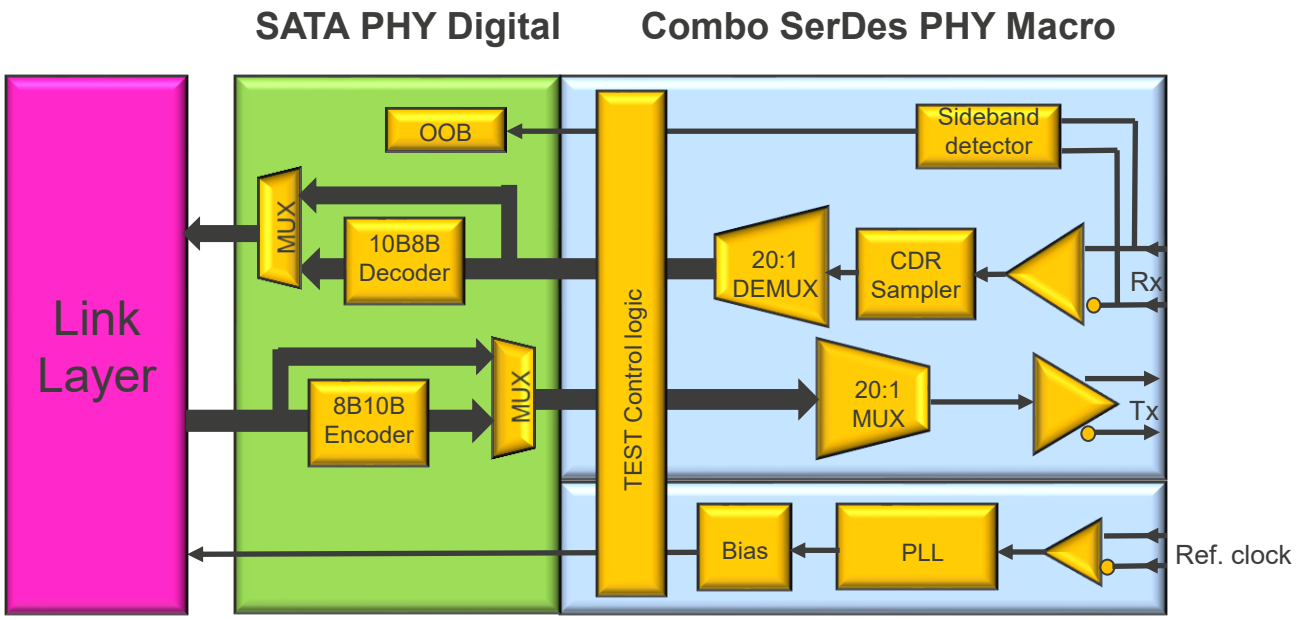
SATA PHY Digital Function Specification

- Based on Serial ATA Revision 3.1 (Gen1:1.5Gbps, Gen2:3.0Gbps and Gen3:6.0Gbps)
- Select of Reference Clock is possible to 100MHz or 80MHz
- Renesas original Interface for Link layer interface
  - Possible to use as SAPIS-like interface
  - OOB detection
  - Power Management
  - Select with/without 8B10B encoder/decoder

Block Diagram (SATA)



**This IP is contract design IP. Please contact for detail.*

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