Interface IP

Combo SerDes PHY for TSMC 28nm HPM

Overview

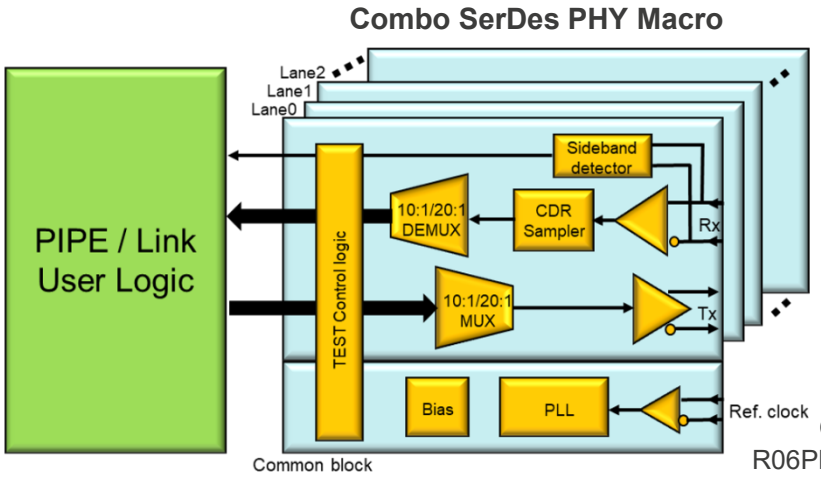
The Renesas Combo SerDes PHY is useful analog transceiver hard macro for various high speed serial interface PHY layer of TSMC 28nm HPM process. This macro is designed for PCI Express 2.1 / USB3.0 SuperSpeed / Serial ATA Revision 3.1 and can be used for each interface as “Combo” without GDS replace.

Key Features

- Renesas Combo PHY can be used for analog transceiver of following interface.
  - PCI Express 2.1 (compliant with “PCI-Express Base Specification Revision 2.1”)
  - USB3.0 SuperSpeed (compliant with “Universal Serial Bus 3.0 Specification Revision 1.0 “)
  - Serial ATA Revision 3.1 (compliant with “Serial ATA Revision 3.1”)
- This macro can also be used for OBSAI/CPRI/SGMII/QSGMII/JESD204/CEI-6G/ 1000BASE-KX standards. (*1)
- Multi-lane support for PCI Express 2.1 (1 / 2 / 4 / 8 lanes available).
- Technology is TSMC 28nm HPM 1p9M.
- Supply voltage is 1.8V (min 1.62V max. 1.98V) / 0.995V (min. 0.935V max. 1.08V) .
- Selectable 10bit / 20bit for parallel side interface.
- 2Tap FIR filter for Tx equalizer / Tunable peaking amplifier for Rx equalizer.
- Built-in differential input buffer for clean reference clock.
- Power shut off mode can be used for avoiding leakage current of power/GND node.

*1 There are some restrictions for use case of these standards. Please contact and consult to Renesas Electronics for detail information before purchasing product.

Block Diagram



*This IP is contract design IP. Please contact for detail.

CTPD-24-109
R06PF0090EJ0100

2024.09