

Internal Connection
Analog Output Ch.1

Analog Output Ch.0 for

Internal Connection

Analog Output Ch.0

## **Analog IP**

# **Dual Channel 12b D/A Converter**

#### **Overview**

A Dual Channel 12b D/A converter are provided with TSMC T40ULP+ESF3 wafer process. They are voltage output D/A Converter, supporting the wide supply range from 1.62 to 3.63V. The reference voltage can be set independently on the power supply. The linearity is excellent and the transition is fast. They support 2 operation choices; at the 1st mode; high buffered mode, they can drive 50pF capacitive load and 5k-ohm resistive load. And at the 2nd mode; high accuracy mode, they can show the high linearity from 0 to FS.

Block Diagram of Dual Channel DAC

Analog Output Ch.1 for

Data Output

Control

Signals

Data Output

Ch.0

12b

12b

Buff

### **Technology**

TSMC T40ULP+ESF3

### **Key Features**

- 12b resolution, 3µs conversion time
- Level Shifter inside. Directly connectable Interface to the digital section.
- Dual channel
- Independent Reference Voltage from the power supply
- Support 2 output mode; highly drivable mode / highly accurate mode.
- High Drivability of 50pF capacitive load and 5k-ohm resistive load at the highly drivable mode.
- Excellent linearity from 0 to FS at the accurate mode.

#### **Electrical Characteristics**

ltem		Unit	Spec			Dogovintion
			MIN	TYP_	MAX	Description
Power Supply AVCC		V	1.62	-	3.63	
Power Supply VDD		V	0.81	-	1.21	
Temperature		°C	-40	25	125	
Output Range	highly drivable mode	V	0.2	-	AVCC-0.2	
	highly accurate mode	V	0	-	AVCC	
Conversion time		μs	-	-	3	
Integral Non-Linearity (INL)		LSB	-4	-	+4	
Differential Non-Linearity (DNL)		LSB	-1	-	+1	
Center Offset Error at highly drivable mode		LSB	-20	-	+20	
Gain Error at highly drivable mode		%	-1	-	+1	
Power consumption	highly drivable mode	mA	-	2.6	-	
	highly accurate mode	mA	-	0.25	-	
Area		mm2	0.113			size on Si

\*This IP is contract design IP. Please contact for detail.

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