Interface IP

SerDes PHY for TSMC 28nm HPC+

Overview

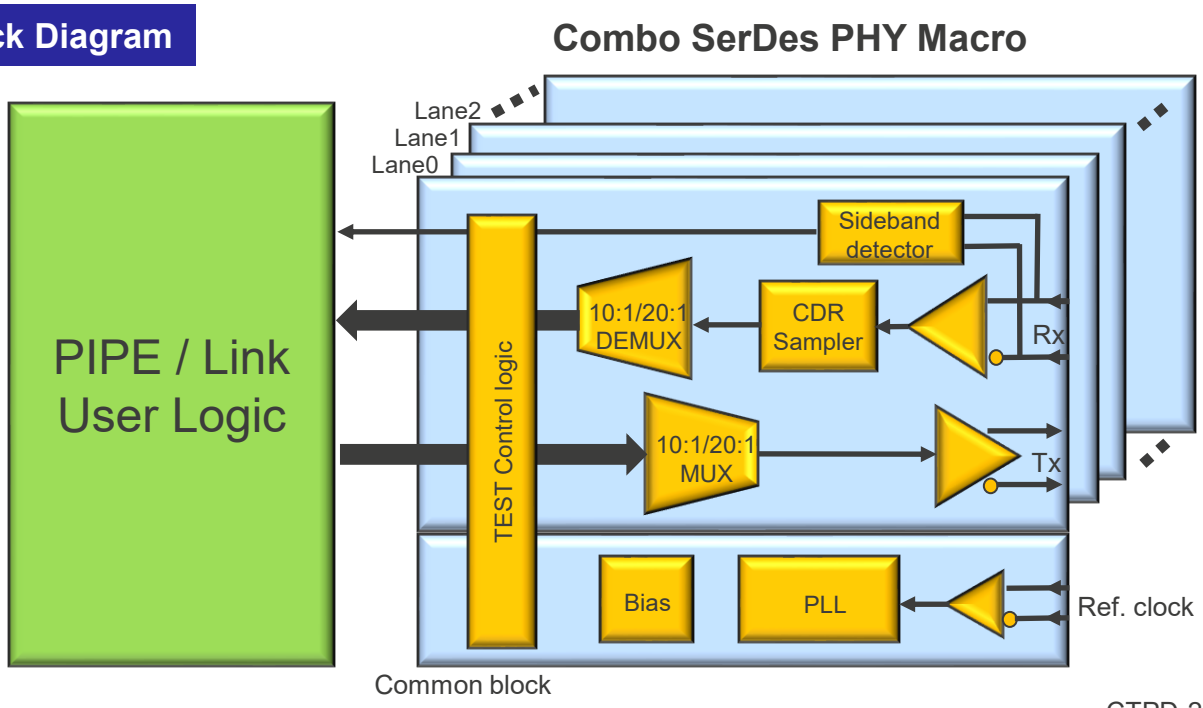
The Renesas SerDes PHY is useful analog transceiver hard macro for various high speed serial interface PHY layer of TSMC 28nm HPC+ process. This macro is designed for PCI Express 2.1 / USB3.0 SuperSpeed.

Key Features

- Renesas SerDes PHY can be used for analog transceiver of following interface .
  - PCI Express 2.1 (compliant with “PCI-Express Base Specification Revision 2.1”) *1
  - USB3.0 SuperSpeed (compliant with “Universal Serial Bus 3.0 Specification Revision 1.0) *1
- PCI Express 2.1 and USB3.0 SuperSpeed can be used as Combo macro *1
- Multi-lane support for PCI Express 2.1 (1 / 2 / 4 / 8 lanes available).
- Technology is TSMC 28nm HPC+ 1p10M .
- Supply voltage can be applied 0.90V for nominal and 1.0V for overdrive of core voltage, 1.8V for IO voltage.
- Selectable 10bit / 20bit for parallel side interface.
- 2Tap FIR filter for Tx equalizer / Tunable peaking amplifier for Rx equalizer.
- Built-in differential input buffer for clean reference clock.

*1 There are some restrictions for use case of these standards. Please contact and consult to Renesas Electronics for detail information before purchasing product.

Block Diagram



This IP is contract design IP. Please contact for detail.

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