

32-bit RISC CPU IP

SH-2A CPU

Overview

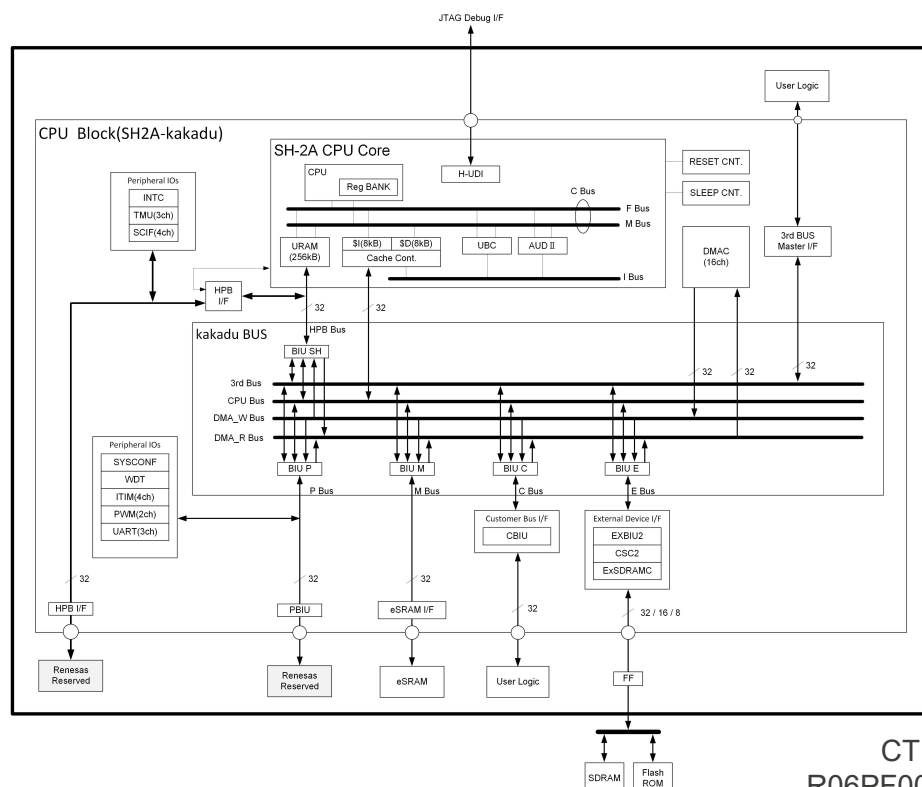
SH-2A is a high-performance 32-bit RISC CPU with two instructions running simultaneously.



Key Features

- 32-bit internal data bus
- General-purpose register architecture: 16 32-bit general general-purpose registers
 - Register bank for fast interrupt response (15 banks)
- RISC type instruction set: Instruction length: 16 bits / 32 bits mixed, 16-bit basic instruction for improving code efficiency, 32-bit instruction for improving performance and usability
- Two instructions simultaneous execution superscalar
- Instruction execution time: Up to 2 instructions / cycle
- Address space: 4GBytes , big endian
- 5 stage pipeline
- Harvard architecture
- Peripheral circuit
 - Cache, URAM, H-UDI, UBC, Peripheral IOs, DMAC, BUS

Block diagram



CTPD-24-094
R06PF0078EJ0100