

# 32-bit RISC CPU IP

## SH-4 CPU

### Overview

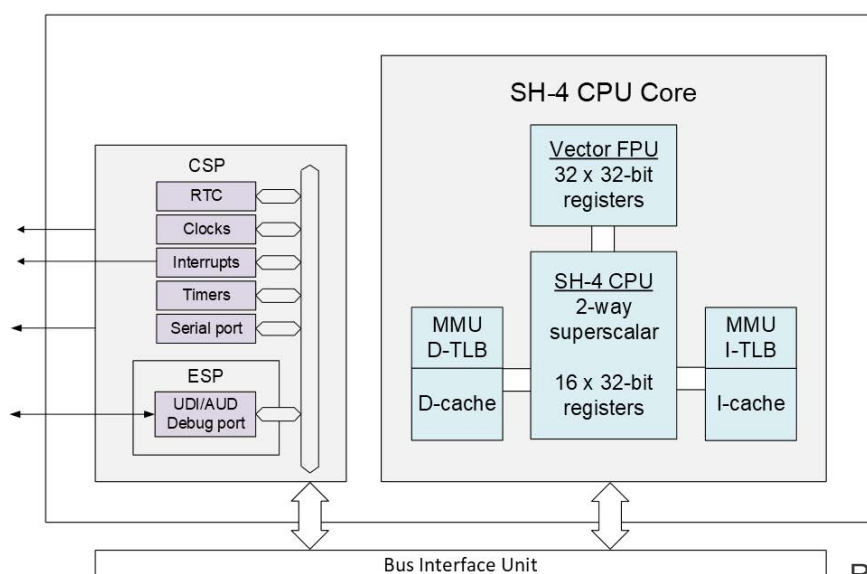
The SH-4 is a 32-bit RISC (reduced instruction set computer) microprocessor, featuring object code upward-compatibility with Renesas SuperH SH-1, SH-2, SH-3, and SH-3E microcomputers. It includes separate instruction and operand caches, the latter supporting both copy-back and write-through modes.



### Key Features

- 32-bit CPU + FPU, MMU option
- CPU with integrated vector FPU
  - 7MFLOPS / MHz
- Dual issue 32-bit CPU
  - 1.5DMIPS / MHz
- 5-stage pipeline
- Configurable
  - 2-way 4, 8, 16, 32, 64k I and D cache sizes
  - Optional emulation, peripheral facility
- Synthesizable core
- Peripherals
  - CSP(Core Support Peripherals)
  - ESP(Emulation Support Peripherals)

### Block diagram



CTPD-24-092  
R06PF0076EJ0100