iEvalADC

JESD204B High-Speed ADC Evaluation Platform

AN1808
Rev 1.00
Jan 23, 2013

- Complete high-speed ADC measurement solution
- Calculation of critical ADC parameters (SNR, SFDR, SINAD, ENOB, Harmonics, Power)
- Multiple display modes: frequency (FFT), time domain
- Integrated SPI control for ADC configuration
- 1M (2^{20}) word capture depth
- 40 to 500MSPS operation
- JESD204B Receiver reference design (automatically loaded by software)
- Compatible with all of Intersil's JESD204B ADC evaluation daughter cards

Evaluation Platform Overview

Intersil's high-speed ADC evaluation platform consists of custom designed hardware and software. The function of the hardware is to provide power to the ADC and to excite and/or measure the appropriate analog and digital inputs and outputs. The software is required to configure the device for initial operation, to modify the device functionality or parameters, and to process and display the output data (see Figure 1).

Hardware

There are two components in the hardware portion of the evaluation platform: the motherboard and the daughter card (Figure 1). The ADC is contained on the daughter card, which conditions the power provided by the motherboard and contains the analog input and clock circuitry. The daughter card interfaces to the motherboard through a High Pin Count (HPC) FPGA Mezzanine Connector (FMC). The daughter card was designed to be compatible with the Vita 57.1 standard. The motherboard contains a USB interface, an FPGA, and four banks of SDRAM. The motherboard serves as the interface between the host PC and the ADC daughter card. Most of the ADC functionality is controlled by the motherboard, although some daughter cards may have jumpers to set certain operating modes. The FPGA accepts output data from the ADC and buffers it in the SDRAMs before passing it to the PC at a lower speed for post-processing. The maximum buffer depth is 32 Megawords (2^{25}), however the evaluation software is capable of processing data records only up to 1 Megaword (2^{20}) deep. If utilization of the full 32 Megaword depth is desired, please contact the high speed data converter applications team for support.

The user must supply low-jitter RF generators for the clock and analog inputs. Recommendations of suitable generators can be found in "Appendix A: RF Generators" on page 7.

Many low-jitter RF generators exhibit high harmonic spectral content relative to the ADC performance. A band-pass filter is recommended to attenuate the harmonics. A wideband attenuator in series with the band-pass filter is also recommended for daughter cards without on-board attenuators. Current spikes from the ADC's switched capacitor sample-and-hold amplifier can create signal reflections in the coaxial cable. The attenuator reduces these reflections and improves performance.

Daughter Cards

Each daughter card is designed to produce optimal ADC performance and simplify the evaluation process. Some boards have multiple connections for the analog input and clock. For example, low-frequency and high-frequency input paths may be provided on certain boards. A high-frequency input path may have a balun interface, while a low frequency path may use a transformer or buffer amplifier (for DC

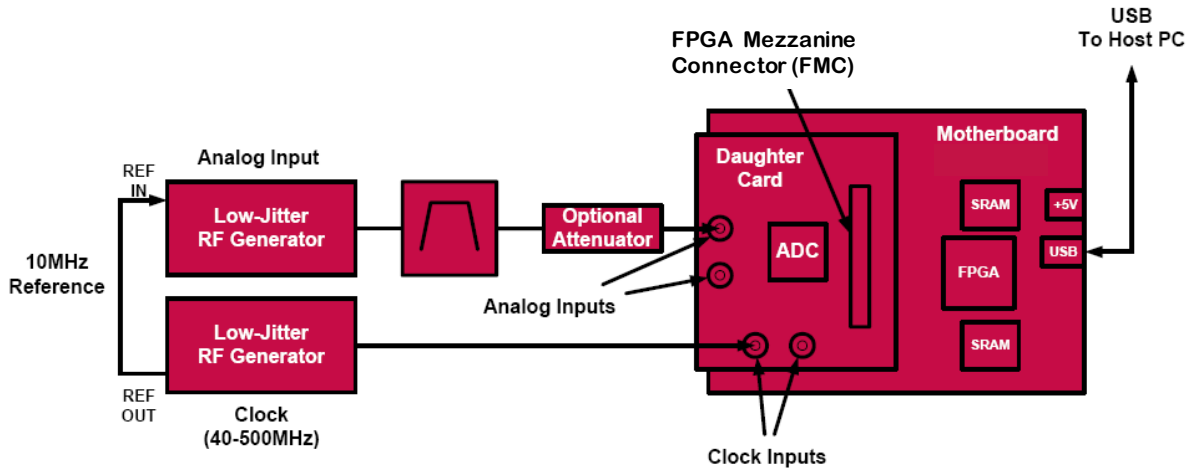


FIGURE 1. EVALUATION PLATFORM BLOCK DIAGRAM

coupling). Refer to “Appendix B: Daughter Cards” on page 7 for details on specific models.

Daughter Card Compatibility with FMC Host Cards

Each daughter card connects to the motherboard through a high pin count (HPC) FPGA mezzanine connector (FMC). The daughter card was designed to be compatible with the Vita 57.1 standard. This is intended to facilitate use of the daughter card with commercially available FMC host cards. “Appendix C: HPC FMC Pin-out” on page 7 lists the pins of the HPC FMC that are used by the daughter card. Signals described as being sourced by the Host must be provided by the FMC host card to the daughter card. These signals are necessary for the daughter card to be fully functional. Signals described as being soured by the Daughter card are provided by the Daughter card to the Host card. These signals may be optionally ignored by the host card, if the functionality they provide is deemed unnecessary.

Motherboard

The only connections required for the motherboard are +5V power and a USB connection to the PC running iEvalADC. No additional configuration of the motherboard is required.

Software

The software component is iEvalADC, a graphical user interface (GUI) created with Java. The GUI configures the ADC through its Serial Peripheral Interface (SPI) port, reads data from the motherboard, optionally post-processes the data (FFT analysis), and displays the result. Data can be viewed in the time or frequency domain, and can be saved for later processing. Critical performance parameters such as SNR, SFDR, harmonic distortion, etc. are calculated and displayed on-screen when viewing in the frequency domain.

Evaluation Kit Setup

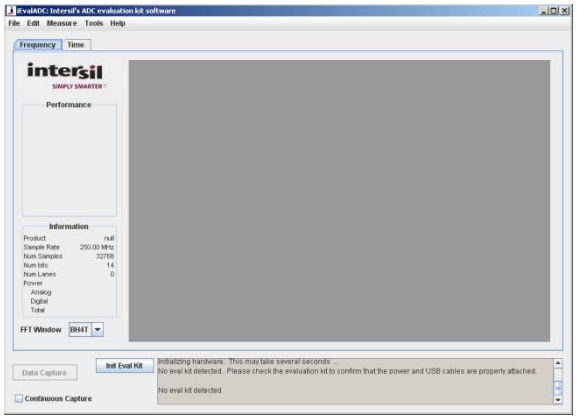
Referring to Figure 1, connect the daughter card to the motherboard by aligning the two mating FMC connectors. Four screws on the motherboard (not shown) align with mounting holes in the daughter card. Next, connect the RF generators to the Clock and Analog input SMA connectors. Set the clock frequency as desired with the power level at +10dBm. Similarly, set the analog input frequency with a power level of approximately +10dBm (the full-scale value will vary depending on the loss of the input path and gain of the ADC). With the RF generators on, apply +5V power (minimum 18W supply) to the motherboard. The motherboard supplies power to the daughter card. The daughter card contains power conditioning circuitry to filter and convert the power provided by the motherboard to the voltages required by the daughter card circuitry.

The iEvalADC software can be launched by double clicking the iEvalADC icon that should have been copied to the desktop during the installation process (refer to Application Note 1809 for detailed installation instructions). iEvalADC can also be launched by selecting Start->All Programs->Intersil iEvalADC->iEvalADC. The main iEvalADC window will open. If the hardware has been setup as previously described, data collection can proceed by pressing the Data Capture button. If the hardware has not been configured or is not functioning properly, the Data Capture button will be inactive and an Init Eval Kit button will be displayed. In this case, the Init Eval Kit button should be pressed once the hardware has been connected.

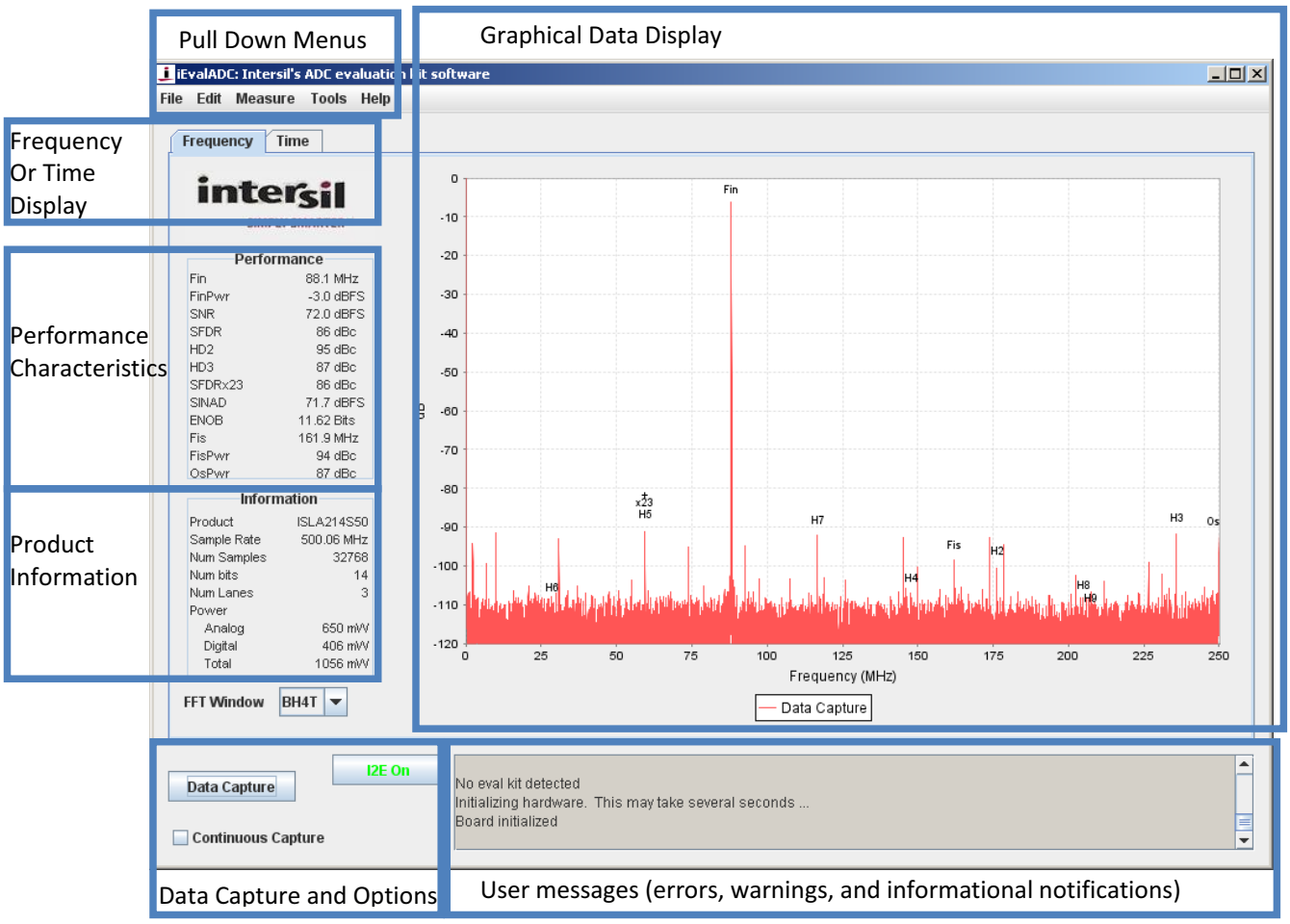
Overview of Software Features

iEvalADC is the evaluation kit control software for evaluation of Intersil's newest high speed converter products. The remainder of this guide assumes you have already installed the iEvalADC software by following the iEvalADC installation guide.

Double clicking on the desktop shortcut iEvalADC will bring up a window similar to the one shown. As shown, iEvalADC can be run without hardware attached to analyze previous data captures.



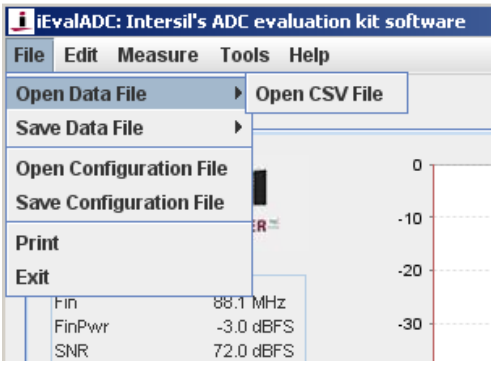
After clicking on the "Data Capture" button with a powered up evaluation kit attached, a window similar to the following is displayed. The diagram shows the major portions of the iEvalADC GUI.



Clicking on the "Time" or "Frequency" display panel will change the display of the current capture between time and frequency domain. The typical ADC performance characteristics, as calculated from the current data capture, are shown on the upper left area of the GUI (including SNR, SFDR, H2, H3, ENOB, etc). Product information is shown on the lower left hand area of the GUI. The product information includes the ADC product name, number of samples captured, and analog and digital power consumption of the ADC, as measured during the last data capture.

FILE MENU

The File pull down menu contains the following sections:



Open Data -> CSV File

Opens a previously saved Comma Separated Format (CSV) file and analyzes the data as if it was received from the evaluation kit. CSV is an industry standard text format. The CSV files saved and loaded by iEvalADC have one ADC sample per line, with each sample represented by a decimal number. The decimal number is generated by taking the raw ADC data in unsigned magnitude format and left shifting as needed until the MSB of the ADC sample is in bit position 16, with the resulting binary number being represented as a decimal. This default format has the advantage that a program can load this CSV file without having prior knowledge of the resolution of the ADC. As an option, iEvalADC can also load and save more traditional LSB-justified CSV files from the Tools->Option drop down selection.

Save Data -> CSV File

Saves the currently displayed data as a CSV file. The saved data is always in the time domain, irrespective of the graphical time or frequency domain display selection.

Open Configuration File

Opens the configuration file previously saved by iEvalADC. Configuration files are a convenient way to save settings for iEvalADC, including FFT windowing, continuous capture, FFT bin width settings, data capture setting such as number of samples, etc.

Save Configuration File

Saves the configuration state of iEvalADC into a configuration file.

Print

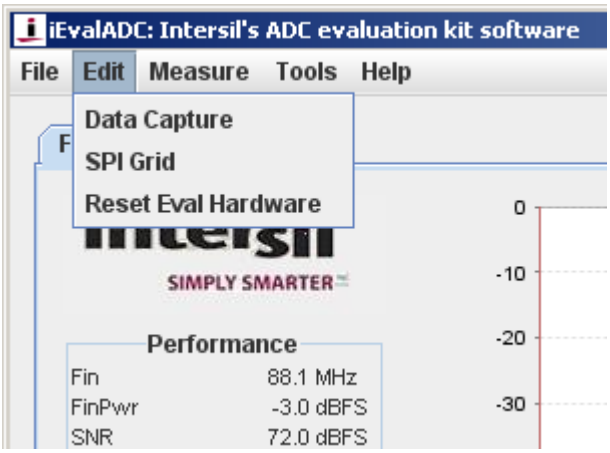
Brings up the printing window.

Exit

Exits iEvalADC.

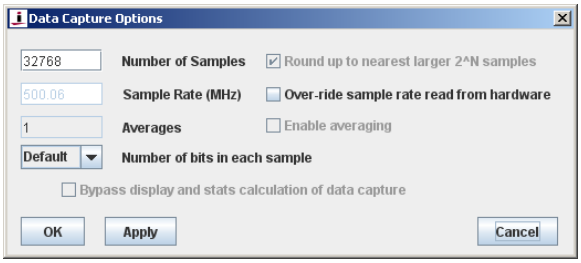
EDIT MENU

The Edit pull down menu contains the following selections:



Data Capture

Brings up a window that allows the user to configure the data capture operation. Each of these settings affects data captures from hardware and from CSV files read in. The user can set the following parameters.



Number of Samples

The user can define the number of contiguous samples they would like to capture each time the Data Capture button is pressed. This number is automatically rounded up to the next largest power of 2 as required by iEvalADC's FFT routine. The hardware supports up to 32Meg (2^{25}) continuous data samples captured. However, it should be noted that downloading in excess of 1Meg (2^{20}) samples can result in long capture times and may cause the program to run out of memory. The long capture times are a driver related issue and the memory limitation is due to the software. Both will be improved in a future revision of iEvalADC.

Sample Rate

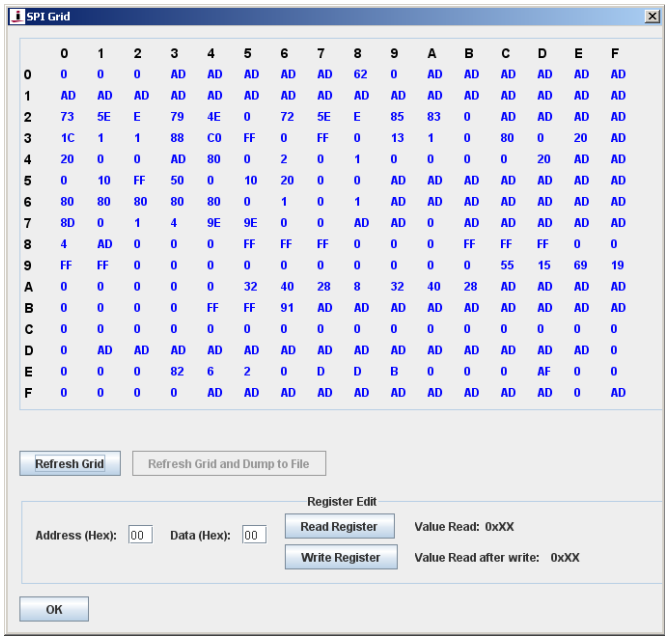
Intended to allow the user to set the sample rate for subsequent data analysis. The motherboard will compare the clock received from the daughter card to a reference frequency and will estimate the ADC sample rate. To override this estimate, click the over-ride sample rate read from hardware check box and enter the desired sample rate, in MHz. This function is also useful when reading in data from a CSV file, as in this case, the sample rate is completely unknown to iEvalADC.

Number of Bits in Each Sample

Allows the user to define the resolution. This is commonly used to evaluate the performance of a lower resolution version of a given ADC product when only the higher resolution hardware is available. For example, to evaluate the ISLA222S25 (Dual, 12-bit, 250MSPS) performance with an ISLA224S25 (Dual, 14-bit, 250MSPS), simply change the drop down from "Default" to 12-bits.

SPI Grid

Brings up a window that allows access to the SPI accessible registers in the ADC.



- In the upper area of the window, the entire SPI address space and data values are supplied in hexadecimal format (0x##). These values are read from the ADC whenever this window appears, and whenever the "Refresh Grid" button is clicked. The SPI address space is 8-bits. The y-axis is the SPI address MSB nibble, while the x-axis is the SPI address LSB nibble. For instance, the value at SPI address 0x70 is 0x80 in this example. The value at SPI address 0x07 is 0xAD.
- Registers accessible through the SPI port can be read or written using the interface at the bottom of the window. To read an individual register byte, simply enter the address in hexadecimal notation (i.e., 8f or c1) in the "Address (Hex)" field and click on "Read Register". The value read from hardware will be displayed. To write an address, fill in the "Address (Hex)" and "Data (Hex)" fields and click on "Write Register". The value will be written to hardware, and subsequently read out, with the read out value being displayed to the right of the "Write Register" button.

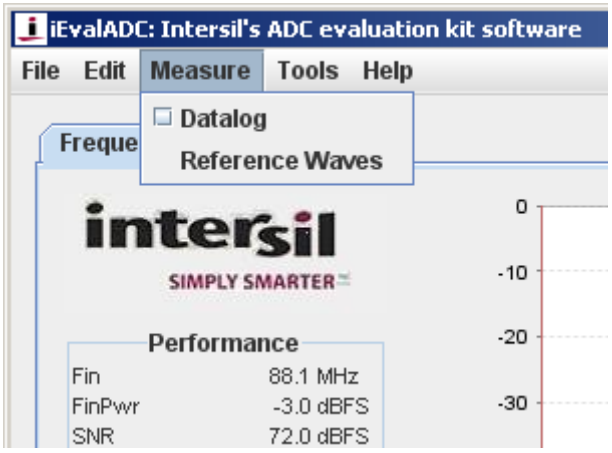
- Registers accessible through the SPI port can also be written to by selecting the appropriate field in the upper grid area. To change a register value, click on the entry corresponding to the desired address, enter the new value in hexadecimal notation, and then press Enter on your keyboard to force the new value to be written through the SPI interface.

Reset Eval Hardware

When selected, this will re-initialize the entire evaluation kit hardware. This process takes several seconds to complete.

MEASURE MENU

The Measure pull down menu contains the following selections.

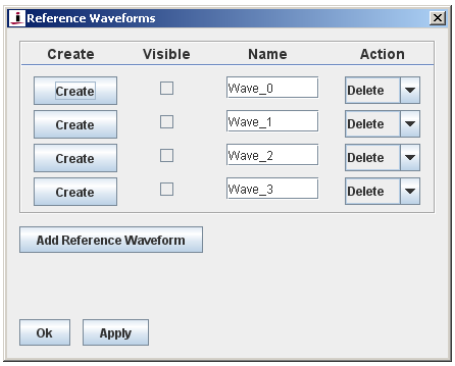


Datalog

This feature provides a simple mechanism to data log all performance characteristics of subsequent captures automatically to a CSV file. Selecting the Datalog will prompt the user for a data log file. Once selected, subsequent data captures will record the performance and information characteristics to the data log file, with one line per data capture. Selecting the Measure->Datalog again will discontinue data logging. If an existing file is selected as the data log file, the file will be appended to without headers, to facilitate intermittent data logging in a lab environment. Several options are available to modify the data logger's behavior in the Tools->Options popup window.

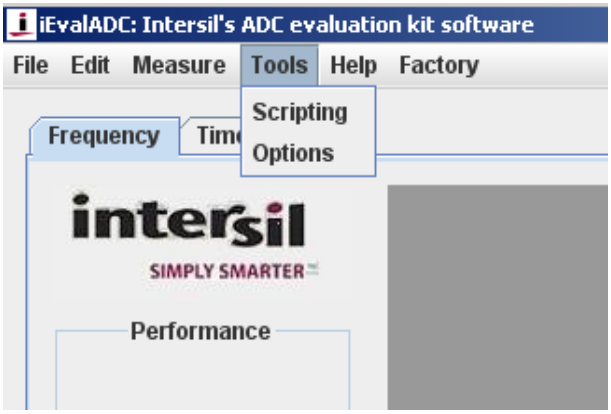
Reference Waves

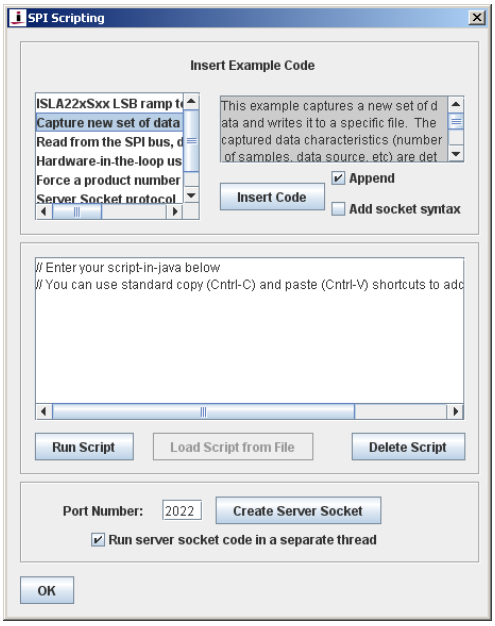
This feature is similar to an oscilloscope's reference memory. It allows the user to store the graphical representation of the current plot on the screen, name the plot, and make the reference wave visible (or not) as desired. Clicking the "Create" button will save the current plot as the reference wave selected. An arbitrary number of reference waves is supported. To add additional reference waves, press the "Add Reference Waveform" button



TOOLS MENU

The Tools pull down menu contains the following selections.





Scripting

This popup window provides access to iEvalADC's automation and test capabilities. The upper left selection box provides a number of examples of scripts that cause the evaluation kit to perform various sequences: program the ADC to create an

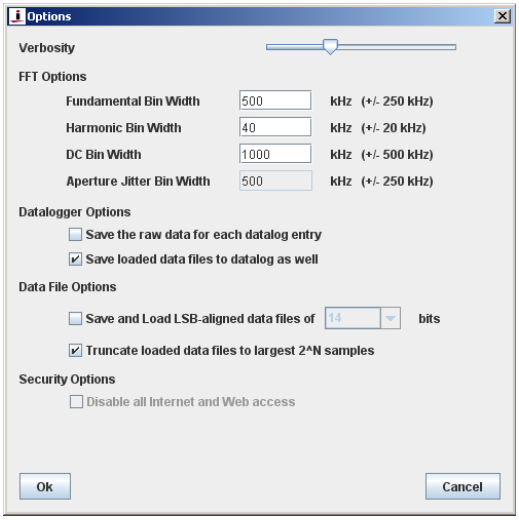
LSB-ramp output test pattern, read from the SPI bus and dump the values to a file, etc. A more advanced example shows how to use file I/O as the interlock mechanism to make hardware-in-the-loop type measurements (hardware-in-the-loop refers to automated data capture by the evaluation kit, post processing by DSP in an arbitrary programming environment, repeating indefinitely in a loop). A description for the selected script is shown in the upper right hand box. Clicking "Insert Code" will insert the code into the editable textbox in the middle of the window. The script then can be modified as desired to change functionality. The language used is BeanShell, a loosely typed version of Java, with user-level methods such as SPI reads and writes and data capture exposed in the script scope. Clicking on "Run Script" will execute the script. Use standard copy (Ctrl-C) and paste (Ctrl-V) to save a custom script to a file or load a custom script from a file.

The same scripting functionality can be automated in a more elegant and powerful, programming language independent fashion, by creating a (TCP) server socket daemon to service requests. Clicking on the "Create Server Socket" will bind the port specified in the entry box and attach a listening daemon to it. This allows the user to issue similar scripting commands to the daemon, and therefore the hardware, from any modern programming language. Optionally, the daemon can be run in the current thread to prevent hardware contention between iEvalADC and the daemon, however, note iEvalADC will be non-responsive until the ":End" protocol command is sent to this socket. Please see the "Server Socket protocol" for an example of the simple protocol used across the socket.

For additional support in using scripting and socket automation, please contact Intersil's high speed converter factory applications group at HSConverterTeam@intersil.com.

Options

Allows the user to set iEvalADC options to adjust the behavior of the software, as desired.



Verbosity

This slider controls which types of messages are printed to the message box, including error messages, informational messages, and debugging-level messages. Moving the slider will result in a printed message in the message window about the current level of verbosity.

FFT Options

This set of options affects the frequency domain performance calculations. The fundamental bin width (in kHz) defines the width of the fundamental, and for instance, could be increased to ignore the added noise from an ADC sample clock with high close in phase noise. The harmonic bin width defines the frequency width of each harmonic. The DC bin width determines the amount of frequency offset from DC, and can be used to fine tune what the application considers to be 1/f noise. Aperture Jitter bin width is not yet implemented.

Datalogger Options

The "Save the raw data..." checkbox makes every datalogged capture dump the raw data for that capture to a new CSV file. A pointer to that file is recorded in the data log file along with the performance numbers for that capture. "Save loaded data..." will make the datalogger add an entry for files loaded from File->Open Data File selections (in addition to new data captures).

Data File Options

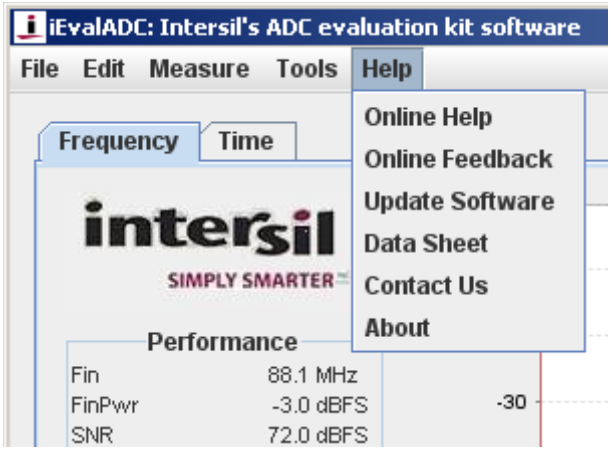
Adjusts the type of data files saved and loaded by iEvalADC. The first option forces iEvalADC to save and load LSB-aligned data files rather than MSB-aligned ones. This option also requires the resolution to be specified. The resolution must be specified because when loading samples, the resolution of LSB-aligned data cannot be automatically determined from the CSV file itself. The "Truncate..." option allows iEvalADC to load CSV files with a non power of 2 number of samples in them. The sample record is truncated to the largest possible power of 2 before analysis.

Security Options

Not yet implemented.

HELP MENU

The Help pull down menu contains the following selections.



The help dropdown menu contains links to various online resources for getting help, leaving feedback, updating the iEvalADC software, and even sending the high speed converter group an email directly to HSConverterTeam@intersil.com. We welcome any feedback you are willing to offer.

References

- JESD204B Evaluation Kit webpage with latest iEvalADC installer: www.intersil.com/jesd204b
- iEvalADC Installation and Quick Start Guide: Application Note AN1809>
- iEvalADC User Guide: (Application Note AN1808)

Appendix A: RF Generators

Intersil uses the following RF generators as clock and signal sources when characterizing high-speed ADCs:

- Rohde & Schwarz: SMA100A
- Agilent: 8644B (with Low-Noise option)

These generators provide very low jitter to optimize the SNR performance of the ADC under test. Other generators with similar phase noise performance can also be used. Contact Intersil Technical Support for recommendations.

Appendix B: Daughter Cards

ISLA214S50IR48EV1Z, ISLA216S25IR48EV1Z

These daughter cards use a common design to accommodate the single-input devices from the ISLA2xxS family of converters. They allow for one clock input path and two analog input paths. The clock path drives the clock input of the ADC as well as provides a reference clock to the FPGA on the motherboard.

The two analog input circuits are both transformer-coupled. The path marked Primary Input (default) uses two back-to-back wideband RF transformers. This path provides excellent performance for input frequencies between 30MHz and 700MHz. The Secondary Input path provides an alternate set of back-to-back transmission line RF transformers with a smaller footprint. These transformers offer a lower cut-off frequency of 4.5MHz. To switch to the Secondary Input, remove 0Ω resistors R67 and R69 and install 0Ω resistors R71 and R72.

ISLA224S25IR48EV1Z

This daughter card uses a common design to accommodate the dual-input devices from the ISLA2xxS family of converters. It allows for one clock input path and one analog input path for each channel. The clock path drives the clock input of the ADC as well as provides a reference clock to the FPGA on the motherboard. The analog input circuit is transformer-coupled and uses two back-to-back wideband RF transformers. This path provides excellent performance for input frequencies between 30MHz and 700MHz.

Appendix C: HPC FMC Pin-out

HPC PIN	FUNCTION	SOURCE
A2	LANE1N (AC-Coupled)	Daughter
A3	LANE1P (AC-Coupled)	Daughter
A6	LANE2N (AC-Coupled)	Daughter
A7	LANE2P (AC-Coupled)	Daughter
B1	CLK_DIR	Daughter
C6	LANE0N (AC-Coupled)	Daughter
C7	LANE0P (AC-Coupled)	Daughter
C39	3.3V Supply	Host
D1	PG_C2M (Host Power Good)	Host
D36	3.3V Supply	Host
D38	3.3V Supply	Host
D40	3.3V Supply	Host
E21	Daughter Power Enable	Host
E22	RESETN	Host
F1	VIO_B_M2C Power Good	Daughter
F4	SYNC_P	Host
F5	SYNC_N	Host
F25	CLKDIV	Host
F26	NAPSLP	Host
H4	ADC Sample Clock P	Daughter
H5	ADC Sample Clock M	Daughter
J24	CSB	Host
J25	SDO	Daughter
J27	ADC Power Good	Daughter
J39	VIO_B_M2C (1.8V)	Daughter
K25	SCLK	Host
K26	SDIO	Host/Daughter
K40	VIO_B_M2C (1.8V)	Daughter

NOTES:

1. In this document, the terms "host" and "motherboard" are interchangeably used.
2. In this document, the terms "daughter card" and "mezzanine card" are interchangeably used.
3. Nets sourced by the Host are used by the daughter card and must be supplied.
4. Nets sourced by the Daughter are provided to the host card. In some cases (VIO_B_M2C, CLK_DIR, Power Good, etc) these can be ignored by the host.

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