

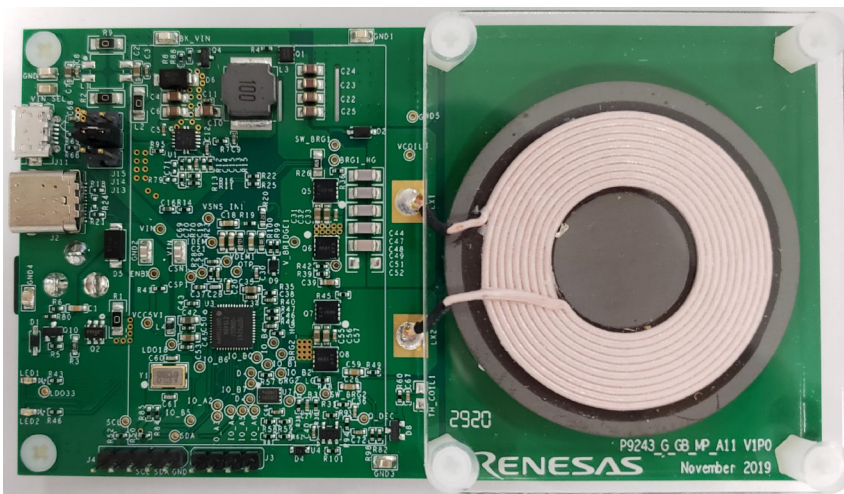
The P9243-GB-EVK Evaluation Board demonstrates the features of the P9243-GB 15W Wireless Power Transmitter (TX) with a fixed frequency. It is intended to evaluate the functionality and performance of the P9243-GB when combined with a Qi power receiver in a wireless charging system. The P9243-GB-EVK offers the flexibility to select parameters, such as Q-factor threshold, LED pattern, power loss FOD threshold, and external temperature sensing function. The printed circuit board (PCB) has four layers, and can be used with the user's WPC-1.2.4 compliant receiver.

The high-efficiency, turnkey reference design is supported by comprehensive digital resources to significantly expedite the design-in effort and enable rapid prototyping.

## Kit Contents

- P9243-GB-EVK Evaluation Board
- Adaptor: 18V/1.38A

## Evaluation Board



18V/1.38A AC Adapter (Not to scale)

## Features

- Power transfer up to 15W at receiver side
- Wide input voltage range: 5V to 19V
- WPC-1.2.4 compatible, MP-A11 coil configuration
- Supports system parameters configuration using GUI
- Integrated drivers for external power MOSFETs
- Embedded 32-bit ARM® Cortex®-M0 processor (trademark of ARM, Ltd.)
- Simultaneous voltage and current demodulation scheme for WPC communication
- Integrated current sense amplifier
- Supports accurate 127.7kHz frequency operation
- Feedback control for external input step-down regulator
- Dedicated remote temperature sensing
- User-programmable power transfer LED indicators
- User-programmable foreign objects detection (FOD)
- WPC EPP-based Q-factor detection
- Active-LOW enable pin for electrical on/off
- Over-current and over-temperature protection
- Supports I2C interface
- Four-layer PCB assembled with test points and coil fixture
- -40°C to +85°C ambient operating temperature range
- 48-VFQFPN (6 × 6 mm) RoHS-compliant package

# Contents

Evaluation Board .....	1
Features .....	1
Contents .....	2
List of Figures .....	4
List of Tables .....	4
Setup .....	6
Required or Recommended User Equipment .....	6
Software Installation, Dongle Connectivity, and FLASH Programming with GUI .....	6
Software Installation .....	6
Dongle Connectivity .....	7
Using GUI to Write to FLASH .....	8
Kit Hardware Connections .....	9
Usage Guide .....	10
Overview of the P9243-GB-EVK .....	10
Programming Interface .....	10
Overview of the P9243-GB Wireless Power Pro GUI .....	11
System (Block Diagram) Tab .....	11
Config (Configuration) Tab .....	11
FOD (Foreign Object Detection) Tab .....	12
Program (Programming FLASH/OTP) Tab .....	13
Register (Manually Register Read/Write and Logging) Tab .....	13
Generating a New HEX File .....	13
External Temperature Sensing – TS .....	14
Control of External Power Stage DC/DC Buck Regulator – GPIO_B4 and GPIO_B7 .....	15
Bypass External DC/DC Buck Regulator – GPIO_A4 .....	16
External Oscillator – GPIO_B5 and GPIO_B6 .....	16
LED Pattern Selection – LED1 and LED2 .....	18
Quality Factor in Digital Ping Phase – QDEC .....	18
Selection of Input Source and Operation Mode .....	19
Transmitter Coil .....	20
List of Register for Default Configuration .....	21
Identification Registers .....	21
Table 4. Read Register – Device ID Register .....	21
Table 5. Read Register – Firmware Revision .....	21
State and Status Registers .....	22
Table 6. Read Register – System State .....	22
Table 7. Read Register – System Error Code .....	22
System Read-Only Registers .....	23

Table 8. Read Register – Input Current.....	23
Table 9. Read Register – Input Voltage .....	23
Table 10. Read Register – Operating Frequency.....	23
Table 11. Read Register – Transmitter Duty Cycle .....	23
Table 12. Read Register – Receiver Reported Q-Factor Value .....	23
Table 13. Read Register – Measured Q Factor Value.....	23
Table 14. Read Register – Threshold Q Factor Value.....	24
Table 15. Read Register – Potential Power .....	24
Table 16. Read Register – Transmitter Power .....	24
Table 17. Read Register – Received Power .....	24
Table 18. Read Register – FOD Threshold .....	24
Table 19. Read Register – Remote Temperature Sensing Voltage .....	24
Table 20. Read Register – Adaptor Type .....	25
Table 21. Read/Write Register – Rx Manufacture ID .....	25
Table 22. Read/Write Register – Rx Type.....	25
Table 23. Read/Write Register – Charge Status Packet .....	25
Configuration Registers .....	26
Table 24. Read/Write Register – Tx Manufacture ID Adjust.....	26
Table 25. Read/Write Register – Over Current Threshold Adjust.....	26
Table 26. Read/Write Register – Low Voltage and Over Voltage Threshold Adjust.....	26
Table 27. Read/Write Register – Over Temperature Threshold Adjust.....	26
Table 28. Read/Write Register – WPC Tuning Threshold Adjust.....	27
Table 29. Read/Write Register – FOD Region Select Adjust .....	27
Table 30. Read/Write Register – FOD Gain Select Adjust .....	28
Table 31. Read/Write Register – FOD Offset Select Adjust .....	28
Table 32. Read/Write Register – FOD Disable Adjust.....	29
Table 33. Read/Write Register – LED Pattern Adjust.....	29
Table 34. Read/Write Register – Sleep Timer Adjust.....	29
Table 35. Read/Write Register – Q-Factor Adjust.....	29
P9243-GB EVB Application Schematic v1.0.....	30
Bill of Materials (BOM).....	31
Board Layout .....	35
Ordering Information.....	39
Revision History.....	40

## List of Figures

Figure 1. Windows Device Manager Display for Troubleshooting the USB Connection.....	6
Figure 2. System Tab of GUI.....	7
Figure 3. Connecting the Dongle and Verifying GUI Connectivity.....	7
Figure 4. USB-to-I2C Dongle Header of “USB-FTDI-V2-1” (FTDI) Dongle and “WPD-USB-Dongle”.....	8
Figure 5. P9243-GB-EVK Successfully Connected to GUI.....	8
Figure 6. FLASH Programming Procedure.....	9
Figure 7. Evaluation Kit Connections using the P9415-R-EVK Receiver Evaluation Board.....	9
Figure 8. P9243-GB-EVK V1.0 Evaluation Board Features.....	10
Figure 9. Sample Q-Factor Test Data.....	12
Figure 10. P9243-GB EVB v1.0 Evaluation Board Detail.....	13
Figure 11. TH_COIL1, R60, and RC67 Schematic Location.....	14
Figure 12. TH_COIL1, R60, and C67 PCB Location.....	14
Figure 13. Buck Regulator Schematic Location.....	15
Figure 14. Buck Regulator PCB Location.....	15
Figure 15. Bypass Path Schematic Location.....	16
Figure 16. Buck Regulator PCB Location.....	16
Figure 17. External Crystal Schematic Location.....	17
Figure 18. External Crystal PCB Location.....	17
Figure 19. Q-factor Detection Schematic Location.....	18
Figure 20. Q-factor PCB Location.....	19
Figure 21. Input Source Selection Jumpers on the PCB.....	19
Figure 22. Silkscreen – Top of Board.....	35
Figure 23. Copper – Top Layer.....	36
Figure 24. Copper L1 Layer.....	37
Figure 25. Copper L2 Layer.....	38
Figure 26. Copper Bottom.....	39

## List of Tables

Table 1. External Oscillator Selection.....	16
Table 2. P9243-GB-EVK Operation Modes.....	20
Table 3. Recommend Coil Manufacturer.....	20
Table 4. Read Register – Device ID Register.....	21
Table 5. Read Register – Firmware Revision.....	21
Table 6. Read Register – System State.....	22
Table 7. Read Register – System Error Code.....	22
Table 8. Read Register – Input Current.....	23
Table 9. Read Register – Input Voltage.....	23

Table 10. Read Register – Operating Frequency.....	23
Table 11. Read Register – Transmitter Duty Cycle.....	23
Table 12. Read Register – Receiver Reported Q-Factor Value.....	23
Table 13. Read Register – Measured Q Factor Value.....	23
Table 14. Read Register – Threshold Q Factor Value.....	24
Table 15. Read Register – Potential Power.....	24
Table 16. Read Register – Transmitter Power.....	24
Table 17. Read Register – Received Power.....	24
Table 18. Read Register – FOD Threshold.....	24
Table 19. Read Register – Remote Temperature Sensing Voltage.....	24
Table 20. Read Register – Adaptor Type.....	25
Table 21. Read/Write Register – Rx Manufacture ID.....	25
Table 22. Read/Write Register – Rx Type.....	25
Table 23. Read/Write Register – Charge Status Packet.....	25
Table 24. Read/Write Register – Tx Manufacture ID Adjust.....	26
Table 25. Read/Write Register – Over Current Threshold Adjust.....	26
Table 26. Read/Write Register – Low Voltage and Over Voltage Threshold Adjust.....	26
Table 27. Read/Write Register – Over Temperature Threshold Adjust.....	26
Table 28. Read/Write Register – WPC Tuning Threshold Adjust.....	27
Table 29. Read/Write Register – FOD Region Select Adjust.....	27
Table 30. Read/Write Register – FOD Gain Select Adjust.....	28
Table 31. Read/Write Register – FOD Offset Select Adjust.....	28
Table 32. Read/Write Register – FOD Disable Adjust.....	29
Table 33. Read/Write Register – LED Pattern Adjust.....	29
Table 34. Read/Write Register – Sleep Timer Adjust.....	29
Table 35. Read/Write Register – Q-Factor Adjust.....	29

# Setup

## Required or Recommended User Equipment

The following additional lab equipment is required for using the kit:

- P9415-R-EVK Receiver Evaluation Board or any WPC-1.2.4 compliant receiver.
- 18V/1.38A power supply or QC3.0 provided by the user.
- REA USB-to-I2C Dongle (sold separately).

## Software Installation, Dongle Connectivity, and FLASH Programming with GUI

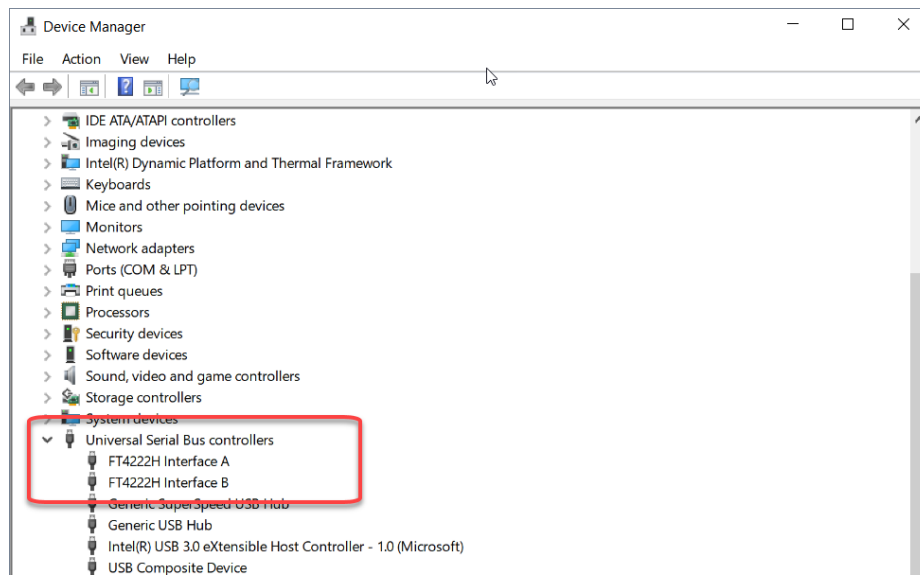
Visit the P9243-GB-EVK webpage and download the latest version of the P9243-GB Wireless Power Pro GUI, USB drivers, and the *P9243-GB A11a Configuration Flash HEX File*. The software provides an intuitive graphical user interface for reading and writing to P9243-GB SRAM registers and generate custom user configurations for the external Flash.

### Software Installation

Follow these procedures to install the software:

1. Do not connect the USB-to-I2C dongle before installing the software.
2. Run the downloaded *USB Drivers Setup* executable file and follow the user prompts to install the USB drivers.
3. After finishing the setup of the USB drivers, connect one of the USB-to-I2C dongles to the USB port. Wait for a few moments to let Windows® map the drivers for the dongle.
4. Open the Device Manager from the Windows control panel and check the devices listed under the “Universal Serial Bus controllers” section. “FT4222H Interface A” and “FT4222H Interface B” should appear in this section as shown in Figure 1.
5. Download and extract the P9243-GB Wireless Power Pro GUI *SWR* compressed file. To launch GUI, click the “Renesas Wireless Power P9243-GB” Application.

Figure 1. Windows Device Manager Display for Troubleshooting the USB Connection

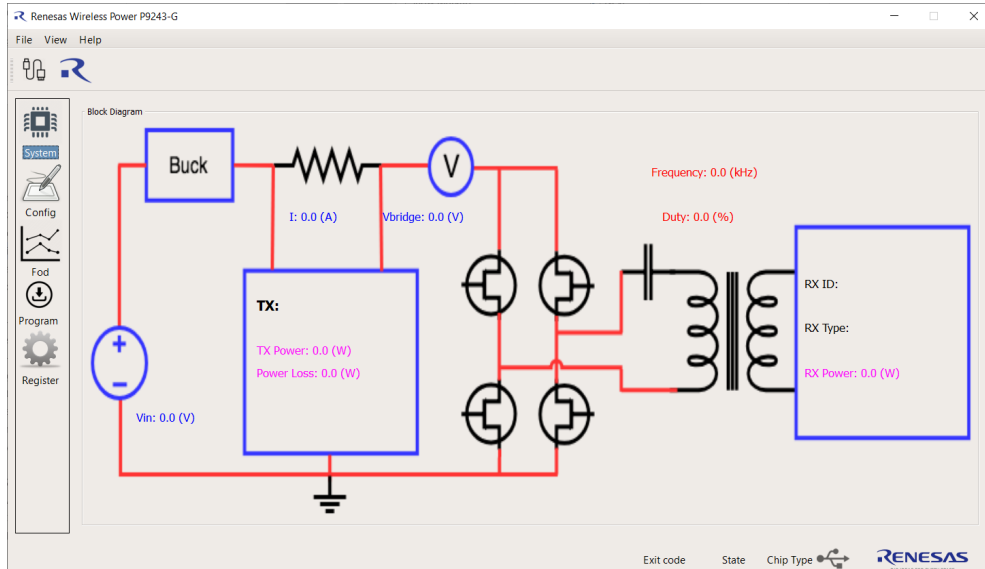


## Dongle Connectivity

Follow these procedures to establish GUI connectivity to the P9243-GB-EVK:

1. Launch the GUI program – Renesas Wireless Power P9243-GB. The initial screen of the GUI is shown in Figure 2.

Figure 2. System Tab of GUI



2. Set up the P9243-GB Evaluation Board by plugging the 5V adapter into J11 (Micro-USB connector) or the user's power supply into VIN (see Figure 4).
3. Connect the USB-to-I2C dongle to the computer and launch the P9243-GB Wireless Power Pro GUI. Once the dongle is detected, the message "Dongle Detected" will appear on the GUI. If the message does not appear, unplug and plug the USB cable at the user's computer.
4. Connect the USB-to-I2C dongle header to J4 of P9243-GB-EVK as shown in Figure 3.

Figure 3. Connecting the Dongle and Verifying GUI Connectivity

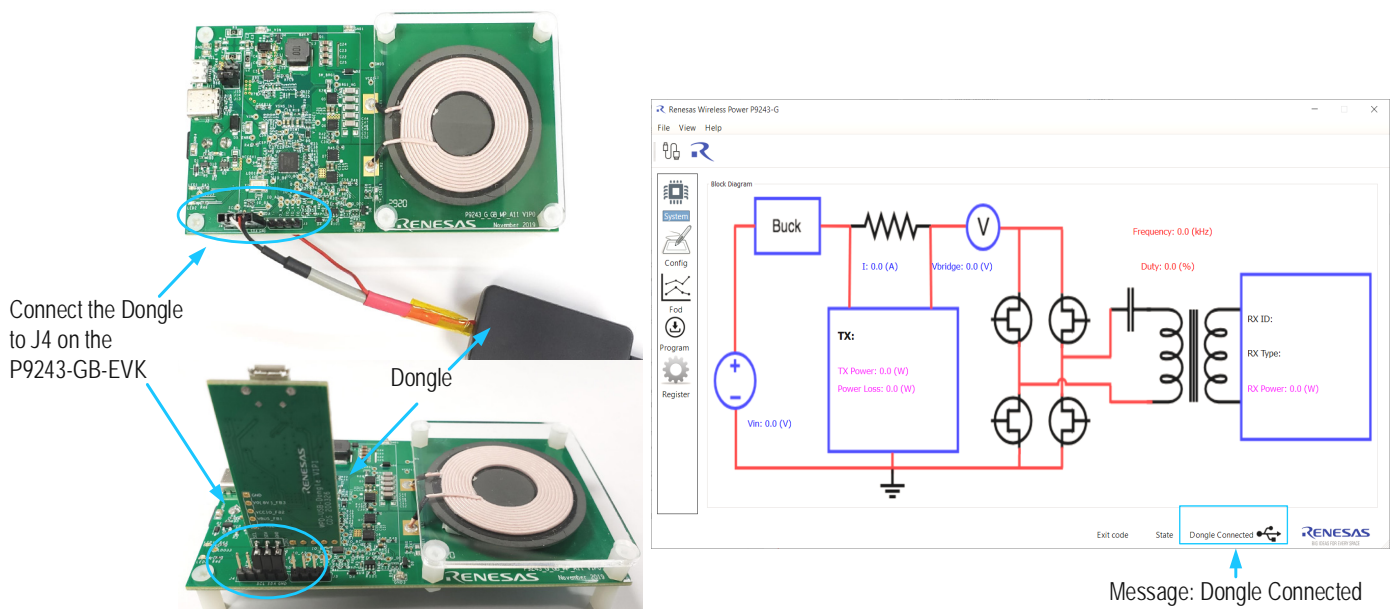
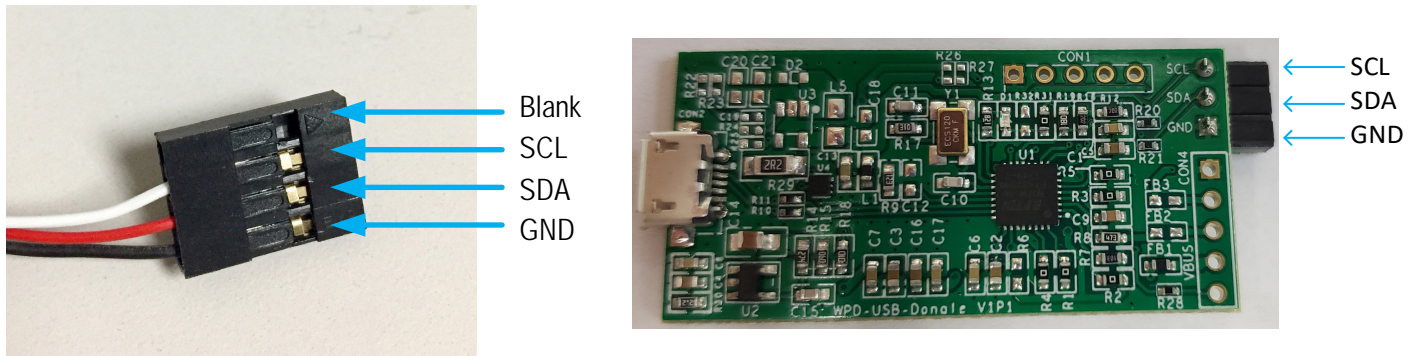




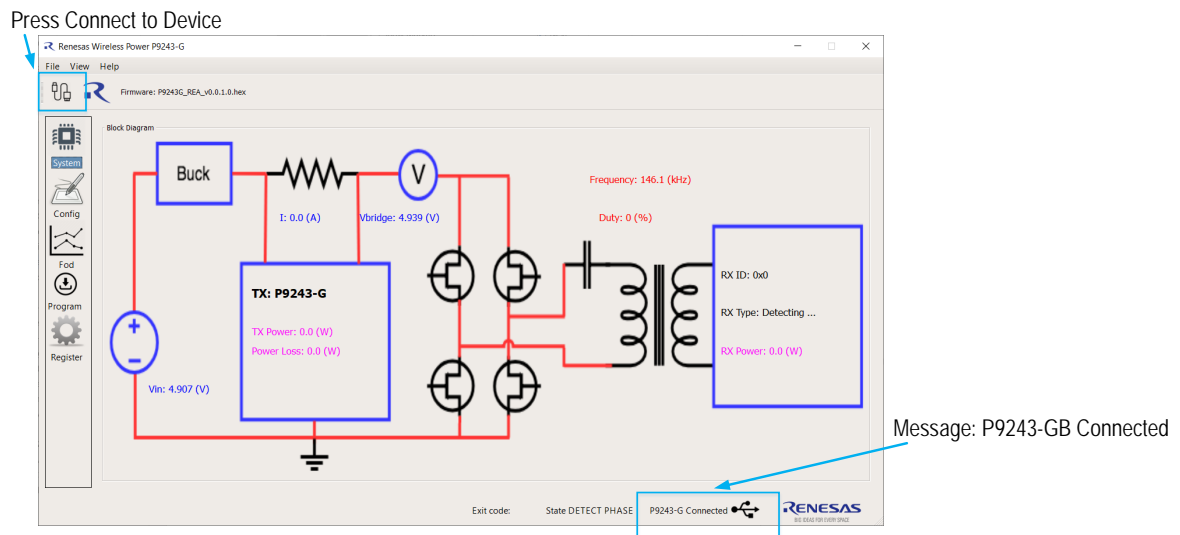
Figure 4. USB-to-I2C Dongle Header of “USB-FTDI-V2-1” (FTDI) Dongle and “WPD-USB-Dongle”



5. Press the “Connect to Device” button in the P9243-GB Wireless Pro GUI to connect to P9243-GB-EVK. Once P9243-GB-EVK is recognized, the message “P9243-GB Connected” will appear (see Figure 5).

Note: To disconnect: Under the File Drop-down menu → disconnect.

Figure 5. P9243-GB-EVK Successfully Connected to GUI



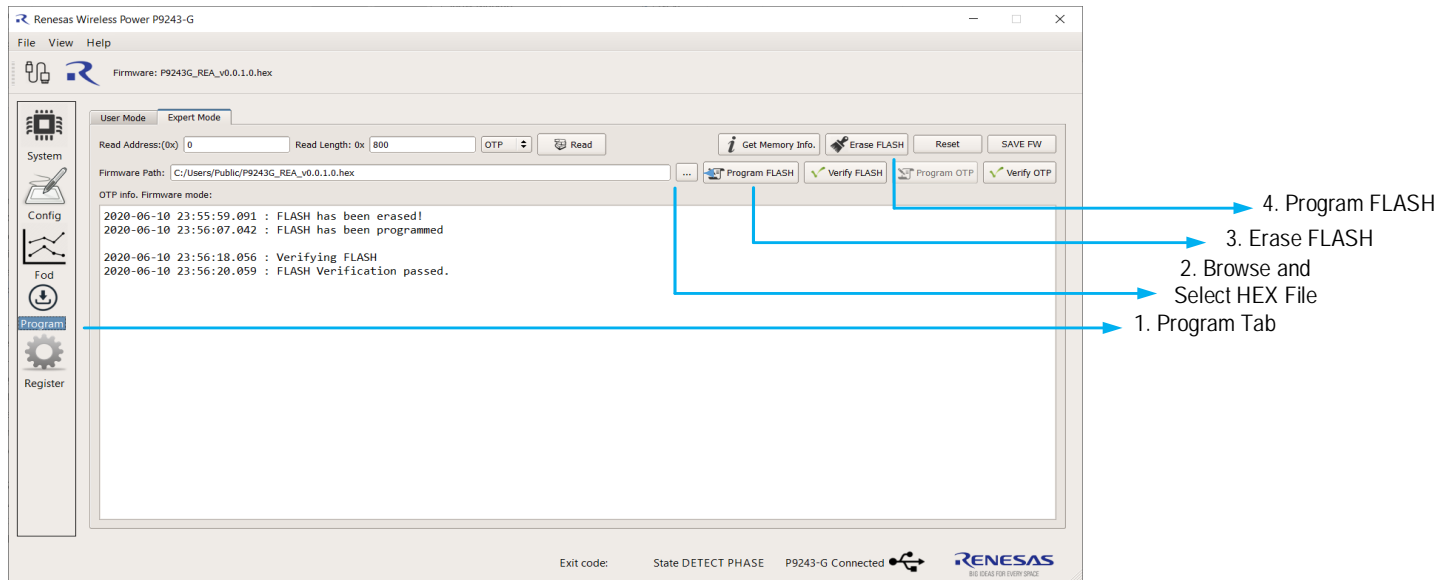
### Using GUI to Write to FLASH

To update the P9243-GB-EVK firmware, follow these steps and refer to Figure 6:

1. Enter the Program Tab of the GUI by Press Program.
2. Browse and select the firmware Hex file in Firmware Path.
3. Press Erase FLASH and accept the prompted messages.
4. Press Program FLASH and accept the prompted messages.
5. (Optional) Power cycle the P9243-GB, then press Verify FLASH and accept the prompted messages.



Figure 6. FLASH Programming Procedure



## Kit Hardware Connections

Follow these procedures to set up the kit as shown on Figure 7.

1. Set up the P9243-GB-EVK Evaluation Board by plugging the 5V/2A adapter or the user's power supply into J11 (Micro-USB connector). Refer to Figure 8.
2. If using the P9415-R-EVK Evaluation Board as the receiver, connect wires to the VOUT and GND test points on the P9415-R-EVK receiver to allow measuring the output voltage and applying a load.
3. Place the P9415-R-EVK or the user's receiver on the transmitter (TX) pad with the components facing up as shown on Figure 7.
4. Verify that the two green LEDs identified in Figure 7 are illuminated indicating that coupling has been established.

Figure 7. Evaluation Kit Connections using the P9415-R-EVK Receiver Evaluation Board

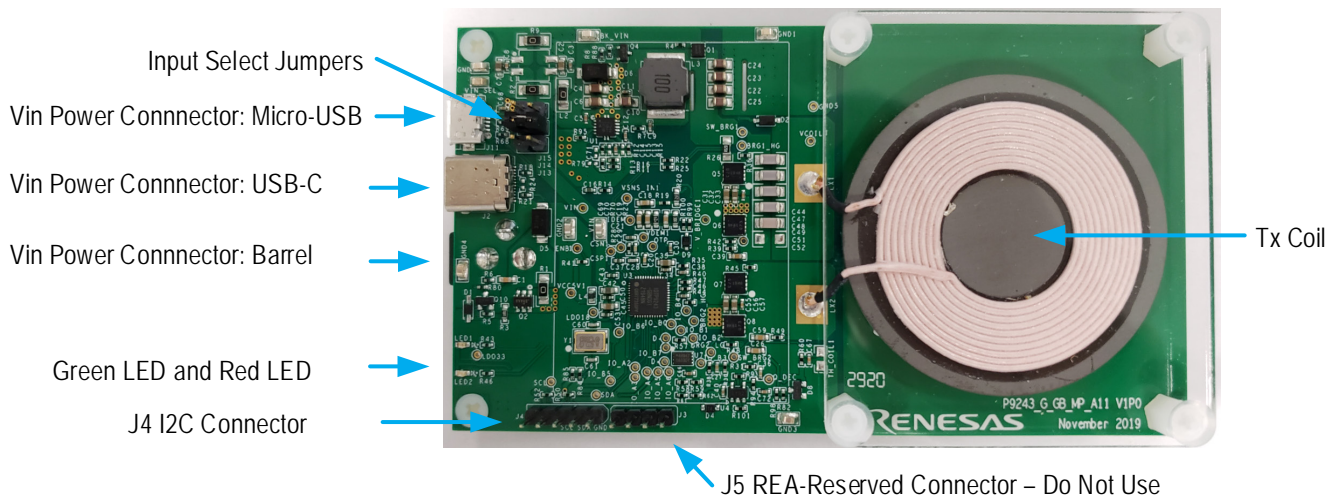


## Usage Guide

The P9243-GB-EVK firmware provides great flexibility to customize operating parameters for custom applications. Default values of the P9243-GB-EVK operating parameters, such as Digital Ping Frequency, FOD parameters, coil over-temperature sensing, and over current limit, are configurable in the firmware and are loaded from the external Flash memory. Based on the end application, the P9243-GB operating parameters can be configured by either writing to internal SRAM registers via the I2C interface, or by creating a new user configuration HEX file that can be generated within the P9243-GB Wireless Power Pro GUI. Once the new user configuration HEX file is generated, the Flash memory can be erased and reprogrammed with the P9243-GB Wireless Power Pro GUI. To customize the P9243-GB-EVK's operating parameters in real-time, use the P9243-GB Wireless Power Pro GUI software along with the USB-to-I2C dongle connected to J4 Header. For any production usages, consult with Renesas before finalizing firmware.

## Overview of the P9243-GB-EVK

Figure 8. P9243-GB-EVK V1.0 Evaluation Board Features



## Programming Interface

The P9243-GB has a pre-programmed bootloader that must be used in conjunction with an external flash memory that contains control firmware. The master P9243-GB accesses the slave external memory using a standard SPI interface (SCLK, MISO, MOSI, and  $\overline{SS}$  pins) to upload the firmware from the flash memory into the P9243-GB internal SRAM. This architecture allows the user to change the firmware in the external flash to meet application-specific requirements. Renesas also provides firmware to implement standard WPC coil configurations, such as the A11a addendum.

The P9243-GB Wireless Power Pro GUI can be used for programming the external flash file. The W25X20CLUXIG is the recommended external flash memory. Smaller memory sizes in the W25X family can be used depending on the total firmware size. For recommended flash memories, please consult Renesas.

## Overview of the P9243-GB Wireless Power Pro GUI

### System (Block Diagram) Tab

The System tab of the P9243-GB Wireless Power Pro GUI offers a dynamic visual block diagram to expand the knowledge base of the wireless power system. This tab provides real-time information of input voltage, input current, transmitted power, power level of the receiver received, power loss, operating frequency, operating duty, receiver identification number, and power contract type.

### Config (Configuration) Tab

The Config Tab of P9243-GB Wireless Power Pro GUI offers users the flexibility to change operating parameters. Operating parameters, such as Digital Ping Frequency/Duty, Operating Frequency/Duty limits, Rx Detection Sensitivity to lower quiescent currents in standby, over-current sensing thresholds, LED1/2 patterns in specific events, Coil over-temperature sensing thresholds, Q-Factor threshold adjustments, and Error mode alarm timer, can be configured in real-time. For more a detailed list of configurable parameters, open the P9243-GB Wireless Power Pro GUI. Once the settings are configured to the user's preference, a new configuration HEX file can be generated. The user must press Configure to RAM before generating a new HEX file.

### Digital Ping Voltage and Operating Frequency Adjustment

The P9243-GB converges all popular wireless charging protocols including WPC Baseline Power Profile (BPP), Extended Power Profile (EPP), up to 7.5W charging for iPhones, and Android proprietary fast charging modes. Depending on the type and capability of the power supply, the P9243-GB may operate in different modes. To support 7.5W charging for iPhone, Digital Ping Frequency and Max Operating Frequency must remain at 127.7kHz in High Voltage mode only. It is not recommended to keep Low Voltage's Digital Ping Frequency and Max Operating Frequency at 127.7kHz.

### Low Voltage and High Voltage Parameter Adjustment

The P9243-GB separates overlapped parameters into two separate modes: low voltage and high voltage. Low voltage parameters are automatically loaded when the DC source is in the 5V sector. When operating in 5V sector, EPP mode is disabled. Additionally, a few selective parameters are in further split into four sectors: 5V, 9V, 12V, and 16V. High-voltage parameters are automatically loaded when the DC source is above the 5V sector.

### WPC Max Voltage Tuning Adjustment

This parameter is applicable to EPP mode only. These adjustable parameters should be tuned according to WPC1.2.4 defined specification in Maximum Voltage (WPC1.2.4 Section 5.4.10) and Over Voltage Protection (WPC1.2.4 Section 5.4.11).

Once the P9243-GB recognizes a fast load dump, the bridge firmware protection will be triggered, whereby the bridge voltage will immediately be fold-back. Once triggered, the PWM control for step-down regulator will quickly jump to the target buck duty. The buck duty controls the bridge voltage via GPIO\_B7.

### Q-Factor Adjustment

This parameter is applicable to EPP mode only. Prior to each digital ping, the P9243-GB detects and measures the coil's quality factor (Q-factor). If an EPP receiver is present, the transmitter compares its own measured Q-factor with the reference Q-factor provided by the EPP receiver. If the difference is considerably large, the P9243-GB will identify this situation as a WPC-defined FOD being present and cannot move on to the Power Transfer Phase for the purpose of system protection. To aid in recognition of devices placed upon the coil pad surface, it is recommended to set Digital Ping Interval to at least 10 and Analog Ping Interval to at least 80ms. The defaults can be defined based on test. Based on sample test, a typical example of an adjusted threshold and its trend line is shown in Figure 9.

Equation 1

$$(Q - \text{Threshold}) = (Q - R_x) \times \frac{QFOD_{GAIN}}{100} - QFOD_{OFFSET}$$

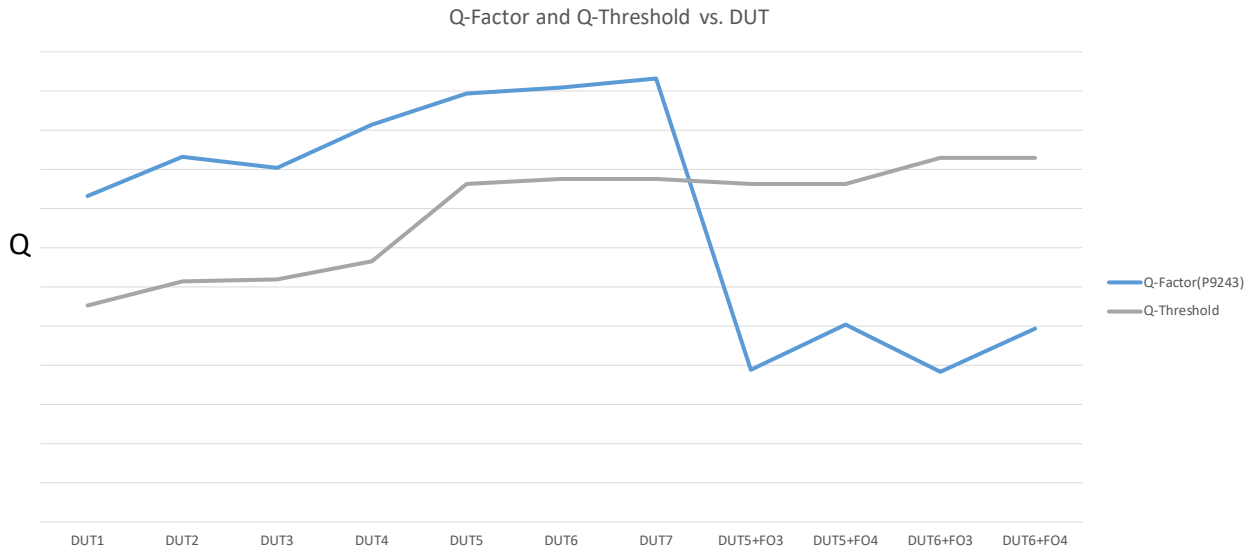
Equation 2

$$(Q - \text{Factor}) < (Q - \text{Threshold})$$

Where:

- Q – Factor = Value of Q returned by P9243
- Q – Threshold = Calculated Q threshold to trigger QFOD
- Q – Rx = Reported Q value of Receiver
- QFOD<sub>GAIN</sub> = Gain used in Q – Threshold calculation
- QFOD<sub>OFFSET</sub> = Offset used in Q – Threshold calculation

Figure 9. Sample Q-Factor Test Data



### FOD (Foreign Object Detection) Tab

The FOD tab of the P9243-GB Wireless Power Pro GUI allows users to adjust the FOD thresholds in real-time. Based on experimentation of at least 3 points with and without a foreign object present, a graphic visualization aid is provided to help with the tuning process. The FOD threshold can be automatically generated using the Auto Calculate button, or it can be manually generated using the Manual Adjust button. Once the settings are configured to the user's preference, a new configuration HEX file can be generated. The user must press Configure to RAM before generating a new HEX file.

The P9243-GB separates the FOD parameters into three operating modes: BPP, EPP (5W), and EPP.

### Program (Programming FLASH/OTP) Tab

The Program tab of the P9243-GB Wireless Power Pro GUI allows users to program FLASH and/or OTP memory. The FLASH and/or OTP memory of the P9243-GB-EVK can be verified with a loaded HEX file in the Firmware Path. From an already programmed P9243-GB, the firmware Hex file can also be extracted and saved to a local target.

### Register (Manually Register Read/Write and Logging) Tab

The Register tab of the P9243-GB Wireless Power Pro GUI allows users to manually log registers up to 32 bits to a maximum of 10 registers at any time. Data Rate and Log Display Format is configurable. Manually Read and Write is also offered in this section.

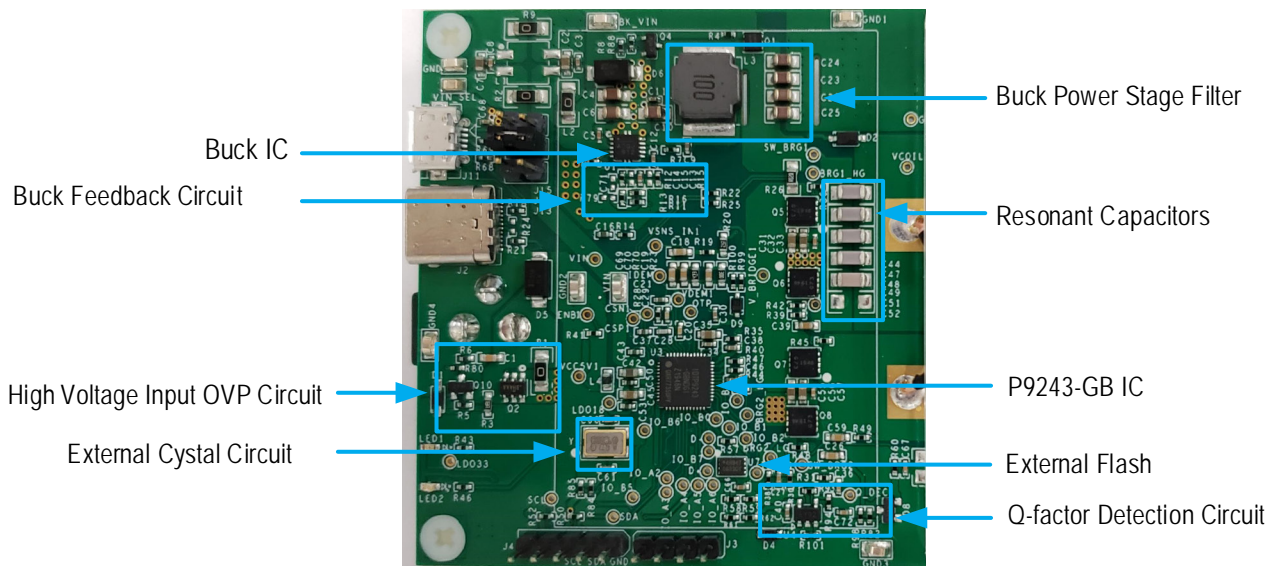
### Generating a New HEX File

It is recommended to complete these steps when generating a HEX file:

1. Program the P9243-GB-EVK with the latest HEX Configuration File from the Renesas website. Start with a golden base hex file first. It is not recommended to daisy-chain the HEX files.
2. Read the defaults before overwriting any parameters by pressing Read Configurations.
3. Enter the desired field value and press Configure to RAM.
4. Confirm acceptance of the desired field value by pressing Read Configurations.
5. Press Generate HEX firmware to create a new HEX file.

Before finalizing firmware for production use, please consult Renesas.

Figure 10. P9243-GB EVB v1.0 Evaluation Board Detail



Note: The P9243-GB has the bootloader and application firmware pre-programmed into the internal one-time programmable (OTP) memory and does not allow users to customize the firmware. The P9243-G, which is pin-to-pin compatible with the P9243-GB, has only a bootloader pre-programmed into the internal OTP memory. Therefore, the P9243-GB must be used in conjunction with an external flash memory. Application firmware is loaded into the external flash for specific system requirements.

The P9243-GB fetches the application firmware from the external flash memory using an SPI interface and executes the code. Users can customize the firmware in external flash and load the new firmware in the flash via the P9243-GB I2C port. The Winbond W25X20CLUXIG is the recommended external flash memory to be used with the P9243-GB.

## External Temperature Sensing – TS

The P9243-GB includes an optional temperature sense input pin, TS, that is used to monitor a remote temperature, such as for a coil or a battery charger. The TS pin voltage can be calculated using Equation 3.

Equation 3

$$V_{TS} = V_{LDO33} \times \frac{NTC}{(NTC + R_{60})}$$

Where:

NTC Thermistor's resistance (TH\_COIL1)

R<sub>60</sub> Pull-up resistor connected to the 3.3V supply voltage on the P9235A-RB Evaluation Board

The over-temperature shutdown is triggered if the voltage on the TS pin is lower than the threshold. To view default thresholds, launch the P9243-GB Wireless Power Pro GUI. The TH\_COIL1 is not populated on the P9243-GB-EVK Evaluation Board.

Figure 11. TH\_COIL1, R60, and RC67 Schematic Location

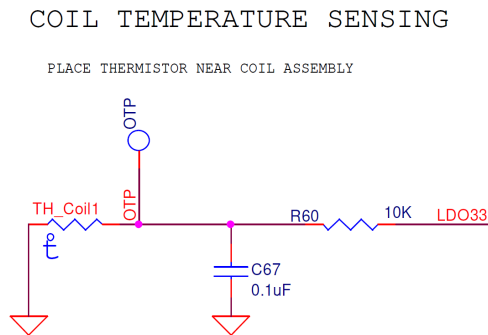
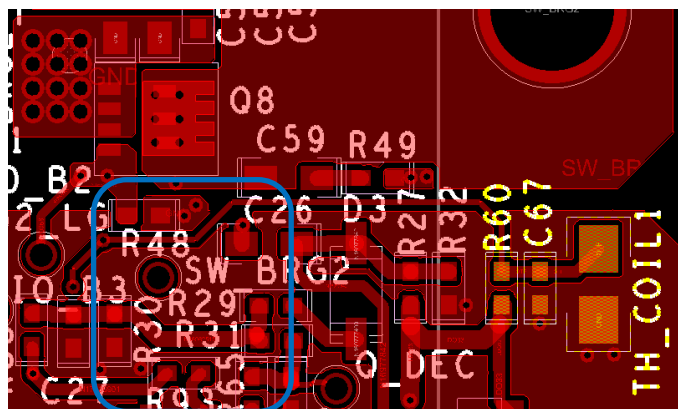


Figure 12. TH\_COIL1, R60, and C67 PCB Location





## Control of External Power Stage DC/DC Buck Regulator – GPIO\_B4 and GPIO\_B7

The P9243-GB is specially designed to support fixed-frequency operation as described in the WPC MP-A11 coil configuration with an external input step-down DC/DC buck regulator. The P9243-GB-EVK uses the on-board DC/DC Buck Regulator IC to adjust the power transfer between the transmitter and receiver. The buck regulator operates at a fixed 500kHz frequency on the board. The buck regulator power stage is designed to accommodate a wide range of input voltages. The feedback loop combined with the external PWM signal are designed for the buck regulator. The resolution of the buck regulator control is approximately 35mV. The buck and external components in the PCB layout should be isolated from any noise generating circuits. For recommended DC/DC buck regulator ICs, please consult Renesas.

For Apple 7.5W charging mode, the P9243-GB supports fixed and precise switching frequency at 127.7kHz, and thus, its bridge input voltage must be adjusted. Another stage of the external buck regulator is added to regulate the input voltage of the full bridge LC circuits. GPIO\_B4 is used to enable/disable this external DC/DC buck regulator. GPIO\_B7 generates a PWM signal that is applied on top of the feedback pin of the buck regulator through a low-pass filter to fine-tune the output voltage of the buck regulator. The resolution of the buck regulator output depends on the buck IC's internal reference voltage, output voltage range, buck regulator compensation design, and resolution of the PWM signal from GPIO\_B7.

Figure 13. Buck Regulator Schematic Location

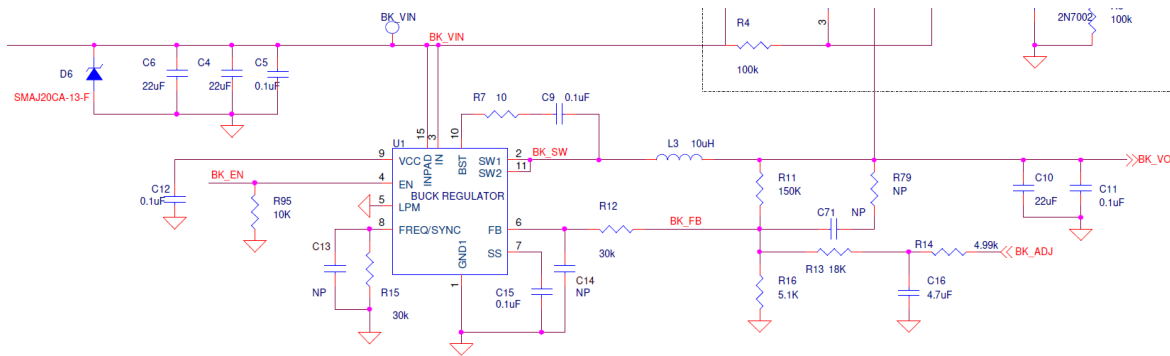
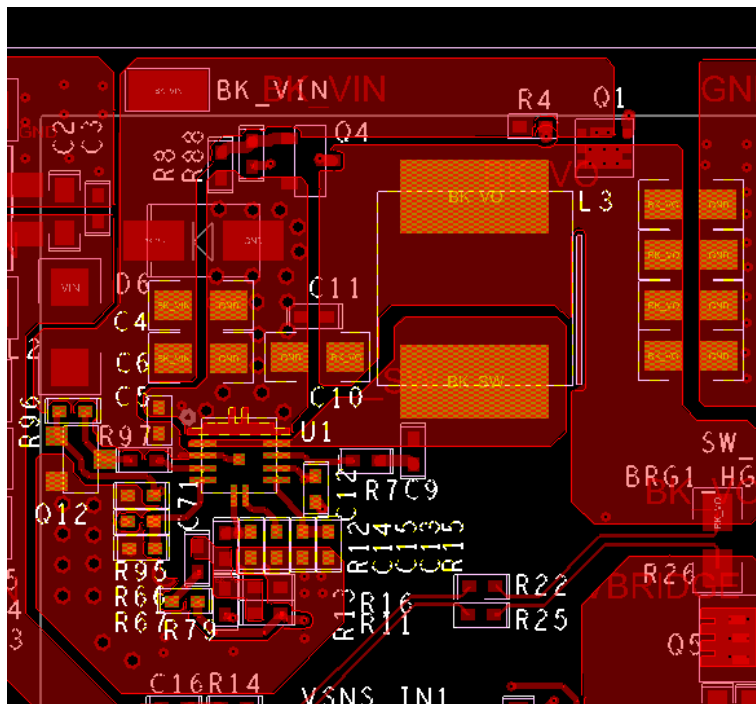


Figure 14. Buck Regulator PCB Location



## Bypass External DC/DC Buck Regulator – GPIO\_A4

When the input voltage is 5V only, the P9243-GB operates in the BPP Mode. However, enabling the external power stage buck regulator at this time compromises the efficiency, thermal performance, and maximum power that can be delivered to the receiver. Under such an application scenario, the P9243-GB will disable the external power stage buck regulator and enable another power path for the input voltage (5V) to be directly applied to the DC/AC inverter. GPIO\_A4 is used to bypass the external power stage buck regulator. In this mode, the device operates in a mode for a fixed input voltage with variable frequency. The operating frequency range depends on the WPC coil configuration specification.

Figure 15. Bypass Path Schematic Location

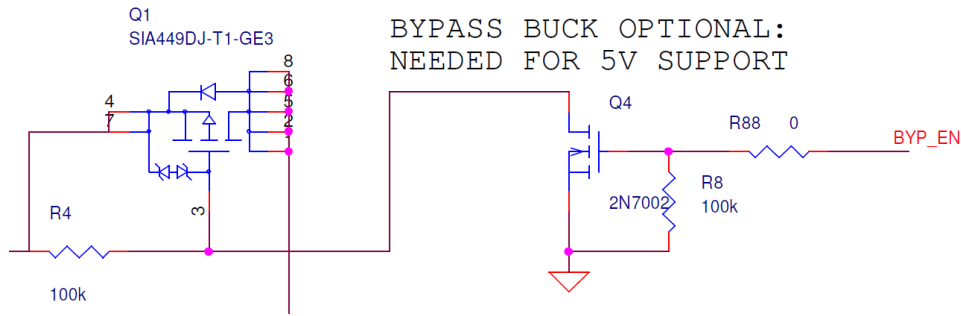
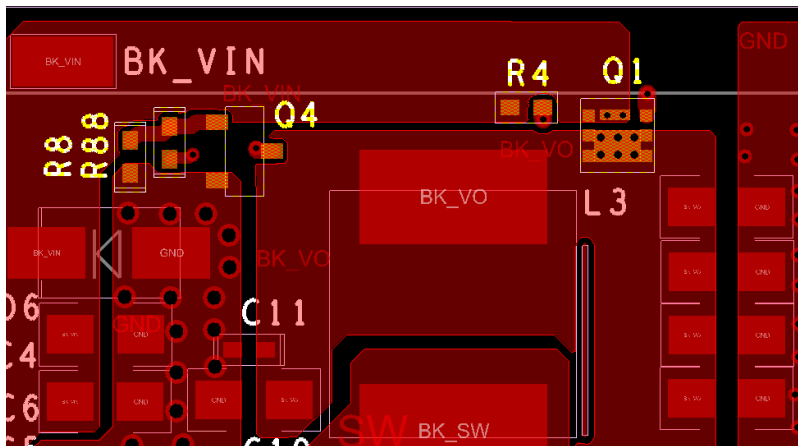


Figure 16. Buck Regulator PCB Location



## External Oscillator – GPIO\_B5 and GPIO\_B6

To guarantee that the operating frequency is precisely at 127.7kHz under different temperature conditions, the P9243-GB requires an external oscillator to provide accurate frequency operation. The PLL and crystal driver circuits inside the P9243-GB guarantee that the internal clock for the ARM® Cortex®-M0 core is synchronized with the external oscillator frequency.

An external 8MHz crystal must be connected between GPIO\_B5 and GPIO\_B6.

Table 1. External Oscillator Selection

Type	Vendor	Part Number	Typical Frequency (MHz)
Crystal Oscillator	ECS Inc.	ECS-80-18-30B-AGN-TR	8MHz + 30ppm

Figure 17. External Crystal Schematic Location

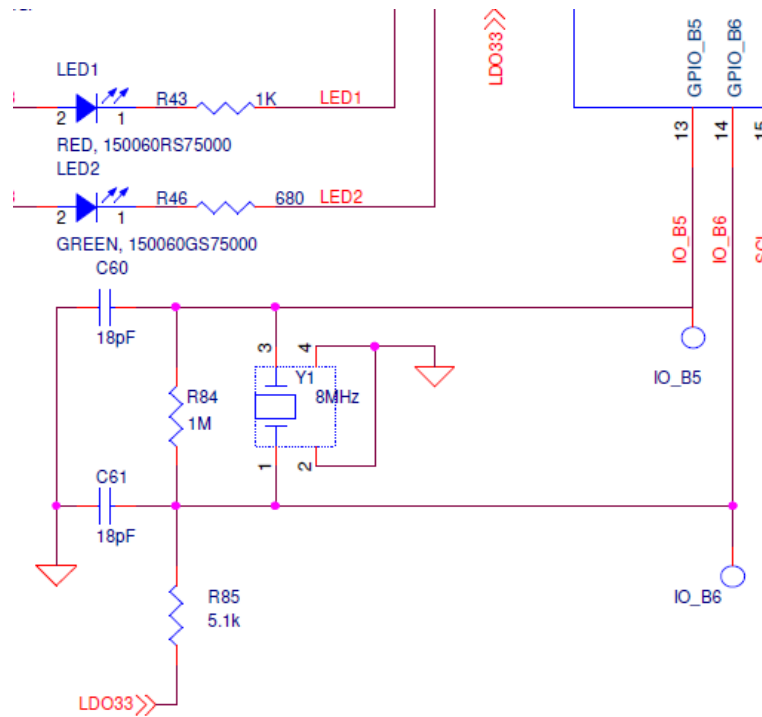
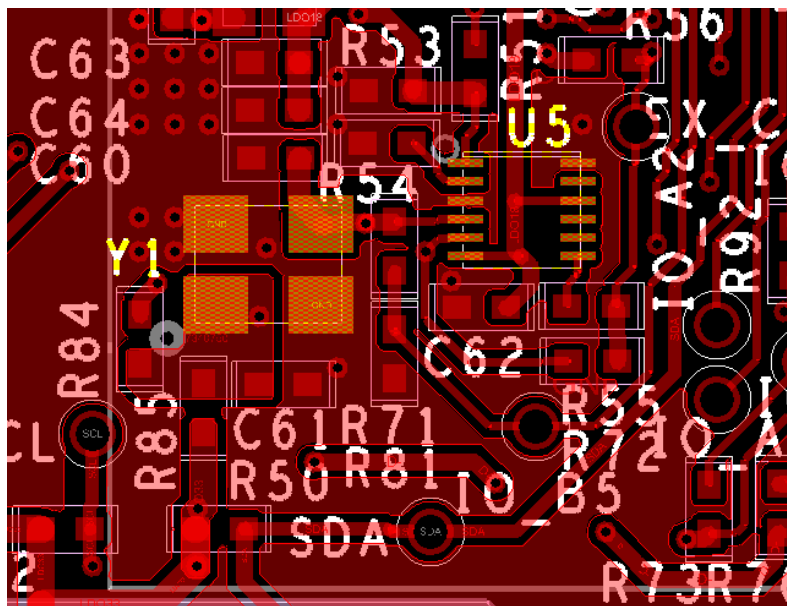


Figure 18. External Crystal PCB Location



## LED Pattern Selection – LED1 and LED2

The P9243-GB uses two LED outputs to indicate power transfer, faults, and operating modes. The LEDs are connected to LED1 and LED2 pins as shown in the typical application schematic. The LED pattern can be modified using the P9243-GB Wireless Power Pro GUI.

There are three states of LED patterns: Charge Complete State, Power Transfer State, and Alarm State. Power Transfer State is triggered upon Power Transfer Phase in System State Register. Alarm State is triggered upon any fault in System Error Register. Charge Complete State is triggered upon receiving either End-Power-Transfer Charge Complete Packet received from Receiver or Charge Status Packet value of 100 received from Receiver.

Once application firmware is boot up, LED2 will be toggle three times at 500 millisecond intervals. The LED pattern for the Boot Up State is not programmable.

## Quality Factor in Digital Ping Phase – QDEC

Before each digital ping, the P9243-GB detects and measures the coil's quality factor (Q-factor). If an EPP receiver is present, the transmitter compares its own measured Q-factor with the reference Q-factor provided by the EPP receiver. If the measured Q-factor is lower than the calculated threshold based on the Receiver's reference Q-factor value, the P9243-GB will identify this situation as a WPC-defined FOD being present and cannot continue on to the Power Transfer Phase for the purpose of system protection. The default Q-factor detection threshold can be adjusted using the P9243-GB Wireless Power Pro GUI.

The method implemented by the P9243-GB to detect the Q-factor is completely based on the nature of the LC resonant circuit. The transmitter LC resonant tank is first charged by a low voltage DC source to ensure that the Rx will not be powered up by using a small amount of energy. Until there is no AC current flowing from the DC source to the LC tank, the DC source voltage will be removed and the LC tank will be shorted. The energy previously stored in the LC resonant tank circulates between the coil and capacitors and generates resonant ringing naturally. The frequency and envelope of the resonant ringing are directly related to the Q-factor. Thus, the Q-factor can be calculated by detecting the envelope of the ringing with the circuit in Figure 19.

The P9243-GB-EVK has implemented the Q-factor detection for WPC EPP receivers. The Q\_DEC pin is used to sample the voltage on the coil. Figure 20 shows the Q-factor detection circuits.

Figure 19. Q-factor Detection Schematic Location

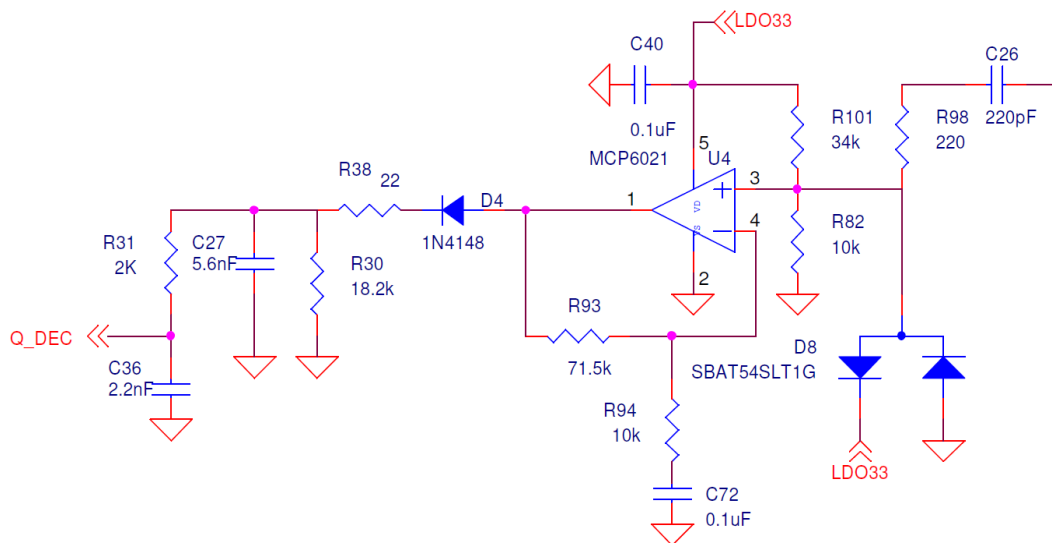
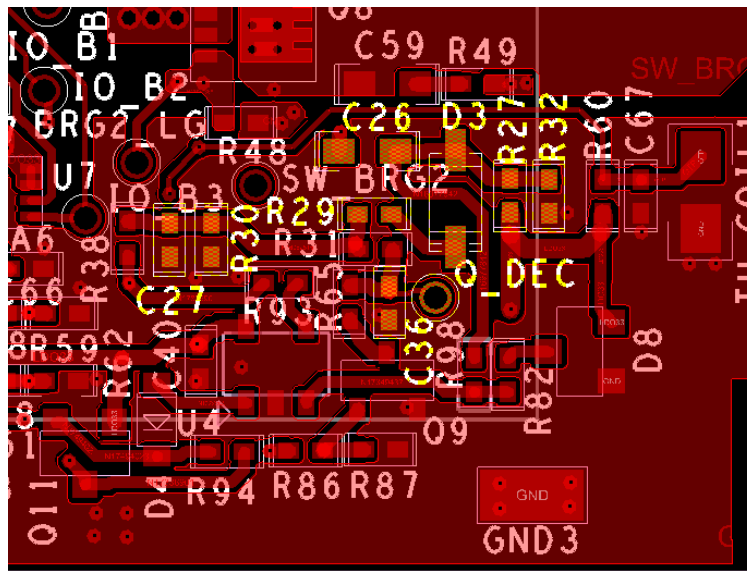


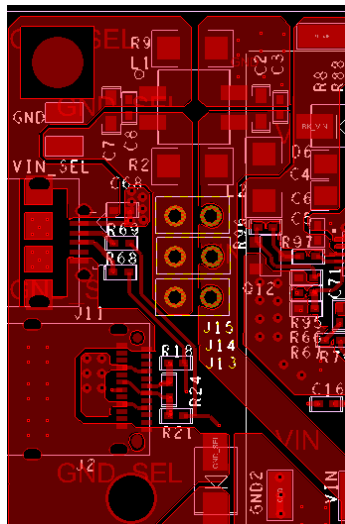
Figure 20. Q-factor PCB Location



### Selection of Input Source and Operation Mode

The P9243-GB-EVK supports different types of AD/DC adaptors and connectors. By selecting the jumpers in Figure 15, the user can select the USB-Micro connector, USB-C connector, or DC jack adaptor.

Figure 21. Input Source Selection Jumpers on the PCB



The P9243-GB-EVK supports a wide range of input DC sources from 5V to 19V. Based on the input source, the P9243-GB-EVK supports different types of receivers. Table 2 lists the P9243-GB-EVK operation modes.

Table 2. P9243-GB-EVK Operation Modes

Input Voltage/Current Rating	Receiver Supported	Operating Frequency
5V/2A	BPP (Bypass External Buck Regulator)	110k – 148k
9V/1.67A	BPP 5W	110kHz – 127.7kHz
	EPP, up to 8W	
	Up to 7.5W charging for iPhones	
12V/2A	BPP 5W	
	EPP, up to 10W	
	Samsung AFC	
	Up to 7.5W charging for iPhones	
15V to 19V/1.8A	BPP 5W	
	EPP, up to 15W	
	Samsung AFC	
	Up to 7.5W charging for iPhones	

## Transmitter Coil

The MP-A11 coils in Table 3 are recommended to be used with the P9243-GB transmitter for 15W applications for optimum performance. The recommended vendor has been tested and verified.

Table 3. Recommend Coil Manufacturer

Output Power	Vendor	Part Number	Inductance at 100kHz	Typical DCR at 25°C
15W	SUNLORD	MQQTC505030S6R3	6.3uH	38mΩ
15W	CYNTEC	WTCL05054F-6R3ABKS-70	6.3uH	38mΩ



## List of Register for Default Configuration

The P9243-GB uses the standard I2C slave implementation protocol to communicate with a host AP or other I2C peripherals. The communication protocol is implemented using 8 bits for data and 16 bits for addresses. The default slave address of the P9243-GB is 61<sub>HEX</sub>. The address of each register is 16 bits. Note that some values require multiple registers and therefore span multiple addresses. For example, the address of the device ID high byte is 0001<sub>HEX</sub> and the low byte address is 0000<sub>HEX</sub>.

The following tables list address locations, field names, available operations (R or RW), default values, and functional descriptions of internally accessible SRAM registers contained within the P9243-GB. The registers are loaded each time the device is powered and cannot be changed except by new firmware programmed into the external Flash device. The SRAM registers are available to make setting changes after the device is powered. These changes are reset to default when the power is cycled or the device is reset. Below are the commonly used SRAM registers for the system configuration or debug.

### Identification Registers

Table 4. Read Register – Device ID Register

Address and Bit	Register Field Name	R/W	Default	Function and Description
0000 <sub>HEX</sub>	Device_ID [15:0]	R	9243 <sub>HEX</sub>	Device ID.

Table 5. Read Register – Firmware Revision

Address and Bit	Register Field Name	R/W	Default	Function and Description
0540 <sub>HEX</sub>	Customer_Code [7:0]	R	-	Customer code.
0541 <sub>HEX</sub>	Project_Code [7:0]	R	-	Project code.
0542 <sub>HEX</sub>	FW_Major_Rev [7:0]	R	-	Major firmware revision.
0543 <sub>HEX</sub>	FW_Minor_Rev [7:0]	R	-	Minor firmware revision.
0544 <sub>HEX</sub>	Month_Code [7:0]	R	-	Month firmware revision.
0545 <sub>HEX</sub>	Day_Code [7:0]	R	-	Day firmware revision.
0546 <sub>HEX</sub>	Year_Code [7:0]	R	-	Year firmware revision.

## State and Status Registers

Table 6. Read Register – System State

Address and Bits	Register Field Name	R/W	Default	Function and Description
0707 <sub>HEX</sub>	System State [7:0]	R	–	0 <sub>DEC</sub> = Detection Phase 1 <sub>DEC</sub> = Selection Phase 2 <sub>DEC</sub> = Ping Phase 3 <sub>DEC</sub> = ID Phase 5 <sub>DEC</sub> = Configuration Phase 6 <sub>DEC</sub> = Negotiation Phase 7 <sub>DEC</sub> = Calibration Phase 8 <sub>DEC</sub> = Power Transfer Phase 9 <sub>DEC</sub> = Renegotiation Phase 10 <sub>DEC</sub> = Remove Power

Table 7. Read Register – System Error Code

Address and Bits	Register Field Name	R/W	Default	Function and Description
0614 <sub>HEX</sub>	System Error [31:0]	R	–	BIT0 = <i>End Power Transfer</i> command from receiver BIT6 = Signal strength BIT7 = WPC packager timeout BIT8 = Control Error Packet timeout BIT9 = Received Power Packet timeout BIT10 = Over-current protection during the Digital Ping Phase BIT11 = Over-voltage BIT12 = Under-voltage BIT13 = FOD in power transfer BIT14 = Over-temperature BIT17 = Over-current BIT21 = Buck error BIT22 = Q-factor FOD

## System Read-Only Registers

Table 8. Read Register – Input Current

Address and Bits	Register Field Name	R/W	Default	Function and Description
0664 <sub>HEX</sub>	Bridge_input_current [15:0]	R	–	Input current ADC reading in mA.

Table 9. Read Register – Input Voltage

Address and Bits	Register Field Name	R/W	Default	Function and Description
0668 <sub>HEX</sub>	Input_voltage [15:0]	R	–	Coil voltage ADC reading in mV.

Table 10. Read Register – Operating Frequency

Address and Bits	Register Field Name	R/W	Default	Function and Description
0632 <sub>HEX</sub>	Freq_Cnt [15:0]	R	–	Operating frequency count. Operating frequency changes based on the CEP packets from the receiver. $f_{OP} = \frac{106667}{\text{FREQ\_CNT}[15:0] - 2}$

Table 11. Read Register – Transmitter Duty Cycle

Address and Bits	Register Field Name	R/W	Default	Function and Description
05CF <sub>HEX</sub>	Transmitter_Duty [7:0]	R	–	Transmitter duty cycle. Duty cycle changes based on the CEP packets from the receiver. $D(\%) = \frac{\text{FREQ\_CNT}[7:0]}{510}$

Table 12. Read Register – Receiver Reported Q-Factor Value

Address and Bits	Register Field Name	R/W	Default	Function and Description
083D <sub>HEX</sub>	Reported_Q [7:0]	R	–	Reported Q value of Receiver.

Table 13. Read Register – Measured Q Factor Value

Address and Bits	Register Field Name	R/W	Default	Function and Description
050A <sub>HEX</sub>	Q_factor [7:0]	R	–	Measured Q value of Transmitter.

Table 14. Read Register – Threshold Q Factor Value

Address and Bits	Register Field Name	R/W	Default	Function and Description
050A <sub>HEX</sub>	Q_threshold [7:0]	R	–	<p>Calculated Q threshold value to trigger QFOD. QFOD alarm triggers when Q_Factor &lt; Q_Threshold. Gain and Offset can be adjusted using the Configuration Registers.</p> $Q\_threshold = \frac{\text{Reported\_Q} \times \text{Gain}}{100} + \text{Offset}$

Table 15. Read Register – Potential Power

Address and Bits	Register Field Name	R/W	Default	Function and Description
083E <sub>HEX</sub>	Potential_Power [7:0]	R	–	Transmitter potential power in W.

Table 16. Read Register – Transmitter Power

Address and Bits	Register Field Name	R/W	Default	Function and Description
0880 <sub>HEX</sub>	Tx_Power [31:0]	R	–	Power transmitted in mW.

Table 17. Read Register – Received Power

Address and Bits	Register Field Name	R/W	Default	Function and Description
0884 <sub>HEX</sub>	Rx_Power [31:0]	R	–	Received Power in mW from the RPP packet received from the Receiver.

Table 18. Read Register – FOD Threshold

Address and Bits	Register Field Name	R/W	Default	Function and Description
088C <sub>HEX</sub>	FOD_Threshold [15:0]	R	–	<p>Gain and Offset values change based on the RPP packet received from the Receiver. Value is in mW. FOD alarm triggers when FOD Threshold &lt; Power Loss.</p> $\text{FOD Threshold} = (\text{GAIN} \times \text{RPP})/100 + \text{OFFSET}$

Table 19. Read Register – Remote Temperature Sensing Voltage

Address and Bits	Register Field Name	R/W	Default	Function and Description
06A4 <sub>HEX</sub>	Thermistor pin voltage [15:0]	R	–	Thermistor raw ADC reading. Value in ADC count.

Table 20. Read Register – Adaptor Type

Address and Bits	Register Field Name	R/W	Default	Function and Description
070E <sub>HEX</sub>	Adaptor Type [7:0]	R	–	0 <sub>DEC</sub> = None 1 <sub>DEC</sub> = USB SDP 2 <sub>DEC</sub> = USB DCP 3 <sub>DEC</sub> = USB CDP 5 <sub>DEC</sub> = QC 2.0 6 <sub>DEC</sub> = QC 3.0 7 <sub>DEC</sub> = Reserved 8 <sub>DEC</sub> = Adaptor Detect Error 9 <sub>DEC</sub> = QC 27W 10 <sub>DEC</sub> = Reserved 11 <sub>DEC</sub> = USB FCP 12 <sub>DEC</sub> = USB SCP 13 <sub>DEC</sub> = Reserved

Table 21. Read/Write Register – Rx Manufacture ID

Address and Bits	Register Field Name	R/W	Default	Function and Description
0892 <sub>HEX</sub>	RX_Manufacture_ID [7:0]	R	–	RX WPC Manufacturer code (PRMC ID). The code is assigned by WPC to each company producing compliant products.

Table 22. Read/Write Register – Rx Type

Address and Bits	Register Field Name	R/W	Default	Function and Description
0893 <sub>HEX</sub>	RX_Type [7:0]	R	–	Displays the Rx Power Profile Type Flag. 0 <sub>DEC</sub> = BPP 1 <sub>DEC</sub> = EPP (5W) 2 <sub>DEC</sub> = EPP 3 <sub>DEC</sub> = AFC 4 <sub>DEC</sub> = iOS

Table 23. Read/Write Register – Charge Status Packet

Address and Bits	Register Field Name	R/W	Default	Function and Description
0718 <sub>HEX</sub>	Charge_Status [7:0]	R	–	Displays the data value of the Charge Status Packet from Receiver. View LED pattern registers for defaults. 100 <sub>DEC</sub> = LED pattern is change to Charge Complete State. Others = LED pattern is changed to Power Transfer State.

## Configuration Registers

Default values can be configured using the P9243-GB Wireless Pro GUI. Visit the P9243-GB-EVK webpage and download the latest version of the P9243-GB Wireless Power Pro GUI, USB drivers, and the P9243-GB A11a Configuration Flash HEX File. The software provides an intuitive GUI for reading and writing to P9243-GB SRAM registers and for generating custom user configurations for the external Flash. Launch the P9243-GB Wireless Power Pro GUI to view more. The following registers are commonly used for system configuration or debug.

Table 24. Read/Write Register – Tx Manufacture ID Adjust

Address and Bits	Register Field Name	R/W	Default	Function and Description
0918 <sub>HEX</sub>	TX_Manufacture_ID [15:0]	R/W	0x0050	TX WPC Manufacturer code (PRMC ID). The code is assigned by WPC to each company producing compliant products.

Table 25. Read/Write Register – Over Current Threshold Adjust

Address and Bits	Register Field Name	R/W	Default	Function and Description
08F4 <sub>HEX</sub>	OVP_5V [15:0]	R/W	2500	Over current protection (OCP) threshold in mA for 5V Vin.
08F6 <sub>HEX</sub>	OVP_9V [15:0]	R/W	2500	Over current protection (OCP) threshold in mA for 9V Vin.
08F8 <sub>HEX</sub>	OVP_12V [15:0]	R/W	1800	Over current protection (OCP) threshold in mA for 12V Vin.
08FA <sub>HEX</sub>	OVP_16V [15:0]	R/W	1800	Over current protection (OCP) threshold in mA for 16V Vin.

Table 26. Read/Write Register – Low Voltage and Over Voltage Threshold Adjust

Address and Bits	Register Field Name	R/W	Default	Function and Description
091E <sub>HEX</sub>	LVP_5V [15:0]	R/W	4200	Low voltage protection (LVP) threshold in mV for 5V Vin.
0920 <sub>HEX</sub>	OVP_5V [15:0]	R/W	6500	Over voltage protection (OVP) threshold in mV for 5V Vin.
0922 <sub>HEX</sub>	LVP_9V [15:0]	R/W	8400	Low voltage protection (LVP) threshold in mV for 9V Vin.
0924 <sub>HEX</sub>	OVP_9V [15:0]	R/W	9600	Over voltage protection (OVP) threshold in mV for 9V Vin.
0926 <sub>HEX</sub>	LVP_12V [15:0]	R/W	8400	Low voltage protection (LVP) threshold in mV for 12V Vin.
0928 <sub>HEX</sub>	OVP_12V [15:0]	R/W	13200	Over voltage protection (OVP) threshold in mV for 12V Vin.
092A <sub>HEX</sub>	LVP_16V [15:0]	R/W	14000	Low voltage protection (LVP) threshold in mV for 16V Vin.
092C <sub>HEX</sub>	OVP_16V [15:0]	R/W	19700	Over voltage protection (OVP) threshold in mV for 16V Vin.

Table 27. Read/Write Register – Over Temperature Threshold Adjust

Address and Bits	Register Field Name	R/W	Default	Function and Description
0930 <sub>HEX</sub>	OTP_Recovery [15:0]	R/W	–	Over temperature protection (OTP) recovery threshold. Thermistor voltage needs to go above this value to restart the normal operation. Value in ADC count.
0932 <sub>HEX</sub>	OTP_Trigger [15:0]	R/W	–	Over temperature protection (OTP) trigger threshold. Thermistor voltage needs to go below this value to trigger OTP. Value in ADC count.



Table 28. Read/Write Register – WPC Tuning Threshold Adjust

Address and Bits	Register Field Name	R/W	Default	Function and Description
096A <sub>HEX</sub>	WPC_Coil_Current_thd [15:0]	R/W	180	Coil Current Threshold for WPC Maximum Voltage Test. Value in mA. Used for WPC conformance.
096C <sub>HEX</sub>	WPC_LD_BuckDuty [15:0]	R/W	775	Controls the VBRG fold back after a load dump occurs for WPC Maximum Voltage test. Used for WPC conformance. Duty Cycle[%] = (1067 – value)/1067 For example, $\frac{1067-775}{1067} = 27.37\%$

Table 29. Read/Write Register – FOD Region Select Adjust

Address and Bits	Register Field Name	R/W	Default	Function and Description
08C0 <sub>HEX</sub>	FOD_Pwr_EPP_0 [15:0]	R/W	6200	Extended Power Profile (>5W). Threshold that separates region 0 and region 1 for FOD Protection in mW.
08C2 <sub>HEX</sub>	FOD_Pwr_EPP_1 [15:0]	R/W	11700	Extended Power Profile (>5W). Threshold that separates region 2 and region 3 for FOD Protection in mW.
08C4 <sub>HEX</sub>	FOD_Pwr_BPP_0 [15:0]	R/W	2000	Baseline Power Profile. Threshold that separates region 0 and region 1 for FOD Protection in mW.
08C6 <sub>HEX</sub>	FOD_Pwr_BPP_1 [15:0]	R/W	5900	Baseline Power Profile. Threshold that separates region 2 and region 3 for FOD Protection in mW.
08C8 <sub>HEX</sub>	FOD_Pwr_EPP_LP_0 [15:0]	R/W	2400	Extended Power Profile (5W). Threshold that separates region 0 and region 1 for FOD Protection in mW.
08CA <sub>HEX</sub>	FOD_Pwr_EPP_LP_1 [15:0]	R/W	4500	Extended Power Profile (5W). Threshold that separates region 2 and region 3 for FOD Protection in mW.

Table 30. Read/Write Register – FOD Gain Select Adjust

Address and Bits	Register Field Name	R/W	Default	Function and Description
08CC <sub>HEX</sub>	FOD_G_EPP_0 [15:0]	R/W	2	Extended Power Profile (>5W). Gain used in FOD threshold calculation in region 0.
08CE <sub>HEX</sub>	FOD_G_EPP_1 [15:0]	R/W	5	Extended Power Profile (>5W). Gain used in FOD threshold calculation in region 1.
08D0 <sub>HEX</sub>	FOD_G_EPP_2 [15:0]	R/W	11	Extended Power Profile (>5W). Gain used in FOD threshold calculation in region 2.
08D2 <sub>HEX</sub>	FOD_G_BPP_0 [15:0]	R/W	5	Baseline Power Profile. Gain used in FOD threshold calculation in region 0.
08D4 <sub>HEX</sub>	FOD_G_BPP_1 [15:0]	R/W	8	Baseline Power Profile. Gain used in FOD threshold calculation in region 1.
08D6 <sub>HEX</sub>	FOD_G_BPP_2 [15:0]	R/W	7	Baseline Power Profile. Gain used in FOD threshold calculation in region 2.
08D8 <sub>HEX</sub>	FOD_G_EPP_LP_0 [15:0]	R/W	25	Extended Power Profile (5W). Gain used in FOD threshold calculation in region 0.
08DA <sub>HEX</sub>	FOD_G_EPP_LP_1 [15:0]	R/W	25	Extended Power Profile (5W). Gain used in FOD threshold calculation in region 1.
08DC <sub>HEX</sub>	FOD_G_EPP_LP_2 [15:0]	R/W	25	Extended Power Profile (5W). Gain used in FOD threshold calculation in region 2.

Table 31. Read/Write Register – FOD Offset Select Adjust

Address and Bits	Register Field Name	R/W	Default	Function and Description
08DE <sub>HEX</sub>	FOD_O_EPP_0 [15:0]	R/W	800	Extended Power Profile (>5W). Offset used in FOD threshold calculation in region 0 in mW. This register is signed.
08E0 <sub>HEX</sub>	FOD_O_EPP_1 [15:0]	R/W	650	Extended Power Profile (>5W). Offset used in FOD threshold calculation in region 1 in mW. This register is signed.
08E2 <sub>HEX</sub>	FOD_O_EPP_2 [15:0]	R/W	-56	Extended Power Profile (>5W). Offset used in FOD threshold calculation in region 2 in mW. This register is signed.
08E4 <sub>HEX</sub>	FOD_O_BPP_0 [15:0]	R/W	630	Baseline Power Profile. Offset used in FOD threshold calculation in region 0 in mW. This register is signed.
08E6 <sub>HEX</sub>	FOD_O_BPP_1 [15:0]	R/W	575	Baseline Power Profile. Offset used in FOD threshold calculation in region 1 in mW. This register is signed.
08E8 <sub>HEX</sub>	FOD_O_BPP_2 [15:0]	R/W	625	Baseline Power Profile. Offset used in FOD threshold calculation in region 2 in mW. This register is signed.
08EA <sub>HEX</sub>	FOD_O_EPP_LP_0 [15:0]	R/W	460	Extended Power Profile (5W). Offset used in FOD threshold calculation in region 0 in mW. This register is signed.
08EC <sub>HEX</sub>	FOD_O_EPP_LP_1 [15:0]	R/W	470	Extended Power Profile (5W). Offset used in FOD threshold calculation in region 1 in mW. This register is signed.
08EE <sub>HEX</sub>	FOD_O_EPP_LP_2 [15:0]	R/W	470	Extended Power Profile (5W). Offset used in FOD threshold calculation in region 2 in mW. This register is signed.

Table 32. Read/Write Register – FOD Disable Adjust

Address and Bits	Register Field Name	R/W	Default	Function and Description
08F4 <sub>HEX</sub>	FOD_Enable [7:0]	R/W	1	Disables FOD Protection. To be used only in development stage. Do not disable in final production. 0 <sub>DEC</sub> = FOD Disabled 1 <sub>DEC</sub> = FOD Enabled

Table 33. Read/Write Register – LED Pattern Adjust

Address and Bits	Register Field Name	R/W	Default	Function and Description
0900 <sub>HEX</sub>	FC_Red_LED_ON [15:0]	R/W	0	Red LED on time in Charge Complete State. Value in ms.
0902 <sub>HEX</sub>	FC_Red_LED_OFF [15:0]	R/W	0	Red LED off time in Charge Complete State. Value in ms.
0904 <sub>HEX</sub>	FC_Green_LED_ON [15:0]	R/W	500	Green LED on time in Charge Complete State. Value in ms.
0906 <sub>HEX</sub>	FC_Green_LED_OFF [15:0]	R/W	500	Green LED off time in Charge Complete State. Value in ms.
0908 <sub>HEX</sub>	Chg_Red_LED_ON [15:0]	R/W	0	Red LED on time in Power Transfer State. Value in ms.
090A <sub>HEX</sub>	Chg_Red_LED_OFF [15:0]	R/W	0	Red LED off time in Power Transfer State. Value in ms.
090C <sub>HEX</sub>	Chg_Green_LED_ON [15:0]	R/W	1000	Green LED on time in Power Transfer State. Value in ms.
090E <sub>HEX</sub>	Chg_Green_LED_OFF [15:0]	R/W	0	Green LED off time in Power Transfer State. Value in ms.
0910 <sub>HEX</sub>	Err_Red_LED_ON [15:0]	R/W	200	Red LED on time in Alarm State. Value in ms.
0912 <sub>HEX</sub>	Err_Red_LED_OFF [15:0]	R/W	200	Red LED off time in Alarm State. Value in ms.
0914 <sub>HEX</sub>	Err_Green_LED_ON [15:0]	R/W	0	Green LED on time in Alarm State. Value in ms.
0916 <sub>HEX</sub>	Err_Green_LED_OFF [15:0]	R/W	0	Green LED off time in Alarm State. Value in ms.

Table 34. Read/Write Register – Sleep Timer Adjust

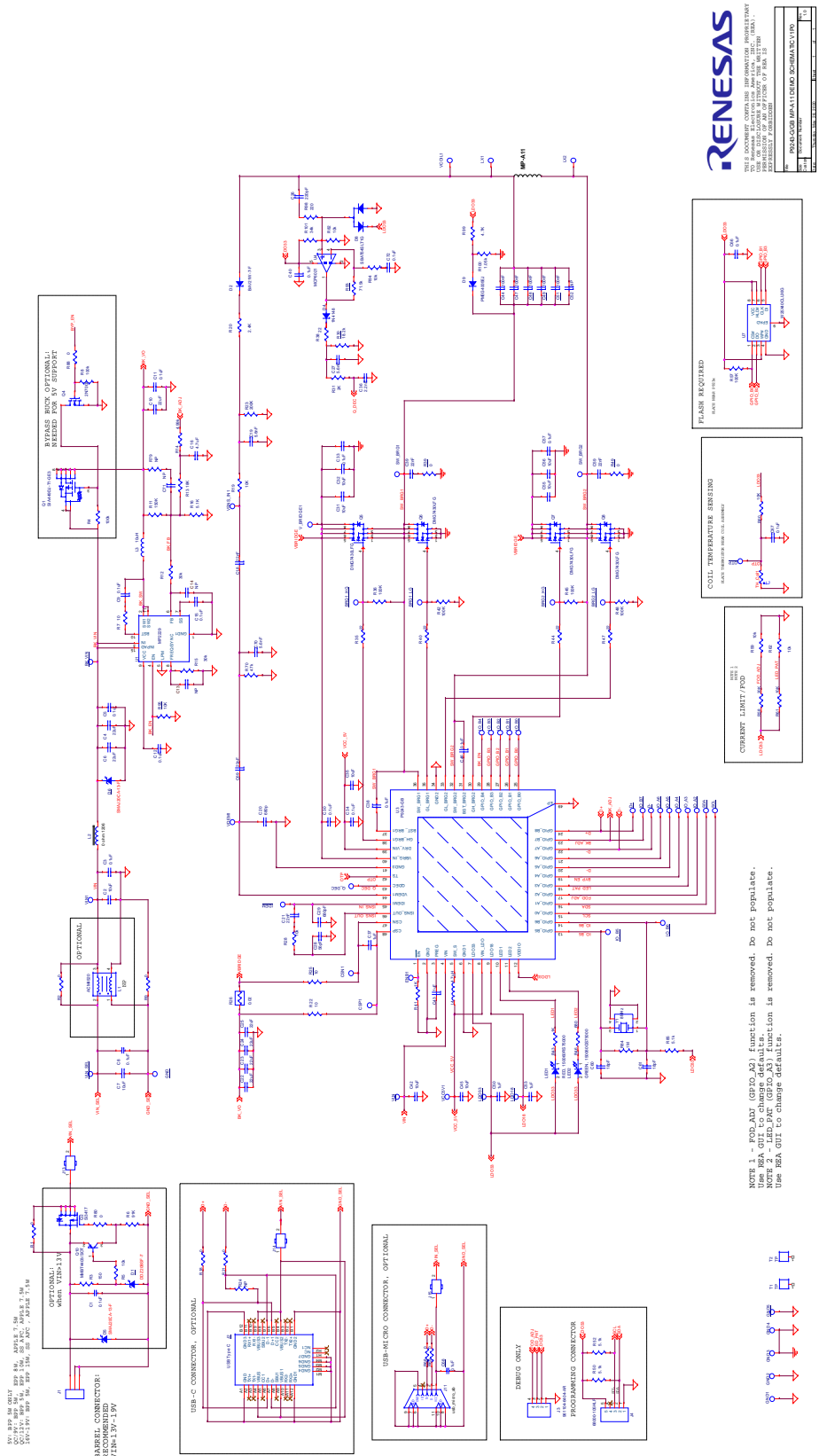
Address and Bits	Register Field Name	R/W	Default	Function and Description
091A <sub>HEX</sub>	Chg_Complete_Timer [15:0]	R/W	60	Sleep timer for which transmitter turns off when it receives a Charge Complete End of Power Transfer (EPT) packet. Value in seconds.
091C <sub>HEX</sub>	Error_Timer [15:0]	R/W	60	Sleep timer for which transmitter turns off when in Alarm State. Value in seconds.

Table 35. Read/Write Register – Q-Factor Adjust

Address and Bits	Register Field Name	R/W	Default	Function and Description
0943 <sub>HEX</sub>	Q_Threshold_Gain [7:0]	R/W	34	Gain for Q-factor threshold calculation
0944 <sub>HEX</sub>	Q_Threshold_Offset [7:0]	R/W	45	Offset for Q-factor threshold calculation
0946 <sub>HEX</sub>	Q_Vbridge_adjust [15:0]	R/W	2500	Bridge voltage in mV adjust during Q measurement. Bridge voltages lower than 1500mV is not recommended.

# P9243-GB EVB Application Schematic v1.0

## P9243-G/GB MP-A11 DEMO SCHEMATIC V1P0



**RENESAS**

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO RENESAS. IT IS TO BE USED ONLY FOR THE PURPOSES SPECIFIED HEREIN. RENESAS ASSUMES NO LIABILITY FOR DAMAGES OF ANY KIND ARISING FROM THE USE OF THIS DOCUMENT. © 2021 RENESAS ELECTRONICS CORPORATION. ALL RIGHTS RESERVED. P9243-GB-EVK-APP-001

**P9243-GB EVALUATION BOARD SCHEMATIC V1.0**

Doc No.	P9243-GB-EVK-APP-001
Rev.	1.0
Date	2021.02.25

## Bill of Materials (BOM)

Table 3. P9243-GB-EVK BOM

Item	QTY	Reference	Description	Value	PCB Footprint	Part Number
1	8	VIN1,GND1,GND2,GND3,GND4,VIN_SEL,GND,BK_VIN	TEST POINT PC MINIATURE SMT	TP	test_pt_sm_135x70	5015
2	38	V_BRIDGE1,VSNS_IN1,VDEM1,VCOIL1,SW_BRG1,IO_B1,ENB1,CSP1,CSN1,BRG1_LG,BRG1_HG,SW_BRG2,IO_B2,IO_A2,BRG2_LG,BRG2_HG,IO_B3,IO_A3,IO_B4,IO_A4,IO_B5,IO_A5,GND5,IO_B6,IO_A6,IO_B7,LDO18,LDO33,VCC5V1,VIN,SDA,SCL,Q_DEC,OTP,IO_B0,IDEM,D-,D+	30 GAUGE WIRE PAD	PTH_TP	TEST_PT30DPAD	NP
3	1	C1	CAP CER 0.1UF 25V X7R 0603	0.1uF	603	CC0603KRX7R8BB104
4	9	C2,C7,C31,C32,C35,C42,C45,C55,C56	CAP CER 10UF 25V X5R 0603	10uF	603	C1608X5R1E106M080AC
5	18	C3,C5,C8,C9,C11,C12,C15,C30,C33,C34,C38,C40,C46,C57,C66,C67,C68,C72	CAP CER 0.1UF 25V X7R 0402	0.1uF	402	CC0402KRX7R8BB104
6	7	C4,C6,C10,C22,C23,C24,C25	CAP CER 22UF 25V X5R 0805	22uF	805	GRM21BR61E226ME44L
7	4	C13,C14,R24,C71	NP	NP	402	NP
8	1	C16	CAP CER 4.7UF 16V X5R 0402	4.7uF	402	CL05A475M05NUNC
9	2	C18,C69	CAP CER 0.022UF 50V X7R 0603	22nF	603	GCJ188R71H223KA01D
10	2	C19,C70	CAP CER 5600PF 50V X7R 0603	5.6nF	603	CC0603KRX7R9BB562
11	1	C20	CAP CER 680PF 50V X7R 0402	680p	402	CL05B681KB5NNNC
12	1	C21	CAP CER 0.022UF 25V X7R 0402	22nF	402	GRM155R71E223JA61D
13	1	C26	CAP CER 220PF 50V X7R 0603	220pF	603	CC0603JRX7R9BB221
14	1	C27	CAP CER 5600PF 16V X7R 0402	5.6nF	402	CC0402KRX7R7BB562
15	1	C28	CAP CER 56PF 50V C0G/NP0 0402	56pF	402	CL05C560JB5NNNC
16	1	C29	CAP CER 680PF 50V X7R 0402	680pF	402	CL05B681KB5NNNC
17	1	C36	CAP CER 2200PF 10V X7R 0402	2.2nF	402	CC0402KRX7R6BB222
18	4	C37,C43,C50,C53	CAP CER 1UF 25V X5R 0402	1uF	402	CGB2A1X5R1E105M033BC
19	2	C39,C59	CAP CER 0.022UF 50V X7R 0603	22nF	603	CL10B223KB8NNNC

Item	QTY	Reference	Description	Value	PCB Footprint	Part Number
20	5	C44,C47,C48,C49,C51	CAP CER 100nF 100V C0G 1206	100nF	1206	C3216C0G2A104K160 AC
21	1	C52	NP	NP	1206	NP
22	2	C60,C61	CAP CER 18pF 50V 5% C0G/NP0 0402	18pF	402	GRM1555C1H180JA01 D
23	1	D1	DIODE ZENER 20V 500MW SOD323F	DDZ20BSF-7	sod123	DDZ20BSF-7
24	1	D2	DIODE GEN PURP 200V 200MA SOD123	BAV21W-7-F	sod123	BAV21W-7-F
25	1	D4	DIODE GEN PURP 75V 150MA SOD323	1N4148	sod-323	1N4148WX-TP
26	2	D5,D6	TVS DIODE 20V 32.4V SMA	SMAJ20CA-13-F	SMAJ20CA	SMAJ20CA-13-F
27	1	D8	DIODE ARRAY SCHOTTKY 30V SOT23-3	SBAT54SLT1G	SOT-23	SBAT54SLT1G
28	1	D9	SHTKY DIODE PURP 200V 500MA	PMEG4005EJ	SOD323F	PMEG4005EJ
29	1	J1	CONN PWR JACK 2.5X5.5MM SOLDER	AC_Adapter	CONN_POWER_JACK5_5MM	PJ-002AH
30	1	J2	CONN RCP USB3.1 TYPEC 24P SMD RA	USB Type C	USB-C12401610E4	12401610E4#2A
31	1	J3	4 Positions Header, Unshrouded Connector 0.100" (2.54mm) Through Hole Gold or Gold, GXT™	961104-6404-AR	sjp-4	961104-6404-AR
32	1	J4	BERGSTIK II .100" SR STRAIGHT	68000-105HLF	sjp5	68000-105HLF
33	1	J11	CONN RCPT USB2.0 MICRO AB SMD RA	ZX62D-AB-5P8(30)	usb_micro_ab	ZX62D-AB-5P8(30)
34	3	J13,J14,J15	CONN HEADER VERT 2POS 2.54MM	JMP	sjp2	68000-102HLF
35	1	LED1	LED RED CLEAR 0603 SMD	RED, 150060RS75000	0603_diode	150060RS75000
36	1	LED2	LED GREEN CLEAR 0603 SMD	GREEN, 150060GS75000	0603_diode	150060GS75000
37	2	LX1,LX2	30 GAUGE WIRE PAD	PTH_TP	TP_TXCoil	NP
38	1	L1	Common mode EMI choke	ACM4520	EMI_TDK_ACM4520L	ACM4520-901-2P-T-000
39	1	L2	RES SMD 0 OHM JUMPER 1/4W 1206	Zero ohm	0 ohm 1206	RC1206JR-070RL
40	1	L3	29mOhm, 3.6A inductor	10uH	5x5-10x10	SWPA8040S100MT
41	1	L4	FIXED IND 4.7UH 620MA 550 MOHM	4.7uH	L0603	LQM18PN4R7MFRL



Item	QTY	Reference	Description	Value	PCB Footprint	Part Number
42	1	Q1	MOSFET P-CH 30V 12A SC70-6	SIA449DJ-T1-GE3	sc70_6ld_fet	SIA449DJ-T1-GE3
43	1	Q2	P-Channel 30 V , 35mOhm, 15nC MOSFET	Si3417	SOT-23-6	Si3417DV-T1-GE3
44	1	Q4	N-Channel 60-V (D-S) MOSFET	2N7002	SOT23_3	2N7002KT1G
45	4	Q5,Q6,Q7,Q8	MOSFET N-CH 30V 10.5A PWRDI3333	DMG7430LFG	powerdi3333_8ld_fet	DMG7430LFG-7
46	1	Q10	TRANS PNP 40V 0.6A SOT-23	MMBT4403/SOT	SOT-23	MMBT4403LT3G
47	3	R1,R2,R9	RES SMD 0.0 OHM JUMPER 1/4W 1206	0	1206	RC1206JR-070R
48	1	R3	RES SMD 150 OHM 1% 1/10W 0603	150	603	RC0603FR-07150RL
49	2	R4,R8	RES SMD 100K OHM 1% 1/16W 0402	100k	402	RC0402FR-07100KL
50	7	R5,R19,R59,R60,R61,R82,R94	RES SMD 10K OHM 1% 1/16W 0402	10k	402	RC0402FR-0710KL
51	1	R6	RES SMD 91K OHM 1% 1/16W 0402	91K	402	RC0402FR-0791K
52	2	R7,R25	RES SMD 10 OHM 1% 1/16W 0402	10	402	RC0402FR-0710RL
53	1	R11	RES SMD 150K OHM 1% 1/16W 0402	150K	402	RC0402FR-07150K
54	2	R12,R15	RES SMD 30K OHM 1% 1/16W 0402	30k	402	RC0402FR-0730KL
55	1	R13	RES SMD 18K OHM 1% 1/10W 0402	18K	402	ERJ-2RKF1802X
56	1	R14	RES SMD 4.99K OHM 1% 1/16W 0402	4.99k	402	RC0402FR-074K99L
57	4	R16,R50,R52,R85	RES SMD 5.1K OHM 1% 1/16W 0402	5.1k	402	RC1005F512CS
58	8	R18,R21,R39,R49,R68,R69,R80,R88	RES SMD 0 OHM JUMPER 1/16W 0402	0	402	RC0402JR-070RL
59	1	R20	RES SMD 2.4K OHM 1% 1/10W 0603	2.4K	603	RC0603FR-072K4L
60	1	R22	RES SMD 10 OHM 1% 1/16W 0402	10	402	RC0402FR-0710RL
61	1	R23	RES SMD 200K OHM 1% 1/10W 0603	200K	603	RC1608F204CS
62	1	R26	RES SMD 0.02 OHM 1% 1/3W 0805	0.02	805	UCR10EVHFSR020
63	2	R28,R62	RES SMD 10K OHM 1% 1/16W 0402	10k	402	RC0402FR-0710KP
64	1	R30	RES SMD 18.2K OHM 1% 1/16W 0402	18.2k	402	RC0402FR-0718K2L
65	1	R31	RES SMD 2K OHM 1% 1/16W 0402	2K	402	RC0402FR-072KL
66	4	R35,R40,R44,R47	RES SMD 22 OHM 5% 1/10W 0402	22	402	ERJ-2GEJ220X
67	5	R36,R42,R45,R48,R57	RES SMD 100K OHM 5% 1/10W 0402	100K	402	ERJ-2GEJ104X

Item	QTY	Reference	Description	Value	PCB Footprint	Part Number
68	1	R38	RES SMD 22 OHM 1% 1/16W 0402	22	402	RC0402FR-0722RL
69	2	R41,R43	RES SMD 1K OHM 5% 1/16W 0402	1K	402	RC0402JR-0711KL
70	1	R46	RES SMD 680 OHM 5% 1/16W 0402	680	402	RC0402JR-07680RL
71	1	R58	RES SMD 20K OHM 0.1% 1/16W 0402	20K	402	RT0402BRD0720KL
72	1	R70	RES SMD 47K OHM 1% 1/10W 0603	47k	603	RC0603FR-0747KL
73	1	R79	RES SMD 51k 1% 1/16W 0402	NP	402	RC0402FR-0751KL
74	1	R84	RES SMD 1M OHM 1% 1/16W 0402	1M	402	RC0402FR-0711ML
75	1	R93	RES SMD 71.5K OHM 1% 1/16W 0402	71.5k	402	RC0402FR-0771K5L
76	1	R95	RES SMD 10K OHM 1% 1/10W 0402	10K	402	RC0402FR-0710KL
77	1	R98	RES SMD 220 OHM 1% 1/16W 0402	220	402	AC0402FR-07220RL
78	1	R99	RES SMD 4.7K OHM 1% 1/16W 0402	4.7K	402	RC0402FR-074K7L
79	1	R100	RES SMD 1.05K OHM 1% 1/16W 0402	1.05k	402	RC0402FR-071K05L
80	1	R101	RES SMD 34K OHM 1% 1/16W 0402	34k	402	RC0402FR-0734KL
81	1	TH_Coil1	NTC Thermistor 10k Bead	NP	805	NTCLE203E3103JB0
82	1	T1		TP	8x250unplated	
83	1	T2		TP	8x320unplated	
84	1	U1	Buck Regulator Chip, QFN-14 (3X3)	MP2229	MP_2229	MP2229GO
85	1	U3	Medium Power Transmitter	P9243-GB	socketqfn_48_6x6_op4	P9243-GB
86	1	U4	1.7-5.5V input, 10MHz R2R OPA	MCP6021	SOT23-5	MCP6021T-E/OT
87	1	U7	SPIFLASH 4M-BIT 4KB UNIFORM SECT	W25X40CLUXIG	uson_2x3_8LD	W25X40CLUXIG
88	1	Y1	8MHz Crystal Oscillator	8MHz	ECX-53B	ECS-80-18-30B-AGN-TR

# Board Layout

Figure 22. Silkscreen - Top of Board

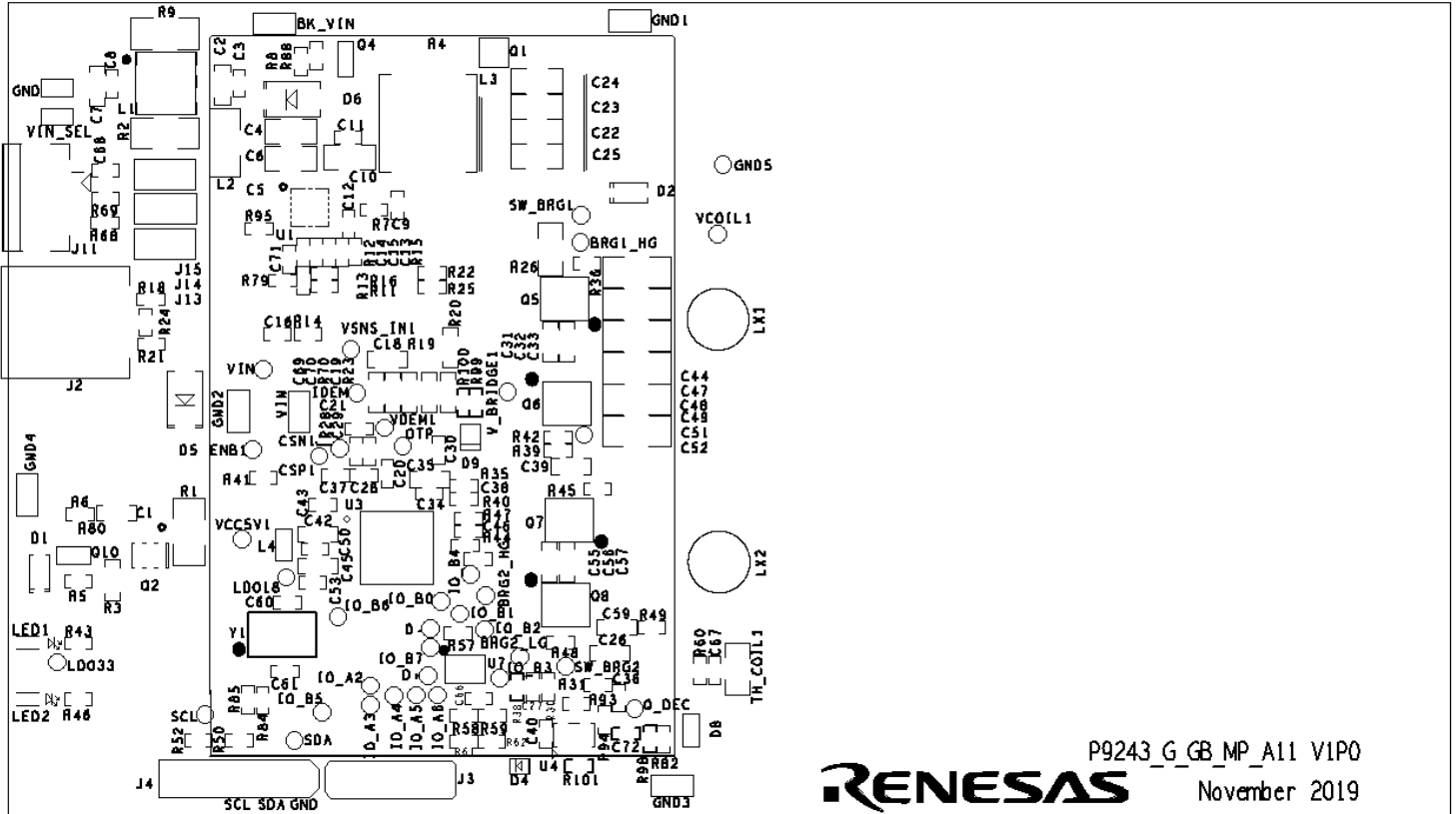


Figure 23. Copper – Top Layer

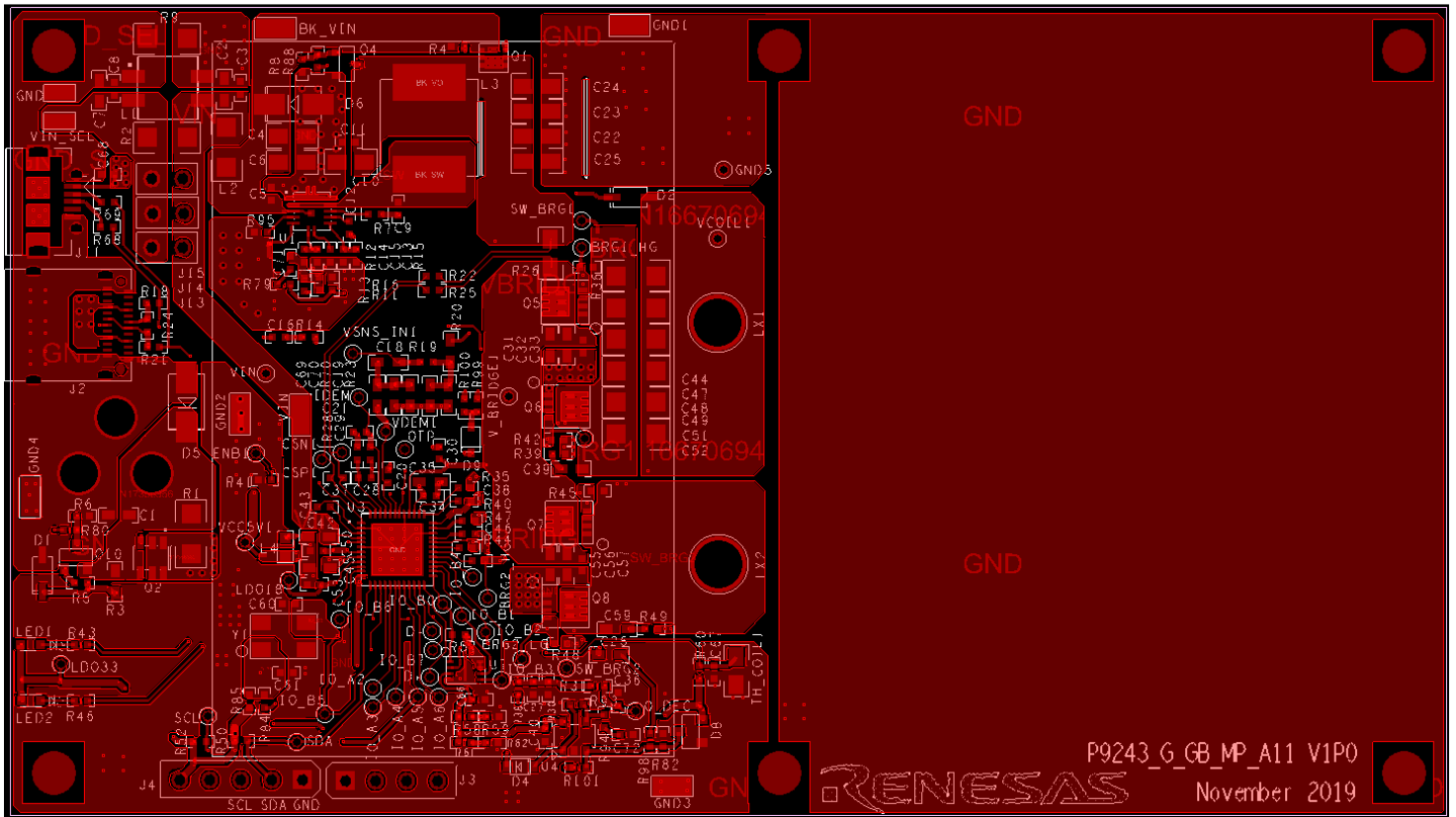


Figure 24. Copper L1 Layer

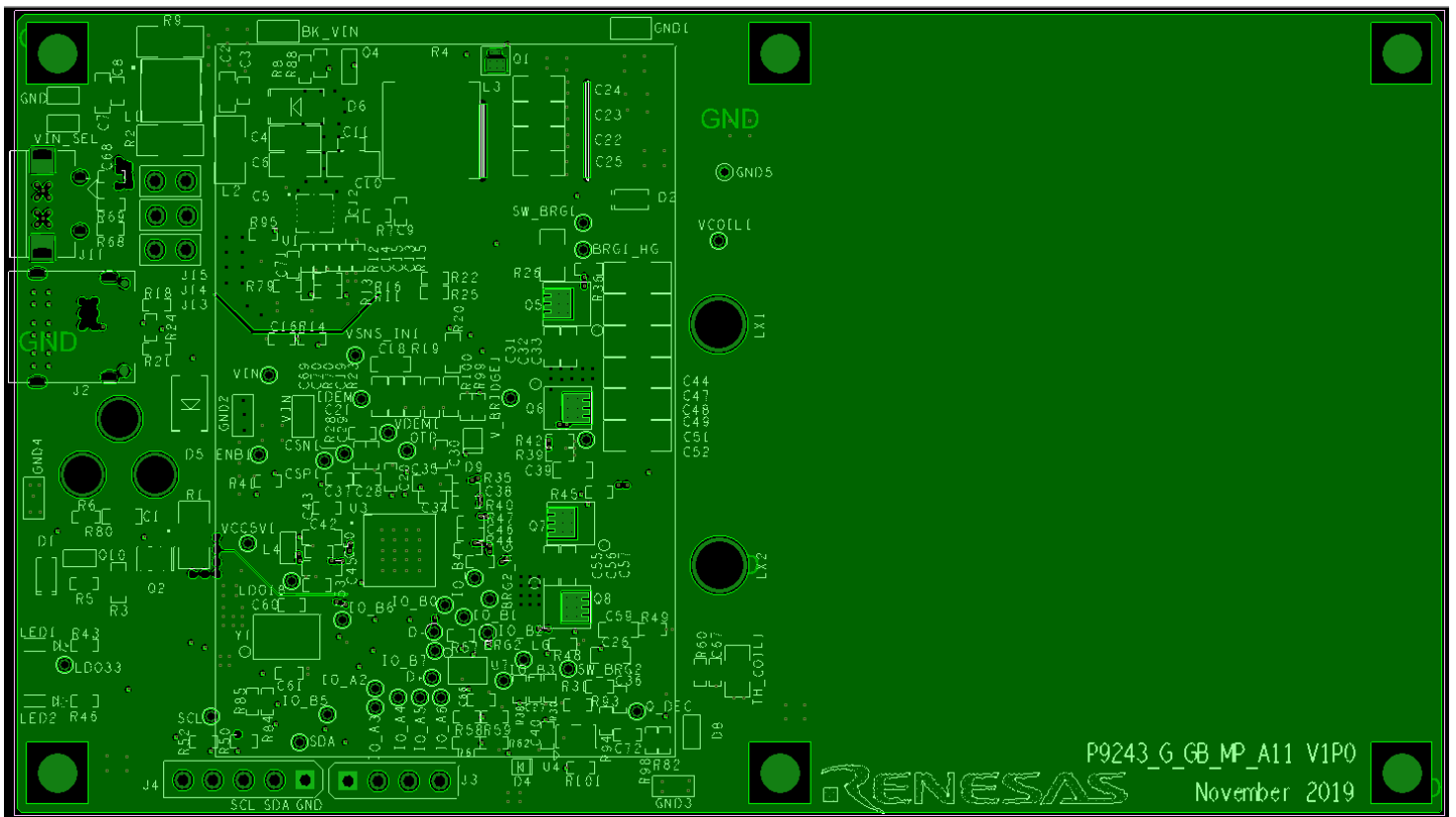


Figure 25. Copper L2 Layer

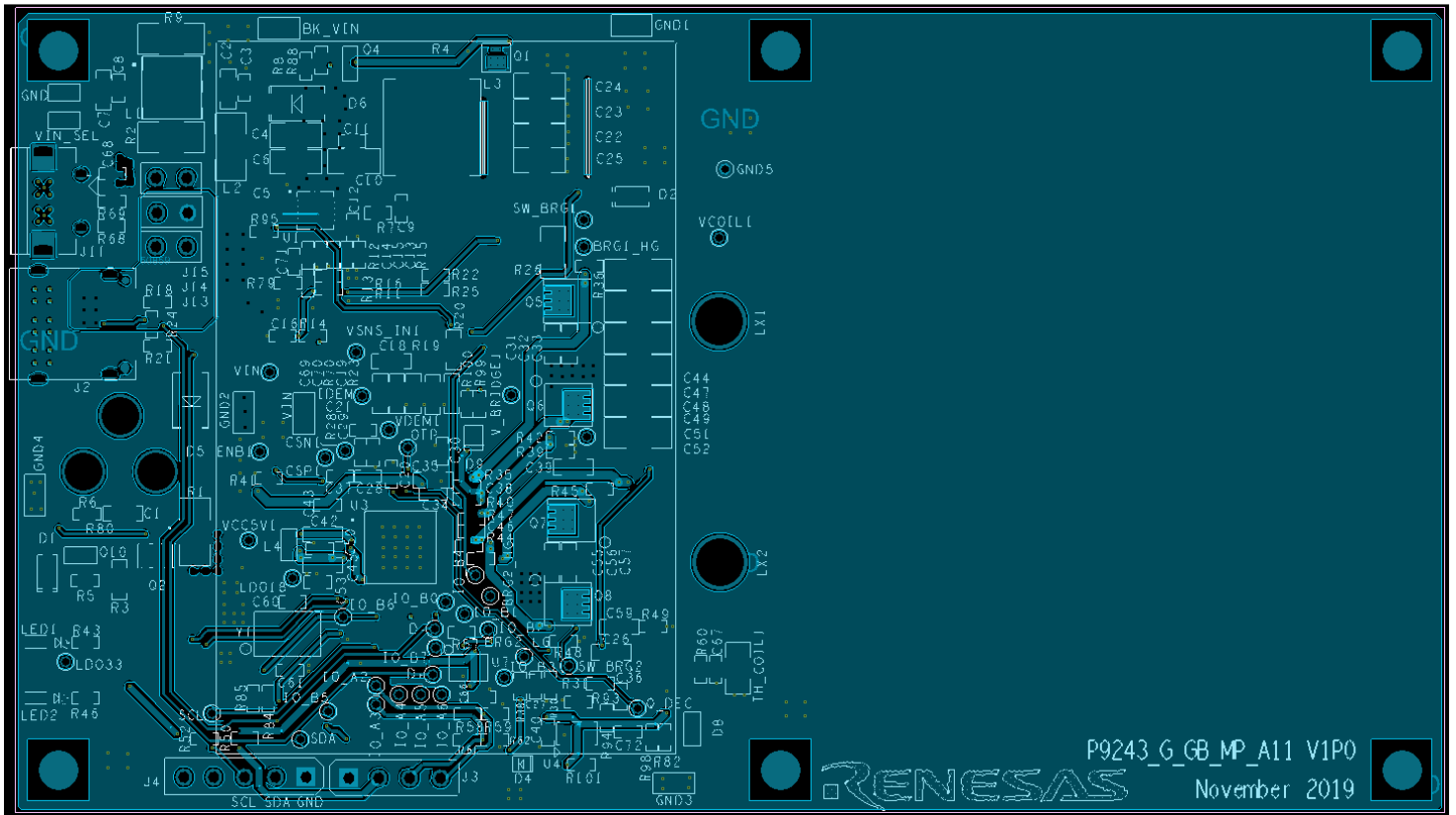
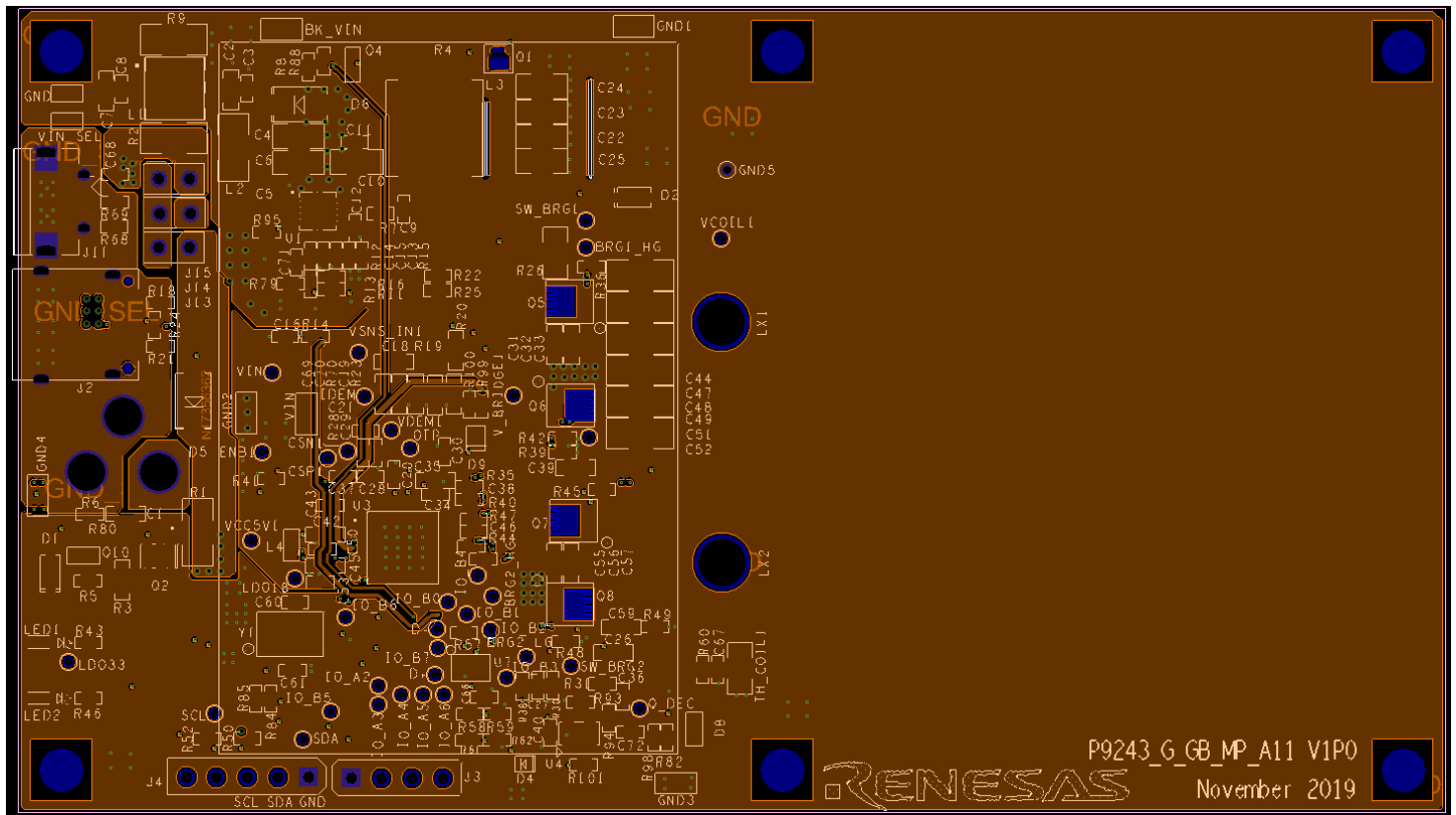


Figure 26. Copper Bottom



## Ordering Information

Orderable Part Number[a]	Description
P9243-GB-EVK	P9243-GB-EVK Evaluation Board
WPD-USB-DONGLE	USB-to-I2C dongle (FTDI). It is not included in the P9243-GB-EVK evaluation kit, and must be ordered separately. USB-FTDI-V2.1 and WPD-USB-DONGLE have the same functionality and can be used interchangeably.

[a] The P9243-GB has only the bootloader firmware pre-programmed into the internal one-time programmable (OTP) memory. The device must be used in conjunction with an external Winbond W25X20CLUXIG flash. For a sizeable business opportunity, the application firmware can also be loaded into the internal one-time programmable (OTP) memory and external flash memory can be removed. For more information, contact the Renesas sales team or your distributor.

## Revision History

Revision Date	Description of Change
February 25, 2021	<ul style="list-style-type: none"> <li>▪ Updated "Control of External Power Stage DC/DC Buck Regulator – GPIO_B4 and GPIO_B7"</li> </ul>
January 31, 2021	<ul style="list-style-type: none"> <li>▪ Updated "LED Pattern Selection – LED1 and LED2"</li> <li>▪ Updated register information pertain to USB PD as Reserved and register addresses for Sleep Timer Adjust.</li> <li>▪ Added Rx Manufacture ID Register, Rx Type Register, Charge Status Packet Registers, and LED Pattern Selection Information.</li> </ul>
September 15, 2020	Initial release.



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).