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1. Introduction

The P9412 wireless power TRx (receiver and transmitter) with Wattshare™ technology is an integrated circuit (IC) consisting of multiple high power blocks along with noise sensitive circuits all controlled by a micro-processor (see Figure 1).

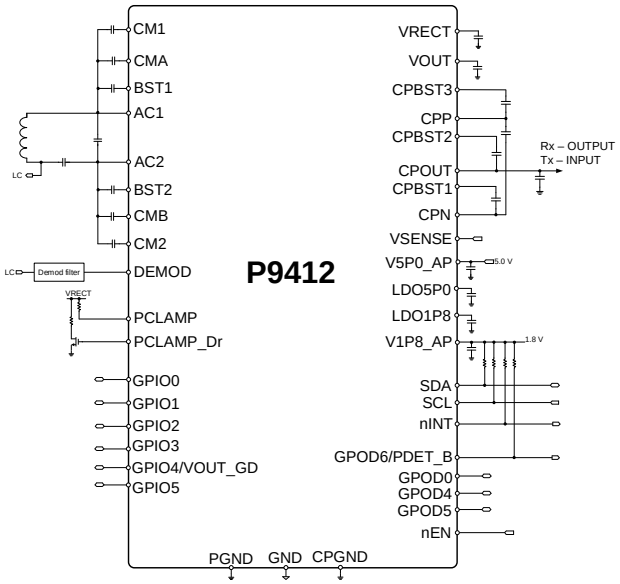


Figure 1. P9412 Block Diagram

When implementing the circuit onto a printed circuit board (PCB) there are often some trade-offs associated with managing the critical current paths with available routing area. In order to optimize the design, components should be placed based on circuit function to guarantee best performance. Furthermore, the thermal management of the IC is critical to the products overall performance and should be optimized while designing the PCB. The following guidance should be used to implement the design into a PCB using up to six layers, two blind-buried via sets, and 100mm2 surface area: place the components in order of priority based on circuit function, route the power connections near the IC, place and route the noise sensitive connections, and finally, place and route the non-sensitive connections. There are three main categories of circuitry, Power Circuits, Sensitive Circuits, and Non-Sensitive Circuits.

Key points for optimal layout:

- Route power connections wide and on the same side of the PCB as the P9412 (≥ 2.54 mm). Use parallel planes for conductivity improvements.
- Use the layer under the P9412 side of the board as a solid GND plane for “Hot loops”.
- Connect all GND (PGND, CPGND, and GND) pins to multiple GND plane(s) using vias-in-pad. Use additional vias for the PGND and CPGND pins.
- Use > 10 vias for layer transitions of the AC power connections and hot loops (VRECT, AC1, AC2, LC nodes, CPP, CPN, VOUT, and GND).
- Attempt to place the P9412 toward the center of the board. Avoid placing along the PCB edge.
- Place in order: VRECT caps, Cfly caps, BST caps, VOUT caps, CPOUT caps, LDO1P8 / LDO5P0 caps, resonance caps, COM/CM caps, and RCLAMP
- Use minimal trace-to-trace separation for all traces and planes connected to and within 10 mm of the P9412 (0.127mm or 5mils is OK).
- Use low ESR resonance capacitors (Cs) for the WPC LC tank (C0G preferred) and maintain minimum effective capacitance on Vrect and VOUT.
- Follow the placement and routing suggestions (use ≥ ½ -oz. copper foil, non-conductive via-in-pad back-fill material, and NSMD CSP pins).

2. Power Circuits

The main power circuits of the P9412 device are the resonance tank (WPC Rx and Tx), the integrated synchronous bridge rectifier/inverter, the MLDO linear regulator (VOUT), and the Capacitor Divider. Secondary power circuits are the BST and COM/CM capacitors, LDO5P0 (or V5P0_AP), and LDO1P8 (or (V1P8_AP) regulators. The concept of Hot Loops must be explained prior to discussing the specifics of component placement and routing to provide insight about successful layout implementation. The phrase Hot Loops refers to any switching high current (amperes) loop that requires the P9412 to change the primary current path during operation. The sudden change in current path of direction or path of current flow causes a discontinuity in the electron flow while the device switches the current loop from one path to another. These hot loops operate independently and are characterized by two arbitrary yet distinct operating phases (based on current path controlled by FET switch conduction).

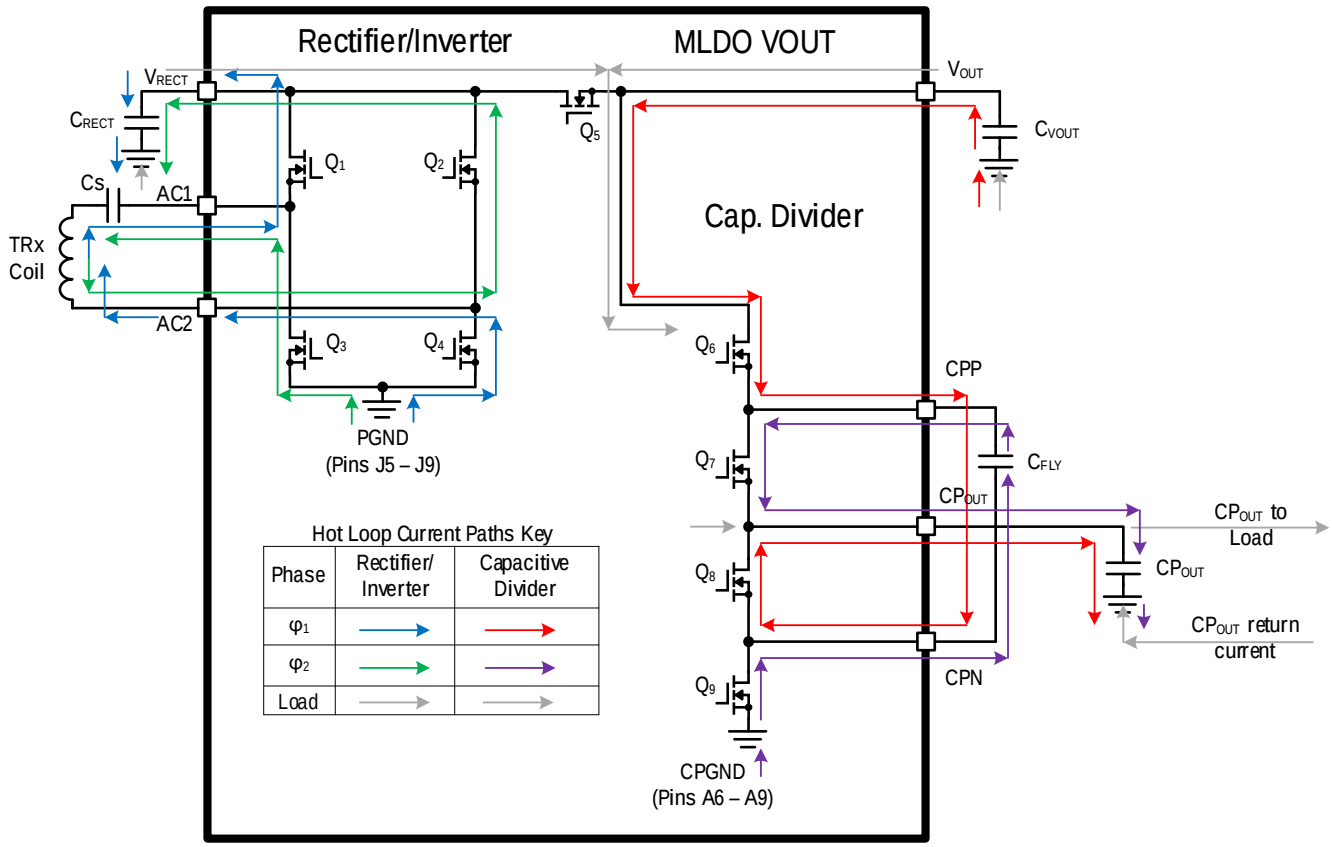


Figure 2. P9412 Power Circuits Hot Loop Current Paths Simplified Schematic Diagram

There are two hot loop current paths in the P9412: the paths associated with the wireless power transfer (Rectifier/Inverter), and the paths associated with CFLY and the Capacitive Divider. There is also a DC current that is common to all switching regulators and provides the current used to charge the device under charge (Load).

Figure 2 shows the two hot loops from each switching regulator and the direction of current flow based on the phase of each switching regulator, as well as the GND pins associated with each power circuit (VOUT GND is common to both Vrect and the Capacitive Divider).

The hot loops geometric area should be limited; thus the indicated components in Figure 2 are identified as those with the highest placement priority and are also the most important to stable regulator operation. The five required BST capacitors are omitted from this drawing for simplification; however, due to the critical function they perform they must be located close to each respective BST pin and switching node.

Considering mechanical requirements of the system under design, it is suggested that as soon as the final shape of the production or development PCB has been determined and the power transfer coils connection points (LRTX) are established that the P9412 be placed onto the board as close to the center of the PCB as possible. After the P9412 is placed, the orientation should be decided based on facing the AC1 and AC2 side (J-row) toward the physical coil connectors.

Additional consideration should be made regarding the ability to route connections and place the necessary capacitors in the following order of priority: CRECT, CFLY, BST1/2, CPBST1/3, VOUT, CPOUT, CPBST2, LDO1P8, LDO5P0, WPC (Cs/Cp, Cd) resonance capacitors, Communication COM1/2 and CMA/B capacitors, then RCLAMP. The main power current path can be followed from the connection from the RTx resonance tanks to the AC1 and AC2 pins to VRECT to PGND and subsequent power rails VOUT provides power to CFLY and CPOUT to CPGND. Low-Drop Out regulators LDO1P8 and LDO5P0 are powered via VRECT or external supplies for reducing P9412 IC heat development during operation.

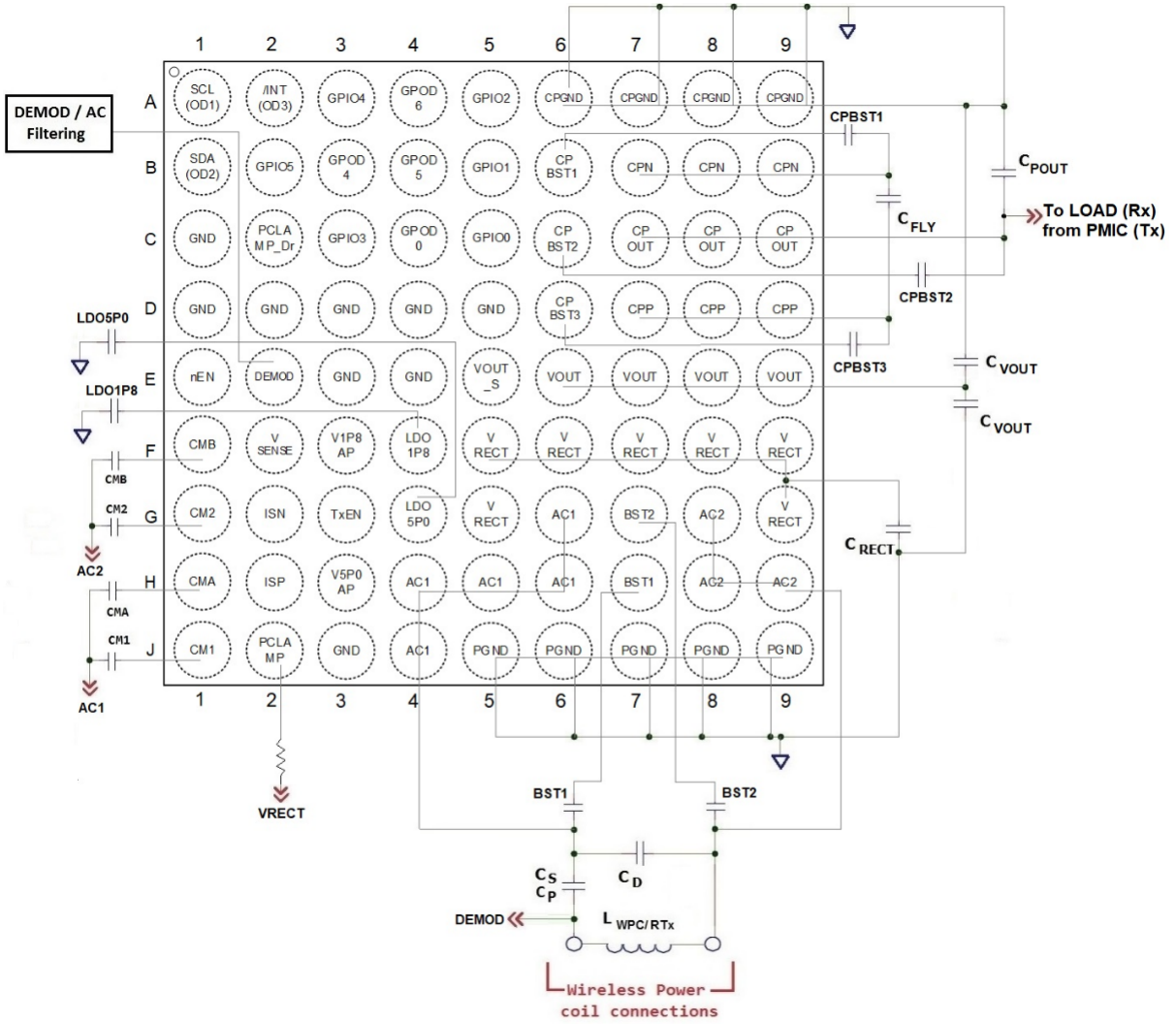


Figure 3. P9412 CSP Suggested Orientation[1]

The optimal P9412 orientation relative to the RTx coil connector physical locations are presented in the following image. If possible, place the Capacitive Divider capacitors on the side of the P9412 closest to the DC load. Capacitors CRECT, CVOUT, and CFLY must be placed near the respective pins and should be placed near each other (adjacent by net) with the exception being CVOUT. Capacitor CVOUT may be split with some near the PGND pin (J-row) and some near CPGND (A-row) due to the shared current purpose these components serve.

[1] Based on coil connector location and critical component placement (not all necessary connections shown).

3. Power Schematic and Layout Examples

Place the VRECT output capacitors first and adjacent to the P9412 (C46, C45, C16, C15, C14, C43), because they are subjected to high current charging and power transmission currents at twice the operating frequency of power transfer, in addition to supplying the battery charge DC current to the CPOUT regulator. The power transfer switching results in dV/dt voltage steps high enough for consideration as noise generating signals at the AC1 and AC2 nodes and high di/dt current surges during normal operation. The ideal placement of the VRECT capacitors is to have them next to the VRECT pins (with all Vrect pins connected together and routed to the capacitors placed around the corner with Vrect and PGND pins of the IC) and with a direct second layer connection to the J-row PGND pins. Figure 4 is a selection from the P9412 CSP Reference PCB schematic portraying the Power Circuits – this figure will be used for reference purposes.

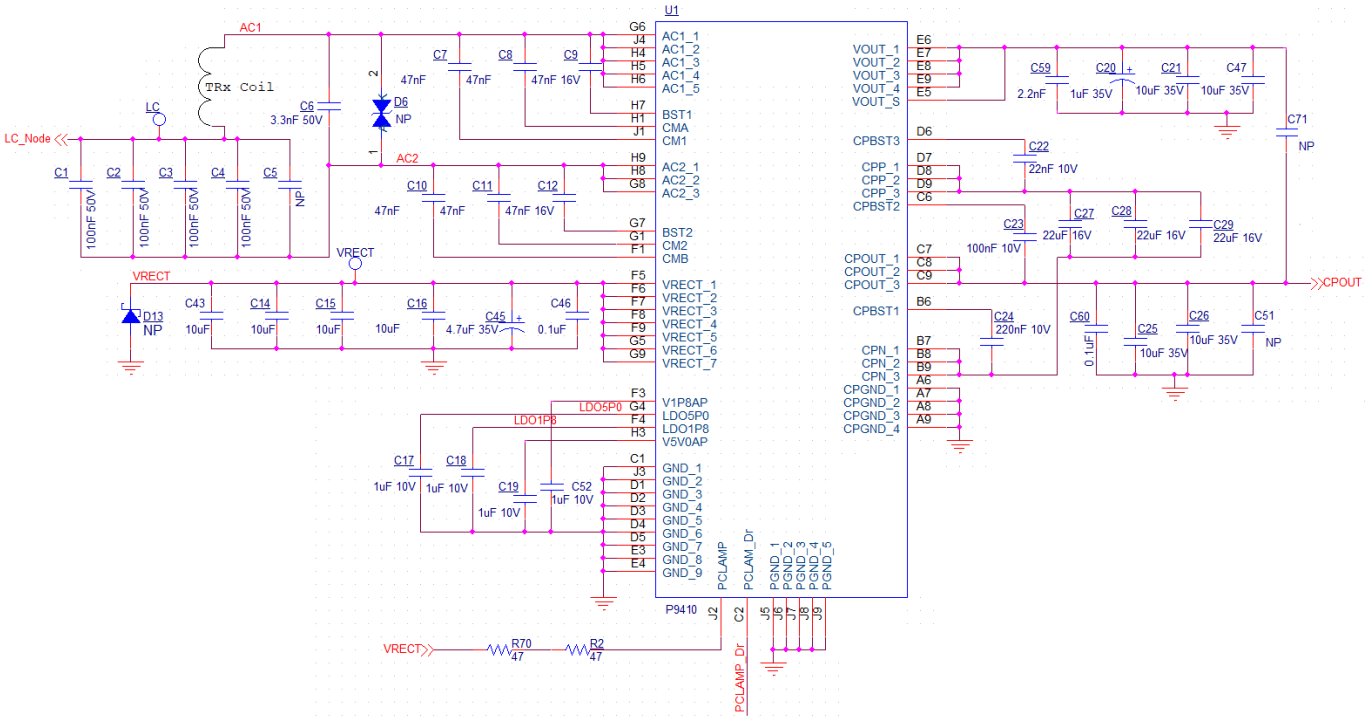


Figure 4. P9412 Power Section, CSP DEMO Board Schematic[2]

In the following top layer layout image, the placement of the VRECT capacitors (C46, C45, C16, C15, C14, C43) should occur first and these are the most critical components. Then the CFLY capacitors (C27, C28, C29), then four of the bootstrap capacitors (C22, C24, C9, C12), CVOUT (C59 (close to VOUT/PGND pins), C20, C21, C47), the CPOUT bootstrap capacitor C23, CPOUT capacitors (C60, C25, C26), and then the LDO1P8 (C18/C52) capacitor should be placed. After placing the previous components, continue with LDO5P0 capacitor (C17/C19), the WPC resonance capacitors (C1, C2, C3, C4, C5, C6) followed by the WPC communication capacitors (C7, C8, C11, C10).

Finally, place DC stability capacitor dividing capacitor C71 followed by Clamping Resistors (R70, R2) and TVS (D6) or Zener (D13) protection diodes. Placing the above listed parts in the listed order and close to the P9412 while allowing room for routing is critical for optimal performance. It is important to keep the area of the hot current loops that conduct AC currents to a minimum.

[2] Not all connections are shown in this figure. For the complete list of pins and recommended connections, see “Pin Descriptions” in the *P9412 Datasheet*.

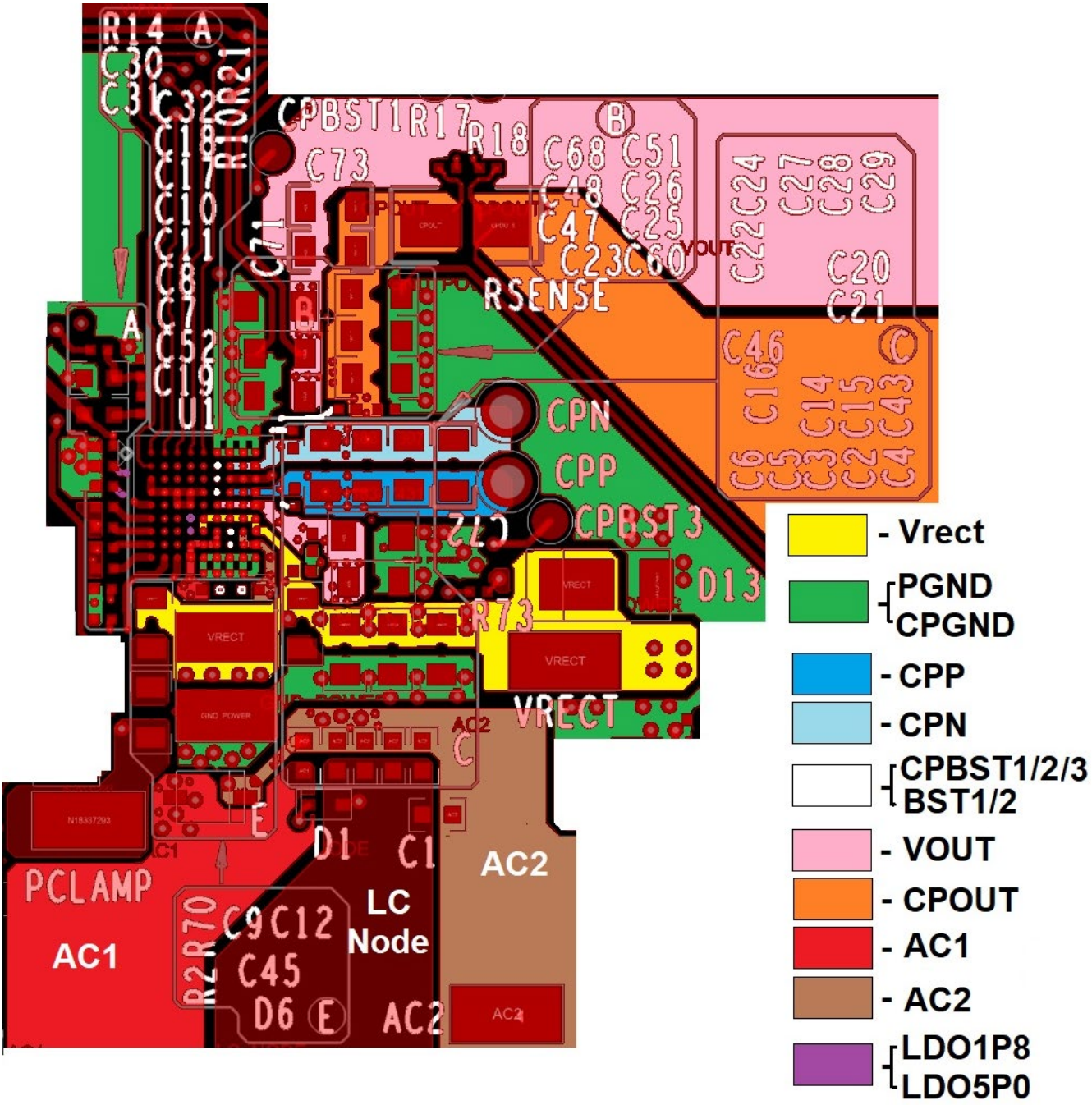


Figure 5. P9412 Physical Layout from CSP Demo PCB (Top Layer)[3]

These are the currents paths from the synchronous bridge rectifier/inverter to the VRECT capacitors / VOUT (C59, C20) to PGND (J-row) as well as the capacitor divider VOUT (C21, C47), CFLY, CPOUT to CPGND (A-row CPGND vias) to keep ripple voltages, GND bounce, potential EMI minimized. In the reference layout, the GND current travels from the VRECT capacitor GND plates to a solid GND plane by using many vias slightly spread apart to allow conduction between vias on all layers. The PGND and CPGND pins on the J-row and A-row of the device should all have vias-in-pad to a solid GND plane and additional copper and vias are recommended to create “thermal tab” filled with vias to transfer heat from the IC to the PCB inner layers. The copper planes should be as wide as possible for the connections for VRECT, VOUT, CFLY, and CPOUT from the IC to the capacitors and back to PGND/CPGND. The reason for the number of capacitors is to maintain the

[3] VRECT, CPP, CPN, VOUT, CPOUT, AC1, AC2, LDO1P8, LDO5P0, COM1/2, CMA/B, PCLAMP placement and routing.

necessary amount of effective capacitance when 5-20V of DC bias is applied across the VRECT or VOUT capacitors (see DC-bias characteristics of selected capacitors and compare with components used in the reference design when substituting). It is recommended to use at least 6 vias per Ampere of CPOUT current supplied to the load for layer transitions. For a full schematic and component placement map, see Appendix A.

The PGND, CPGND, and GND vias should all have vias-in-pad to internal GND planes and additional vias to GND planes should be added next to pins J6-J10 and A6-A10 in order to decrease AC impedance and increase thermal conductivity. It is recommended to have at least 8 vias next to the PGND and CPGND pins for current conduction and heat dissipation purposes. For best thermal performance, multiple GND planes are recommended and connections should be direct and not thermally relieved.

Additional thermal performance improvements can be made by connecting large copper planes to the power pins, using multiple parallel planes, and wider than necessary copper connections to every P9412 pin to improve heat transfer from the device to the PCB. C0G capacitors will offer the highest performance and are recommended for the WPC resonance circuit. Capacitors with X7R and X5R Class-II dielectrics can be substituted for the resonance capacitors, but low ESR components should be identified and used.

Since all of the load current and the current required to charge the VRECT/VOUT/CFLY/CPOUT capacitors flows through the resonance capacitors, the heat developed within the resonance capacitors should be given opportunity to spread into large copper planes. Higher voltage ratings are recommended because higher rated components tend to have lower derating and dielectric loss factors at the working voltage which typically results in lower operating temperatures. All layer transitions involving AC signals (AC1, AC2, LC Node, CPP, CPN, PGND, and CPGND) and high current DC nodes (Vrect, VOUT, CPOUT, and PGND/CPGND) should be made using numerous vias (8 or more) for any layer transition.

Effort should be made to keep the first PCB layer under the P9412 free from unnecessary connections and a solid GND plane is recommended. This plane will carry electrical current, mirror currents from power conductors, and heat from heat sources to be spread across the PCB. Since it is often impractical to avoid connections on adjacent inner layers, it is recommended to concentrate low-power signal connections on inner layers to one or two layers to improve heat transfer by allowing more surface area for planes and parallel planes connected to the high power nodes of the P9412.

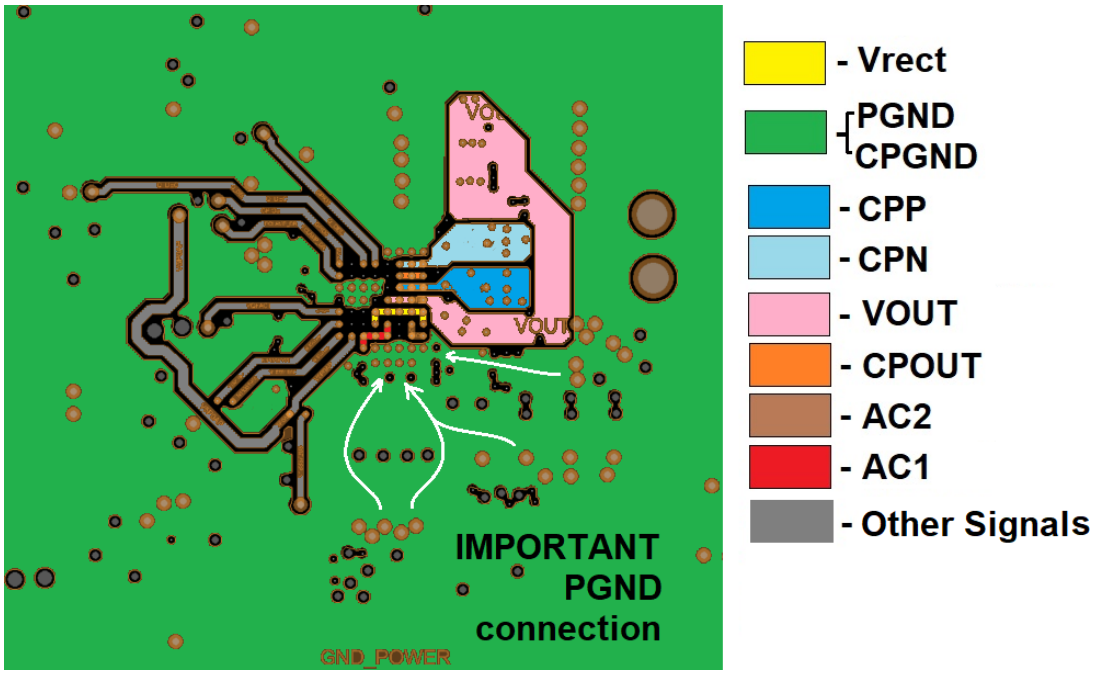


Figure 6. P9412 Physical Layout from Demo PCB Second Layer (MID1)[4]

[4] Solid GND plane and parallel conduction planes for CPP, CPN, and VOUT. Minimal Signal Routing not blocking PGND return current path.

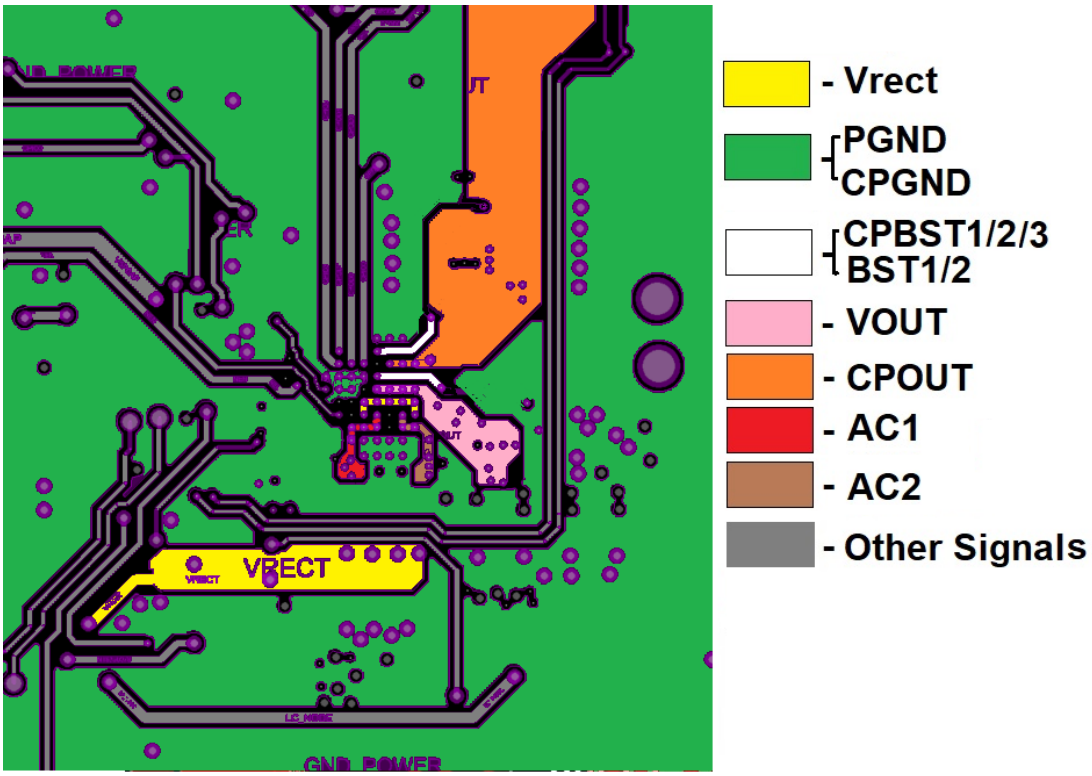


Figure 7. P9412 Layout from Demo PCB Third Layer (MID2)[5]

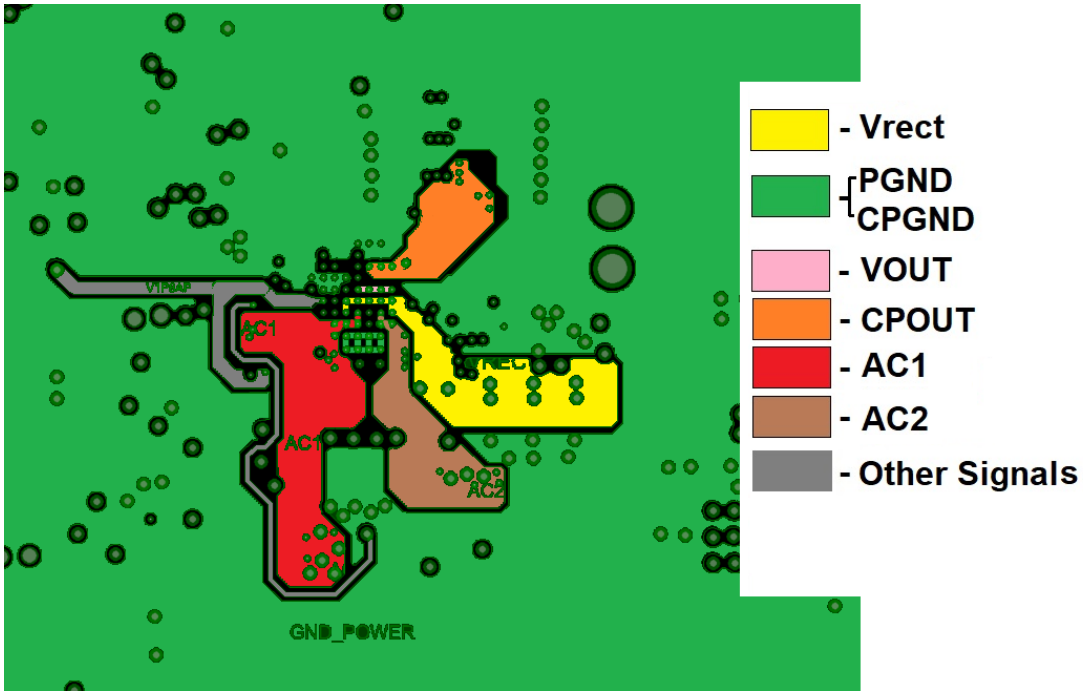


Figure 8. P9412 Layout from Demo PCB Fourth Layer (MID3)[6]

[5] Parallel conduction planes for VOUT, AC1, AC2, CPOUT, Vrect to PCLAMP and all GND; CPBST1, CPBST3, Signal routing layer.
[6] Parallel conduction planes for VRECT, AC1, AC2, CPOUT, Signal routing layer with GND plane for heat dissipation and parallel conduction.

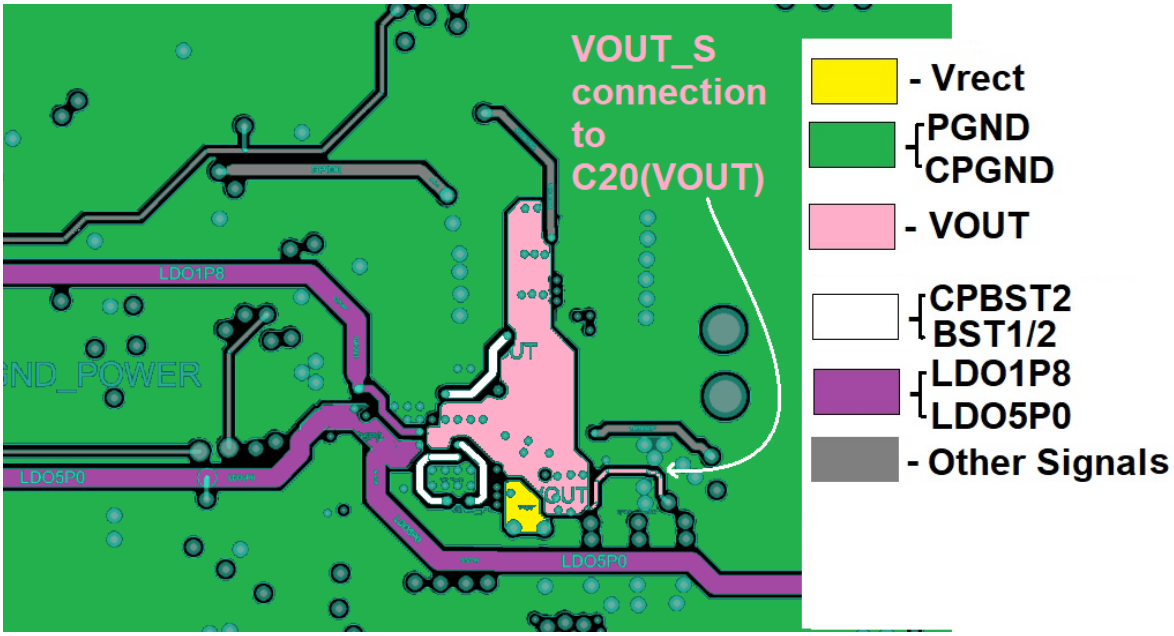


Figure 9. P9412 Layout from Demo PCB Fifth Layer (MID4)[7]

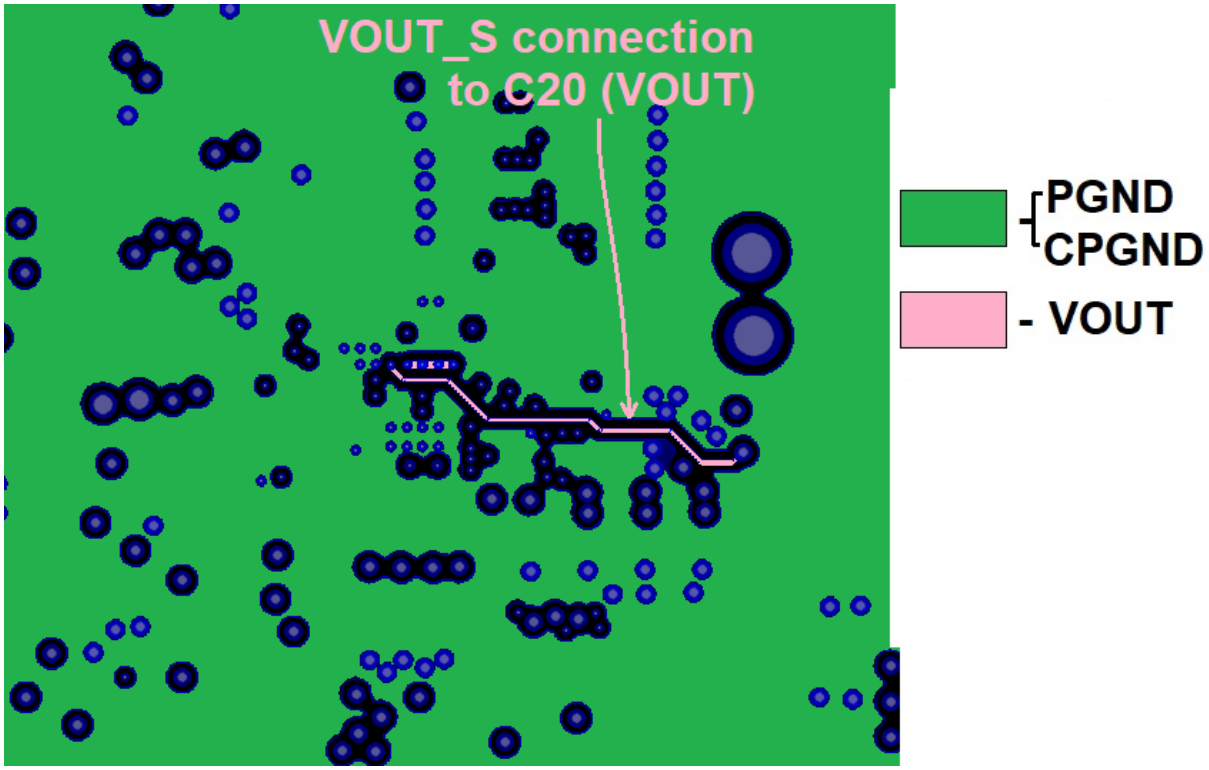


Figure 10. P9412 Layout from Demo PCB Sixth Layer (Bottom)

Parallel conduction planes for all GND plane for heat dissipation and parallel conduction (connect as many PGND, CPGND, and GND vias-in-pad to as many GND planes as possible). VOUT_S connection escape from P9412 routing.

[7] Parallel conduction planes for VOUT, Vrect, and all GND; CPBST2, BST1, BST2, LDO1P8, LDO5P0, VOUT_S, and Signal routing layer.

4. BST Capacitors

As discussed, after the VRECT, VOUT, and CFLY capacitors are placed the CPBST1, CPBST3, BST1, BST2, and CPBST2 should be placed. In Figure 11, the BST capacitors (C24, C22, C9, C12, and C23) are placed adjacent to the P9412 while leaving room for the CPP, CPN, AC1, and AC2 nodes to be routed to Cfly and in from the resonance tank. Proper blind-buried via sets should be used to optimize routing width for power connections and to make room on lower layers for routing of the Bootstrap capacitor connections. All BST capacitors should have fairly direct connections to the respective pins (route 12-20 mil wide). When routing begins, it is recommended to route the BST capacitors on the same side of the PCB as the P9412 and use the following inner layers and blind-buried via stack-up to route these connections.

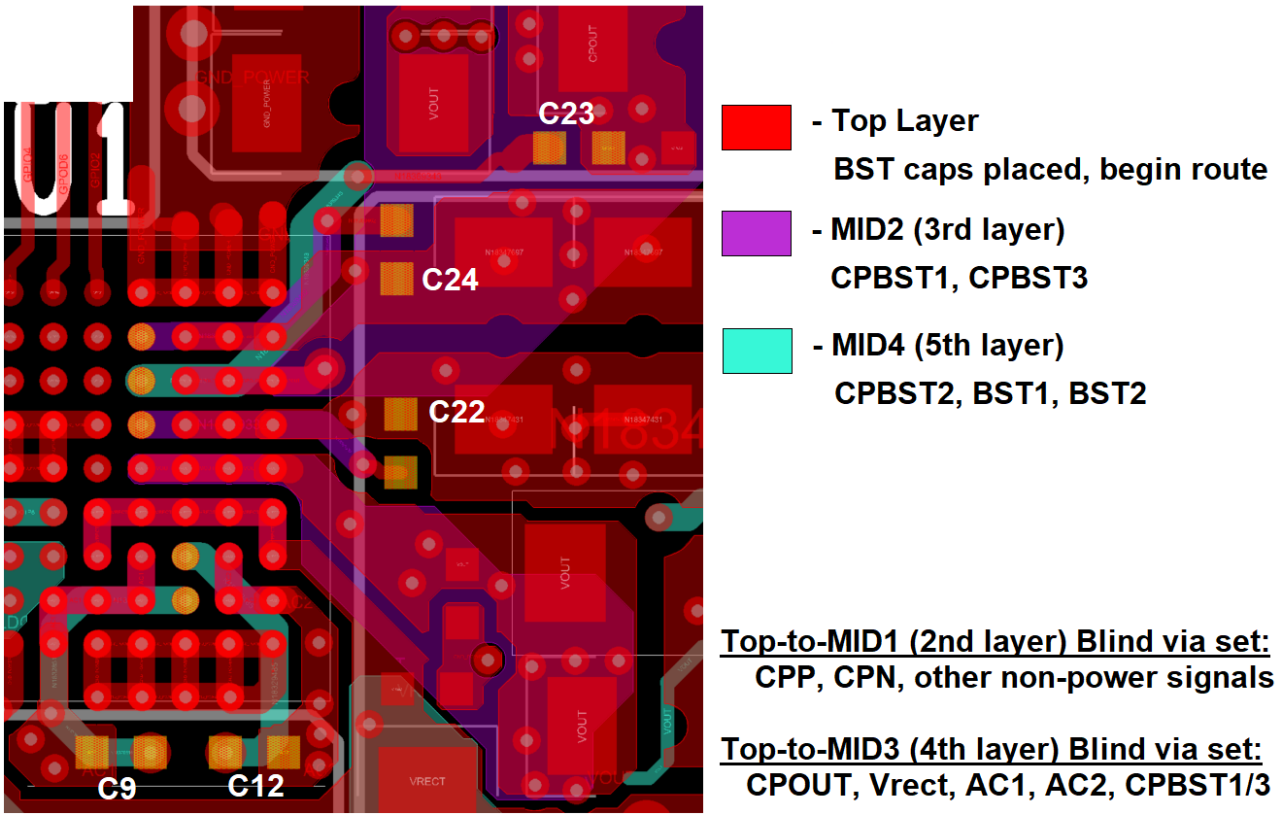


Figure 11. BST Capacitors Placement and Routing Example

5. LDO1P8 (V1P8_AP), LDO5P0 (V5P0_AP), and Communication Capacitors

The LDO1P8 (C18) capacitor is used to stabilize the P9412 internal voltage supply for the ARM-M0 processor and provide stable output power for any auxiliary loads. This capacitor must be located close to the P9412 and should be located close to pin F4. Optimal placement is directly next to the P9412 column 1 and requires a direct connection back to GND pins. An optional 10nF capacitor is recommended for high-frequency filtering of system noise but is not required (package size should be smaller than C50 or at least placed closer to the P9412 than C50). Then the LDO5P0 capacitor (C17) should be placed close to the respective pins as well as V5P0_AP and V1P8_AP capacitors. The communication capacitors can be placed at this time as well. An example of placement and routing is shown in the following figure.

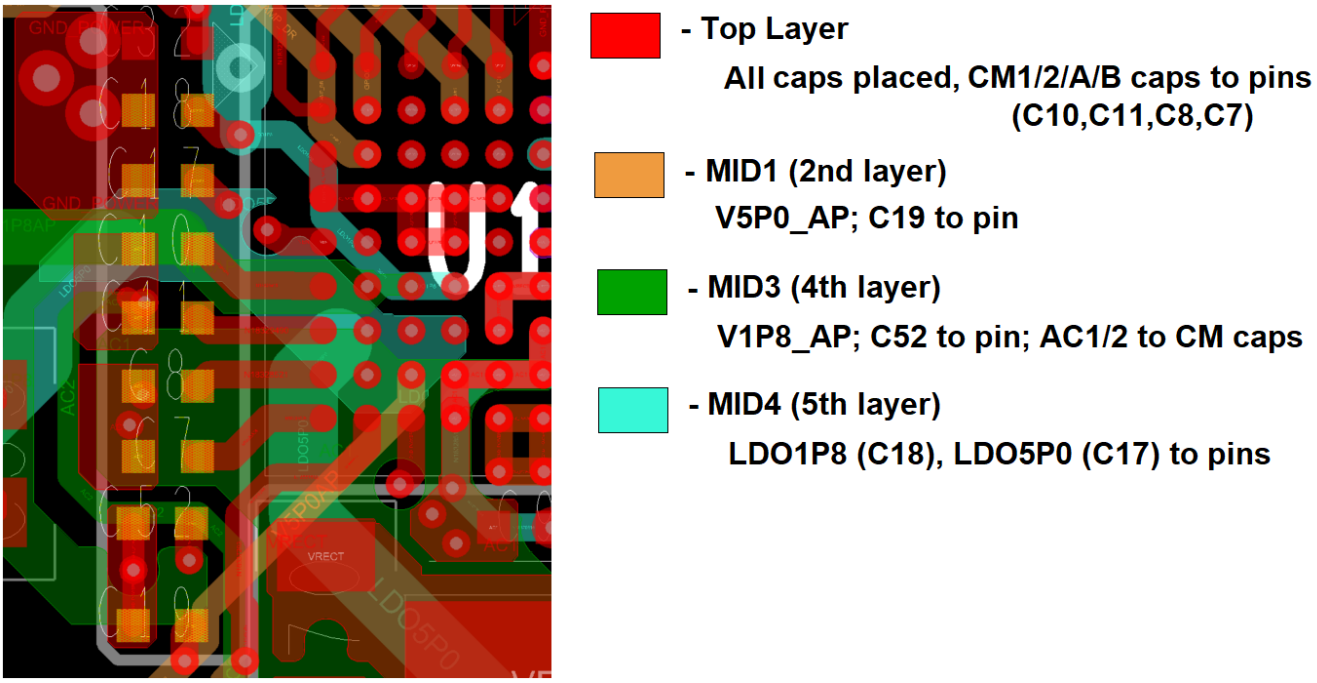


Figure 12. LDO1P8, LDO5P0, V1P8_AP, V5P0_AP, and Communication Capacitors[8]

The following table provides a guideline for meeting minimum routing widths for power traces (routing these traces wider will improve performance and the listed values are the minimum widths).

[8] All are placed next to the P9412, with layer usage highlighted for routing these components. LDO capacitors need a direct GND connection back to the P9412.

Table 1. Minimum Trace Width Routing Guide

1/2-oz copper foil weight assumed, wider connections reduce losses and improve performance. Parallel planes can be used to increase effective width.

Name	PCB Pattern Width (mm (mils))
VOUT, CPOUT, CPP, CPN	1.5 (less than 50 squares[1]) (60)
VRECT	2 (expand rapidly from pins to capacitors) (80)
AC1, AC2, LC_Node	2.54 (100)
PCLAMP, ECLAMP	0.5 (20)
BST1, BST2, CPBST1, CPBST2, CPBST3	0.3 (12)
CM1, CM2, CMA, CMB	0.3 (12)
LDO5P0, LDO1P8, V5P0_AP, V1P8_AP	0.25 (10)
GP0 – GP6; OD0, OD1 (SCL, SDA); OD2 – OD6; DEMOD; ECLMP_DRV; nEN, VOUT_S	0.127 (5)

6. Sensitive Circuits

The sensitive circuits refer to noise sensitive circuits and they include the DEMOD FILTERING with AC coupling (Tx only), VOUT_S, and any other pin used as an ADC input (such as XY alignment connections). In order to optimize the signal to noise performance, it is suggested that the VOUT_S connection be routed with at least two GND planes separation from the pin under the Vrect/VOUT hot loop to the VOUT connection to C20 or C21 (VOUT capacitors near PGND).

The DEMOD components should be placed near the A1 pin/corner of the P9412 to provide adequate GND isolation from the Rectifier/Inverter and Capacitor Divider Hot Loops. A single GND plane shared by all PGND, CPGND, and GND pins is highly recommended to optimize electrical and thermal conduction and avoid potential GND loops that extent the hot loop area.

The Rectifier, resonance nodes, and capacitive divider generate the highest noise and operate at the frequencies that need to be filtered; therefore, ADC inputs filtering capacitors are best placed near the LDO bypass capacitors or DEMOD filter. If using the RSENSE current sense resistor, the ISP and ISN signals should be routed like a differential pair, be shielded by at least two GND planes from CPP and CPN noise injection, and filter capacitor C33 should be placed near the respective pins.

7. Tx Specific Circuits for WattshareTM Technologies

The main power circuits of the P9412 in Tx mode are the synchronous bridge inverter and the resonance tank (capacitive divider operates in Bypass mode and passes the applied voltage directly to VRECT). Secondary power circuits are the LDO1P8, LDO5P0 regulators and the slew rate control capacitors (CM1, CM2) which are used for Zero-Voltage Switching control capacitors in Tx mode (follow Rx mode placement guidance).

In Tx mode the CPOUT node is the main input and the series integrated FETs are fully saturated to reduce the RDSon from CPOUT to VRECT (full-bridge inverter input voltage). In this operating mode the Vrect capacitors supply the primary switching energy to the LC tank and CPOUT and VOUT capacitors and bulk capacitors are used to further stabilize the VRECT voltage rail. The critical power components needed for the Tx mode layout are the same as in Rx mode (for recommendation on placement and routing, see the above Power Layout examples). The DEMOD envelope filter and peak detector and optional Qmeasurement circuitry are the only additional circuits and connections required for the P9412 to operate as a WPC compatible Tx.

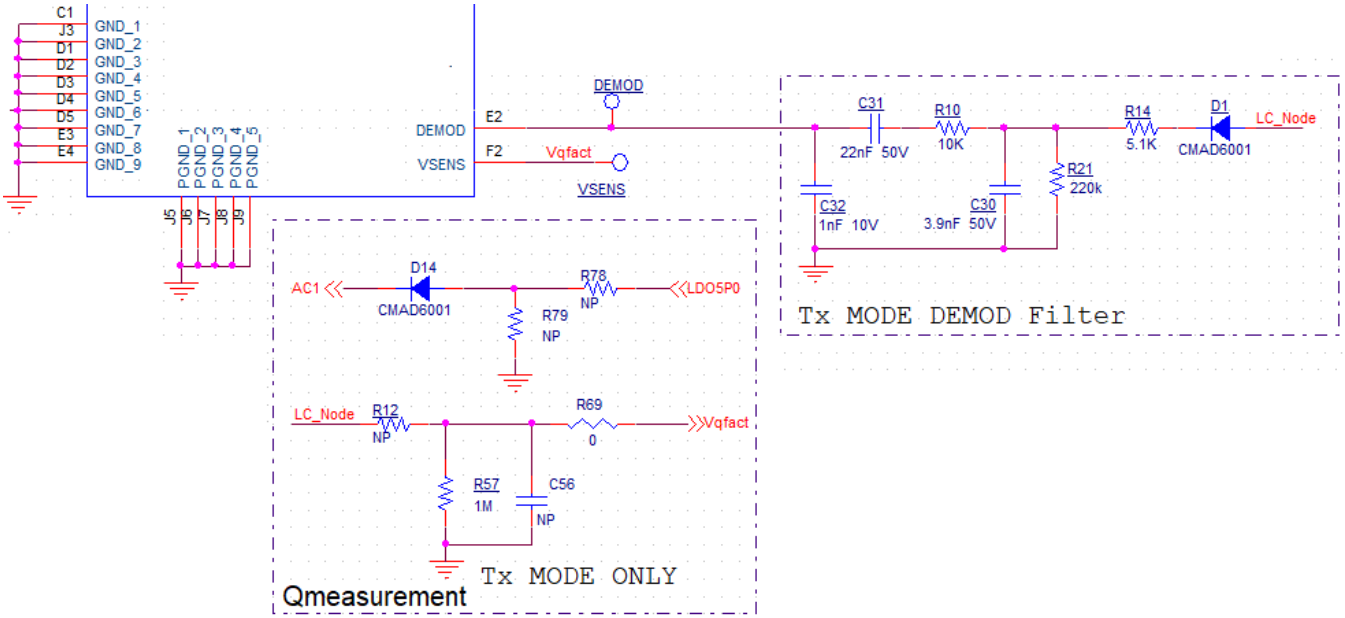


Figure 13. P9412 Transmitter DEMOD Circuit and Q-Factor Measurement Schematic[9]

[9] Not all connections are shown in this figure. For the complete list of pins and recommended connections, see the “Pin Descriptions” section in the *P9412 Datasheet*.

Figure 14 is an example of the DEMOD circuit and Qmeasurement layout. D1 should be placed near the resonance capacitors and routed to R14 on an inner layer as well as the DEMOD signal from C32 to the DEMOD pin E2. This section of the DEMOD path can be exposed to high voltages, so it should be electrically isolated by at least 0.127mm (10mils) from all other connections.

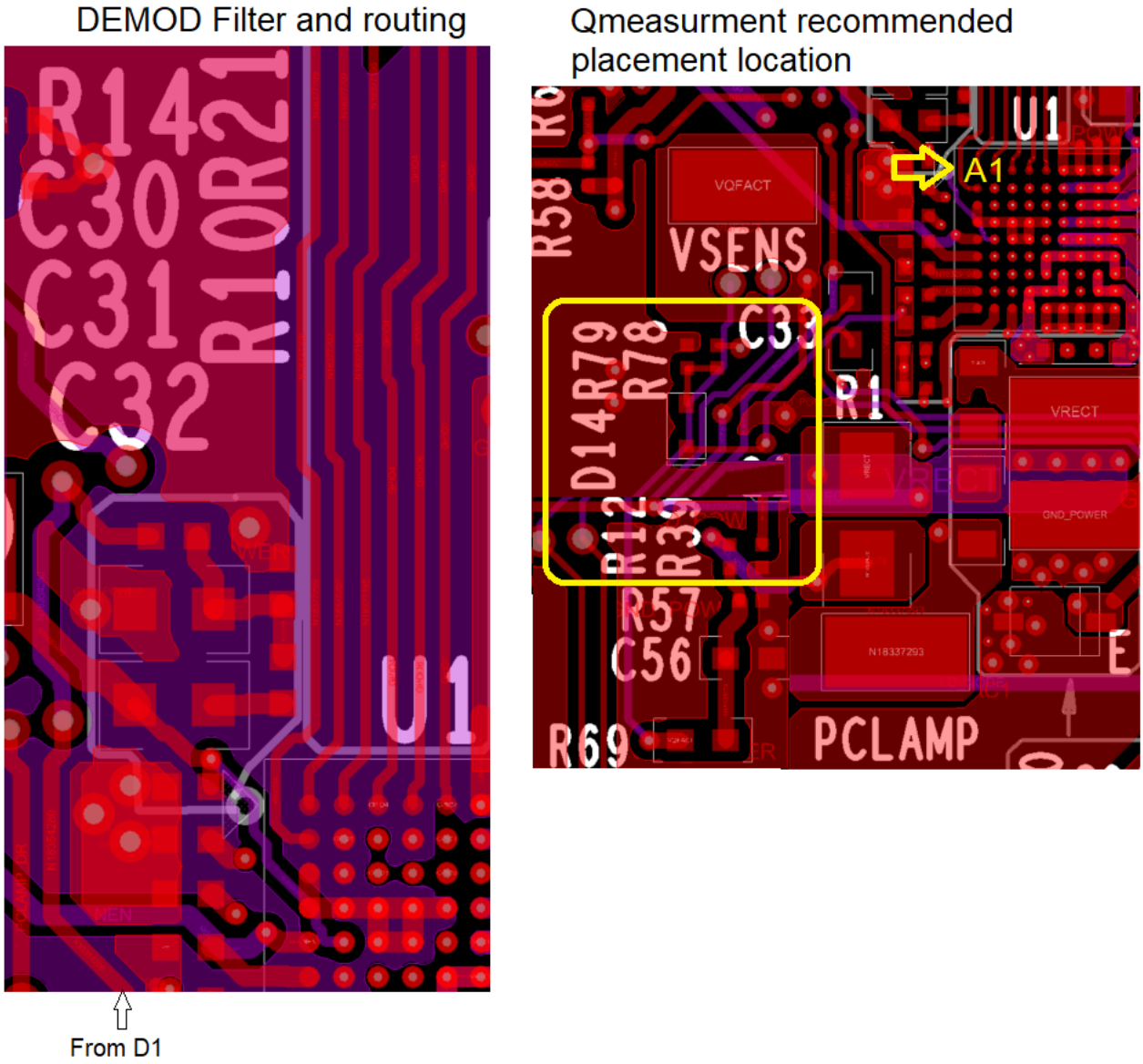


Figure 14. P9412 Tx DEMOD Filter and Qmeasurement Layout Example

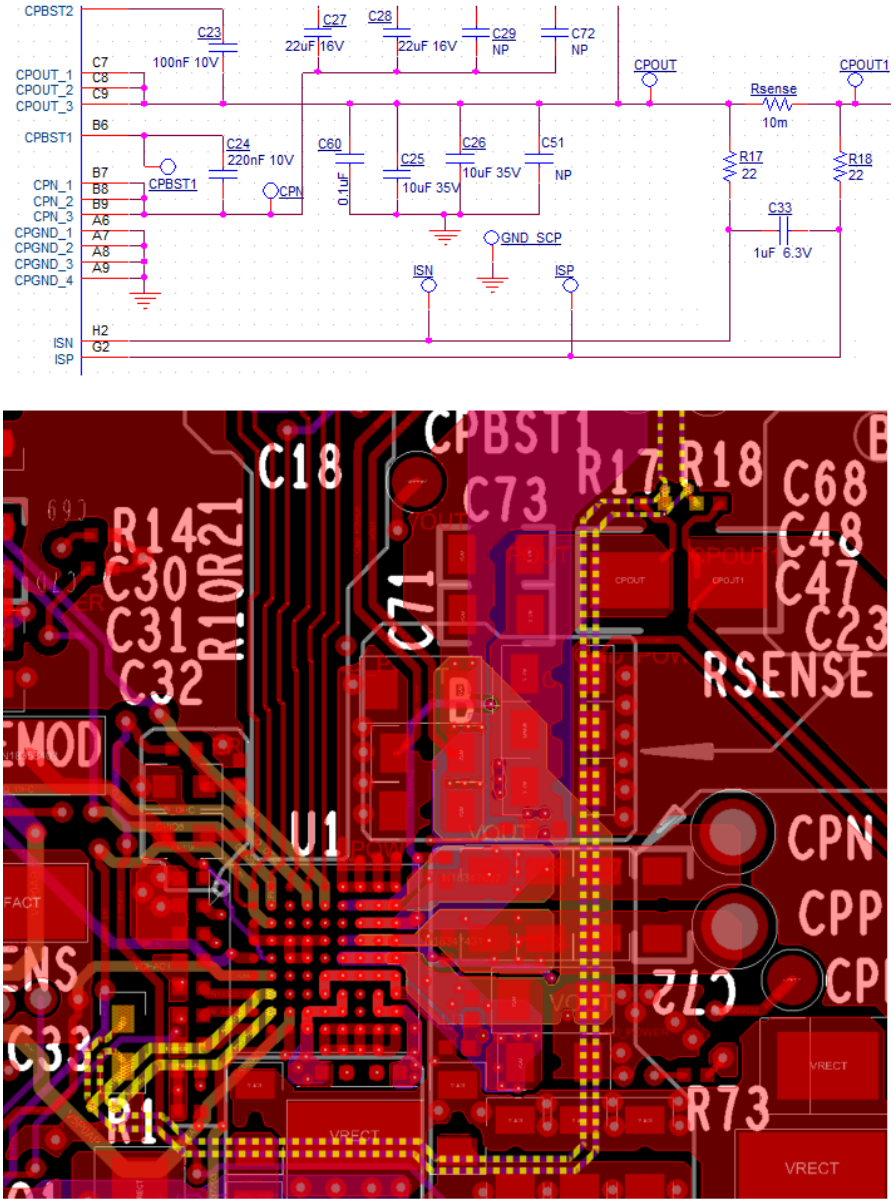


Figure 15. P9412 Optional External CPOUT Current Sense Schematic and Layout

8. Non-Sensitive Circuits

The remaining components and pins that have not been mentioned are regarded as non-sensitive circuits. The placement and routing of these nodes is not considered critical to performance or functionality: they simply need to be present and properly connected. In most cases, 0.127mm (5 mil) wide traces and any method of connectivity will suffice to complete the circuit.

9. PCB Footprint Design

The P9412 package is a fine pitch CSP device and the PCB footprint is an important part of production assembly yields. Improper footprint design can lead to solder shorts or open circuits. Poor PCB footprint design can also cause the performance to be degraded by limiting the robustness and diameter of the pin-to-board connections. In order to minimize the risk of such events, it is recommended that the PCB pin pads and via-in-pads be designed using the following guidance. Non-solder mask defined (NSMD) pins are recommended and solder paste should be applied with stencil openings of 0.127 – 0.268 mm (0.19mm typical recommendation) based on stencil thickness and solder paste selected. Pin diameter should be set to 0.268mm, solder mask should be 0.3315 mm, and vias in pad should be 0.127mm diameter holes. All vias-in-pad should be back-filled (non-conductive fill material) and be plated even within 1mil of surface level for non-via-in-pad pins.

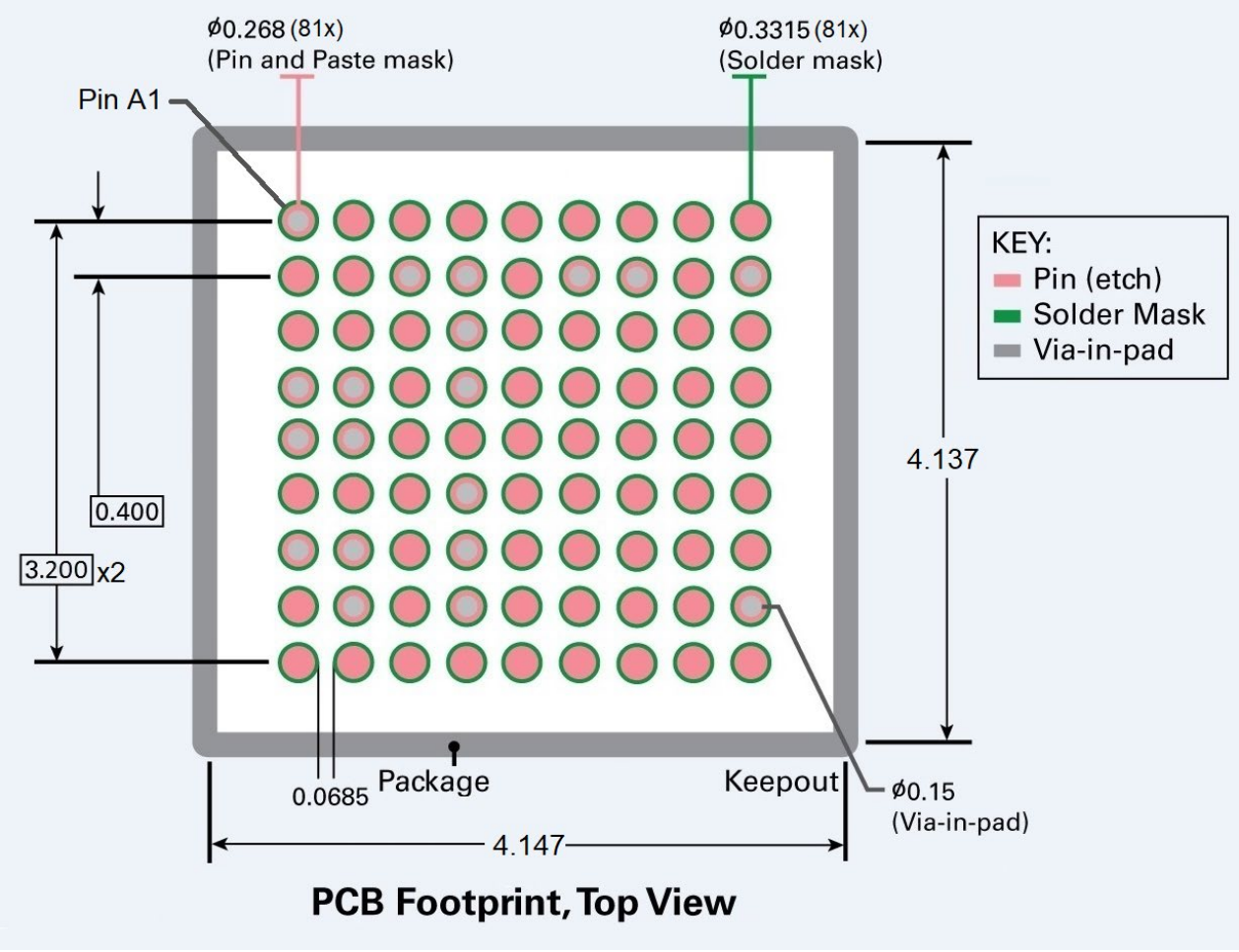


Figure 16. P9412 CSP Recommended PCB Footprint Design Dimensions

10. Thermal Considerations

The heat or thermal management of the P9412 PCB design is critical to performance and from the thermal perspective it is recommended to route the main power connections as wide as possible when connecting to the device and use the outer layer of the PCB for these connections. This allows for optimal electrical and thermal performance. Power connections to the P9412 using traces/planes should avoid multiple layer changes in order to reduce voltage drops and thermal resistance induced by thin via walls. If these traces need to transfer layers, it should be completed using multiple vias that have enough spacing such that they do not block the electrical current or heat path leading up to the via on either target layer.

The P9412 operating temperature will be influenced by the PCB design. In order to minimize the IC temperature rise, the following measures should be taken:

- Use Multiple GND planes directly connected to the all PGND, CPGND, and GND pins with vias-in-pad. Add extra vias for the PGND and CPGND pins to assist with conduction.
- Use thicker copper foil weights (1oz minimum recommended, 2oz preferred).
- Route wide copper planes/traces to every pin of the P9412, even for digital signals.
- Maximize the copper area on the component side directly connected to P9412 pins.
- Use a thinner PCB (thinner PCBs will transfer heat through their volume more readily).
- Use surfaces on all layers with copper. Avoid areas of the PCB that have all copper removed by adding GND fill to all layers after routing.

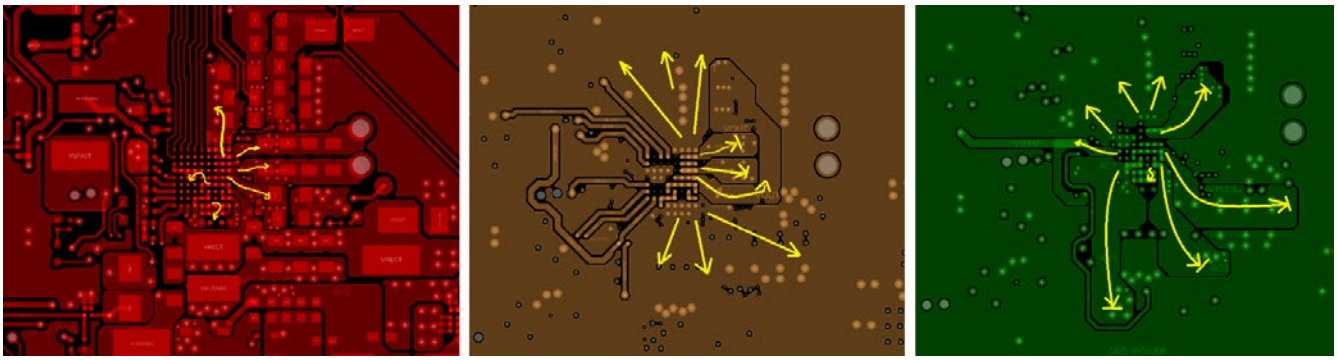


Figure 17. Examples of Heat Flow Paths and Multiple Layer Interactions

Use of multiple vias assists with current conduction and heat dissipation (Top, MID1, and MID3 shown).

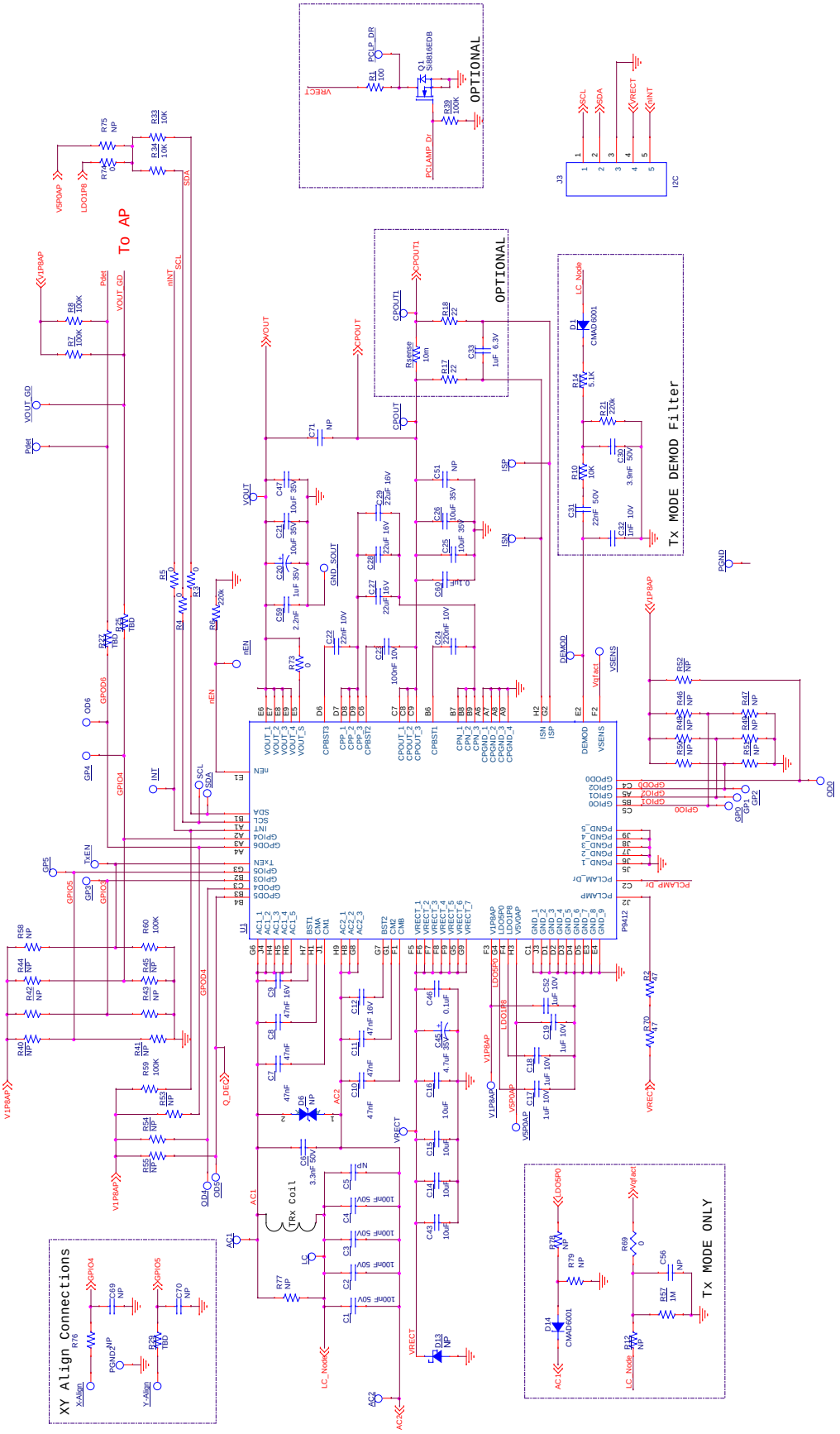
11. Audible Noise Suppression

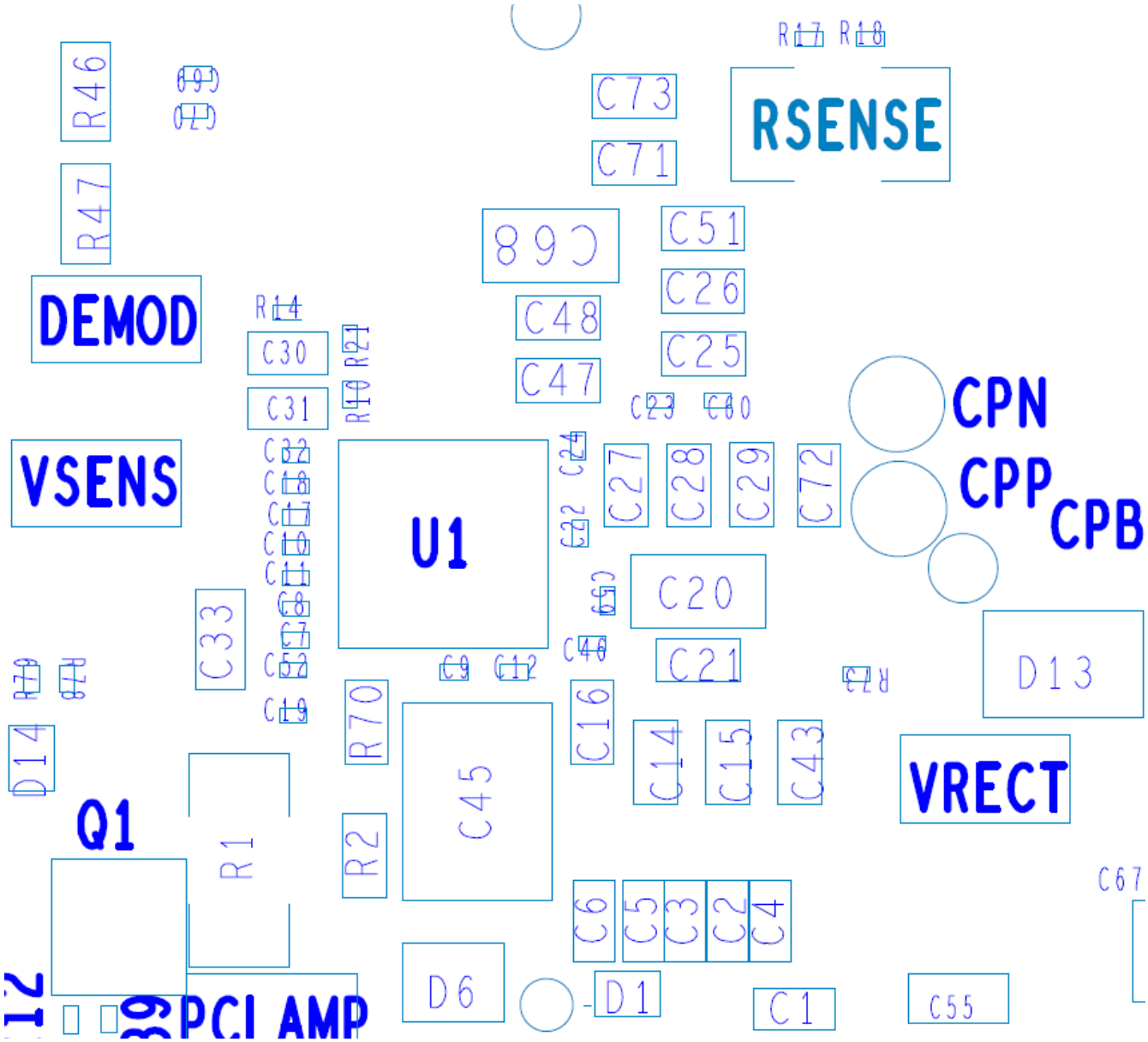
Wireless power receiver solutions have been observed to produce audible noise. If sound is detected there are several steps that can be taken to reduce or eliminate the noise. The first priority should be identifying the source (i.e., the rectifier capacitors, the TRx coil ferrite, COM/CM capacitors). Typically, the rectifier capacitors are the components that generate the audible noise. The reason the noise is present and associated with the rectifier capacitors is due to the WPC communication signals being generating in the audible frequency range and the use of small form factor ceramic capacitors. The noise occurs due to the piezoelectric effect of ceramic capacitors. The capacitors constrict and expand while providing the communication pulses due to the resulting electric field changes and this noise is amplified as it flexes the PCB. The primary solution to this issue is to use low-acoustic noise capacitors or tantalum capacitors in parallel with the ceramic capacitors. Alternately, higher voltage rated components may have superior piezoelectric properties that can reduce the audible noise.

Additionally, placing the capacitors on both sides of the PCB (directly above and below each other) counters the piezoelectric forces applied to the PCB (cancels the force by each capacitor). Another method is to add slots through the PCB on both outer sides of the capacitors or directly under each capacitor. One additional approach is to place more, lower capacitance value components in parallel to reduce the mechanical force of the piezoelectric effect per component.

For any additional questions, please refer them to your local Renesas Field Applications Engineer or Marketing Department and they will be addressed as soon as possible.

Appendix A. Full Reference Schematic and Placement Diagram




R46
R47
DEMOD
VSENS
C30
C31
C33
U1
C73
C71
RSENSE
C51
C26
C48
C25
C47
C27
C28
C29
C72
CPN
CPP
CPB
C20
C21
D13
VRECT
R70
C45
C16
C14
C15
C43
R2
R1
Q1
C6
C5
C3
C2
C4
D6
D1
C1
C55
C67
PCI AMP

References

- Spataro, Vincent. Counting squares: A method to quickly estimate PWB trace resistance. EDN Network. 2013 April 12. Web. 2016 June 3

Revision History

Revision	Date	Description
1.0	Jul.14.20	Initial release.

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