RC21008A/RC21012A

This document describes the functional description, register organization, and byte addresses of the RC21008A/RC21012A. Detailed register definitions can be located by following the hyperlinks in the document.

Contents

1. Functional Description

The RC21008A/RC21012A is a small-form factor, fully integrated, low-power, high-performance frequency synthesizer providing excellent PCIe and Ethernet phase jitter, while covering a wide range of output frequencies up to 650MHz. It can simultaneously provide low phase jitter non-spreading clocks for Ethernet and storage applications, while providing spread-spectrum PCIe Gen6 clocks.

The following sections provide an overview of the RC21008A/RC21012A.

1.1 Power-Up, Configuration, and Serial Interfaces

The RC21008A/RC21012A can be powered up and configured in three ways:

- From internal non-volatile memory using OTP user configurations (UserCfgs)
- From its slave serial interface
- From an external I2C EEPROM

The power-up sequence loads one of up to 27 *internal* UserCfgs from OTP. This configuration can be selected via external GPIO pins or by programming a field to select the default configuration to load. This is useful when external GPIO are not used to select the UserCfg at power-up. After the device is powered up, the slave serial interface can be used to select preprogrammed UserCfgs or load entirely new UserCfgs stored outside the device.

The RC21008A/RC21012A supports three slave serial interfaces: I2C, SPI, SMBUS, and one serial master interface (I2C).

These interfaces share the same pins so only one is available at a time. The I2C master interface that is used to load UserCfgs from an external I2C EEPROM is only active after loading an OTP UserCfg that indicates a further load from external I2C EEPROM. An external master (I2C, SPI, SMBUS) can be used to access internal registers. If the slave serial port is configured as SPI then loading from external EEPROM is not available.

1.2 Input Clocks

The RC21008A/RC21012A supports one crystal/reference input and up to two differential or four single-ended clock inputs.

1.2.1 Crystal/Reference Input

The crystal input supports crystal frequencies of 8MHz to 62.5MHz. It has programmable internal load capacitors to support crystals with CL = 6pF to 12pF. Internal crystal variants of RC21008A/RC21012A support a trim value in OTP that can be set during ATE to compensate for initial frequency offset of the internal crystal. The crystal input supports being over-driven with a clipped sine-wave TCXO with 0.8VPP signal.

The crystal input can being over-driven with differential or single-ended inputs with proper external terminations. The supported frequency range is same as reference clock inputs:

- 1kHz to 650MHz in differential mode
- 1kHz to 200MHz in single-ended mode

An available LOS monitor detects the loss of signal on crystal input.

1.2.2 Clock Inputs

There are two differential clock inputs that support LVDS, HCSL, or single-ended CMOS logic levels without external terminations. LVPECL or CML clock inputs can be supported with external terminations and/or AC coupling. Internal terminations are available for both HCSL and LVDS logic levels. Additionally, HCSL input terminations support both 100ohm and 85ohm operating environments.

If the cmos_sel register bit is set to single-ended type, the differential inputs turn into two single-ended inputs. CLKIN0 drives clkin0 internally, CLKIN0b drives clkin1 internally. CLKIN1 drives clkin2 internally, and CLKIN1b drives clkin3 internally. If set to differential type, CLKIN0/CLKIN0b pair drives clkin0, while CLKIN1/CLKIN1b pair

drives clkin2. Internal biasing is available for AC-coupled applications. The two clock inputs can be left floating when unused. An available LOS monitor detects the loss of signal on crystal input. The LOS status is stored in registers bits and can also be steered to a GPIO pin.

1.3 APLL

The APLL is fractional LC-VCO based PLL with an operating range from 9.5GHz to 10.7GHz. Any of the available input clocks can be selected to drive the APLL, and the input clock can be frequency doubled for increased performance. The APLL is temperature compensated for the utmost frequency stability. For synchronous, deterministic requirements, the APLL also supports ZDB mode where CLKIN0 is used for the feedback input.

1.3.1 APLL Lock Detector

The APLL lock detector indicates whether the APLL is locked to a functioning crystal or reference input by monitoring the phase errors. Lock status can be sent on to a GPIO pin and register apll_lock_sts. The falling edge of apll_lock_sts sets apll_lol event sticky bit. The apll_lol event also increments a 7-bit loss of lock counter that starts from power on. The counter values represents the total number of loss of lock since power on and can be read back from register apll_lol_cnt.

1.4 Output Dividers

The RC21008A/RC21012A provide four integer and three fractional output dividers.

1.4.1 Integer Output Dividers

All four IODs are identical and use a 25-bit divider to provide output frequencies from 1kHz to 650MHz from the VCO clock. Changing IOD values results in an immediate change to the new frequency. Glitch-less squelch and release of the IOD clock is supported with an iod_squelch bit. When enabled, this mimics a gapped clock behavior when an IOD frequency is changed.

1.4.2 Fractional Output Dividers

There are three fractional output dividers (FOD). Each FOD can divide down the VCO clock to provide frequencies of 1kHz to 650MHz. Each FOD is implemented in two stages. The first stage is an 8-bit fractional divider with Digital Control Delay (DCD) correction followed by a divide-by-2. The DCD FOD allows a divide down of the VCO clock to 30MHz to 657MHz. The FOD's second stage divider is a 17-bit integer divider with minimum divide ratio of 4. This allows output frequencies lower than 30MHz. For output frequencies above 30MHz, this second-stage divider may be bypassed.

1.4.2.1 Spread-Spectrum Clocking (SSC)

FOD0 and FOD1 support spectrum spreading.

If spreading is enabled by setting ssc_en to 1, the spread-spectrum engine generates a triangular frequency modulation on to FOD's divider ratio. The modulation amplitude is programmable in ssc_ampl register fields. The modulation can be programmed to either down spread or center spread in register ssc_mode. The peak-to-peak amplitude is two times of ssc_ampl for center spreading, and one ssc_ampl for down spreading. The supported modulation frequency is from 30kHz to 63kHz. It can be set by programming register ssc_step based on the equations provided in the register description.

When turning off spreading, it stops when the current spreading cycle's modulation returns to zero.

If FOD0 and FOD1 SSC are programmed to the same modulation frequency, the register bit ssc_share can be set to 1 to ensure that SSC for FOD0 and FOD1 are in phase. The modulation amplitude and mode (down or center spread) can be set differently. The spread engine of FOD0 will act as the master for the spread engine of FOD1 with respect to synchronization. The zero crossing of the spread triangles is where the synchronization occurs. If the center spread is used on FOD0, then the zero crossing of the upwards frequency ramp of the triangle is the synchronization point. When ssc_share is set to 1, then FOD1 ssc_en must be set to 1 before FOD0 ssc_en is set

to 1 since FOD1 SSC will start when FOD0 ssc_en is set to 1. This restriction does not apply when loading the device configuration from OTP/EEPROM on startup, but does apply if dynamically changing these settings later through a dynamic configuration load from the OTP/EEPROM, or by writing registers from the serial interface.

The minimum output frequency that can be spread is 33MHz. A spreading output clock meets the PCIe Gen1 to Gen6 standard at 100MHz.

1.4.2.2 Sync and Phase Adjustment

Each FOD can adjust its output clock phase with a step size of 1/4 VCO period up to about ±20ns. The amount of phase adjustment is programmed in register fod_phase. The adjustment can be of either positive or negative directions. The phase adjustment can be applied immediately if the fod_ph_adj_now bit is set to 1, and/or it will be applied after each time the divider is synchronized if fod_ph_adj_post_sync is set to 1.

IOD phase adjustment is same as FOD phase adjustment but with a step size of one VCO period. The amount of phase adjustment is programmed in register iod_phase. The phase adjustment can be applied immediately if the iod_ph_adj_now bit is set to 1, and/or it will be applied after each time the divider is synchronized if iod_ph_adj_post_sync is set to 1.

There are two sync groups, group0 and group1. An FOD or IOD can be assigned to either group or none by fod_sync_group or iod_sync_group, respectively. The dividers in the same group can be re-synchronized together after any one of them is re-programmed by writing 1 to od_grp0_sync or od_grp1_sync. To disable all clock outputs sourced from the dividers belonging to sync group 0 or 1 prior to re-programming until re-synchronization completes, first write 1 to clr_grp0_oe or clr_grp1_oe. If a divider is in neither group, it will not re-synchronize.

Upon power-up, after OTP has been loaded and VCO calibration completes and APLL gets locked, a sync pulse is generated automatically to all dividers including FODs, IODs, that are assigned to sync group 0 or 1.

A sync pulse can also be initiated by writing 1 to register divider_sync to synchronize all dividers assigned to group 0 and 1, or od_grp0_sync and od_grp1_sync can be used to synchronize only the dividers assigned to each group.

Writing the apll_reinit bit causes the power-up sequence to restart from the VCO calibration step, which will synchronize the dividers after the APLL locks.

1.4.2.3 Numerically Controlled Oscillator (NCO) Mode

In NCO mode, each FOD can adjust its output clock frequency with a step size of $1/2^{34}$ or 58.21ppt, and is based on incrementing the numerator while holding the 34-b denominator at a fixed value. This frequency change at the output clock is gradual without glitches.

1.5 Clock Outputs

The RC21008A/RC21012A supports up to 12 differential or 24 single-ended clock outputs, or any combination of differential and single-ended clock outputs. Every differential clock output can be programmed as two single-ended clock outputs.

1.5.1 Output Types

Differential outputs can be set to 85ohm HCSL, 100ohm HCSL, or LVDS. The HCSL outputs types are low-power push-pull HCSL (LPHCSL) with integrated terminations. They do not require external terminations to drive standard HCSL inputs, such as those found in PCIe applications. HCSL outputs have programmable output swing and HCSL outputs also have two slew rate settings (2V/ns to 4V/ns and 3V/ns to 5V/ns). LVDS outputs require only a 100ohm resistor between the true and complement inputs of the clock input being driven. Both LVDS and HCSL provide output swing levels that are compatible with LVPECL and CML with external AC coupling.

If set to single-ended mode, the output pair can drive either pin or both pins. If both pins are enabled, they can be in phase or inverted phase. The single-ended outputs support CMOS swings of 1.8V, 2.5V, or 3.3V as determined by their VDDO voltage.

1.5.2 Output Banks

The RC21008A/RC21012A maps the internal and external frequency sources to output banks that can be programmed in register output_bank_src, according to the following table. There are up to 12 clock outputs arranged in seven output banks. Each bank sits on its own VDDO (each VDDO also supplies an IOD or FOD as listed below).

Table 1. Output Bank Source Mapping

	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6
output_bank_src	**OUT0**	**OUT1**	**OUT[2:3]**	**OUT[4:7]**	**OUT[8:9]**	**OUT10**	**OUT11**
0x0	IOD0		N/A		CLKIN1		
0x1	IOD1			N/A		XIN_REFIN	N/A
0x2	N/A				IOD2		
0x3	N/A					IOD3	
0x4	FOD0				N/A		
0x5	FOD1						
0x6	N/A			FOD2			
0x7	N/A				CLKIN0		

1.6 Output Enable Control

During the power-up sequence, the clock output drivers are tri-stated until the power supplies have stabilized, then both OUTx and OUTxb are held low. After the OTP configuration load completes, the clock output drivers can be enabled or held disabled until the APLL lock according to the setting of out_startup. This behavior can be overridden by setting out_dis_group to 0x7.

After power-up, the clock output driver is then enabled, either by setting the corresponding out_dis register bit or by the designated OE pin, if assigned to an OE group. It is enabled when both the register bit and the OE pin are active. If configured in CMOS mode, OUT*x* and OUT*x*b can be enabled or disabled individually through out_prog3 and out_prog2.

There are five OE groups, each output driver can optionally be assigned to a OE group in register out_dis_group. A GPI or GPIO pin can be assigned as OE pin to a OE group in register gpi_func or gpio_func or can also be assigned as a global OE (GOE) pin with the goe register bit.

2. Register Organization

2.1 Overview

Register sizes are denoted as:

- byte: 8-bit
- hword: 16-bit
- word: 32-bit
- dword: 64-bit

Register types are defined in the following table.

Table 2. Register Type Definition

Type Indicator	Definition
R/W1C	Read/Write 1 to Clear
R/W1S	Read/Write 1 to Set
RO	Read-only
RW	Read/Write
WO	Write-only

2.2 Register Block Offsets

Table 3. Register Block Offsets

Block Offset	Block Name	Address Table	Register Description
0x000	GLOBAL	Global Addresses	Global Registers
0x020	SSI	SSI Addresses	SSI Registers
0x02C	XO	Crystal Addresses	XO Register
0x030 += 0x004	CLKIN[0:1]	Clock Input Addresses	CLKIN Register
0x050 += 0x010	LOSMON[0:4]	LOS Monitor Addresses	LOSMON Registers
0x120	APLL	APLL Addresses	APLL Registers
0x1C0 += 0x008	IOD[0:3]	IOD Addresses	IOD Registers
0x1E0 += 0x010	FOD[0:2]	FOD Addresses	FOD Registers
0x240 += 0x004	OUT[0:11]	Clock Output Driver Addresses	OUT Registers
0x280 += 0x004	BANK[0:6]	Output Bank Addresses	BANK Register
0x29C += 0x004	GPI[0:3]	GPI Addresses	GPI Registers
0x2AC += 0x004	GPIO[0:4]	GPIO Addresses	GPIO Registers
0x300 += 0x004	SSC[0:1]	SSC Addresses	SSC Register
0x308	INT	Interrupt Addresses	INT Registers

2.3 Register Offsets

2.3.1 Global Address Map

Table 4. Global Addresses

Block Offset	Size	Register Name	Register Description
0x00	hword	VENDOR_ID	VENDOR_ID - Vendor ID
0x02	hword	DEVICE_ID	DEVICE_ID - Device ID
0x04	hword	DEVICE_REV	DEVICE_REV - Device Revision
0x06	hword	DEVICE_PGM	DEVICE_PGM - Device Programming
0x0E	byte	PWR_CTL	PWR_CTL - Power Control
0x10	byte	REG_LOCK	REG_LOCK - Configuration Register Lock
0x11	byte	INIT_SYNC	INIT_SYNC - Initialization and Synchronization Register
0x12	hword	SW_RESET	SW_RESET - Software Reset Register
0x16	hword	MISC_CNFG	MISC_CNFG - Miscellaneous Configuration
0x1C	hword	STARTUP_STS	STARTUP_STS - Start-up Status
0x1E	hword	DEVICE_STS	DEVICE_STS - Device Status

2.3.2 SSI Address Map

Table 5. SSI Addresses

Offset	Size	Register Name	Register Description
0x00	byte	SPI_CNFG	SPI_CNFG - SPI Configuration
0x01	byte	I2C_FLTR_CNFG	I2C_FLTR_CNFG - I2C Filter Configuration
0x02	byte	I2C_TIMING_CNFG	I2C_TIMING_CNFG - I2C Timing Configuration
0x03	byte	I2C_ADDR_CNFG	I2C_ADDR_CNFG - I2C Address Configuration
0x04	byte	BYTE_CNT	BYTE_CNT - Byte Count
0x05	byte	SMB_CTL	SMB_CTL - SMBus Control
0x06	byte	SSI_GLOBAL_CNFG	SSI_GLOBAL_CNFG - SSI Global Configuration
0x07	byte	SSI_STS	SSI_STS - Serial Port Status

2.3.3 Crystal Address Map

Table 6. Crystal Addresses

Offset	Size	Register Name	Register Description
0x00	word	XO_CNFG	XO_CNFG - Crystal Configuration

2.3.4 Clock Input Address Map

Table 7. Clock Input Addresses

Offset	Size	Register Name	Register Description
0x00	hword	CLKIN_CNFG	CLKIN_CNFG - Clock Input Pad Configuration

2.3.5 LOS Monitor Address Map

Table 8. LOS Monitor Addresses

Offset	Size	Register Name	Register Description
0x00	hword	LOSMON_WINDOW	LOSMON_WINDOW - LOS Monitor Window Configuration
0x02	hword	LOSMON_NOMINAL	LOSMON_NOMINAL - LOS Monitor Nominal Number Configuration
0x04	word	LOSMON_THRESH	LOSMON_THRESH - LOS Monitor Threshold Configuration
0x08	byte	LOSMON_QUAL	LOSMON_QUAL - LOS Monitor Qualify Counter Configuration
0x09	byte	LOSMON_STS	LOSMON_STS - LOS Monitor Status
0x0A	byte	LOSMON_EVENT	LOSMON_EVENT - LOS Monitor Event Status
0x0B	byte	LOSMON_CNT	LOSMON_CNT - LOS Monitor Count

2.3.6 APLL Address Map

Table 9. APLL Addresses

Offset	Size	Register Name	Register Description
0x00	word	APLL_FB_DIV_FRAC	APLL_FB_DIV_FRAC - APLL Feedback Divider Fraction Configuration
0x04	hword	APLL_FB_DIV_INT	APLL_FB_DIV_INT - APLL Feedback Divider Integer Configuration
0x06	byte	APLL_FB_SDM_CNFG	APLL_FB_SDM_CNFG - APLL Feedback SDM Configuration
0x07	byte	APLL_CNFG	APLL_CNFG - APLL Configuration
0x08	hword	CP_CNFG	CP_CNFG - APLL Charge Pump Configuration
0x0A	byte	LPF_CNFG	LPF_CNFG - APLL Loop Filter Configuration
0x0B	byte	LPF_3RD_CNFG	LPF_3RD_CNFG - APLL Loop Filter 3rd Pole Configuration
0x18	word	BANK_MUX_CLK_EN	BANK_MUX_CLK_EN - Bank Mux Clock Enable

2.3.7 IOD Address Map

Table 10. IOD Addresses

Offset	Size	Register Name	Register Description
0x00	word	IOD_INT_CNFG	IOD_INT_CNFG - IOD Integer Ratio Configuration
0x04	hword	IOD_PHASE_CNFG	IOD_PHASE_CNFG - IOD Phase Configuration

2.3.8 FOD Address Map

Table 11. FOD Addresses

Offset	Size	Register Name	Register Description
0x00	dword	FOD_INT_CNFG	FOD_INT_CNFG - FOD Integer Configuration
0x08	hword	FOD_PHASE_CNFG	FOD_PHASE_CNFG - FOD Phase Configuration

2.3.9 SSC Address Map

Table 12. SSC Addresses

Offset	Size	Register Name	Register Description
0x00	word	SSC_CNFG	SSC_CNFG - Spectrum Spreading Configuration

2.3.10 Output Bank Address Map

Table 13. Output Bank Addresses

Offset	Size	Register Name	Register Description
0x00	byte	OUT_BANK_CNFG	OUT_BANK_CNFG - Output Bank Configuration

2.3.11 Clock Output Driver Address Map

Table 14. Clock Output Driver Addresses

Offset	Size	Register Name	Register Description
0x00	byte	ODRV_EN	ODRV_EN - Output Driver Enable
0x02	hword	ODRV_CNFG	ODRV_CNFG - Output Driver Configuration

2.3.12 GPI Address Map

Table 15. GPI Addresses

Offset	Size	Register Name	Register Description
0x00	hword	GPI_CNFG	GPI_CNFG - GPI Configuration
0x02	byte	GPI_STS	GPI_STS - GPI Status

2.3.13 GPIO Address Map

Table 16. GPIO Addresses

Offset	Size	Register Name	Register Description
0x00	hword	GPIO_CNFG	GPIO_CNFG - GPIO Configuration
0x02	byte	GPIO_STS	GPIO_STS - GPIO Status

2.3.14 Interrupt Address Map

Table 17. Interrupt Addresses

Offset	Size	Register Name	Register Description
0x00	word	SCRATCH0	SCRATCH0 - Software Scratch Register 0
0x04	word	INT_EN	INT_EN - Interrupt Enable
0x08	word	INT_STS	INT_STS - Interrupt Status

3. Physical Register Addresses

3.1 Global Block

Table 18. Global Block Physical Register Addresses

Address	Block Name	Register	Type	Default
0x0	GLOBAL	VENDOR_ID[0]	RO	0x33
0x1	GLOBAL	VENDOR_ID[1]	RO	0x10
0x2	GLOBAL	DEVICE_ID[0]	RW	0x00
0x3	GLOBAL	DEVICE_ID[1]	RW	0x00
0x4	GLOBAL	DEVICE_REV[0]	RO	0x22
0x5	GLOBAL	DEVICE_REV[1]	RO	0x01
0x6	GLOBAL	DEVICE_PGM[0]	RW	0x00
0x7	GLOBAL	DEVICE_PGM[1]	RW	0x00
0xe	GLOBAL	PWR_CTL	RW	0x01
0x10	GLOBAL	REG_LOCK	RW	0x00
0x11	GLOBAL	INIT_SYNC	R/W1S	0x30
0x12	GLOBAL	SW_RESET[0]	RW	0x00
0x13	GLOBAL	SW_RESET[1]	RW	0x00
0x16	GLOBAL	MISC_CNFG[0]	RW	0x05
0x17	GLOBAL	MISC_CNFG[1]	RW	0x80
0x1c	GLOBAL	STARTUP_STS[0]	RO	0x00
0x1d	GLOBAL	STARTUP_STS[1]	RO	0x00
0x1e	GLOBAL	DEVICE_STS[0]	RO	0x00
0x1f	GLOBAL	DEVICE_STS[1]	RO	0x00

3.2 SSI Block

Table 19. SSI Block Physical Register Addresses

Address	Block Name	Register	Type	Default
0x20	SSI	SPI_CNFG	RW	0x00
0x21	SSI	I2C_FLTR_CNFG	RW	0x01
0x22	SSI	I2C_TIMING_CNFG	RW	0x22
0x23	SSI	I2C_ADDR_CNFG	RW	0x09
0x24	SSI	BYTE_CNT	RW	0x08
0x25	SSI	SMB_CTL	RW	0x79
0x26	SSI	SSI_GLOBAL_CNFG	RW	0x01
0x27	SSI	SSI_STS	R/W1C	0x00

3.3 XO Block

Table 20. XO Block Physical Register Addresses

Address	Block Name	Register	Type	Default
0x2c	XO	XO_CNFG[0]	RW	0x45
0x2d	XO	XO_CNFG[1]	RW	0x28
0x2e	XO	XO_CNFG[2]	RW	0x68
0x2f	XO	XO_CNFG[3]	RW	0x20

3.4 CLKIN Block

Table 21. CLKIN Block Physical Register Addresses

Address	Block Name	Register	Type	Default
0x30	CLKIN[0]	CLKIN_CNFG[0]	RW	0x01
0x31	CLKIN[0]	CLKIN_CNFG[1]	RW	0x80
0x34	CLKIN[1]	CLKIN_CNFG[0]	RW	0x01
0x35	CLKIN[1]	CLKIN_CNFG[1]	RW	0x80

3.5 LOSMON Block

Table 22. LOSMON Block Physical Register Addresses

Address	Block Name	Register	Type	Default
0x50	LOSMON[0]	LOSMON_WINDOW[0]	RW	0x00
0x51	LOSMON[0]	LOSMON_WINDOW[1]	RW	0x00
0x52	LOSMON[0]	LOSMON_NOMINAL[0]	RW	0x00
0x53	LOSMON[0]	LOSMON_NOMINAL[1]	RW	0x00
0x54	LOSMON[0]	LOSMON_THRESH[0]	RW	0x00
0x55	LOSMON[0]	LOSMON_THRESH[1]	RW	0x00
0x56	LOSMON[0]	LOSMON_THRESH[2]	RW	0x00
0x57	LOSMON[0]	LOSMON_THRESH[3]	RW	0x00
0x58	LOSMON[0]	LOSMON_QUAL	RW	0x44
0x59	LOSMON[0]	LOSMON_STS	RO	0x03
0x5a	LOSMON[0]	LOSMON_EVENT	R/W1C	0x01
0x5b	LOSMON[0]	LOSMON_CNT	RW	0x00
0x60	LOSMON[1]	LOSMON_WINDOW[0]	RW	0x00
0x61	LOSMON[1]	LOSMON_WINDOW[1]	RW	0x00
0x62	LOSMON[1]	LOSMON_NOMINAL[0]	RW	0x00
0x63	LOSMON[1]	LOSMON_NOMINAL[1]	RW	0x00
0x64	LOSMON[1]	LOSMON_THRESH[0]	RW	0x00
0x65	LOSMON[1]	LOSMON_THRESH[1]	RW	0x00
0x66	LOSMON[1]	LOSMON_THRESH[2]	RW	0x00
0x67	LOSMON[1]	LOSMON_THRESH[3]	RW	0x00
0x68	LOSMON[1]	LOSMON_QUAL	RW	0x44
0x69	LOSMON[1]	LOSMON_STS	RO	0x03
0x6a	LOSMON[1]	LOSMON_EVENT	R/W1C	0x01
0x6b	LOSMON[1]	LOSMON_CNT	RW	0x00
0x70	LOSMON[2]	LOSMON_WINDOW[0]	RW	0x00
0x71	LOSMON[2]	LOSMON_WINDOW[1]	RW	0x00
0x72	LOSMON[2]	LOSMON_NOMINAL[0]	RW	0x00
0x73	LOSMON[2]	LOSMON_NOMINAL[1]	RW	0x00
0x74	LOSMON[2]	LOSMON_THRESH[0]	RW	0x00
0x75	LOSMON[2]	LOSMON_THRESH[1]	RW	0x00
0x76	LOSMON[2]	LOSMON_THRESH[2]	RW	0x00
0x77	LOSMON[2]	LOSMON_THRESH[3]	RW	0x00
0x78	LOSMON[2]	LOSMON_QUAL	RW	0x44
0x79	LOSMON[2]	LOSMON_STS	RO	0x03
0x7a	LOSMON[2]	LOSMON_EVENT	R/W1C	0x01
0x7b	LOSMON[2]	LOSMON_CNT	RW	0x00

Table 22. LOSMON Block Physical Register Addresses (Cont.)

Address	Block Name	Register	Type	Default
0x80	LOSMON[3]	LOSMON_WINDOW[0]	RW	0x00
0x81	LOSMON[3]	LOSMON_WINDOW[1]	RW	0x00
0x82	LOSMON[3]	LOSMON_NOMINAL[0]	RW	0x00
0x83	LOSMON[3]	LOSMON_NOMINAL[1]	RW	0x00
0x84	LOSMON[3]	LOSMON_THRESH[0]	RW	0x00
0x85	LOSMON[3]	LOSMON_THRESH[1]	RW	0x00
0x86	LOSMON[3]	LOSMON_THRESH[2]	RW	0x00
0x87	LOSMON[3]	LOSMON_THRESH[3]	RW	0x00
0x88	LOSMON[3]	LOSMON_QUAL	RW	0x44
0x89	LOSMON[3]	LOSMON_STS	RO	0x03
0x8a	LOSMON[3]	LOSMON_EVENT	R/W1C	0x01
0x8b	LOSMON[3]	LOSMON_CNT	RW	0x00
0x90	LOSMON[4]	LOSMON_WINDOW[0]	RW	0x00
0x91	LOSMON[4]	LOSMON_WINDOW[1]	RW	0x00
0x92	LOSMON[4]	LOSMON_NOMINAL[0]	RW	0x00
0x93	LOSMON[4]	LOSMON_NOMINAL[1]	RW	0x00
0x94	LOSMON[4]	LOSMON_THRESH[0]	RW	0x00
0x95	LOSMON[4]	LOSMON_THRESH[1]	RW	0x00
0x96	LOSMON[4]	LOSMON_THRESH[2]	RW	0x00
0x97	LOSMON[4]	LOSMON_THRESH[3]	RW	0x00
0x98	LOSMON[4]	LOSMON_QUAL	RW	0x44
0x99	LOSMON[4]	LOSMON_STS	RO	0x03
0x9a	LOSMON[4]	LOSMON_EVENT	R/W1C	0x01
0x9b	LOSMON[4]	LOSMON_CNT	RW	0x00

3.6 APLL Block

Table 23. APLL Block Physical Register Addresses

Address	Block Name	Register	Type	Default
0x120	APLL	APLL_FB_DIV_FRAC[0]	RW	0x00
0x121	APLL	APLL_FB_DIV_FRAC[1]	RW	0x00
0x122	APLL	APLL_FB_DIV_FRAC[2]	RW	0x00
0x123	APLL	APLL_FB_DIV_FRAC[3]	RW	0x00
0x124	APLL	APLL_FB_DIV_INT[0]	RW	0x69
0x125	APLL	APLL_FB_DIV_INT[1]	RW	0x00
0x126	APLL	APLL_FB_SDM_CNFG	RW	0x03
0x127	APLL	APLL_CNFG	RW	0x01

Table 23. APLL Block Physical Register Addresses (Cont.)

Address	Block Name	Register	Type	Default
0x128	APLL	CP_CNFG[0]	RW	0x33
0x129	APLL	CP_CNFG[1]	RW	0x03
0x12a	APLL	LPF_CNFG	RW	0x74
0x12b	APLL	LPF_3RD_CNFG	RW	0x44
0x13f	APLL	APLL_STS	RO	0x00

3.7 IOD Block

Table 24. IOD Block Physical Addresses

Address	Block Name	Register	Type	Default
0x1c0	IOD[0]	IOD_INT_CNFG[0]	RW	0x64
0x1c1	IOD[0]	IOD_INT_CNFG[1]	RW	0x00
0x1c2	IOD[0]	IOD_INT_CNFG[2]	RW	0x00
0x1c3	IOD[0]	IOD_INT_CNFG[3]	RW	0x00
0x1c4	IOD[0]	IOD_PHASE_CNFG[0]	RW	0x00
0x1c5	IOD[0]	IOD_PHASE_CNFG[1]	R/W1S	0x00
0x1c8	IOD[1]	IOD_INT_CNFG[0]	RW	0x64
0x1c9	IOD[1]	IOD_INT_CNFG[1]	RW	0x00
0x1ca	IOD[1]	IOD_INT_CNFG[2]	RW	0x00
0x1cb	IOD[1]	IOD_INT_CNFG[3]	RW	0x00
0x1cc	IOD[1]	IOD_PHASE_CNFG[0]	RW	0x00
0x1cd	IOD[1]	IOD_PHASE_CNFG[1]	R/W1S	0x00
0x1d0	IOD[2]	IOD_INT_CNFG[0]	RW	0x64
0x1d1	IOD[2]	IOD_INT_CNFG[1]	RW	0x00
0x1d2	IOD[2]	IOD_INT_CNFG[2]	RW	0x00
0x1d3	IOD[2]	IOD_INT_CNFG[3]	RW	0x00
0x1d4	IOD[2]	IOD_PHASE_CNFG[0]	RW	0x00
0x1d5	IOD[2]	IOD_PHASE_CNFG[1]	R/W1S	0x00
0x1d8	IOD[3]	IOD_INT_CNFG[0]	RW	0x64
0x1d9	IOD[3]	IOD_INT_CNFG[1]	RW	0x00
0x1da	IOD[3]	IOD_INT_CNFG[2]	RW	0x00
0x1db	IOD[3]	IOD_INT_CNFG[3]	RW	0x00
0x1dc	IOD[3]	IOD_PHASE_CNFG[0]	RW	0x00
0x1dd	IOD[3]	IOD_PHASE_CNFG[1]	R/W1S	0x00

3.8 FOD Block

Table 25. FOD Block Physical Addresses

Address	Block Name	Register	Type	Default
0x1e0	FOD[0]	FOD_INT_CNFG[0]	RW	0x64
0x1e1	FOD[0]	FOD_INT_CNFG[1]	RW	0x00
0x1e2	FOD[0]	FOD_INT_CNFG[2]	RW	0x00
0x1e3	FOD[0]	FOD_INT_CNFG[3]	RW	0x00
0x1e4	FOD[0]	FOD_INT_CNFG[4]	RW	0x00
0x1e5	FOD[0]	FOD_INT_CNFG[5]	RW	0x00
0x1e6	FOD[0]	FOD_INT_CNFG[6]	RW	0x00
0x1e7	FOD[0]	FOD_INT_CNFG[7]	RW	0x00
0x1e8	FOD[0]	FOD_PHASE_CNFG[0]	RW	0xf0
0x1e9	FOD[0]	FOD_PHASE_CNFG[1]	R/W1S	0x43
0x1f0	FOD[1]	FOD_INT_CNFG[0]	RW	0x64
0x1f1	FOD[1]	FOD_INT_CNFG[1]	RW	0x00
0x1f2	FOD[1]	FOD_INT_CNFG[2]	RW	0x00
0x1f3	FOD[1]	FOD_INT_CNFG[3]	RW	0x00
0x1f4	FOD[1]	FOD_INT_CNFG[4]	RW	0x00
0x1f5	FOD[1]	FOD_INT_CNFG[5]	RW	0x00
0x1f6	FOD[1]	FOD_INT_CNFG[6]	RW	0x00
0x1f7	FOD[1]	FOD_INT_CNFG[7]	RW	0x00
0x1f8	FOD[1]	FOD_PHASE_CNFG[0]	RW	0xf0
0x1f9	FOD[1]	FOD_PHASE_CNFG[1]	R/W1S	0x43
0x200	FOD[2]	FOD_INT_CNFG[0]	RW	0x64
0x201	FOD[2]	FOD_INT_CNFG[1]	RW	0x00
0x202	FOD[2]	FOD_INT_CNFG[2]	RW	0x00
0x203	FOD[2]	FOD_INT_CNFG[3]	RW	0x00
0x204	FOD[2]	FOD_INT_CNFG[4]	RW	0x00
0x205	FOD[2]	FOD_INT_CNFG[5]	RW	0x00
0x206	FOD[2]	FOD_INT_CNFG[6]	RW	0x00
0x207	FOD[2]	FOD_INT_CNFG[7]	RW	0x00
0x208	FOD[2]	FOD_PHASE_CNFG[0]	RW	0xf0
0x209	FOD[2]	FOD_PHASE_CNFG[1]	R/W1S	0x43

3.9 OUT Block

Table 26. OUT Block Physical Addresses

Address	Block Name	Register	Type	Default
0x240	OUT[0]	ODRV_EN	RW	0x06
0x242	OUT[0]	ODRV_CNFG[0]	RW	0x3c
0x243	OUT[0]	ODRV_CNFG[1]	RW	0x00
0x244	OUT[1]	ODRV_EN	RW	0x06
0x246	OUT[1]	ODRV_CNFG[0]	RW	0x3c
0x247	OUT[1]	ODRV_CNFG[1]	RW	0x00
0x248	OUT[2]	ODRV_EN	RW	0x06
0x24a	OUT[2]	ODRV_CNFG[0]	RW	0x3c
0x24b	OUT[2]	ODRV_CNFG[1]	RW	0x00
0x24c	OUT[3]	ODRV_EN	RW	0x06
0x24e	OUT[3]	ODRV_CNFG[0]	RW	0x3c
0x24f	OUT[3]	ODRV_CNFG[1]	RW	0x00
0x250	OUT[4]	ODRV_EN	RW	0x06
0x252	OUT[4]	ODRV_CNFG[0]	RW	0x3c
0x253	OUT[4]	ODRV_CNFG[1]	RW	0x00
0x254	OUT[5]	ODRV_EN	RW	0x06
0x256	OUT[5]	ODRV_CNFG[0]	RW	0x3c
0x257	OUT[5]	ODRV_CNFG[1]	RW	0x00
0x258	OUT[6]	ODRV_EN	RW	0x06
0x25a	OUT[6]	ODRV_CNFG[0]	RW	0x3c
0x25b	OUT[6]	ODRV_CNFG[1]	RW	0x00
0x25c	OUT[7]	ODRV_EN	RW	0x06
0x25e	OUT[7]	ODRV_CNFG[0]	RW	0x3c
0x25f	OUT[7]	ODRV_CNFG[1]	RW	0x00
0x260	OUT[8]	ODRV_EN	RW	0x06
0x262	OUT[8]	ODRV_CNFG[0]	RW	0x3c
0x263	OUT[8]	ODRV_CNFG[1]	RW	0x00
0x264	OUT[9]	ODRV_EN	RW	0x06
0x266	OUT[9]	ODRV_CNFG[0]	RW	0x3c
0x267	OUT[9]	ODRV_CNFG[1]	RW	0x00
0x268	OUT[10]	ODRV_EN	RW	0x06
0x26a	OUT[10]	ODRV_CNFG[0]	RW	0x3c
0x26b	OUT[10]	ODRV_CNFG[1]	RW	0x00
0x26c	OUT[11]	ODRV_EN	RW	0x06
0x26e	OUT[11]	ODRV_CNFG[0]	RW	0x3c
0x26f	OUT[11]	ODRV_CNFG[1]	RW	0x00

3.10 BANK Block

Table 27. BANK Block Physical Addresses

Address	Block Name	Register	Type	Default
0x280	BANK[0]	OUT_BANK_CNFG	RW	0x05
0x284	BANK[1]	OUT_BANK_CNFG	RW	0x05
0x288	BANK[2]	OUT_BANK_CNFG	RW	0x05
0x28c	BANK[3]	OUT_BANK_CNFG	RW	0x05
0x290	BANK[4]	OUT_BANK_CNFG	RW	0x05
0x294	BANK[5]	OUT_BANK_CNFG	RW	0x05
0x298	BANK[6]	OUT_BANK_CNFG	RW	0x05

3.11 GPI Block

Table 28. GPI Block Physical Addresses

Address	Block Name	Register	Type	Default
0x29c	GPI[0]	GPI_CNFG[0]	RW	0x7f
0x29d	GPI[0]	GPI_CNFG[1]	RW	0x00
0x29e	GPI[0]	GPI_STS	RO	0x00
0x2a0	GPI[1]	GPI_CNFG[0]	RW	0x7f
0x2a1	GPI[1]	GPI_CNFG[1]	RW	0x00
0x2a2	GPI[1]	GPI_STS	RO	0x00
0x2a4	GPI[2]	GPI_CNFG[0]	RW	0x7f
0x2a5	GPI[2]	GPI_CNFG[1]	RW	0x00
0x2a6	GPI[2]	GPI_STS	RO	0x00
0x2a8	GPI[3]	GPI_CNFG[0]	RW	0x7f
0x2a9	GPI[3]	GPI_CNFG[1]	RW	0x00
0x2aa	GPI[3]	GPI_STS	RO	0x00

3.12 GPIO Block

Table 29. GPIO Block Physical Addresses

Address	Block Name	Register	Type	Default
0x2ac	GPIO[0]	GPIO_CNFG[0]	RW	0x90
0x2ad	GPIO[0]	GPIO_CNFG[1]	RW	0x04
0x2ae	GPIO[0]	GPIO_STS	RO	0x00
0x2b0	GPIO[1]	GPIO_CNFG[0]	RW	0x90
0x2b1	GPIO[1]	GPIO_CNFG[1]	RW	0x04

Table 29. GPIO Block Physical Addresses (Cont.)

Address	Block Name	Register	Type	Default
0x2b2	GPIO[1]	GPIO_STS	RO	0x00
0x2b4	GPIO[2]	GPIO_CNFG[0]	RW	0x90
0x2b5	GPIO[2]	GPIO_CNFG[1]	RW	0x04
0x2b6	GPIO[2]	GPIO_STS	RO	0x00
0x2b8	GPIO[3]	GPIO_CNFG[0]	RW	0x90
0x2b9	GPIO[3]	GPIO_CNFG[1]	RW	0x04
0x2ba	GPIO[3]	GPIO_STS	RO	0x00
0x2bc	GPIO[4]	GPIO_CNFG[0]	RW	0x90
0x2bd	GPIO[4]	GPIO_CNFG[1]	RW	0x04
0x2be	GPIO[4]	GPIO_STS	RO	0x00

3.13 SSC Block

Table 30. SSC Block Physical Register Addresses

Address	Block Name	Register	Type	Default
0x300	SSC[0]	SSC_CNFG[0]	RW	0x8c
0x301	SSC[0]	SSC_CNFG[1]	RW	0x2b
0x302	SSC[0]	SSC_CNFG[2]	RW	0x51
0x303	SSC[0]	SSC_CNFG[3]	RW	0x00
0x304	SSC[1]	SSC_CNFG[0]	RW	0x8c
0x305	SSC[1]	SSC_CNFG[1]	RW	0x2b
0x306	SSC[1]	SSC_CNFG[2]	RW	0x51
0x307	SSC[1]	SSC_CNFG[3]	RW	0x00

3.14 INT Block

Table 31. INT Block Physical Register Addresses

Address	Block Name	Register	Type	Default
0x308	INT	SCRATCH0[0]	RW	0x00
0x309	INT	SCRATCH0[1]	RW	0x00
0x30a	INT	SCRATCH0[2]	RW	0x00
0x30b	INT	SCRATCH0[3]	RW	0x00
0x30c	INT	INT_EN[0]	RW	0x00
0x30d	INT	INT_EN[1]	RW	0x00
0x30e	INT	INT_EN[2]	RW	0x00
0x30f	INT	INT_EN[3]	RW	0x00

Table 31. INT Block Physical Register Addresses (Cont.)

Address	Block Name	Register	Type	Default
0x310	INT	INT_STS[0]	RO	0x00
0x311	INT	INT_STS[1]	RO	0x00
0x312	INT	INT_STS[2]	RO	0x00
0x313	INT	INT_STS[3]	RO	0x00

4. Register Descriptions

4.1 Global Registers

Table 32. VENDOR_ID - Vendor ID

Bit Field	Field Name	Type	Default Value	Description
15:12	dev_id_type	RO	0x1	Device ID Block Type A value of 0x1 indicates that this register is followed by a 16-bit Device ID register and an 16-bit Device Revision register, and a 16-bit Device Programming register.
11	reserved	RO	0x0	Reserved.
10:0	vendor_id	RO	0x33	Vendor ID. Renesas/IDT JEDEC ID.

Table 33. DEVICE_ID - Device ID

Bit Field	Field Name	Type	Default Value	Description
15:0	device_id	RW	0x0	Device ID. For default value refer to Product Identification. This field is writeable so it can be configured from OTP.

Table 34. DEVICE_REV - Device Revision

Bit Field	Field Name	Type	Default Value	Description
15:13	reserved	RO	0x0	Reserved.
12:8	font_id	RO	0x1	Font ID. ID to distinguish die variants. Decode as follows: ▪ 0x0 = Font 0 (Test Vehicle) ▪ 0x1 = Font 1 (Rev A Font 1)
7:4	ana_rev	RO	0x2	Hardware analog revision. Decode as follows: ▪ 0x1 = Test vehicle ▪ 0x2 = Rev A
3:0	dig_rev	RO	0x2	Hardware digital revision. Decode as follows: ▪ 0x1 = Test vehicle ▪ 0x2 = Rev A

Table 35. DEVICE_PGM - Device Programming

Bit Field	Field Name	Type	Default Value	Description
15:0	dash_code	RW	0x0	Dash code. Decimal value assigned by IDT to identify the user configuration loaded in OTP at the factory. This field is write-able and is configured from the OTP common configuration programmed at the factory. 0x0 = No user configurations are programmed at the factory

Table 36. PWR_CTL - Power Control

Bit Field	Field Name	Type	Default Value	Description
7:1	reserved	RO	0x0	Reserved.
0	pd_restoreb	RW	0x1	Power Down Restore (Active Low) Controls the device behavior when PWRGD/PWRDN# falls to enter power down.If pd_restoreb is set to 0, it will be reset back to 1 by the reset sequence. ▪ 0x0 = Full power-on-reset. The falling edge of the PWRGD/PWRDN# pin resets the device, including configuration registers, to the initial power-on-reset state. The startup sequence is executed. It will wait for the rising edge of the PWRGD/PWRDN# pin to re-latch static CSEL inputs and load the corresponding user configuration, as on initial power-up. ▪ 0x1 = Quick power down and power up sequence. The falling and subsequent rising edge of the PWRGD/PWRDN# pin trigger dynamic configuration loads which program the device to enter the powered down and powered up states, respectively. The startup sequence is not executed, and static CSEL inputs are not re-latched.

Table 37. REG_LOCK - Configuration Register Lock

Bit Field	Field Name	Type	Default Value	Description
7:0	reg_lock_key	RW	0x0	Configuration register lock key. Writing this field with 0xCB sets the config_reg_ro bit to 1. Writing this field with 0x34 clears the config_reg_ro bit to 0.

Table 38. INIT_SYNC - Initialization and Synchronization Register

Bit Field	Field Name	Type	Default Value	Description
7	clr_grp1_oe	RW1S	0x0	Clear Reset Sequencer Sync Group 1 Output Enable. Writing this bit to 1 clears the sync group 1 output enable from the reset sequencer. The reset sequencer will set it back to 1 after the next group 1 divider synchronization completes. This affects all outputs in banks that select a divider assigned to sync group 1. Self-cleared immediately. Must not be set to 1 at the same time as any of divider_sync, od_grp0_sync and od_grp1_sync are set to 1.
6	clr_grp0_oe	RW1S	0x0	Clear Reset Sequencer Sync Group 0 Output Enable. Writing this bit to 1 clears the sync group 0 output enable from the reset sequencer. The reset sequencer will set it back to 1 after the next group 0 divider synchronization completes. This affects all outputs in banks that select a divider assigned to sync group 0. Self-cleared immediately. Must not be set to 1 at the same time as any of divider_sync, od_grp0_sync and od_grp1_sync are set to 1.

Table 38. INIT_SYNC - Initialization and Synchronization Register

Bit Field	Field Name	Type	Default Value	Description
5	id_global_setb	RW	0x1	Input Dividers Common Set. When cleared, all input dividers are held in set mode (bit is active low). This allows set and release of all dividers at roughly the same time.
4	goe	RW	0x1	Output Global OE. This bit allows manual CSR control of the global output OE.
3	od_grp1_sync	RW1S	0x0	Divider Group 1 Sync Trigger Write 1 to trigger synchronization of output dividers in group 1 as defined in iod_sync_group and fod_sync_group. The affected output clocks will be squelched for approximately the sync_dis_wait duration. Self-cleared immediately.
2	od_grp0_sync	RW1S	0x0	Divider Group 0 Sync Trigger Write 1 to trigger synchronization of output dividers in group 0 as defined in iod_sync_group and fod_sync_group. The affected output clocks will be squelched for approximately the sync_dis_wait duration. Self-cleared immediately.
1	divider_sync	RW1S	0x0	Divider Synchronization. Write 1 to trigger synchronization of output dividers in groups 0 and 1 as defined in iod_sync_group and fod_sync_group.The affected output clocks will be squelched for approximately the sync_dis_wait duration. Self-cleared immediately.
0	apll_reinit	RW1S	0x0	APLL Reinitialization. Writing this bit to 1 re-starts the startup sequence from the VCO calibration step, including divider synchronization. Self-cleared immediately.

Table 39. SW_RESET - Software Reset Register

Bit Field	Field Name	Type	Default Value	Description
15:12	reserved	RO	0x0	Reserved.
11	out_rst	RW	0x0	Output Driver Reset. This bit resets and disables all output drivers. Reset assertion acts asynchronously and can cause output glitches or runt pulses. Reset assertion acts synchronously.
10	config_rst	RW	0x0	Configuration reset. Writing this bit to 1 resets the digital logic including the registers and re-starts the startup sequence at the bias calibration, if the device is not already executing the startup sequence (during the startup sequence, writes to this bit are masked). This bit can be set to 1 by the first write in a static OTP/EEPROM User Configuration in order to revert the CSRs to their default values. The static CSEL pins are not latched. If written from a User Configuration, that same User Configuration is loaded during the startup sequence. If written from the serial port, the User Configuration to load during the startup sequence is determined by the originally latched CSEL pins, as on device power-up. If written from the serial port, the reset is triggered after the serial port write transaction completes. Self-cleared by the reset.
9	dig_sw_rst	RW	0x0	Digital Logic Software reset. Writing this bit to 1 resets all digital logic including the registers and re-starts the startup sequence at the latching of the static CSEL pins. The reset is triggered after the serial port write transaction completes. Self-cleared by the reset.

Table 39. SW_RESET - Software Reset Register (Cont.)

Bit Field	Field Name	Type	Default Value	Description
8	otp_sw_rst	RW	0x0	Configuration Loader Software reset. The configuration loader logic is held in reset while this bit is set to 1. This bit must not be set through the OTP/EEPROM configuration, otherwise the part will become unresponsive.
7	oc_ssc_sw_rst	RW	0x0	Over-Clock and Spread-Spectrum Engine Software reset. The over-clocking engine and both spread-spectrum blocks are held in reset while this bit is set to 1.
6	reserved	RW	0x0	Reserved
5	reserved	RW	0x0	Reserved
4	clkmon4_sw_rst	RW	0x0	CLKMON4 Software reset. The Clock Monitor 4 is held in reset while this bit is set to 1. While re-programming the refin LOS monitor CSRs after device start-up, clkmon4_sw_rst must be set to 1.
3	clkmon3_sw_rst	RW	0x0	CLKMON3 Software reset. The Clock Monitor 3 is held in reset while this bit is set to 1. While re-programming the clkin3 LOS or Frequency monitor CSRs after device start-up, clkmon3_sw_rst must be set to 1.
2	clkmon2_sw_rst	RW	0x0	CLKMON2 Software reset. The Clock Monitor 2 is held in reset while this bit is set to 1. While re-programming the clkin2 LOS or Frequency monitor CSRs after device start-up, clkmon2_sw_rst must be set to 1.
1	clkmon1_sw_rst	RW	0x0	CLKMON1 Software reset. The Clock Monitor 1 is held in reset while this bit is set to 1. While re-programming the clkin1 LOS or Frequency monitor CSRs after device start-up, clkmon1_sw_rst must be set to 1.
0	clkmon0_sw_rst	RW	0x0	CLKMON0 Software reset. The Clock Monitor 0 is held in reset while this bit is set to 1. While re-programming the clkin0 LOS or Frequency monitor CSRs after device start-up, clkmon0_sw_rst must be set to 1.

Table 40. MISC_CNFG - Miscellaneous Configuration

Bit Field	Field Name	Type	Default Value	Description
15:10	Reserved	RW	0x20	Reserved
9:8	fanout_buf_mode1	RW	0x0	CLKIN1 Fan-out Buffer Mode. Configures the device to operate in fan-out buffer mode from CLKIN1. Independent from the CLKIN0 fanout_buf_mode setting. ▪ 0x0 = CLKIN1 Fan-out buffer mode disabled or Manual fan-out buffer mode, output banks select their clock sources according to output_bank_src. fanout_clkmode1 reads back as 0. ▪ 0x1 = Automatic fan-out buffer mode. In banks where bank_fanout_mode is set to 2 (not available on Bank 6), output bank clock source selection is based on CLKIN1 LOS and is latched at the rising edge of PERST1#. The selected mode can be read in fanout_clkmode1. ▪ 0x3 = Manual fan-out buffer mode, CLKIN1 fans out to output clocks in banks where bank_fanout_mode is set to 2. fanout_clkmode1 reads back as 1.

Table 40. MISC_CNFG - Miscellaneous Configuration (Cont.)

Bit Field	Field Name	Type	Default Value	Description
7:6	out_startup	RW	0x0	Output Disable on startup until PLL locks. Controls whether the clock output drivers are disabled until the APLL or DPLL locks during the startup sequence. When output_startup is not set to 0x2, individual output clocks may be configured to ignore APLL/DPLL lock status by setting their out_dis_group to 0x7. ▪ 0x0 = Clock output drivers are disabled until APLL lock asserts ▪ 0x1 = Clock output drivers are disabled until DPLL lock asserts ▪ 0x2 = Clock output drivers are not disabled by APLL or DPLL lock status ▪ 0x3 = Reserved
5	ssc_share	RW	0x0	Spectrum Spreading Share When two SSC engines have the same modulation frequency, setting this bit to 1 will align the phase of FOD1 SSC to FOD0 SSC. Refer to ssc_en for restrictions on enabling the SSCs when ssc_share is set to 1.
4:3	fanout_buf_mode	RW	0x0	CLKIN0 Fan-out Buffer Mode. Configures the device to operate in fan-out buffer mode from CLKIN0. Independent from the CLKIN1 fanout_buf_mode1 setting. ▪ 0x0 = CLKIN0 Fan-out buffer mode disabled or Manual fan-out buffer mode, output banks select their clock sources according to output_bank_src. fanout_clkmode reads back as 0. ▪ 0x1 = Automatic fan-out buffer mode. In banks where bank_fanout_mode is set to 1, output bank clock source selection is based on CLKIN0 LOS and is latched at the rising edge of PERST#. The selected mode can be read in fanout_clkmode. ▪ 0x3 = Manual fan-out buffer mode, CLKIN0 fans out to output clocks in banks where bank_fanout_mode is set to 1. fanout_clkmode reads back as 1.
2:0	Reserved	RW	0x5	Reserved

Table 41. STARTUP_STS - Start-up Status

Bit Field	Field Name	Type	Default Value	Description
15:6	reserved	RO	0x0	Reserved.
5:4	gpio2_latched	RO	0x0	GPIO2 Value Latched at Startup. Value of GPIO2 latched at startup (when PWRGD/PWRDN# first becomes high, if pwrdn_sel selects a PWRGD/PWRDN# pin). ▪ 0x0 = tri-level low ▪ 0x1 = tri-level mid ▪ 0x2 = unused ▪ 0x3 = tri-level high

Table 41. STARTUP_STS - Start-up Status (Cont.)

Bit Field	Field Name	Type	Default Value	Description
3:2	gpio1_latched	RO	0x0	GPIO1 Value Latched at Startup. Value of GPIO1 latched at startup (when PWRGD/PWRDN# first becomes high, if pwrdn_sel selects a PWRGD/PWRDN# pin). ▪ 0x0 = tri-level low ▪ 0x1 = tri-level mid ▪ 0x2 = unused ▪ 0x3 = tri-level high
1:0	gpio0_latched	RO	0x0	GPIO0 Value Latched at Startup. Value of GPIO0 latched at startup (when PWRGD/PWRDN# first becomes high, if pwrdn_sel selects a PWRGD/PWRDN# pin). ▪ 0x0 = tri-level low ▪ 0x1 = tri-level mid ▪ 0x2 = unused ▪ 0x3 = tri-level high

Table 42. DEVICE_STS - Device Status

Bit Field	Field Name	Type	Default Value	Description
15	fanout_clkmode1	RO	0x0	CLKIN1 Fanout Clock Mode. Set to 1 when CLKIN1 fanout buffer mode is enabled (fanout_buf_mode1 is not set to 0x0) and CLKIN1 is passed to the output clocks.
14	fanout_clkmode	RO	0x0	CLKIN0 Fanout Clock Mode. Set to 1 when CLKIN0 fanout buffer mode is enabled (fanout_buf_mode is not set to 0x0) and CLKIN0 is passed to the output clocks.
13:10	reserved	RO	0x0	Reserved.
9	device_ready	RO	0x0	Device Ready. Set to 1 when the configuration load (OTP and/or EEPROM) completes during the startup sequence. Cleared during a dynamic configuration load.
8	config_reg_ro	RO	0x0	Configuration register read-only status. When this bit is 1, writes to configuration registers are ignored. Writes to bits of type RW1C, reg_lock_key and certain RW and RW1S bits always succeed. Use the reg_lock_key field to set/clear this bit.
7	otp_detect_se	RO	0x0	OTP Loader Detected Single-Ended Mode. When high, indicates that the OTP loader detected that the OTP image is configured for single-ended mode.
6	eeprom_config_valid	RO	0x0	Valid EEPROM User Configuration Loaded. Indicates that the user configuration in config_loaded was successfully loaded from EEPROM. Only valid when device_ready is 1.
5	otp_config_valid	RO	0x0	Valid OTP User Configuration Loaded. Indicates that the user configuration in config_loaded was successfully loaded from OTP. Only valid when device_ready is 1.
4:0	config_loaded	RO	0x0	User Configuration Loaded. Indicates the user configuration loaded from OTP/EEPROM on start-up or a dynamic configuration load. Note that on startup, the common configuration is always loaded prior to the user configuration. Only valid when device_ready is 1.

4.2 SSI Registers

Table 43. SPI_CNFG - SPI Configuration

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	Reserved.
3	spi_del_out	RW	0x0	SDO delay. ▪ 0x0 = SDO is driven on opposite SCLK edge than the sampling edge ▪ 0x1 = SDO is delayed one half cycle of SCLK
2	reserved	RO	0x0	Reserved.
1	spi_clk_sel	RW	0x0	SDI sampling edge selection. ▪ 0x0 = SDI is sampled on rising SCLK edge ▪ 0x1 = SDI is sampled on falling SCLK edge
0	spi_3wire	RW	0x0	Select SPI 3 or 4-wire mode. ▪ 0x0 = Normal 4-wire SPI. Data is received on the GPI/GPIO pin assigned as SDI, and transmitted on the GPIO pin assigned as SDO. ▪ 0x1 = 3-wire SPI. Data is received and transmitted on the GPIO pin assigned as SDIO.

Table 44. I2C_FLTR_CNFG - I2C Filter Configuration

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	Reserved
3:0	i2c_spike_fltr	RW	0x1	I2C/SMBus digital spike filter duration. Controls the duration of the digital spike filters on the SCL and SDA inputs, specified in number of system clock cycles (16.7ns). 0 disables filtering.

Table 45. I2C_TIMING_CNFG - I2C Timing Configuration

Bit Field	Field Name	Type	Default Value	Description
7:4	i2c_sda_high_hold	RW	0x2	I2C/SMBus transmit one bit delay. Delays transmission of 1 value by this number of 133ns periods (8 system clock cycles).
3:0	i2c_sda_low_hold	RW	0x2	I2C/SMBus transmit zero bit delay. Delays transmission of 0 value by this number of 133ns periods (8 system clock cycles).

Table 46. I2C_ADDR_CNFG - I2C Address Configuration

Bit Field	Field Name	Type	Default Value	Description
7	reserved	RO	0x0	Reserved
6:0	i2c_addr	RW	0x09	I2C device address. Sets I2C or SMBus device address that the SSI will acknowledge and accept accesses on.

Table 47. BYTE_CNT - Byte Count

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	Reserved
5:0	bc	RW	0x08	Byte Count Defines how many bytes are in an SMBus block transaction. This register is modified by the SMBus interface logic when a block transaction is processed.

Table 48. SMB_CTL - SMBus Control

Bit Field	Field Name	Type	Default Value	Description
7	reserved	RO	0x0	Reserved
6	smb_d_to_en	RW	0x1	SMBus Data Timeout Enable Enables the SMBus data timeout check. When this bit is set to 1, the clock timeout must also be enabled (smb_to_cnt is not 0). When a data timeout is detected, the smb_d_to bit is set to 1.
5	smb_to_en	RW	0x1	Reserved
4:0	smb_to_cnt	RW	0x19	SMBus Timeout Duration Sets the clock and data timeout duration in milliseconds. When this field is set to 0, the clock timeout is disabled and smb_d_to_en must also be set to 0 to disable the data timeout. When a clock timeout is detected, the smb_to bit is set to 1.

Table 49. SSI_GLOBAL_CNFG - SSI Global Configuration

Bit Field	Field Name	Type	Default Value	Description
7:5	reserved	RO	0x0	Reserved
4:3	sda_sdi_drv	RW	0x0	I2C/SMBus Drive Strength. Selects the output driver slew rate of the SDA_nCS and SCL_SCLK pins when the serial slave interface is configured for I2C/SMBus mode (higher settings means higher drive strength). This setting does not affect the internal timing. As an I2C/SMBus slave, the external I2C/SMBus master must provide the appropriate SCL frequency and other timing requirements according to the selected speed. ▪ 0x0 = 1.8V Standard mode (100 kHz) or 2.5V/3.3V standard (100kHz) and Fast mode (400kHz) ▪ 0x1 = 1.8V Fast mode (400 kHz) ▪ 0x2 = Reserved ▪ 0x3 = 1.8V/2.5V/3.3V Fast mode plus (1MHz)
2	ssi_addr_size	RW	0x0	SSI address size When 0 the SSI expects 1-byte CSR addresses; when 1 the SSI expects 2-byte CSR addresses. Upper address bits are taken from the SSI's page register to create a full 32-bit CSR address. ▪ 0x0 = 1-byte address ▪ 0x1 = 2-byte address
1:0	ssi_enable	RW	0x1	SSI mode. ▪ 0x0 = SSI is disabled ▪ 0x1 = SSI is in I2C mode ▪ 0x2 = SSI is in SPI mode ▪ 0x3 = SSI is in SMBus mode

Table 50. SSI_STS - Serial Port Status

Bit Field	Field Name	Type	Default Value	Description
7:2	reserved	RO	0x0	Reserved
1	smb_d_to	RW1C	0x0	SMBus Data Timeout. Set when the SMBus interface detects a data timeout.
0	smb_to	RW1C	0x0	SMBus Clock Timeout. Set when the SMBus interface detects a clock timeout.

4.3 XO Register

Table 51. XO_CNFG - Crystal Configuration

Bit Field	Field Name	Type	Default Value	Description
31:30	reserved	RO	0x0	Reserved
29	xo_ib_h_div_setb	RW	0x1	XO / Input Buffer High Frequency Divider Set When cleared, the XO/IB high frequency divider is held in set mode (bit is active low). Unless this divider is bypassed (xo_ib_h_div = 0), clearing this bit will halt the refin_div clock.
28:24	xo_ib_h_div	RW	0x0	XO / Input Buffer high frequency divide ratio Divide by 2 to 31. Bypass if set to 0. 1 is reserved.
23:22	en_gain	RW	0x1	XO gain boosting control. Selects the number of gain boosting amplifiers enabled during startup. ▪ 0x0 = Gain boosting amplifiers are disabled ▪ 0x1 = One parallel amplifier is enabled ▪ 0x2 = Two parallel amplifiers are enabled ▪ 0x3 = All three parallel amplifiers are enabled
21:16	en_cap_x2	RW	0x28	XO capacitance at X2 terminal. Controls the internal tuning capacitance applied at the XOUT_REFINb terminalintegrated crystal. The capacitance rises monotonically in steps of 0.375pF from 0pF to 24pF as the control setting increases from 0x00 to the maximum of 0x3F. This must be set to 0 when sel_ib_xo is set to 0.
15	reserved	RO	0x0	Reserved.
14	xo_buff_dis	RW	0x0	XO buffer disable. Forces the XO buffer to the core logic to be disabled. This setting is intended for debug purposes only. ▪ 0x0 = XO buffer enable is controlled by the hardware. It is enabled during the startup sequence and remains enabled until the device is power cycled. ▪ 0x1 = XO buffer is disabled
13:8	en_cap_x1	RW	0x28	XO capacitance at X1 terminal. Controls the internal tuning capacitance applied at the XIN_REFIN terminal integrated crystal. The capacitance rises monotonically in steps of 0.375pF from 0pF to 24pF as the control setting increases from 0x00 to the maximum of 0x3F. This must be set to 0 when sel_ib_xo is set to 0.
7	reserved	RO	0x0	Reserved.
6:4	xo_res	RW	0x4	XO Resistor Configuration. Series resistance array control for limiting driving power level.

Table 51. XO_CNFG - Crystal Configuration (Cont.)

Bit Field	Field Name	Type	Default Value	Description
3	xo_ib_en_dc_bias	RW	0x0	Input Buffer internal DC bias enable. When the input buffer clock input signal is AC-coupled external to the device, the internal DC bias voltage must be enabled. ▪ 0x0 = Internal DC bias is disabled (input signal is DC-coupled) ▪ 0x1 = Internal DC bias is enabled (input signal is AC-coupled)
2	sel_ib_xo	RW	0x1	XO / Input Buffer select. Selects the mode of the XO / Input Buffer. ▪ 0x0 = Input buffer ▪ 0x1 = XO
1	xo_ib_cmos_sel	RW	0x0	Input Buffer CMOS / differential select. Configures the input buffer for single-ended CMOS or differential input signal. ▪ 0x0 = Differential input is selected ▪ 0x1 = CMOS input is selected
0	xo_ib_p_n_diff_sel	RW	0x1	Input Buffer PMOS / NMOS select. Configures the input buffer according to the common mode voltage of the provided input signal. ▪ 0x0 = PMOS input pair is enabled (low common mode voltage) ▪ 0x1 = NMOS input pair is enabled (higher common mode voltage)

4.4 CLKIN Register

Table 52. CLKIN_CNFG - Clock Input Pad Configuration

Bit Field	Field Name	Type	Default Value	Description
15	h_div_setb	RW	0x1	Reference Clock High Frequency Divider Set When cleared, the corresponding reference clock high-frequency divider is held in set mode (bit is active low). Unless this divider is bypassed (h_div = 0), clearing this bit will halt the clkin0_div/clkin2_div clock.
14:10	h_div	RW	0x0	Reference clock high frequency divide ratio Divide by 2 to 31. Bypass if set to 0. 1 is reserved.
9	trim_term	RW	0x0	Reference Clock Input Pad termination trim. Selects the HCSL and LVDS termination resistance to ground / across the inputs for modes to: ▪ 0x0 = 50Ω / 100Ω ▪ 0x1 = 42.5Ω / 85Ω
8	en_lvpecl	RW	0x0	Reference Clock Input Pad LVPECL termination enable. Enables compatible termination when the reference clock input signal is LVPECL. ▪ 0x0 = LVPECL input termination is disabled ▪ 0x1 = LVPECL input termination is enabled
7	en_lvds	RW	0x0	Reference Clock Input Pad LVDS termination enable. Enables compatible termination when the reference clock input signal is LVDS. ▪ 0x0 = LVDS input termination is disabled ▪ 0x1 = LVDS input termination is enabled

Table 52. CLKIN_CNFG - Clock Input Pad Configuration (Cont.)

Bit Field	Field Name	Type	Default Value	Description
6	en_hcsl	RW	0x0	Reference Clock Input Pad HCSL termination enable. Enables compatible termination when the reference clock input signal is HCSL. ▪ 0x0 = HCSL input termination is disabled ▪ 0x1 = HCSL input termination is enabled
5	en_cml	RW	0x0	Reference Clock Input Pad CML termination enable. Enables compatible termination when the reference clock input signal is CML. ▪ 0x0 = CML input termination is disabled ▪ 0x1 = CML input termination is enabled
4	en_dc_bias	RW	0x0	Reference Clock Input Pad internal DC bias enable. When the reference clock input signal is AC-coupled external to the device, the internal DC bias voltage must be enabled. ▪ 0x0 = Internal DC bias is disabled (input signal is DC-coupled) ▪ 0x1 = Internal DC bias is enabled (input signal is AC-coupled)
3	en_inbuff	RW	0x0	Reference Clock Input Pad enable. The reference clock input pad must be enabled to allow the clock to be used by the device, and should be left disabled if unused. To fully power down the input pad, en_inbuff, en_dc_bias, en_cml, en_hcsl, en_lvds, and en_lvpecl all must be set to 0. ▪ 0x0 = Input pad is disabled ▪ 0x1 = Input pad is enabled
2:1	cmos_sel	RW	0x0	Reference Clock Input Pad CMOS / differential select. Configures the reference clock input pad for two single-ended CMOS or differential input signal. ▪ 0x0 = Differential input is selected ▪ 0x1 = Single CMOS input is selected on positive pin ▪ 0x2 = Single CMOS input is selected on negative pin ▪ 0x3 = Dual CMOS inputs are selected
0	p_n_diff_sel	RW	0x1	Reference Clock Input Pad PMOS / NMOS select. Configures the reference clock input pad according to the common mode voltage of the provided input signal. ▪ 0x0 = PMOS input pair is enabled (low common mode voltage) ▪ 0x1 = NMOS input pair is enabled (higher common mode voltage)

4.5 LOSMON Registers

Note that before reprogramming a Loss of Signal Monitor, the corresponding clkmon0_sw_rst, clkmon1_sw_rst, clkmon2_sw_rst, clkmon3_sw_rst or clkmon4_sw_rst bit should be set. Once programming is done, it should then be cleared.

Table 53. LOSMON_WINDOW - LOS Monitor Window Configuration

Bit Field	Field Name	Type	Default Value	Description
15:12	reserved	RO	0x0	Reserved.
11:8	los_cnt_thresh	RW	0x0	Loss-of-Signal Counter Threshold. While the Loss-of-Signal counter (los_cnt) exceeds this threshold, the los_lmt_evt bit is set.
7	reserved	RO	0x0	Reserved.

Table 53. LOSMON_WINDOW - LOS Monitor Window Configuration (Cont.)

Bit Field	Field Name	Type	Default Value	Description
6	ref_disable	RW	0x0	Reference Clock Selection Disable Controls whether this reference clock can be selected as the DPLL reference clock. Not applicable for LOSMON4 (XO/IB monitor). ▪ 0x0 = Reference clock can be selected, subject to qualification by the Loss-of-Signal and Frequency monitors, and prioritization according to ref_priority ▪ 0x1 = Reference clock cannot be selected, ref_invalid set to 1
5	los_fail_mask	RW	0x0	LOS Monitor Failure Mask Masks the LOS monitor status contribution to ref_invalid. ▪ 0x0 = los_sts contributes to ref_invalid ▪ 0x1 = los_sts does not contribute to ref_invalid
4:0	los_div_ratio	RW	0x0	LOS Monitor Divide Ratio This divide ratio must be set such that the monitored clock nominal frequency divided by los_div_ratio is less than 1/8 of the measuring clock frequency (see losmon_clksel) to achieve 25% accuracy. One period of the divided clock is the monitoring window duration. A value of 0 or 1 means divide by 1.

Table 54. LOSMON_NOMINAL - LOS Monitor Nominal Number Configuration

Bit Field	Field Name	Type	Default Value	Description
15:0	los_nom_num	RW	0x0	LOS Monitor Nominal Cycle Count Sets the expected number of measuring clock periods (see losmon_clksel) within one monitor window. Set to 0x0 to disable the LOS monitor. Disabling the monitor will cause the los_sts bit to be asserted, therefore the los_fail_mask bit should also be set when this field is written to 0x0.

Table 55. LOSMON_THRESH - LOS Monitor Threshold Configuration

Bit Field	Field Name	Type	Default Value	Description
31	reserved	RO	0x0	Reserved.
30:16	los_acc_margin	RW	0x0	LOS Monitor Accept Threshold An accepted clock monitoring window occurs when the final monitor counter value is within los_nom_num ± los_acc_margin.
15	reserved	RO	0x0	Reserved.
14:0	los_rej_margin	RW	0x0	LOS Monitor Reject Threshold A rejected clock monitoring window occurs when the final monitor counter value is outside of los_nom_num ± los_rej_margin.

Table 56. LOSMON_QUAL - LOS Monitor Qualify Counter Configuration

Bit Field	Field Name	Type	Default Value	Description
7:4	los_good_times	RW	0x4	LOS Monitor Qualification Count If this number of consecutive accepted clock LOS monitoring windows occur without a rejected window, then the clock is qualified and los_sts is set to 0. A value of 0 is reserved.
3:0	los_fail_times	RW	0x4	LOS Monitor Disqualification Count If this number of rejected clock LOS monitoring windows occur without qualifying the clock, then the clock is disqualified and los_sts is set to 1. A value of 0 is reserved.

Table 57. LOSMON_STS - LOS Monitor Status

Bit Field	Field Name	Type	Default Value	Description
7:2	reserved	RO	0x0	Reserved.
1	ref_invalid	RO	0x1	Reference Clock Invalid status. Indicates whether this reference clock is currently considered to be invalid. This occurs if the clock is disqualified by one or more of the Loss-of-Signal and Frequency monitors, or ref_disable is set to 1. ▪ 0x0 = Clock is valid ▪ 0x1 = Clock is invalid
0	los_sts	RO	0x1	Loss-of-Signal status. Current value of the LOS status from the clock monitor: ▪ 0x0 = Clock meets the monitoring criteria ▪ 0x1 = Loss-of-signal detected

Table 58. LOSMON_EVENT - LOS Monitor Event Status

Bit Field	Field Name	Type	Default Value	Description
7:2	reserved	RO	0x0	Reserved.
1	los_lmt_evt	RW1C	0x0	Loss-of-Signal Counter Threshold Exceeded status. Set while the Loss-of-Signal counter (los_cnt) exceeds the threshold set in los_cnt_thresh. This bit cannot be cleared by software while the condition persists. ▪ 0x0 = Loss-of-signal counter has not exceeded the threshold since the last time the bit was cleared ▪ 0x1 = Loss-of-signal counter exceeded the threshold since the last time the bit was cleared
0	los_evt	RW1C	0x1	Loss-of-Signal Event status. Set while the clock monitor asserts LOS. This bit cannot be cleared by software while the LOS condition persists. This bit is set when the block comes out of reset and needs to be cleared after proper programming. ▪ 0x0 = Loss-of-signal not detected since the last time the bit was cleared ▪ 0x1 = Loss-of-signal detected since the last time the bit was cleared

Table 59. LOSMON_CNT - LOS Monitor Count

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	Reserved.
3:0	los_cnt	RW	0x0	Loss-of-Signal Failure Counter This counter increments each time the clock monitor asserts LOS and saturates at 0xF. It is cleared by writing 0x0 to it, and can be preset by writing the desired value. Preset can be used either as a debug tool or to cause a threshold alarm to happen sooner. This register can only be written if the block is not clock gated (clkmon0_cg:clkmon4_cg) or held in reset (clkmon0_sw_rst:clkmon4_sw_rst).

4.6 APLL Registers

Table 60. APLL_FB_DIV_FRAC - APLL Feedback Divider Fraction Configuration

Bit Field	Field Name	Type	Default Value	Description
31:27	reserved	RO	0x0	Reserved.
26:0	apll_fb_div_frac	RW	0x0	APLL Feedback Divider Fraction. APLL feedback divider numerator value. The denominator is a fixed value of 2^27.

Table 61. APLL_FB_DIV_INT - APLL Feedback Divider Integer Configuration

Bit Field	Field Name	Type	Default Value	Description
15:10	reserved	RO	0x0	Reserved.
9:0	apll_fb_div_int	RW	0x69	APLL Feedback Divider Integer. APLL feedback divider integer value.

Table 62. APLL_FB_SDM_CNFG - APLL Feedback SDM Configuration

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	Reserved.
5	apll_fb_dither_en	RW	0x0	APLL Feedback SDM Dither Enable. Dither enable for the SDM controlling the APLL feedback divider. After device startup, should only be changed while filter_update_dis is set to 1. ▪ 0x0 = dither disabled ▪ 0x1 = dither enabled
4	apll_fb_dither_ns	RW	0x0	APLL Feedback SDM Dither Noise shaping. Dither noise shaping enable for the SDM controlling the APLL feedback divider. After device startup, should only be changed while filter_update_dis is set to 1. ▪ 0x0 = dither not shaped ▪ 0x1 = dither shaped

Table 62. APLL_FB_SDM_CNFG - APLL Feedback SDM Configuration

Bit Field	Field Name	Type	Default Value	Description
3:2	apll_fb_dither_gain	RW	0x0	APLL Feedback SDM Dither Gain. Gain control for the SDM controlling the APLL feedback divider. After device startup, should only be changed while filter_update_dis is set to 1. ▪ 0x0 = LSB ▪ 0x1 = 2*LSB ▪ 0x2 = 4*LSB ▪ 0x3 = 8*LSB
1:0	apll_fb_sdm_order	RW	0x3	APLL Feedback SDM Order. Selects the order of the SDM controlling the feedback divider for the APLL. When the feedback divide ratio is fractional, or to allow xtal_trim or write_freq to operate correctly, the order must be set greater than 0. After device startup, should only be changed while filter_update_dis is set to 1. ▪ 0x0 = Integer ▪ 0x1 = 1st order ▪ 0x2 = 2nd order ▪ 0x3 = 3rd order

Table 63. APLL_CNFG - APLL Configuration

Bit Field	Field Name	Type	Default Value	Description
7	apll_dis	RW	0x0	APLL disable. Forces the sub-blocks of the APLL to be disabled. This setting is intended for debug purposes only. ▪ 0x0 = APLL enable is controlled by the hardware. It is enabled during the startup sequence and remains enabled until the device is power cycled. ▪ 0x1 = APLL is disabled
6	reserved	RO	0x0	Reserved.
5	cp_dis	RW	0x0	Charge pump disable. Forces the APLL charge pump to be disabled. This setting is intended for debug purposes only. ▪ 0x0 = Charge pump enable is controlled by the hardware. It is enabled during the startup sequence and remains enabled until the device is power cycled. ▪ 0x1 = Charge pump is disabled
4	vco_dis	RW	0x0	VCO disable. Forces the VCO to be disabled. This setting is intended for debug purposes only. ▪ 0x0 = VCO enable is controlled by the hardware. It is enabled during the startup sequence and remains enabled until the device is power cycled. ▪ 0x1 = VCO is disabled
3:2	reserved	RO	0x0	Reserved.

Table 63. APLL_CNFG - APLL Configuration (Cont.)

Bit Field	Field Name	Type	Default Value	Description
1	doubler_sel	RW	0x0	Frequency doubler select. Selects the frequency doubler to use when en_doubler is set to 1. ▪ 0x0 = PLL frequency doubler ▪ 0x1 = PFD frequency doubler
0	en_doubler	RW	0x1	Frequency doubler enable. Enables the frequency doubler selected by the doubler_sel bit. ▪ 0x0 = disable ▪ 0x1 = enable

Table 64. CP_CNFG - APLL Charge Pump Configuration

Bit Field	Field Name	Type	Default Value	Description
15:14	reserved	RO	0x0	Reserved.
13	cp_offset_en	RW	0x0	Charge Pump offset current enable. Enables the charge pump offset current. The magnitude of the current is selected by cnf_cp_offset. ▪ 0x0 = disabled ▪ 0x1 = enabled
12	cp_offset_boost	RW	0x0	Charge Pump offset current boost. Increases the magnitude of the offset current. ▪ 0x0 = charge pump offset range from 0uA to 145uA ▪ 0x1 = charge pump offset range from 0uA to 236uA
11:8	cnf_cp_offset	RW	0x3	Charge Pump offset current setting. Controls the charge pump offset current when enabled by cp_offset_en. When cp_offset_boost is set to 0 / 1, the charge pump current is: ▪ 0x0 = 0uA / 0uA ▪ 0x1 = 10.3uA / 99.7uA ▪ 0x2 = 20.5uA / 118.7uA ▪ 0x3 = 30.6uA / 128.1uA ▪ 0x4 = 40.7uA / 137.5uA ▪ 0x5 = 50.5uA / 146.7uA ▪ 0x6 = 60.3uA / 155.9uA ▪ 0x7 = 70.0uA / 165.1uA ▪ 0x8: 79.7uA / 174.2uA ▪ 0x9 = 89.2uA / 183.2uA ▪ 0xA = 98.7uA / 192.2uA ▪ 0xB = 108.1uA / 201.2uA ▪ 0xC = 117.5uA / 210.0uA ▪ 0xD = 126.7uA / 218.9uA ▪ 0xE = 135.9uA / 227.7uA ▪ 0xF = 145.0uA / 236.0uA
7	reserved	RO	0x0	Reserved.

Table 64. CP_CNFG - APLL Charge Pump Configuration (Cont.)

Bit Field	Field Name	Type	Default Value	Description
6:4	cnf_cp_up	RW	0x3	Charge Pump up current setting. ▪ 0x0 = 250uA ▪ 0x1 = 500uA ▪ 0x2 = 750uA ▪ 0x3 = 1mA ▪ 0x4 = 1.25mA ▪ 0x5 = 1.5mA ▪ 0x6 = 1.75mA ▪ 0x7 = 2mA
3	reserved	RO	0x0	Reserved.
2:0	cnf_cp_dn	RW	0x3	Charge Pump down current setting. ▪ 0x0 = 250uA ▪ 0x1 = 500uA ▪ 0x2 = 750uA ▪ 0x3 = 1mA ▪ 0x4 = 1.25mA ▪ 0x5 = 1.5mA ▪ 0x6 = 1.75mA ▪ 0x7 = 2mA

Table 65. LPF_CNFG - APLL Loop Filter Configuration

Bit Field	Field Name	Type	Default Value	Description
7	apll_vco_filter_byp	RW	0x0	VCO current source filter bypass. ▪ 0x0 = filter active ▪ 0x1 = filter bypassed

Table 65. LPF_CNFG - APLL Loop Filter Configuration

Bit Field	Field Name	Type	Default Value	Description
6:4	cnf_LPF_cp	RW	0x7	Loop filter pole capacitor setting. ▪ 0x0 = 11pF ▪ 0x1 = 14.7pF ▪ 0x2 = 18.4pF ▪ 0x3 = 22.1pF ▪ 0x4 = 25.8pF ▪ 0x5 = 29.5pF ▪ 0x6 = 33.2pF ▪ 0x7 = 36.9pF
3:0	cnf_LPF_res	RW	0x4	Loop filter resistor setting. ▪ 0x0 = 0Ω ▪ 0x1 = 400Ω ▪ 0x2 = 800Ω ▪ 0x3 = 1.2kΩ ▪ 0x4 = 1.6kΩ ▪ 0x5 = 2kΩ ▪ 0x6 = 2.4kΩ ▪ 0x7 = 2.8kΩ ▪ 0x8: 3.2kΩ ▪ 0x9 = 3.6kΩ ▪ 0xA = 4kΩ ▪ 0xB = 4.4kΩ ▪ 0xC = 4.8kΩ ▪ 0xD = 5.2kΩ ▪ 0xE = 5.6kΩ ▪ 0xF = 6kΩ

Table 66. LPF_3RD_CNFG - APLL Loop Filter 3rd Pole Configuration

Bit Field	Field Name	Type	Default Value	Description
7	byp_p3	RW	0x0	Bypass 3rd pole. This bit can only be set to 1 when operating with an integer feedback divider. ▪ 0x0 = 3rd pole active ▪ 0x1 = 3rd pole bypassed
6:4	cnf_LPF_R3	RW	0x4	Loop filter 3rd pole resistor setting. ▪ 0x0 = 0Ω ▪ 0x1 = 800Ω ▪ 0x2 = 1.6kΩ ▪ 0x3 = 2.4kΩ ▪ 0x4 = 3.2kΩ ▪ 0x5 = 4kΩ ▪ 0x6 = 4.8kΩ ▪ 0x7 = 5.6kΩ

Table 66. LPF_3RD_CNFG - APLL Loop Filter 3rd Pole Configuration

Bit Field	Field Name	Type	Default Value	Description
3	reserved	RO	0x0	Reserved.
2:0	cnf_LPF_C3	RW	0x4	Loop filter 3rd pole capacitor setting. ▪ 0x0 = 0pF ▪ 0x1 = 1pF ▪ 0x2 = 2pF ▪ 0x3 = 3pF ▪ 0x4 = 4pF ▪ 0x5 = 5pF ▪ 0x6 = 6pF ▪ 0x7 = 7pF

Table 67. BANK_MUX_CLK_EN - Bank Mux Clock Enable

Bit Field	Field Name	Type	Default Value	Description
31	en_refin_omux	RW	0x1	XO/IB Clock to Bank 5 Output Mux Enable. Enables fanout of the XO/IB clock to Bank 5 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled
30	en_clkin2_bnk6	RW	0x1	Reference Clock 2 to Bank 6 Output Mux Enable. Enables fanout of reference clock 2 (CLKIN1) to Bank 6 output mux. When bank 6 is in automatic fanout buffer mode and bank_fanout_mode is set to 2, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
29	en_clkin2_bnk5	RW	0x1	Reference Clock 2 to Bank 5 Output Mux Enable. Enables fanout of reference clock 2 (CLKIN1) to Bank 5 output mux. When bank 5 is in automatic fanout buffer mode and bank_fanout_mode is set to 2, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
28	en_clkin2_bnk4	RW	0x1	Reference Clock 2 to Bank 4 Output Mux Enable. Enables fanout of reference clock 2 (CLKIN1) to Bank 4 output mux. When bank 4 is in automatic fanout buffer mode and bank_fanout_mode is set to 2, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
27	en_clkin0_bnk6	RW	0x1	Reference Clock 0 to Bank 6 Output Mux Enable. Enables fanout of reference clock 0 (CLKIN0) to Bank 6 output mux. When bank 6 is in automatic fanout buffer mode and bank_fanout_mode is set to 1, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled

Table 67. BANK_MUX_CLK_EN - Bank Mux Clock Enable (Cont.)

Bit Field	Field Name	Type	Default Value	Description
26	en_clkin0_bnk5	RW	0x1	Reference Clock 0 to Bank 5 Output Mux Enable. Enables fanout of reference clock 0 (CLKIN0) to Bank 5 output mux. When bank 5 is in automatic fanout buffer mode and bank_fanout_mode is set to 1, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
25	en_clkin0_bnk4	RW	0x1	Reference Clock 0 to Bank 4 Output Mux Enable. Enables fanout of reference clock 0 (CLKIN0) to Bank 4 output mux. When bank 4 is in automatic fanout buffer mode and bank_fanout_mode is set to 1, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
24	en_fod2_bnk6	RW	0x1	FOD 2 to Bank 6 Output Mux Enable. Enables fanout of FOD 2 output clock to Bank 6 output mux. When bank 6 is in automatic fanout buffer mode and output_bank_src is set to 6, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
23	en_fod2_bnk5	RW	0x1	FOD 2 to Bank 5 Output Mux Enable. Enables fanout of FOD 2 output clock to Bank 5 output mux. When bank 4 is in automatic fanout buffer mode and output_bank_src is set to 6, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
22	en_fod2_bnk4	RW	0x1	FOD 2 to Bank 4 Output Mux Enable. Enables fanout of FOD 2 output clock to Bank 4 output mux. When bank 4 is in automatic fanout buffer mode and output_bank_src is set to 6, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
21	en_fod2_bnk3	RW	0x1	FOD 2 to Bank 3 Output Mux Enable. Enables fanout of FOD 2 output clock to Bank 3 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled
20	en_fod1_bnk6	RW	0x1	FOD 1 to Bank 6 Output Mux Enable. Enables fanout of FOD 1 output clock to Bank 6 output mux. When bank 6 is in automatic fanout buffer mode and output_bank_src is set to 5, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled

Table 67. BANK_MUX_CLK_EN - Bank Mux Clock Enable (Cont.)

Bit Field	Field Name	Type	Default Value	Description
19	en_fod1_bnk5	RW	0x1	FOD 1 to Bank 5 Output Mux Enable. Enables fanout of FOD 1 output clock to Bank 5 output mux. When bank 5 is in automatic fanout buffer mode and output_bank_src is set to 5, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
18	en_fod1_bnk4	RW	0x1	FOD 1 to Bank 4 Output Mux Enable. Enables fanout of FOD 1 output clock to Bank 4 output mux. When bank 4 is in automatic fanout buffer mode and output_bank_src is set to 5, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
17	en_fod1_bnk3	RW	0x1	FOD 1 to Bank 3 Output Mux Enable. Enables fanout of FOD 1 output clock to Bank 3 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled
16	en_fod1_bnk2	RW	0x1	FOD 1 to Bank 2 Output Mux Enable. Enables fanout of FOD 1 output clock to Bank 2 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled
15	en_fod1_bnk1	RW	0x1	FOD 1 to Bank 1 Output Mux Enable. Enables fanout of FOD 1 output clock to Bank 1 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled
14	en_fod1_bnk0	RW	0x1	FOD 1 to Bank 0 Output Mux Enable. Enables fanout of FOD 1 output clock to Bank 0 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled
13	en_fod0_bnk3	RW	0x1	FOD 0 to Bank 3 Output Mux Enable. Enables fanout of FOD 0 output clock to Bank 3 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled
12	en_fod0_bnk2	RW	0x1	FOD 0 to Bank 2 Output Mux Enable. Enables fanout of FOD 0 output clock to Bank 2 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled
11	en_fod0_bnk1	RW	0x1	FOD 0 to Bank 1 Output Mux Enable. Enables fanout of FOD 0 output clock to Bank 1 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled
10	en_fod0_bnk0	RW	0x1	FOD 0 to Bank 0 Output Mux Enable. Enables fanout of FOD 0 output clock to Bank 0 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled

Table 67. BANK_MUX_CLK_EN - Bank Mux Clock Enable (Cont.)

Bit Field	Field Name	Type	Default Value	Description
9	en_iod3_bnk6	RW	0x1	IOD 3 to Bank 6 Output Mux Enable. Enables fanout of IOD 3 output clock to Bank 6 output mux. When bank 6 is in automatic fanout buffer mode and output_bank_src is set to 3, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
8	en_iod3_bnk5	RW	0x1	IOD 3 to Bank 5 Output Mux Enable. Enables fanout of IOD 3 output clock to Bank 5 output mux. When bank 5 is in automatic fanout buffer mode and output_bank_src is set to 3, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
7	en_iod2_bnk6	RW	0x1	IOD 2 to Bank 6 Output Mux Enable. Enables fanout of IOD 2 output clock to Bank 6 output mux. When bank 6 is in automatic fanout buffer mode and output_bank_src is set to 2, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
6	en_iod2_bnk5	RW	0x1	IOD 2 to Bank 5 Output Mux Enable. Enables fanout of IOD 2 output clock to Bank 5 output mux. When bank 5 is in automatic fanout buffer mode and output_bank_src is set to 2, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
5	en_iod2_bnk4	RW	0x1	IOD 2 to Bank 4 Output Mux Enable. Enables fanout of IOD 2 output clock to Bank 4 output mux. When bank 4 is in automatic fanout buffer mode and output_bank_src is set to 2, this bit is automatically controlled according to the output mux selection and cannot be written. ▪ 0x0 = disabled ▪ 0x1 = enabled
4	en_iod1_bnk2	RW	0x1	IOD 1 to Bank 2 Output Mux Enable. Enables fanout of IOD 1 output clock to Bank 2 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled
3	en_iod1_bnk1	RW	0x1	IOD 1 to Bank 1 Output Mux Enable. Enables fanout of IOD 1 output clock to Bank 1 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled
2	en_iod1_bnk0	RW	0x1	IOD 1 to Bank 0 Output Mux Enable. Enables fanout of IOD 1 output clock to Bank 0 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled

Table 67. BANK_MUX_CLK_EN - Bank Mux Clock Enable (Cont.)

Bit Field	Field Name	Type	Default Value	Description
1	en_iod0_bnk1	RW	0x1	IOD 0 to Bank 1 Output Mux Enable. Enables fanout of IOD 0 output clock to Bank 1 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled
0	en_iod0_bnk0	RW	0x1	IOD 0 to Bank 0 Output Mux Enable. Enables fanout of IOD 0 output clock to Bank 0 output mux. ▪ 0x0 = disabled ▪ 0x1 = enabled

Table 68. APLL_STS - APLL Status

Bit Field	Field Name	Type	Default Value	Description
7:1	reserved	RO	0x0	Reserved.
0	apll_lock_sts	RO	0x0	APLL lock status. Set to 1 when the APLL is locked to its reference. ▪ 0x0 = unlocked ▪ 0x1 = locked

4.7 IOD Registers

Table 69. IOD_INT_CNFG - IOD Integer Ratio Configuration

Bit Field	Field Name	Type	Default Value	Description
31	iod_pd	RW	0x0	Integer Output Divider Power Down Powers down the integer output divider by turning off the regulator. If this bit is set to 1, iod_rst must also be set to 1. When clearing this bit, iod_rst must remain set and then it can be cleared afterwards. ▪ 0x0 = divider is powered up ▪ 0x1 = divider is powered down
30	iod_dis	RW	0x0	Integer Output Divider Disable Disables the integer output divider. If this bit is set to 1, iod_rst must also be set to 1. When clearing this bit, iod_rst must remain set and then it can be cleared afterwards. ▪ 0x0 = divider enabled ▪ 0x1 = divider disabled
29	iod_rst	RW	0x0	Integer Output Divider Reset Resets the integer output divider. ▪ 0x0 = divider reset de-asserted ▪ 0x1 = divider reset asserted
28	iod_squelch	RW	0x0	Integer Output Divider Squelch Synchronously squelches and releases the IOD output clock. ▪ 0x0 = IOD output is not squelched ▪ 0x1 = IOD output is squelched

Table 69. IOD_INT_CNFG - IOD Integer Ratio Configuration (Cont.)

Bit Field	Field Name	Type	Default Value	Description
27:25	reserved	RO	0x0	Reserved.
24:0	iod_int	RW	0x64	Integer Output Divider Ratio Integer output divider ratio. The minimum value is 14. This register is atomic. When the most significant byte (bit [24]) is written, the new value is applied to the IOD.

Table 70. IOD_PHASE_CNFG - IOD Phase Configuration

Bit Field	Field Name	Type	Default Value	Description
15	iod_ph_adj_now	RW1S	0x0	Integer Output Divider Phase Adjustment Now When this bit is written from 0 to 1, the phase adjustment in iod_phase is applied to the divider. This bit self-clears when the adjust completes.
14	iod_ph_adj_post_sync	RW	0x0	Integer Output Divider Phase Adjustment After Synchronization When this bit is set to 1, the phase adjustment in iod_phase is applied to the divider whenever the divider is synchronized.
13:11	reserved	RO	0x0	Reserved.
10:9	iod_sync_group	RW	0x0	Integer Output Divider Sync Group Sets the sync group that this divider belongs to ▪ 0x0 = group0 ▪ 0x1 = group1 ▪ 0x2 = none ▪ 0x3 = none
8:0	iod_phase	RW	0x0	Integer Output Divider Phase Configuration Signed 2's complementary value sets the phase, a positive value means lag from 0 phase, a negative value means lead from 0 phase, in steps of one VCO period. The available range is ± 0~255 steps (approximately ± 0~20ns). In SYSREF mode (sysref_mode is set to 1), the range is also limited to ± (iod_int/2 - 5) steps. This register is atomic. When the most significant byte (bit [8]) is written, the new value is applied to the IOD according to iod_ph_adj_now and iod_ph_adj_post_sync.

4.8 FOD Registers

Table 71. FOD_INT_CNFG - FOD Integer Configuration

Bit Field	Field Name	Type	Default Value	Description
63	fod_pd	RW	0x0	Fractional Output Divider Power Down Powers down the fractional output divider by turning off the regulator. If this bit is set to 1, fod_rst must also be set to 1. When clearing this bit, fod_rst must remain set and then it can be cleared afterwards. ▪ 0x0 = divider is powered up ▪ 0x1 = divider is powered down
62	fod_dis	RW	0x0	Fractional Output Divider Disable Disables the fractional output divider. If this bit is set to 1, fod_rst must also be set to 1. When clearing this bit, fod_rst must remain set and then it can be cleared afterwards. ▪ 0x0 = divider enabled ▪ 0x1 = divider disabled
61	fod_rst	RW	0x0	Fractional Output Divider Reset Resets the fractional output divider. ▪ 0x0 = divider reset de-asserted ▪ 0x1 = divider reset asserted
60	fod_acc_reset	RW	0x0	Fractional Output Divider Accumulator Reset Resets the FOD SDM accumulator. ▪ 0x0 = accumulator reset de-asserted ▪ 0x1 = accumulator reset asserted

Table 71. FOD_INT_CNFG - FOD Integer Configuration (Cont.)

Bit Field	Field Name	Type	Default Value	Description
59:26	fod_frac	RW	0x0	Fractional Output Divider Ratio Fraction portion Denominator is fixed to 2^34. This register field is part of an atomic group consisting of fod_1st_int and fod_frac. When the most significant byte (bits [33:30]) of fod_frac is written, the value of all these fields are applied to the FOD. *Note*: When an FOD has spread-spectrum and/or over-clocking enabled, fod_frac[5:0] *must* be set to 0x0. The fractional settings related to over-clocking (oc_target_frac, oc_hrdrst_frac) and all hard and soft reset scenarios only affect fod_frac[33:6] (the upper 28 bits). To ramp smoothly from the current divide ratio to a new divide ratio, program oc_target_int and oc_target_frac instead of fod_1st_int and fod_frac. The device will update fod_1st_int and fod_frac after the transition completes, as described below. When over-clocking is enabled (oc_en is set to 1), fod_1st_int and fod_frac for the FOD selected by oc_fod_sel can be updated automatically by the device as follows: ▪ In SFT mode, when a ramp completes, fod_1st_int/fod_frac latch the final divide ratio. ▪ In Target mode, when a ramp to the target divide ratio completes, latch the final divide ratio (i.e., the target divide ratio). ▪ If SFTRST# is triggered by the watchdog timer or sftrst_req, the over-clocking operation is halted and fod_1st_int/fod_frac latch the current divide ratio. ▪ If HRDRST# is triggered and revert_mode is set to 0, then fod_1st_int/fod_frac revert to the divide ratio before the last over-clocking operation started and are immediately applied to the FOD. If no over-clocking operation has occurred since oc_en was set or oc_fod_sel changed value, then fod_1st_int/fod_frac hold their values. ▪ When over-clocking is enabled (oc_en is set to 1), fod_1st_int and fod_frac for *both* FOD0 and FOD1 can be updated automatically by the device as follows: ▪ If HRDRST# is triggered by the watchdog timer or hrdrst_req, and revert_mode is set to 1, then fod_1st_int/fod_frac are set to oc_hrdrst_int/oc_hrdrst_frac.
25:9	fod_2nd_int	RW	0x0	Fractional Output Divider Ratio 2nd Integer portion Half integer divide ratio of second stage. The actual divide ratio is (fod_2nd_int * 2). A setting of 1 is invalid: the minimum divide ratio is 4. Set to 0 to bypass the second stage.
8:0	fod_1st_int	RW	0x64	Fractional Output Divider Ratio 1st Integer portion Integer divide ratio of first stage (MMD). The first stage divides the VCO clock down to a range of 33MHz to 650MHz, giving a minimum divide ratio of 9.5GHz / 650MHz = 14.61 and maximum divide ratio of 10.7GHz / 33MHz = 324.25 If the first stage frequency is less than 70MHz, the fod_slow_freq_en bit must be set to 1. This register field is part of an atomic group consisting of fod_1st_int and fod_frac. When the most significant byte (bits [33:30]) of fod_frac is written, the value of all these fields are applied to the FOD. *Note*: Refer to fod_frac for details about serial bus writes to this register field and automatic updates performed by the over-clocking engine.

Table 72. FOD_PHASE_CNFG - FOD Phase Configuration

Bit Field	Field Name	Type	Default Value	Description
15	fod_ph_adj_now	RW1S	0x0	Fraction Output Divider Phase Adjustment Now When this bit is written from 0 to 1, the phase adjustment in fod_phase is applied to the divider. This bit self-clears when the adjust completes.
14	fod_ph_adj_post_sync	RW	0x1	Fraction Output Divider Phase Adjustment After Synchronization When this bit is set to 1, the phase adjustment in fod_phase is applied to the divider whenever the divider is synchronized.
13	fod_slow_freq_en	RW	0x0	FOD Slow Frequency enable Must be set to 1 when the MMD (first stage) frequency is under 70MHz.
12	reserved	RO	0x0	Reserved.
11:10	fod_sync_group	RW	0x0	Fraction Output Divider Sync Group Sets the sync group that this divider belongs to: ▪ 0x0 = group0 ▪ 0x1 = group1 ▪ 0x2 = none ▪ 0x3 = none
9:0	fod_phase	RW	0x3F0	Fraction Output Divider Phase Configuration Signed 2's complementary value sets the phase. A positive value means lag from 0 phase, and a negative value means lead from 0 phase, in steps of 1/4 VCO period. The default value of -16 (decimal), or -4.0 VCO periods, approximately aligns the FOD output clock with the IOD output clock, when the FOD is configured with an integer divide ratio. This register is atomic. When the most significant byte (bits [9:8]) is written, the new value is applied to the FOD according to fod_ph_adj_now and fod_ph_adj_post_sync.

4.9 SSC Register

Table 73. SSC_CNFG - Spectrum Spreading Configuration

Bit Field	Field Name	Type	Default Value	Description
31	ssc_en	RW	0x0	Spectrum Spreading Enable Enable spread spectrum. The spread configuration is determined by the other register fields in this register. ▪ 0x0 = SSC disabled ▪ 0x1 = SSC enabled If the FOD0 and FOD1 SSC modulation frequencies are the same, the FOD1 SSC phase can be aligned to FOD0 SSC by setting ssc_share to 1. *Note*: When ssc_share is set to 1, then FOD1 ssc_en must be set to 1 before FOD0 ssc_en is set to 1 since FOD1 SSC will start when FOD0 ssc_en is set to 1. This restriction does not apply when loading the device configuration from OTP/EEPROM on startup, but does apply if dynamically changing these settings later through a dynamic configuration load from the OTP/EEPROM, or by writing registers from the serial interface.
30	ssc_mode	RW	0x0	Spectrum Spreading Mode ▪ 0x0 = down spreading ▪ 0x1 = center spreading
29:24	reserved	RO	0x0	Reserved
23:16	ssc_ampl	RW	0x51	Spectrum Spreading Amplitude Sets the positive and negative spreading amplitude. For down spread, ssc_ampl is only used for the negative limit and the positive limit is internally set to 0. For center spread, the peak-to-peak spread amplitude is twice the specified amplitude (for a 1% peak-to-peak center spread, define ssc_ampl as 0.5%). ssc_ampl = spread_percentage / 100 * 2^14 For example, for 1% spread, set ssc_ampl to 0.01 * 2^14 = 163 decimal, or 0xA3. The default value corresponds to a 0.5% down spread at 31.5kHz.
15:0	ssc_step	RW	0x2B8C	Spectrum Spreading Step Size Set ramp step size to get the target modulation rate. For down spread: ▪ ssc_step = ssc_ampl * 2^16 * ssc_freq / 15MHz For center spread: ▪ ssc_step = 2 * ssc_ampl * 2^16 * ssc_freq / 15MHz where: ssc_freq is the target modulation rate from 30kHz to 63kHz 15MHz is the system clock divided by 4, assuming the system clock is 60MHz Example 1. For a 32kHz 1% down spread: ssc_ampl = 163 ssc_step = 163 * 2^16 * 32kHz / 15MHz = 0x5905 Example 2. For a 32kHz ± 0.5% center spread: ssc_ampl = 81 ssc_step = 2 * 81 * 2^16 * 32kHz / 15MHz = 0x5879 The default value corresponds to a 0.5% down spread at 31.5kHz.

4.10 BANK Register

Table 74. OUT_BANK_CNFG - Output Bank Configuration

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	Reserved.
5	bank_pd	RW	0x0	Output Bank Power Down Powers down the output bank by turning off the regulator. When a bank is powered down, all output driver(s) in that bank should also be powered down by setting their out_pd bit(s) to 1. ▪ 0x0 = bank is powered up ▪ 0x1 = bank is powered down
4:3	bank_fanout_mode	RW	0x0	Output Bank Fan-out Buffer Mode Configures the bank selection for fanout buffer mode. Only available on banks 4, 5, and 6. The device must be configured for fanout buffer mode by fanout_buf_mode (CLKIN0) / fanout_buf_mode1 (CLKIN1) for this setting to take effect. ▪ 0x0 = Normal operation mode. The output bank source clock is selected by output_bank_src. ▪ 0x1 = CLKIN0 Fan-out buffer mode. When fanout_clkmode is 1, the output bank selects CLKIN0. When fanout_clkmode is 0, the output bank source clock is selected by output_bank_src. ▪ 0x2 = CLKIN1 Fan-out buffer mode. When fanout_clkmode1 is 1, the output bank selects CLKIN1. When fanout_clkmode1 is 0, the output bank source clock is selected by output_bank_src.
2:0	output_bank_src	RW	0x5	Output Bank Source Sets the clock source of each output bank, in conjunction with bank_fanout_mode. Some configurations can be reserved based on Output Bank Source Mapping table. The bits in BANK_MUX_CLK_EN - Bank Mux Clock Enable must be set appropriately to enable only the selected source for each bank. ▪ 0x0 = IOD0 for Banks 0, 1 / clkin2_div (CLKIN1) for Banks 4, 5, 6 ▪ 0x1 = IOD1 for Banks 0, 1, 2 / refin_div (XIN_REF) for Bank 5 ▪ 0x2 = IOD2 for Banks 4, 5, 6 ▪ 0x3 = IOD3 for Banks 5, 6 ▪ 0x4 = FOD0 for Banks 0, 1, 2, 3 ▪ 0x5 = FOD1 ▪ 0x6 = FOD2 for Banks 3, 4, 5, 6 ▪ 0x7 = clkin0_div (CLKIN0) for Banks 4, 5, 6

4.11 OUT Registers

Table 75. ODRV_EN - Output Driver Enable

Bit Field	Field Name	Type	Default Value	Description
7	out_pd	RW	0x0	Output Driver Power Down Powers down the output clock driver. ▪ 0x0 = output driver is powered up ▪ 0x1 = output driver is powered down
6	out_oe_mode	RW	0x0	Output Driver OE Mode Controls whether the output enable acts synchronously or asynchronously with respect to the output divider clock. Must be set to asynchronous mode when outputting SYSREF. ▪ 0x0 = OE is synchronized to the divider clock. Enabling and disabling the output clock is glitchless. OE transitions take effect after 1 divider clock cycle. ▪ 0x1 = OE is asynchronous to the divider clock. OE transitions while the divider clock is toggling can result in glitches/runt pulses.
5:3	out_dis_group	RW	0x0	Output Driver OE Group Select and Global Output Enable Exclusion Sets which OE group this driver is in, and if not assigned to a group, can also exclude global output enables from applying to the clock. ▪ 0x0 = group0 ▪ 0x1 = group1 ▪ 0x2 = group2 ▪ 0x3 = group3 ▪ 0x4 = group4 ▪ 0x5 = none ▪ 0x7 = none, and exclude global output enables When set to 0x7, allows the output clock to be enabled regardless of: ▪ APLL lock status (equivalent to out_startup set to 2) ▪ goe register bit ▪ GOE pin, if one is assigned with gpi_func/gpio_func The output clock can still be disabled by the out_dis register bit. This setting is intended to allow an output clock to run freely following the configuration load so that it can be used as an external APLL or DPLL feedback clock. In that application, if the output clock's divider is resynchronized after the startup sequence completes, the output clock will stop running for less than 1us and then the APLL or DPLL will re-align the feedback clock to the reference clock.
2:1	out_dis_state	RW	0x3	OUT Driver disabled state Controls the state of OUTx / OUTxb when the output driver is disabled. ▪ 0x0 = Held High / Low ▪ 0x1 = Held Low / High ▪ 0x2 = Held Hi-Z / Hi-Z ▪ 0x3 = Held Low / Low (except LVDS mode is held High / Low)
0	out_dis	RW	0x0	OUTx and/or OUTxb Driver disable Forces both OUTx and OUTxb Drivers to be disabled if in differential mode or force OUT Driver to be disabled if in CMOS mode. For more information, see Output Enable Control. ▪ 0x0 = OUTx and/or OUTxb Driver is enabled if not disabled by other means ▪ 0x1 = OUTx and/or OUTxb Driver is disabled

Table 76. ODRV_CNFG - Output Driver Configuration

Bit Field	Field Name	Type	Default Value	Description
15	out_prog7	RW	0x0	Output Driver Programmability Bit 7. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: reserved / flip output polarity / flip output polarity
14	out_prog6	RW	0x0	Output Driver Programmability Bit 6. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: reserved / reserved / reserved
13	out_prog5	RW	0x0	Output Driver Programmability Bit 5. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: reserved / cross point lower / cross point tune
12	out_prog4	RW	0x0	Output Driver Programmability Bit 4. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: reserved / cross point increase for double termination / cross point tune
11	out_prog3	RW	0x0	Output Driver Programmability Bit 3. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: tristate OUT*x* / driver impedance -5% / cross point tune
10	out_prog2	RW	0x0	Output Driver Programmability Bit 2. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: tristate OUT*x*b / driver impedance +5% / cross point tune
9	out_prog1	RW	0x0	Output Driver Programmability Bit 1. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: flip OUT*x* polarity / amplitude -10% / amplitude -10%
8	out_prog0	RW	0x0	Output Driver Programmability Bit 0. When set to 1, controls the output driver as follows according to CMOS mode / LPHCSL mode / LVDS mode: flip OUT*x*b polarity / amplitude +5% / amplitude +5%
7	reserved	RO	0x0	Reserved.
6	out_lpamp	RW	0x0	Output Driver LPHCSL amplitude control. Controls the amplitude of the output driver when LPHCSL mode is selected. ▪ 0x0 = 800mV ▪ 0x1 = 900mV
5	out_lpsr	RW	0x1	Output Driver LPHCSL slew rate control. Controls the slew rate of the output driver when LPHCSL mode is selected. Based on 5" transmission line simulation condition. Slew rates are measured from -150mV to +150mV from crossing point. ▪ 0x0 = slow, 2-4 V/ns ▪ 0x1 = fast, >4 V/ns

Table 76. ODRV_CNFG - Output Driver Configuration (Cont.)

Bit Field	Field Name	Type	Default Value	Description
4	out_lpimp	RW	0x1	Output Driver LPHCSL impedance control. Controls the output impedance of the output driver when LPHCSL mode is selected. ▪ 0x0 = 85Ω ▪ 0x1 = 100Ω
3:2	out_cmdrv	RW	0x3	Output Driver CMOS slew rate control. Controls the slew rate of the output driver (in V/ns) when CMOS mode is selected, according to the supply voltage level of 3.3V / 2.5V / 1.8V: ▪ 0x0 = 4.2 / 2.7 / 1.8 ▪ 0x1 = 2.7 / 1.5 / 1.8 ▪ 0x2 = 2.7 / 1.5 / 1.8 ▪ 0x3 = 3.4 / 2.0 / 1.9
1:0	out_mode	RW	0x0	Output Driver type. Selects the output driver type. ▪ 0x0 = LPHCSL ▪ 0x1 = LVDS ▪ 0x2 = LVDS ▪ 0x3 = CMOS

4.12 GPI Registers

Table 77. GPI_CNFG - GPI Configuration

Bit Field	Field Name	Type	Default Value	Description
15:10	reserved	RO	0x0	Reserved.
9	gpi_pol	RW	0x0	GPI Polarity Sets the pin polarity. This bit is ignored if gpi_func configures the pin as a reference clock input. ▪ 0x0 = Normal sense. Pin functions denoted with a # are active low, others are active high. ▪ 0x1 = Inverted sense. Pin functions denoted with a # are active high, others are active low.
8	gpi_pullup	RW	0x0	GPI Pull-up Enable Sets the internal pull-up mode. This bit is ignored and the internal pull-down is enabled if gpi_func configures the pin as a reference clock input. ▪ 0x0 = pull-up disabled ▪ 0x1 = pull-up enabled

Table 77. GPI_CNFG - GPI Configuration

Bit Field	Field Name	Type	Default Value	Description
7	gpi_pulldn	RW	0x0	GPI Pull-down Enable Sets the internal pull-up or pull-down modes. This bit is ignored and the internal pull-down is enabled if gpi_func configures the pin as a reference clock input. ▪ 0x0 = pull-down disabled ▪ 0x1 = pull-down enabled
6:0	gpi_func	RW	0x7F	GPI Functions Sets the general purpose input function. ▪ 0x0 = OE[0], input, enable output drivers in OE group 0 ▪ 0x1 = OE[1], input, enable output drivers in OE group 1 ▪ 0x2 = OE[2], input, enable output drivers in OE group 2 ▪ 0x3 = OE[3], input, enable output drivers in OE group 3 ▪ 0x4 = OE[4], input, enable output drivers in OE group 4 ▪ 0x5 = PERST#, input, latches CLKIN0 fanout buffer mode clock selection on active edge ▪ 0x6 = GOE, input, enable all output drivers ▪ 0x7 = DPLL_CLK_SEL[0], input ▪ 0x8 = DPLL_CLK_SEL[1], input ▪ 0x9 =PERST1#, input, latches XO/IB fanout buffer mode clock selection on active edge ▪ 0xA = RESET_IN#, input ▪ 0xB = SFT+, input ▪ 0xC = SFT-, input ▪ 0xD = SOD_EN#, input ▪ 0xE = SDI, input (SPI 4-wire mode) ▪ 0xF = SYSREF_IN ▪ 0x10 = GPI, input, input status allowed read back via SSI ▪ 0x7F = GPI function disabled, pin used as reference clock input

Table 78. GPI_STS - GPI Status

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	Reserved.
3:0	gpi_sts	RO	0x0	GPI Status Indicates the status of the GPI0/1/2/3 pins without latching and without applying optional polarity inversion (gpi_pol). If a pin is configured to be a reference clock input (see gpi_func), the status reads back as 0. Bit [3] = GPI3 status Bit [2] = GPI2 status Bit [1] = GPI1 status Bit [0] = GPI0 status

4.13 GPIO Registers

Table 79. GPIO_CNFG - GPIO Configuration

Bit Field	Field Name	Type	Default Value	Description
15	reserved	RO	0x0	Reserved.
14:13	gpo_drv	RW	0x0	GPO Drive Strength Applies to the pad when configured as an output (gpio_type is 0x0 or 0x2). Drive strength increases as this setting increases.
12	gpo_ctrl	RW	0x0	GPO output control signal value Sets the value to drive the GPO pin when configured as a general purpose output.
11:10	gpio_type	RW	0x1	GPIO type Sets the direction and type following reset. ▪ 0x0 = output (driven high/low), or bidirectional if configured as SDIO by gpio_func ▪ 0x1 = input (2-level) ▪ 0x2 = output (open-drain) ▪ 0x3 = input (tri-level). Only valid for GPIO0/1/2 when set to GPI mode or Dynamic CSEL; reserved for GPIO3/4.
9	gpio_pol	RW	0x0	GPIO Polarity Sets the pin polarity. This bit is ignored if gpio_func configures the pin as a tri-level Dynamic CSEL, GPO, or test clock output. ▪ 0x0 = Normal sense. Pin functions denoted with a # are active low, others are active high. ▪ 0x1 = Inverted sense. Pin functions denoted with a # are active high, others are active low.
8	gpio_pullup	RW	0x0	GPIO Pull-up Enable Sets the internal pull-up mode. ▪ 0x0 = pull-up disabled ▪ 0x1 = pull-up enabled
7	gpio_pulldn	RW	0x1	GPIO Pull-down Enable Sets the internal pull-down mode. ▪ 0x0 = pull-down disabled ▪ 0x1 = pull-down enabled

Table 79. GPIO_CNFG - GPIO Configuration (Cont.)

Bit Field	Field Name	Type	Default Value	Description
6:0	gpio_func	RW	0x10	GPIO Functions Sets the general purpose input/output function. Refer to pwrdn_sel for PWRGD/PWRDN# assignment. 0x0 = OE[0], input, enable output drivers in OE group 0 0x1 = OE[1], input, enable output drivers in OE group 1 0x2 = OE[2], input, enable output drivers in OE group 2 0x3 = OE[3], input, enable output drivers in OE group 3 0x4 = OE[4], input, enable output drivers in OE group 4 0x5 = PERST#, input, latches CLKIN0 fanout buffer mode clock selection on active edge 0x6 = GOE, input, enable all output drivers 0x7 = DPLL_CLK_SEL[0], input 0x8: DPLL_CLK_SEL[1], input 0x9 = PERST1#, input, latches XO/IB fanout buffer mode clock selection on active edge 0xA = RESET_IN#, input 0xB = SFT+, input 0xC = SFT-, input 0xD = SOD_EN#, input 0xE = SDI, input (SPI 4-wire mode) 0xF = SYSREF_IN, input 0x10 = GPI, input, input status allowed read back via SSI 0x11 = Dynamic CSEL, input, dynamic configuration control. Only valid for GPIO0/1/2. May be tri-level or 2-level. 0x17 = RSTOUT# (SFTRST# AND HRDRST#), output 0x18 = SFTRST#, output 0x19 = HRDRST#, output 0x1A = OC_ACTIVE#, output, reflects ~oc_active. 0x1B = SOD_ACTIVE#, output, reflects ~sod_active. 0x1C = INT, output 0x1D = GPO, output, to control external functions such as LEDs. The output value is set in gpo_ctrl. 0x1E = SDO, output (SPI 4-wire mode) or SDIO, bidirectional (SPI-3-wire mode; gpio_type must be set to 0, and is internally controlled as 0 or 1 by the SPI logic). 0x20 = clkin0 los_sts, output 0x21 = clkin1 los_sts, output 0x22 = clkin2 los_sts, output 0x23 = clkin3 los_sts, output 0x24 = refin los_sts, output 0x25 = apll_lock_sts, output 0x26 = dpll_lock_sts, output 0x28 = clkin0 los_evt, output 0x29 = clkin1 los_evt, output 0x2A = clkin2 los_evt, output 0x2B = clkin3 los_evt, output 0x2C = refin los_evt, output 0x2D = apll_lol, output 0x2E = dpll_lol, output 0x30 = clkin0 los_lmt_evt, output 0x31 = clkin1 los_lmt_evt, output 0x32 = clkin2 los_lmt_evt, output 0x33 = clkin3 los_lmt_evt, output 0x34 = refin los_lmt_evt, output 0x35 = apll_lol_lmt, output 0x36 = dpll_lol_lmt, output 0x37 = CLKMODE (fanout_clkmode), output 0x38 = device_ready, output 0x39 = CLKMODE1 (fanout_buf_mode1), output 0x7F = test clock according to test_clock_sel (GPIO0 only)

Table 80. GPIO_STS - GPIO Status

Bit Field	Field Name	Type	Default Value	Description
7:0	gpio_sts	RO	0x0	GPIO Status Indicates the status of the GPIO0/1/2/3/4 pins without latching and without applying optional polarity inversion (gpio_pol). For GPIO0/1/2, the possible encodings are: ▪ 0x0 = tri-level low, 2-level low ▪ 0x1 = tri-level mid, 2-level unused ▪ 0x2 = unused ▪ 0x3 = tri-level high, 2-level high Bit [7] = GPIO4 status Bit [6] = GPIO3 status Bits [5:4] = GPIO2 status Bits [3:2] = GPIO1 status Bits [1:0] = GPIO0 status

4.14 INT Registers

Table 81. SCRATCH0 - Software Scratch Register 0

Bit Field	Field Name	Type	Default Value	Description
31:0	scratch0	RW	0x0	Scratch register. For arbitrary software use.

Table 82. INT_EN - Interrupt Enable

Bit Field	Field Name	Type	Default Value	Description
31	device_int_en	RW	0x0	Device interrupt enable. Overall device interrupt enable. When this field is set to 1, the device interrupt is asserted while device_int_sts is 1.
30	reserved	RO	0x0	Reserved.
29	load_fail_int_en	RW	0x0	Configuration Loader Failure Interrupt Enable When this field is set to 1, the load_fail_int_sts bit contributes to the device interrupt
28	load_err_int_en	RW	0x0	Configuration Loader Error Interrupt Enable When this field is set to 1, the load_err_int_sts bit contributes to the device interrupt
27	otp_manual_rdy_int_en	RW	0x0	OTP Manual Request Ready Interrupt Enable When this field is set to 1, the otp_manual_rdy_int_sts bit contributes to the device interrupt
26	wd_alarm_int_en	RW	0x0	Watch Dog interrupt enable. When this field is set to 1, the wd_alarm_int_sts bit contributes to the device interrupt
25	los4_lmt_int_en	RW	0x0	REFIN Monitor LOS Threshold Exceeded interrupt enable. When this field is set to 1, the los4_lmt_int_sts bit contributes to the device interrupt

Table 82. INT_EN - Interrupt Enable (Cont.)

Bit Field	Field Name	Type	Default Value	Description
24	los3_lmt_int_en	RW	0x0	CLKIN3 Monitor LOS Threshold Exceeded interrupt enable. When this field is set to 1, the los3_lmt_int_sts bit contributes to the device interrupt
23	los2_lmt_int_en	RW	0x0	CLKIN2 Monitor LOS Threshold Exceeded interrupt enable. When this field is set to 1, the los2_lmt_int_sts bit contributes to the device interrupt
22	los1_lmt_int_en	RW	0x0	CLKIN1 Monitor LOS Threshold Exceeded interrupt enable. When this field is set to 1, the los1_lmt_int_sts bit contributes to the device interrupt
21	los0_lmt_int_en	RW	0x0	CLKIN0 Monitor LOS Threshold Exceeded interrupt enable. When this field is set to 1, the los0_lmt_int_sts bit contributes to the device interrupt
20	reserved	RO	0x0	Reserved.
19	apll_lol_lmt_int_en	RW	0x0	APLL Loss-of-lock Threshold Exceeded interrupt enable. When this field is set to 1, the apll_lol_lmt_int_sts bit contributes to the device interrupt
18	reserved	RO	0x0	Reserved.
17	freq3_int_en	RW	0x0	CLKIN3 Frequency Monitor interrupt enable. When this field is set to 1, the freq3_int_sts bit contributes to the device interrupt
16	freq2_int_en	RW	0x0	CLKIN2 Frequency Monitor interrupt enable. When this field is set to 1, the freq2_int_sts bit contributes to the device interrupt
15	freq1_int_en	RW	0x0	CLKIN1 Frequency Monitor interrupt enable. When this field is set to 1, the freq1_int_sts bit contributes to the device interrupt
14	freq0_int_en	RW	0x0	CLKIN0 Frequency Monitor interrupt enable. When this field is set to 1, the freq0_int_sts bit contributes to the device interrupt.
13:9	reserved	RO	0x0	Reserved.
8	los4_int_en	RW	0x0	REFIN Monitor Loss-of-Signal interrupt enable. When this field is set to 1, the los4_int_sts bit contributes to the device interrupt
7	los3_int_en	RW	0x0	CLKIN3 Monitor Loss-of-Signal interrupt enable. When this field is set to 1, the los3_int_sts bit contributes to the device interrupt
6	los2_int_en	RW	0x0	CLKIN2 Monitor Loss-of-Signal interrupt enable. When this field is set to 1, the los2_int_sts bit contributes to the device interrupt
5	los1_int_en	RW	0x0	CLKIN1 Monitor Loss-of-Signal interrupt enable. When this field is set to 1, the los1_int_sts bit contributes to the device interrupt
4	los0_int_en	RW	0x0	CLKIN0 Monitor Loss-of-Signal interrupt enable. When this field is set to 1, the los0_int_sts bit contributes to the device interrupt.

Table 82. INT_EN - Interrupt Enable (Cont.)

Bit Field	Field Name	Type	Default Value	Description
3:1	reserved	RO	0x0	Reserved.
0	apll_lol_int_en	RW	0x0	APLL Loss-of-Lock interrupt enable. When this field is set to 1, the apll_lol_int_sts bit contributes to the device interrupt.

Table 83. INT_STS - Interrupt Status

Bit Field	Field Name	Type	Default Value	Description
31	device_int_sts	RO	0x0	Device interrupt status. Overall device interrupt status. This bit is the OR of all the other interrupt status bits in this register after masking by their respective interrupt enable bits in the INT_EN - Interrupt Enable register. This bit is masked by device_int_en. The resulting signal can be output on the assigned GPIO pin.
30	reserved	RO	0x0	Reserved.
29	load_fail_int_sts	RO	0x0	Configuration Loader Failure interrupt status The logical OR of the otp_load_fail and eeprom_load_fail event bits
28	load_err_int_sts	RO	0x0	Configuration Loader Error interrupt status The logical OR of the otp_crc_err and eeprom_crc_err event bits
27	otp_manual_rdy_int_sts	RO	0x0	OTP Manual Request Ready interrupt status Mirrors the OTP manual_rdy event bit
26	wd_alarm_int_sts	RO	0x0	Watch Dog interrupt status Mirrors the watch dog wdt_expired_evt event bit
25	los4_lmt_int_sts	RO	0x0	REFIN Monitor LOS Threshold Exceeded interrupt status Mirrors the REFIN los_lmt_evt event bit
24	los3_lmt_int_sts	RO	0x0	CLKIN3 Monitor LOS Threshold Exceeded interrupt status Mirrors the CLKIN3 los_lmt_evt event bit
23	los2_lmt_int_sts	RO	0x0	CLKIN2 Monitor LOS Threshold Exceeded interrupt status Mirrors the CLKIN2 los_lmt_evt event bit
22	los1_lmt_int_sts	RO	0x0	CLKIN1 Monitor LOS Threshold Exceeded interrupt status Mirrors the CLKIN1 los_lmt_evt event bit
21	los0_lmt_int_sts	RO	0x0	CLKIN0 Monitor LOS Threshold Exceeded interrupt status Mirrors the CLKIN0 los_lmt_evt event bit
20	reserved	RO	0x0	Reserved.
19	apll_lol_lmt_int_sts	RO	0x0	APLL Loss-of-lock Threshold Exceeded interrupt status Mirrors the apll_lol_lmt event bit
18	reserved	RO	0x0	Reserved.
17	freq3_int_sts	RO	0x0	CLKIN3 Frequency Monitor interrupt status Mirrors the CLKIN3 freq_evt event bit
16	freq2_int_sts	RO	0x0	CLKIN2 Frequency Monitor interrupt status Mirrors the CLKIN2 freq_evt event bit
15	freq1_int_sts	RO	0x0	CLKIN1 Frequency Monitor interrupt status Mirrors the CLKIN1 freq_evt event bit

Table 83. INT_STS - Interrupt Status (Cont.)

Bit Field	Field Name	Type	Default Value	Description
14	freq0_int_sts	RO	0x0	CLKIN0 Frequency Monitor interrupt status Mirrors the CLKIN0 freq_evt event bit
13:9	reserved	RO	0x0	Reserved.
8	los4_int_sts	RO	0x0	REFIN Monitor Loss-of-Signal interrupt status Mirrors the REFIN los_evt event bit
7	los3_int_sts	RO	0x0	CLKIN3 Monitor Loss-of-Signal interrupt status Mirrors the CLKIN3 los_evt event bit
6	los2_int_sts	RO	0x0	CLKIN2 Monitor Loss-of-Signal interrupt status Mirrors the CLKIN2 los_evt event bit
5	los1_int_sts	RO	0x0	CLKIN1 Monitor Loss-of-Signal interrupt status Mirrors the CLKIN1 los_evt event bit
4	los0_int_sts	RO	0x0	CLKIN0 Monitor Loss-of-Signal interrupt status Mirrors the CLKIN0 los_evt event bit
3:1	reserved	RO	0x0	Reserved.
0	apll_lol_int_sts	RO	0x0	APLL Loss-of-lock interrupt status Mirrors the apll_lol event bit

5. Revision History

Revision	Date	Description
0.1	Apr 8, 2021	Initial release.