R9A02G011

Board Design Guide

Introduction

This document describes guidelines for designing boards using Renesas Electronics USB Power Delivery devices. These guidelines offer Renesas Electronics' recommendations with no guarantee of results.

This document only guides designing around the R9A02G011, refer to the document of power management IC for designing around the power IC.

Target Device

R9A02G011

Related Document

- R9A02G011 Data Sheet: R19DS0088EJ
- R9A02G011 User's Manual: R19UH0102EJ
- RTK-251-BuckBoostConverter2 Instruction Manual: R19AN0057EJ
- RTK-251-1PowerBank3 Instruction Manual: R19AN0056EJ
- RTK-251-DRPEVB Instruction Manual: R19AN0059EJ

Contents

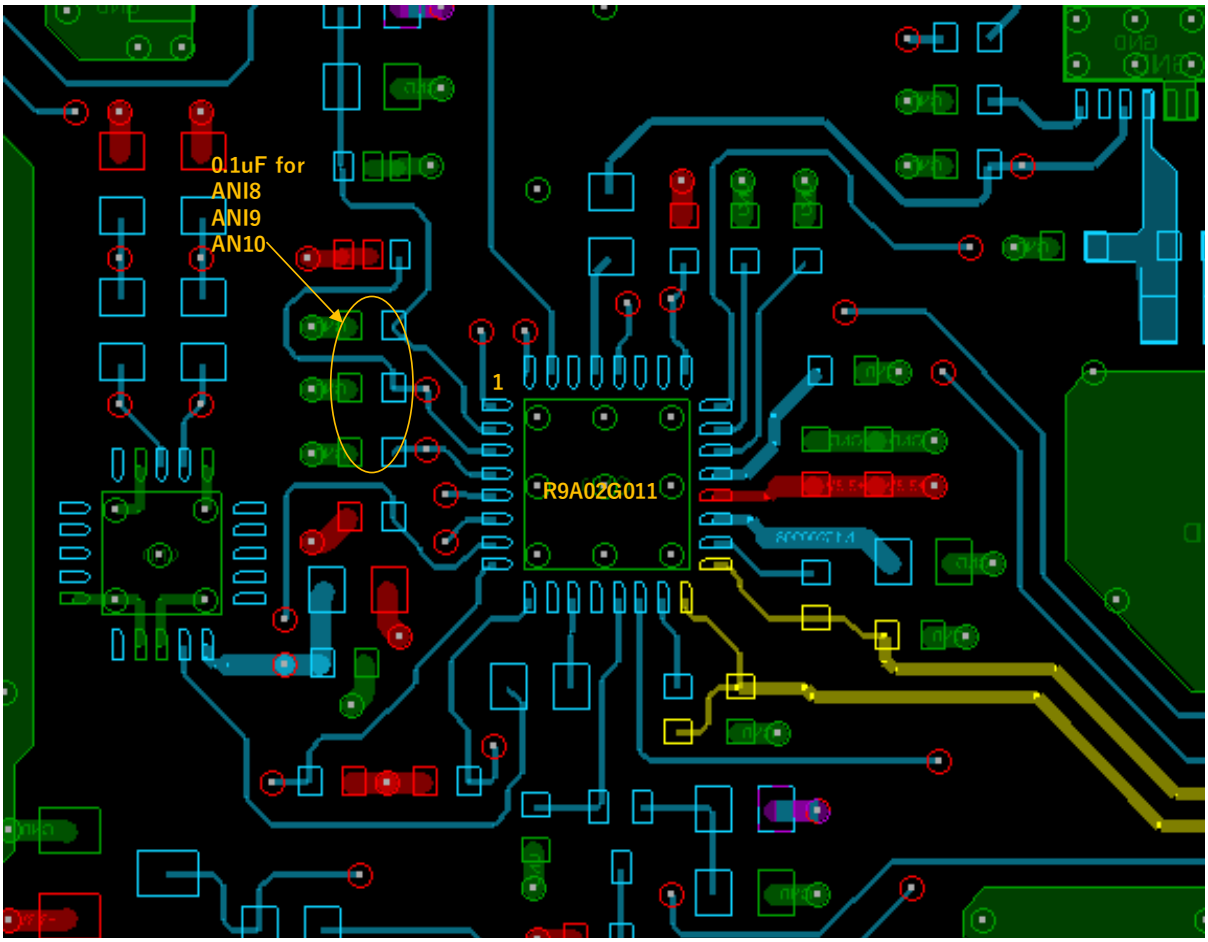
1. Consideration to design a PCB on the R9A02G011

It is necessary to have several considerations if design a PCB on the R9A02G011.

1.1 Analog input pin connection

Put 0.1 uF near each “ANI” pin individually (P20, P21 and P22 are ANI).

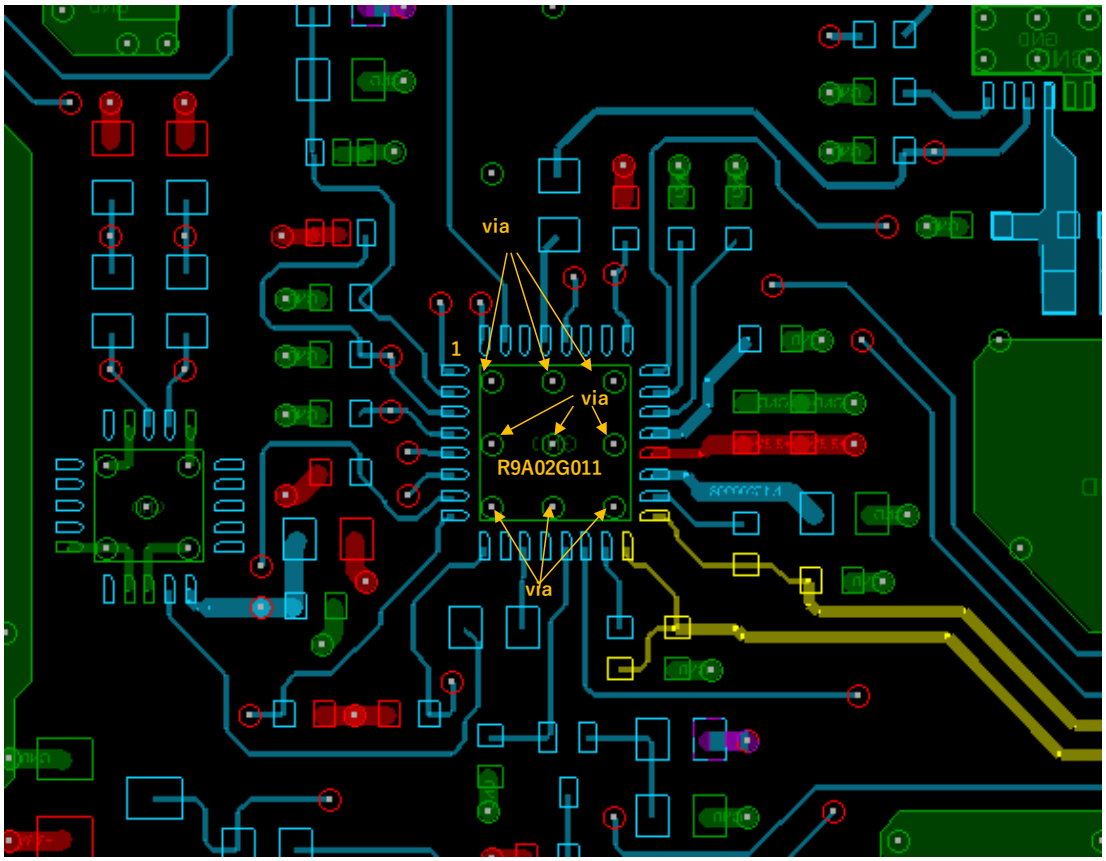
Figure 1-1 Analog input pin connection



1.2 Via under E-pad

Make ϕ 0.3 mm via under E-pad as following pattern.

Figure 1-2 Via under E-pad

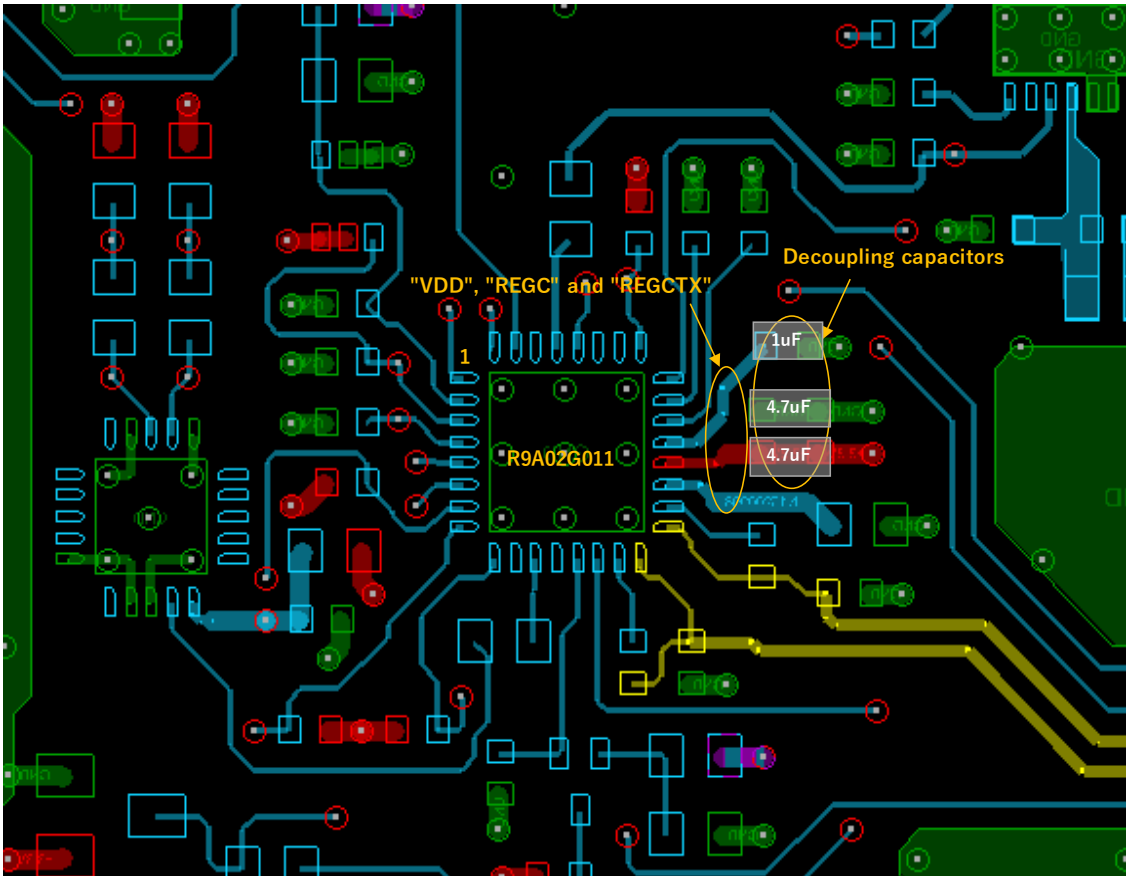


1.3 Decoupling capacitor and “VDD”, “REGC” and “REGCTX” power lines

Each Decoupling capacitor should be put on near each pin (VDD, REGC, REGCTX) individually.

Make these traces connected to "VDD", "REGC" and "REGCTX" thick enough. Because ""VDD", "REGC" and "REGCTX" are power pins.

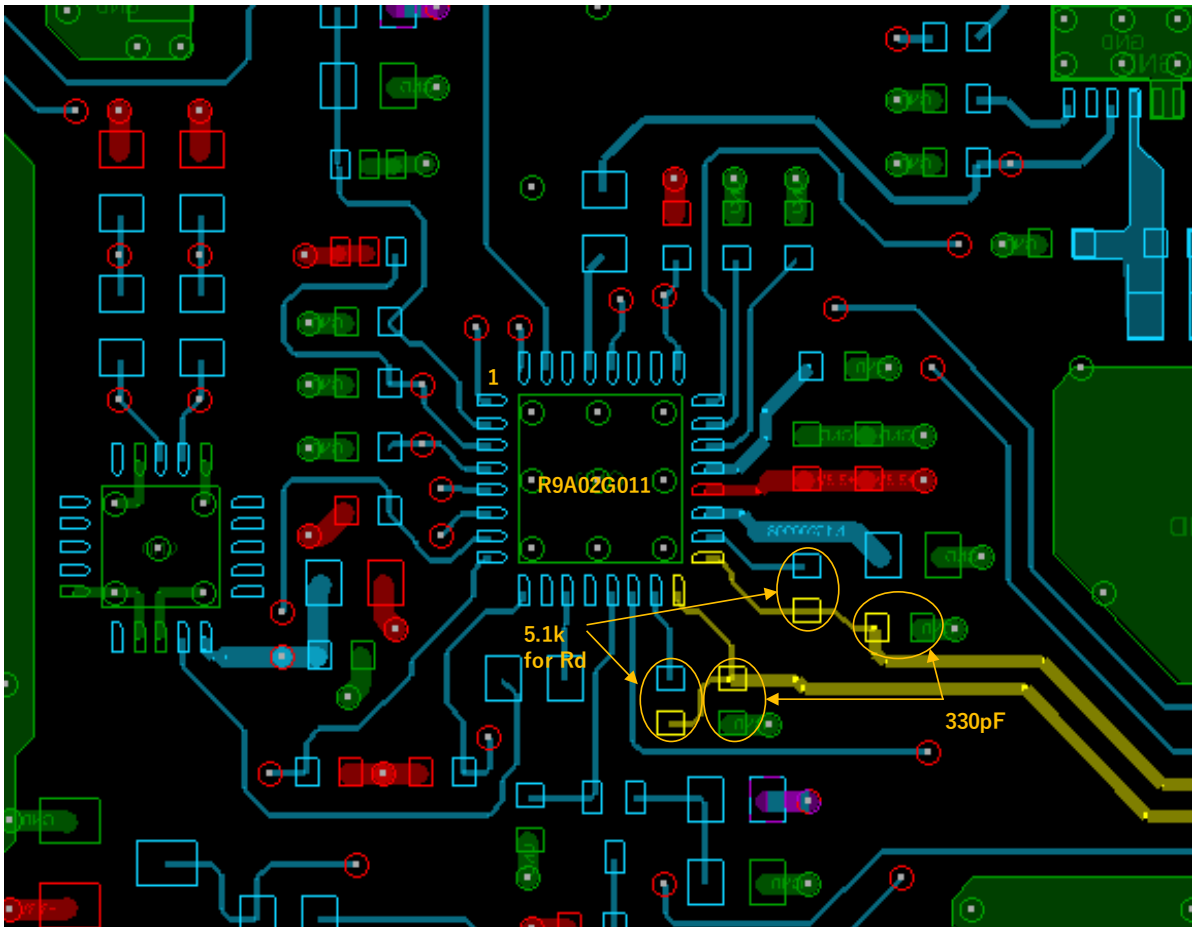
Figure 1-3 Decoupling capacitor



1.4 Rd resister and decoupling capacitor for CC line

Put 5.1 kohm near RD1, RD2 pin individually, and put 330 pF near CC1, CC2 pin individually.

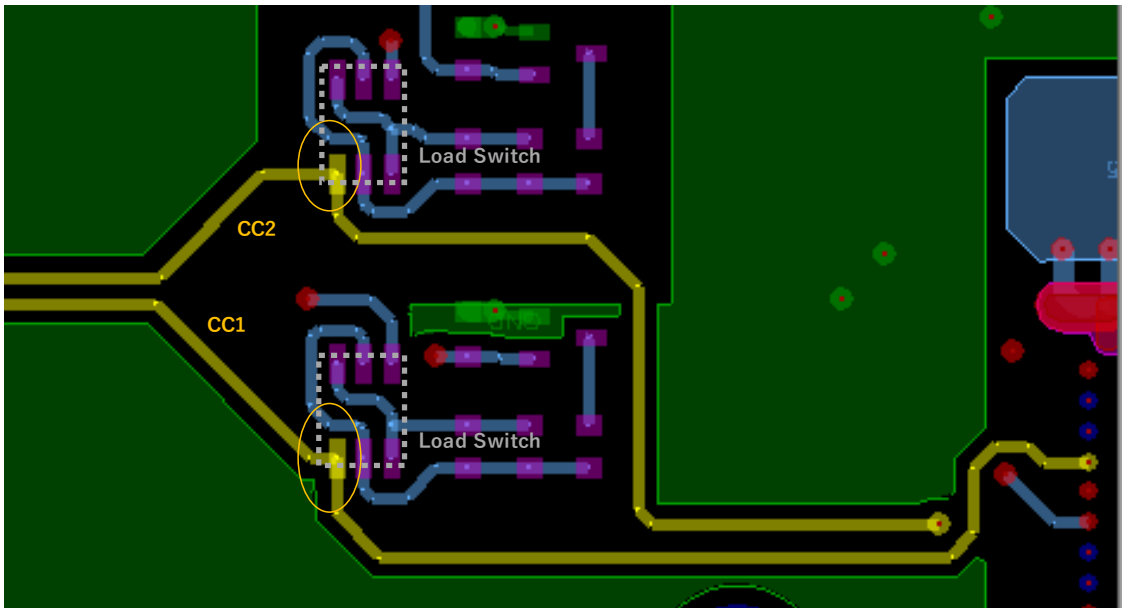
Figure 1-4 Rd resister and decoupling capacitor for CC line



1.5 Load switch for supplying VCONN power

Do not make a stub on CC trace by VCONN power supply. Put on Load Switch near CC trace.

Figure 1-5 Load switch for suppling VCONN power



2. Design check list

Following checklists are written based on Renesas Reference Design Note which are designed by Renesas recommended guideline. The result of design by using following checklists is no guarantee. Use them for reference only.

Note The information of reference design is available in Renesas web site.

2.1 Check list for source-only device

(1) Power / Data Role check

Power Role	**SRC**	
Data Role		UFP DFP DRD

(2) Power supply and USB Type-C™ check

Section	Sub-section	Description	Check
Power supply	**Operating Range**	Check **"VDD**" is supplied from the power source within 3.0 V - 5.5 V	
System Reset	**Power Stabilization**	Check 4.7 uF decoupling capacitor is put on near **"REGCTX"** pin.	
		Check 1 uF decoupling capacitor is put on near **"REGC"** pin.	
	Reset	Check **"RESETB"** pin is pulled up VDD via 10 kohm resistor.	
USB Type-C	**VBUS**	Check VBUS leakage impedance is more than **"72.4 kohm"** on USB Type-C Receptacle (VBUS) pin.	
		Check VBUS capacitance is less than **"10 uF"** on USB Type-C Receptacle (VBUS) pin.	
	CC trace	Connect **"CC1"** and **"CC2"** to USB Type-C Receptacle (CC1/CC2) pin.	
		Check 330 pF is put on near **"CC1"** and **"CC2"** pins individually.	
		Check "RD1" and "RD2" are open individually.	
		Check VCONN source is connected to **"CC1"** and **"CC2"** individually.	

(3) GPIOs check

Section	Sub-section	Function	Description	Check
GPIOs	**P20/ANI8**	VBUSM	Pull-up to VBUS via 100 kohm (1%) and pull-down to GND via 15 kohm (1%)	
			Check 0.1 uF decoupling capacitor and clipping diodes are put on near **"P20/ANI8/VBUSM"** pin.	
	P21/ANI9	ANI9	Check 0.1 uF decoupling capacitor and clipping diodes are put on near **"P21/ANI9"** pin.	
		Unused	Output: Open	
	P22/ANI10	ANI10	Check 0.1 uF decoupling capacitor and clipping diodes are put on near **"P22/ANI10"** pin.	
		Unused	Output: Open	
	P31/MSTSDA	MSTSDA	Connect to I2C slave serial data pin with 4.7 kohm pull-up resistor.	
		Unused	Output: Open	
	P30/MSTSCL	MSTSCL	Connect to I2C slave serial clock pin with 4.7 kohm pull-up resistor.	
		Unused	Output: Open	
	P40/TOOL0	TOOL0	Pull-up to VDD via 1 kohm resistor	
		Unused	Input: Pull-up to VDD via the resistor. Output: Open	
	P61/SLVSDA	SLVSDA	Connect to I2C master serial data pin with 4.7 kohm pull-up resistor.	
		Unused	Output: Open	
	P60/SLVSCL	SLVSCL	Connect to I2C master serial clock pin with 4.7 kohm pull-up resistor.	
		Unused	Output: Open	
	P62/SLVSALTB	SLVSALTB	Connect to I2C master input (GPIO, INT or other) with 10 kohm pull-up resistor.	
		Unused	Output: Open	
	P137/MSTSALTB	MSTSALTB	Connect to I2C slave input (GPIO, INT or other) with 10 kohm pull-up resistor.	
		Unused	Input: Pull-up to VDD via the resistor.	
	P16, P17, P32 P50, P51, P70, P71, P72, P73, P80, P81, P82, P121, P122		Refer to “Configurable function” check	

(4) Configurable function check

Following list is based on the RTK-251-BuckBoostConverter2. Refer to the RTK-251-BuckBoostConverter2 Instruction Manual (R19AN0057EJ), if you have detail information.

Port	Function	Description	Check
P16	VCONN1_DRV	Output: Connect to VCONN source load switch circuit of CC1	
P17	VCONN2_DRV	Output: Connect to VCONN source load switch circuit of CC2	
P32	Not used	Output: Open	
P50	Not used	Output: Open	
P51	Not used	Output: Open	
P70	Not used	Output: Open	
P71	AGATE	Output: Connect to VBUS load switch circuit	
P72	DISCHG	Output: Connect to VBUS discharge circuit	
P73	Not used	Output: Open	
P80	Not used	Output: Open	
P81	LED_CTRL	Output: Connect to LED circuit	
P82	Not used	Output: Open	
P121	SLVADDR0	Input: Connect to VDD or GND via resister	
P122	SLVADDR1	Input: Connect to VDD or GND via resister	

2.2 Check list for DRP device

(1) Power / Data Role check

Power Role	**DRP**	
Data Role		UFP DFP DRD

(2) Power supply and USB Type-C check

Section	Sub-section	Description	Check
Power supply	**Operating Range**	Check **"VDD"** is supplied from the power source within 3.0 V - 5.5 V	
System Reset	**Power Stabilization**	Check 4.7 uF decoupling capacitor is put on near **"REGCTX"** pin.	
		Check 1 uF decoupling capacitor is put on near **"REGC"** pin.	
	Reset	Check "RESETB" pin is pulled up VDD via 10 kohm resistor.	
USB Type-C	**VBUS**	Check VBUS leakage impedance is more than **"72.4 kohm"** on USB Type-C Receptacle (VBUS) pin.	
		Check VBUS capacitance is less than **"10 uF"** on USB Type-C Receptacle (VBUS) pin.	
		Check VBUS capacitance is less than **"100 uF"** on USB Type-C Receptacle (VBUS) pin to the regulator, to meet cSnkBulkPd.	
	CC trace	Connect **"CC1"** and **"CC2"** to USB Type-C Receptacle (CC1/CC2) pin.	
		Check 330 pF is put on near **"CC1"** and **"CC2"** pins individually.	
		Check **"RD1"** and **"RD2"** are open individually.	
		Check VCONN source is connected to **"CC1"** and **"CC2"** individually.	

(3) GPIOs check

Section	Sub-section	Function	Description	Check
GPIOs	**P20/ANI8**	VBUSM	Pull-up to VBUS via 100 kohm (1%) and pull-down to GND via 15 kohm (1%)	
			Check 0.1 uF decoupling capacitor and clipping diodes are put on near **"P20/ANI8/VBUSM"** pin.	
	P21/ANI9	ANI9	Check 0.1 uF decoupling capacitor and clipping diodes are put on near **"P21/ANI9"** pin.	
		Unused	Output: Open	
	P22/ANI10	ANI10	Check 0.1 uF decoupling capacitor and clipping diodes are put on near **"P22/ANI10"** pin.	
		Unused	Output: Open	
	P31/MSTSDA	MSTSDA	Connect to I2C slave serial data pin with 4.7 kohm pull-up resistor.	
		Unused	Output: Open	
	P30/MSTSCL	MSTSCL	Connect to I2C slave serial clock pin with 4.7 kohm pull-up resistor.	
		Unused	Output: Open	
	P40/TOOL0	TOOL0	Pull-up to VDD via 1 kohm resistor	
		Unused	Input: Pull-up to VDD via the resistor. Output: Open	
	P61/SLVSDA	SLVSDA	Connect to I2C master serial data pin with 4.7 kohm pull-up resistor.	
		Unused	Output: Open	
	P60/SLVSCL	SLVSCL	Connect to I2C master serial clock pin with 4.7 kohm pull-up resistor.	
		Unused	Output: Open	
	P62/SLVSALTB	SLVSALTB	Connect to I2C master input (GPIO, INT or other) with 10 kohm pull-up resistor.	
		Unused	Output: Open	
	P137/MSTSALTB	MSTSALTB	Connect to I2C slave input (GPIO, INT or other) with 10 kohm pull-up resistor.	
		Unused	Input: Pull-up to VDD via the resistor.	
	P16, P17, P32 P50, P51, P70, P71, P72, P73, P80, P81, P82, P121, P122		Refer to “Configurable function” check	

(4) Configurable function check

Following list is based on the RTK-251-1PowerBank3. Refer to the RTK-251-1PowerBank3 Instruction Manual (R19AN0056EJ), if you have detail information.

Port	Function	Description	Check
P16	VCONN1_DRV	Output: Connect to VCONN source load switch circuit of CC1	
P17	VCONN2_DRV	Output: Connect to VCONN source load switch circuit of CC2	
P32	Not used (AUTH_RESB)	Output: Open (Connect to RES of R5H30313XB08)	
P50	WAKEUP	Input: Connect to WAKEUP circuit	
P51	ROLE_SW	Input: Connect to ROLE_SW circuit	
P70	BATLV1	Output: Connect to BATLV1 LED circuit	
P71	BATLV2	Output: Connect to BATLV2 LED circuit	
P72	DISCHG	Output: Connect to VBUS discharge circuit	
P73	BATLV3	Output: Connect to BATLV3 LED circuit	
P80	MON_EN	Output: Connect to Battery monitoring circuit	
P81	BATLV4	Output: Connect to BATLV4 LED circuit	
P82	LED_CTRL	Output: Connect to TYPEC_ROLE LED circuit	
P121	SLVADDR0	Input: Connect to VDD or GND via resister	
P122	SLVADDR1	Input: Connect to VDD or GND via resister	

2.3 Check list for sink-only device

(1) Power / Data Role check

Power Role	**SNK**	
Data Role		UFP DFP DRD

(2) Power supply and USB Type-C check

Section	Sub-section	Description	Check
Power supply	**Operating Range**	Check "VDD" is supplied from the power source within 3.0 V - 5.5 V	
System Reset	**Power Stabilization**	Check 4.7 uF decoupling capacitor is put on near "REGCTX" pin.	
		Check 1 uF decoupling capacitor is put on near "REGC" pin.	
	Reset	Check "RESETB" pin is pulled up VDD via 10 kohm resistor.	
USB Type-C	**VBUS**	Check VBUS leakage impedance is more than "72.4 kohm" on USB Type-C Receptacle (VBUS) pin.	
		Check VBUS capacitance is less than "10 uF" on USB Type-C Receptacle (VBUS) pin.	
		Check VBUS capacitance is less than "100 uF" on USB Type-C Receptacle (VBUS) pin to the regulator, to meet cSnkBulkPd.	
	CC trace	Connect "CC1" and "CC2" to USB Type-C Receptacle (CC1/CC2) pin.	
		Check 330 pF is put on near "CC1" and "CC2" pins individually.	
		Check "RD1" and "RD2" are open individually.	

(3) GPIOs check

Section	Sub-section	Function	Description	Check
GPIOs	**P20/ANI8**	VBUSM	Pull-up to VBUS via 100 kohm (1%) and pull-down to GND via 15 kohm (1%)	
			Check 0.1 uF decoupling capacitor and clipping diodes are put on near **"P20/ANI8/VBUSM"** pin.	
	P21/ANI9	ANI9	Check 0.1 uF decoupling capacitor and clipping diodes are put on near **"P21/ANI9"** pin.	
		Unused	Output: Open	
	P22/ANI10	ANI10	Check 0.1 uF decoupling capacitor and clipping diodes are put on near **"P22/ANI10"** pin.	
		Unused	Output: Open	
	P31/MSTSDA	MSTSDA	Connect to I2C slave serial data pin with 4.7 kohm pull-up resistor.	
		Unused	Output: Open	
	P30/MSTSCL	MSTSCL	Connect to I2C slave serial clock pin with 4.7 kohm pull-up resistor.	
		Unused	Output: Open	
	P40/TOOL0	TOOL0	Pull-up to VDD via 1 kohm resistor	
		Unused	Input: Pull-up to VDD via the resistor. Output: Open	
	P61/SLVSDA	SLVSDA	Connect to I2C master serial data pin with 4.7 kohm pull-up resistor.	
		Unused	Output: Open	
	P60/SLVSCL	SLVSCL	Connect to I2C master serial clock pin with 4.7 kohm pull-up resistor.	
		Unused	Output: Open	
	P62/SLVSALTB	SLVSALTB	Connect to I2C master input (GPIO, INT or other) with 10 kohm pull-up resistor.	
		Unused	Output: Open	
	P137/MSTSALTB	MSTSALTB	Connect to I2C slave input (GPIO, INT or other) with 10 kohm pull-up resistor.	
		Unused	Input: Pull-up to VDD via the resistor.	
	P16, P17, P32 P50, P51, P70, P71, P72, P73, P80, P81, P82, P121, P122		Refer to “Configurable function” check	

(4) Configurable function check

Following list is based on the RTK-251-DRPEVB (Bus-powered sink). Refer to the RTK-251-DRPEVB Instruction Manual (R19AN0059EJ), if you have detail information.

Port	Function	Description	Check
P16	Not used	Output: Open	
P17	Not used	Output: Open	
P32	Not used (AUTH_RESB)	Output: Open (Connect to RES of R5H30313XB08)	
P50	Not used	Output: Open	
P51	Not used	Output: Open	
P70	Not used	Output: Open	
P71	DISCHG	Output: Connect to VBUS discharge circuit	
P72	Not used	Output: Open	
P73	DRP_Drv	Output: Connect to VBUS load switch	
P80	Not used	Output: Open	
P81	SW	Input: tactile switch circuit	
P82	LED	Output: Connect to LED control circuit	
P121	SLVADDR0	Input: Connect to VDD or GND via resister	
P122	SLVADDR1	Input: Connect to VDD or GND via resister	

Revision History

Rev.	Date	Description	
		Page	Summary
1.0	Apr 04, 2019	-	Initial release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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