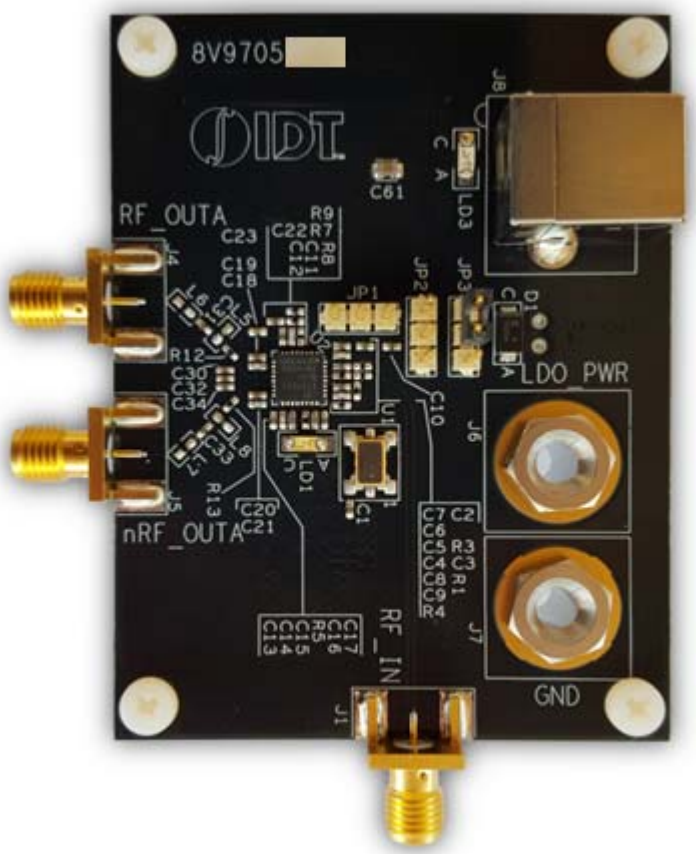
APPLICATION NOTE
Network Communications Division

8V9705x Evaluation Board User Guide
IDT Applications

October 2016



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Introduction

The 8V9705x evaluation board is designed to help the customer evaluate the 8V97051, 8V97051L, 8V97053 and 8V97053L IDT Wideband RF synthesizers. When the board is connected to a PC running IDT Timing Commander Software through USB, the device can be configured and programmed to generate frequencies with best-in-class performances.

Contents

The 8V9705x evaluation board kit ships with the following:

- (1) 8V9705x Evaluation Board
- (1) USB Cable

Requirements

PC Requirements:

- IDT Timing Commander Software Installed.
- USB 2.0 or USB 3.0 interface.
- Windows XP SP3 or later.
- Processor: Minimum 1GHz.
- Memory: Minimum 512MB, recommended 1GB.
- Available Disk Space: Min 600MB (1.5GB 64bit), recommended 1GB (2GB 64bit)
- Network access during installation if the .NET framework is not currently installed on the system.

Quick Start

(1) Connect a cable from a PC to the Evaluation Board USB port.
(2) Verify that the board is configured to power from the USB (see JP3 jumper position in Fig.1)
(3) JP2 and JP3 can be left floating.
(4) Connect 50ohm cables from the RF_OUTA output to the measurement equipment.
(5) Configure the device using Timing Commander.

Default Power-Up Condition

The board ships with a 25MHz TXCO and is configured to power from the USB. No external reference is required and no external power source, aside from the USB connection, is required. Outputs are disabled by default. The device must be configured using Timing Commander in order to activate the output.

Note: this device also has an RF_OUTb differential output that is not routed out on the evaluation board.

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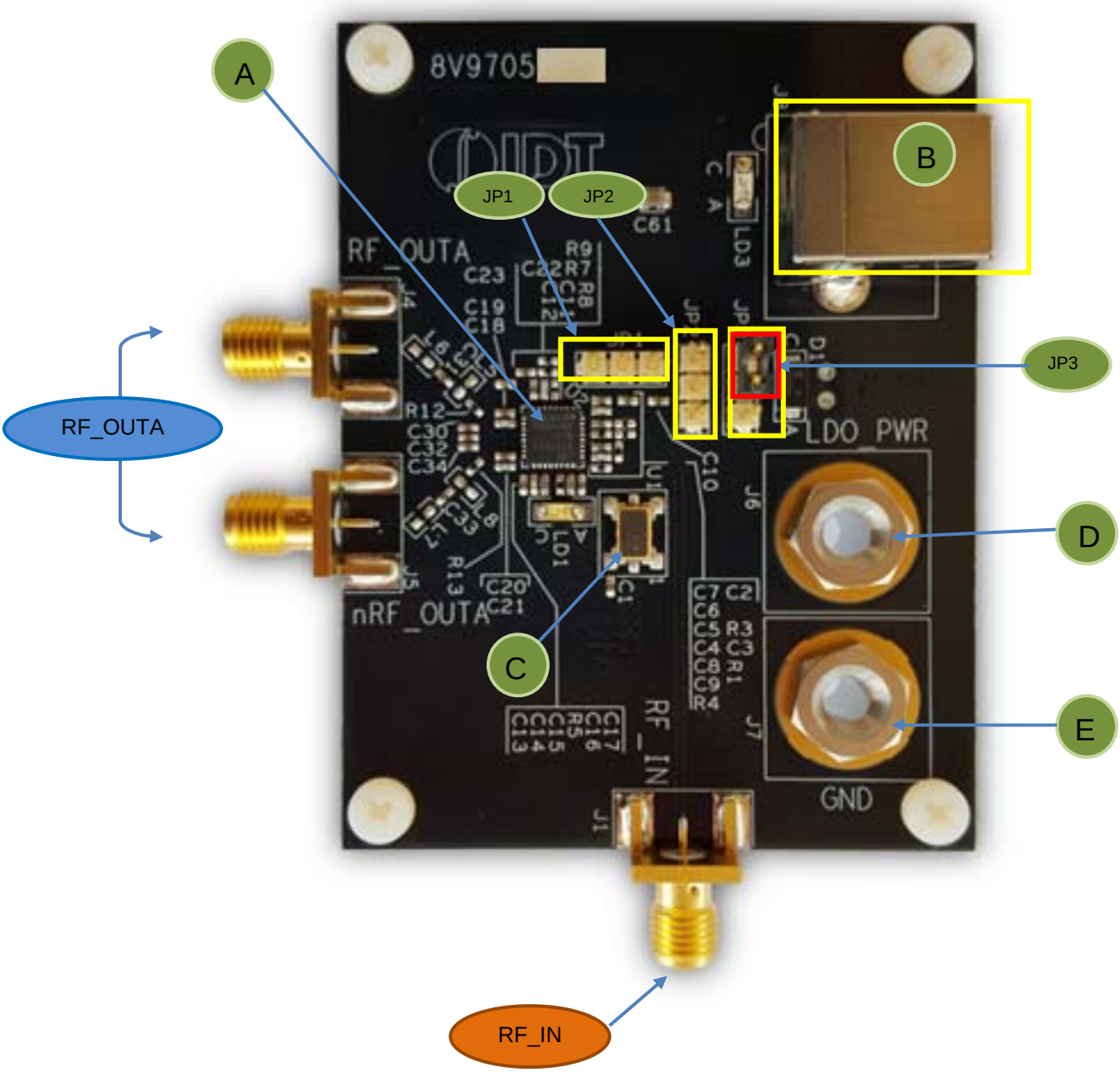
Board Overview

Use the following diagram to identify: power supply jacks, USB connector, input and output SMA connectors, TCXO, etc.

Figure 1. Evaluation Board Top View



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Legend

Inputs

RF_IN Reference input (the board requires re-work to enable this option)

Outputs

RF_OUTA Open-drain, ac-coupled output.

Other

A IDT8V9705x- the device to be evaluated
B USB connector (also powers the board)
C 25 MHz TXCO (default reference source)
D External LDO_POWER (alternate power source)
E GND
JP1 MUTE control (can be left floating)
JP2 CE control (can be left floating)
JP3 Power Source selector (USB vs LDO_PWR power source)

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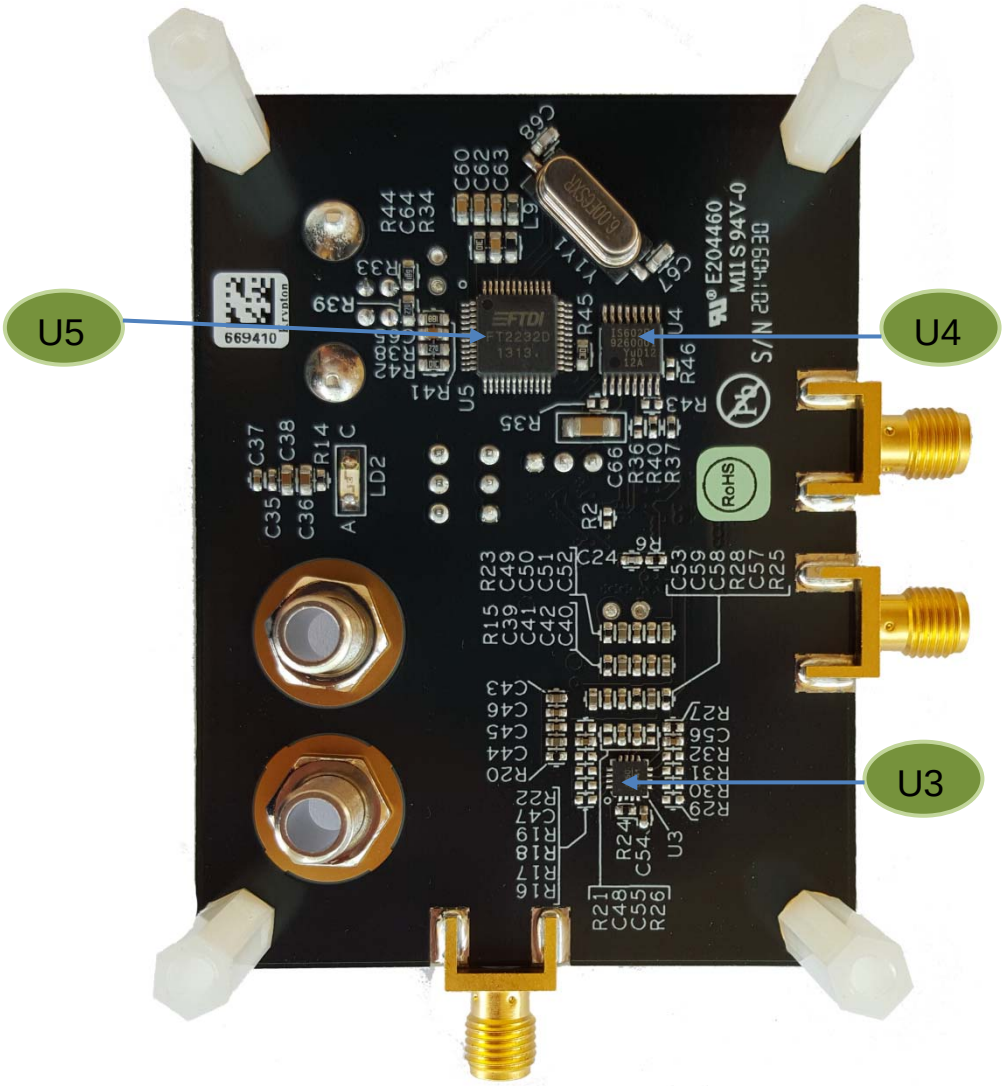
Figure 2. Evaluation Board Bottom View



Legend

U5 FTDI USB-to-I2C chip
U4 USB-to-SPI translator
U3 LDO

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Schematics

The following figures are schematics that are applicable to specific sections of this User Guide. The complete schematics are available in a separate document.

Figure 3. Input Schematic

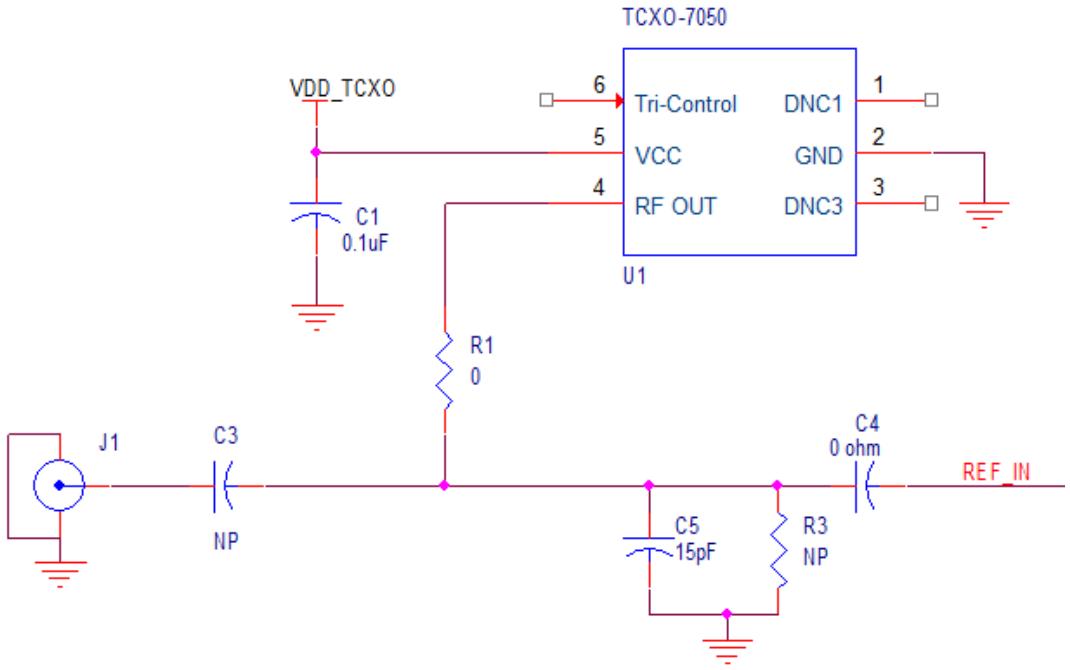

Figure 4. Output Termination Schematic

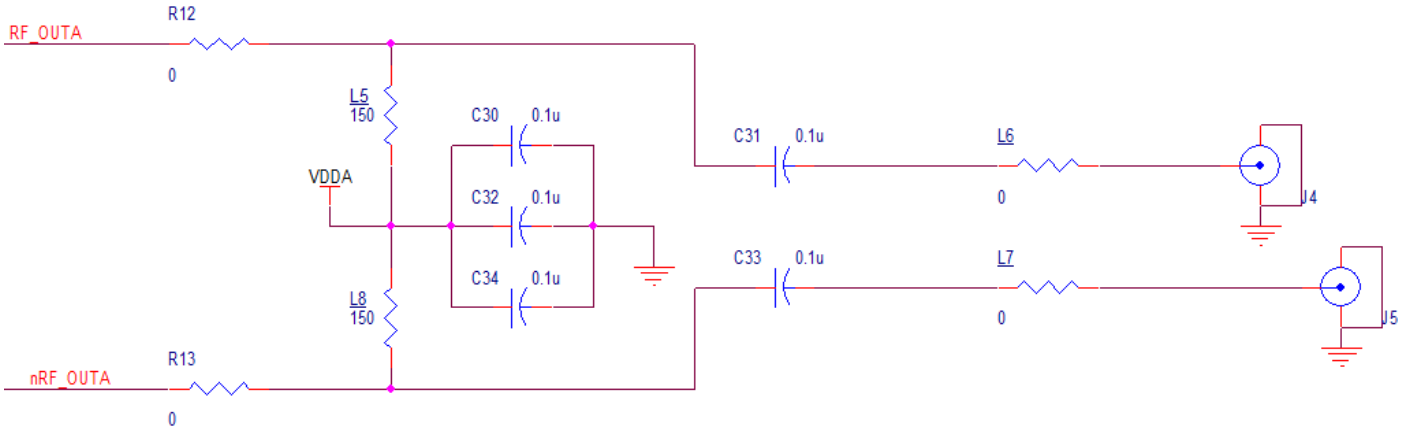

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Figure 5. Loop Filter Schematic

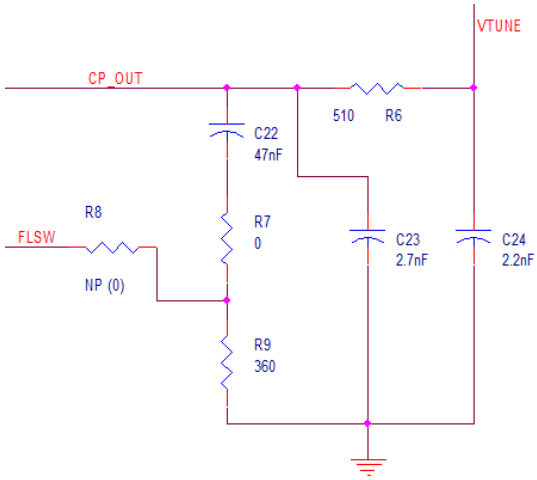

Figure 6 . Power Source Selection Schematic

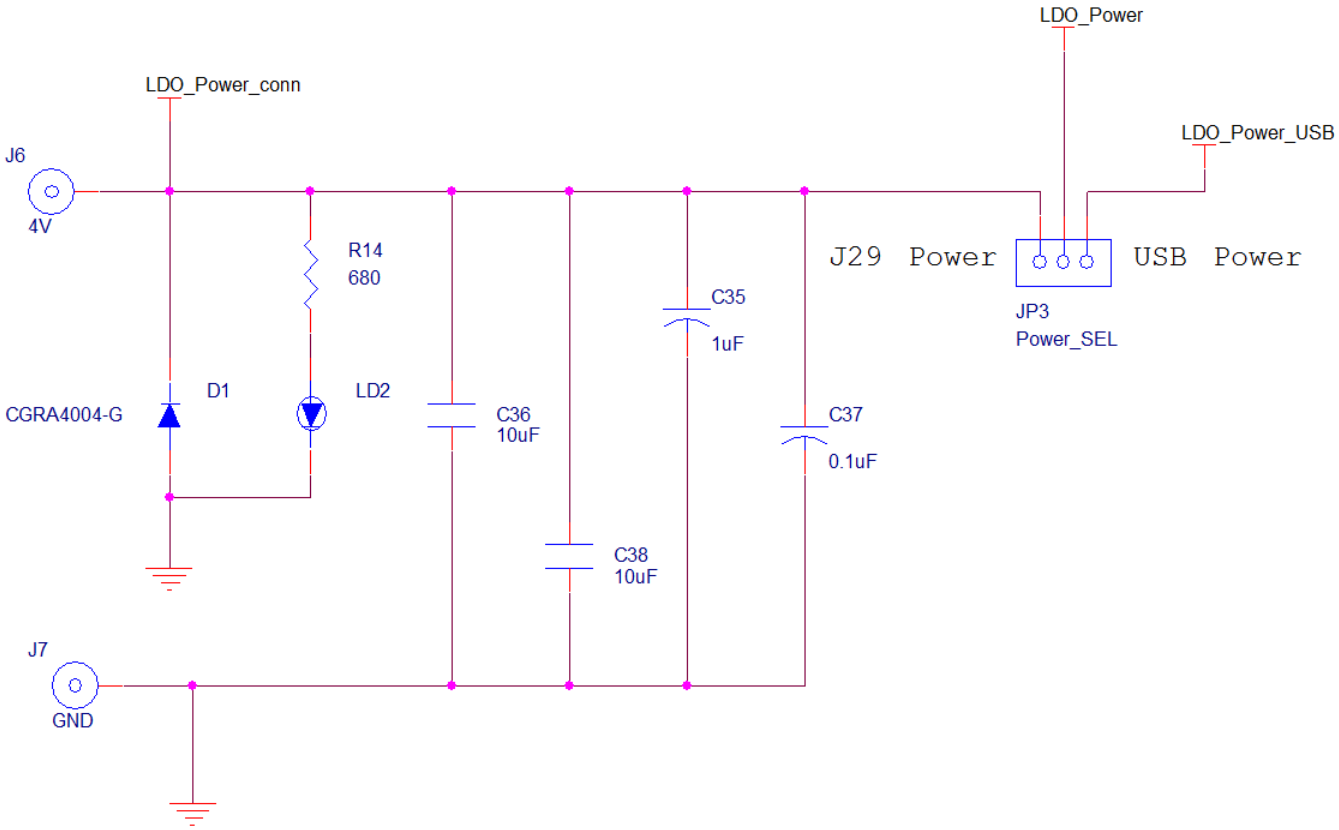

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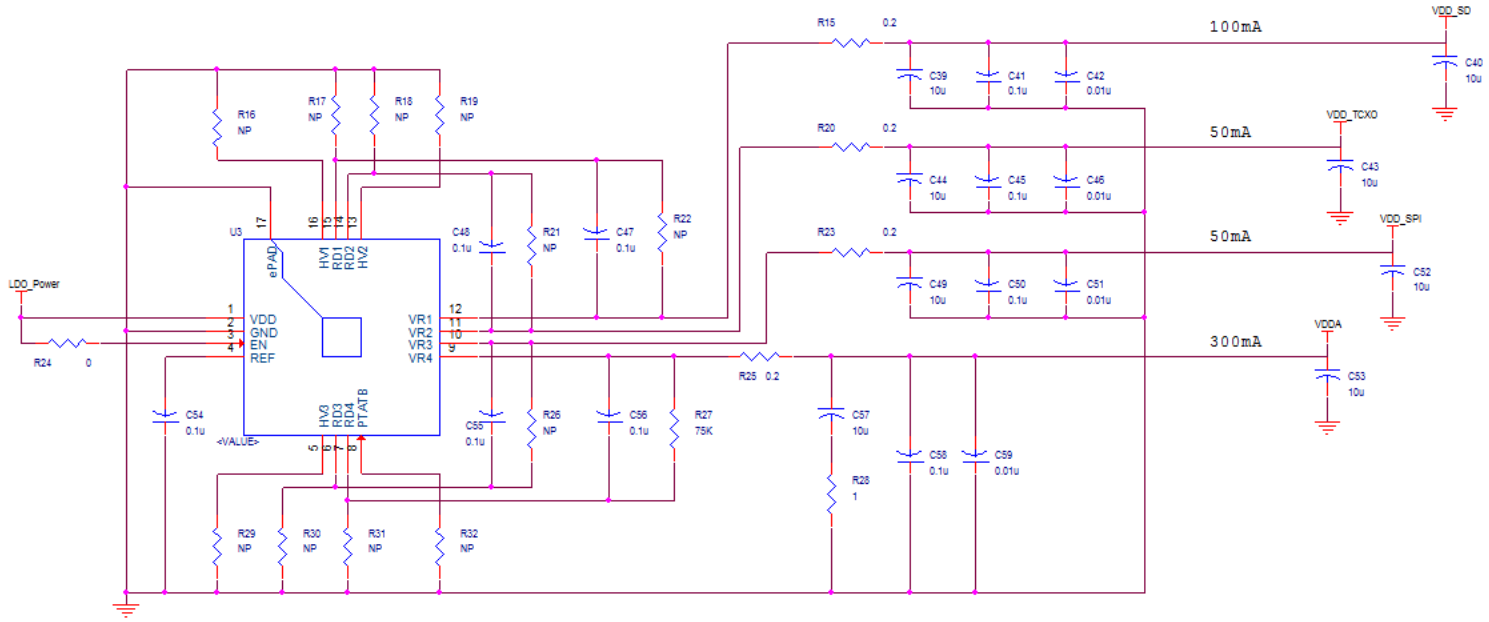
Figure 7. LDO Power Schematic



VDDA = V_CP, VDDA, V_VCO, VDDD

VDD_SPI = Translator, I2C PU, SPI PU

Figure 8. I2C-to-SPI Translation Schematic

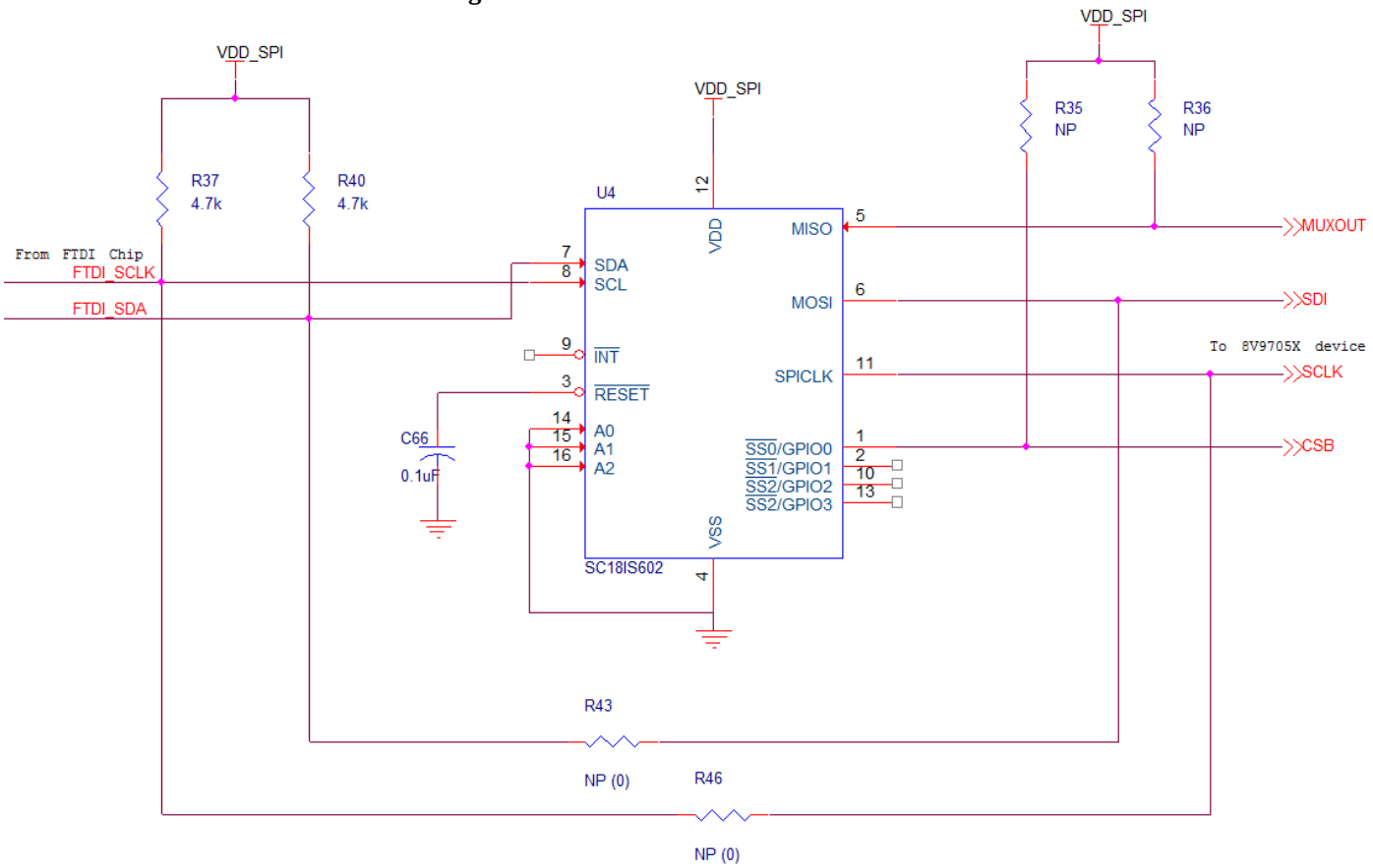


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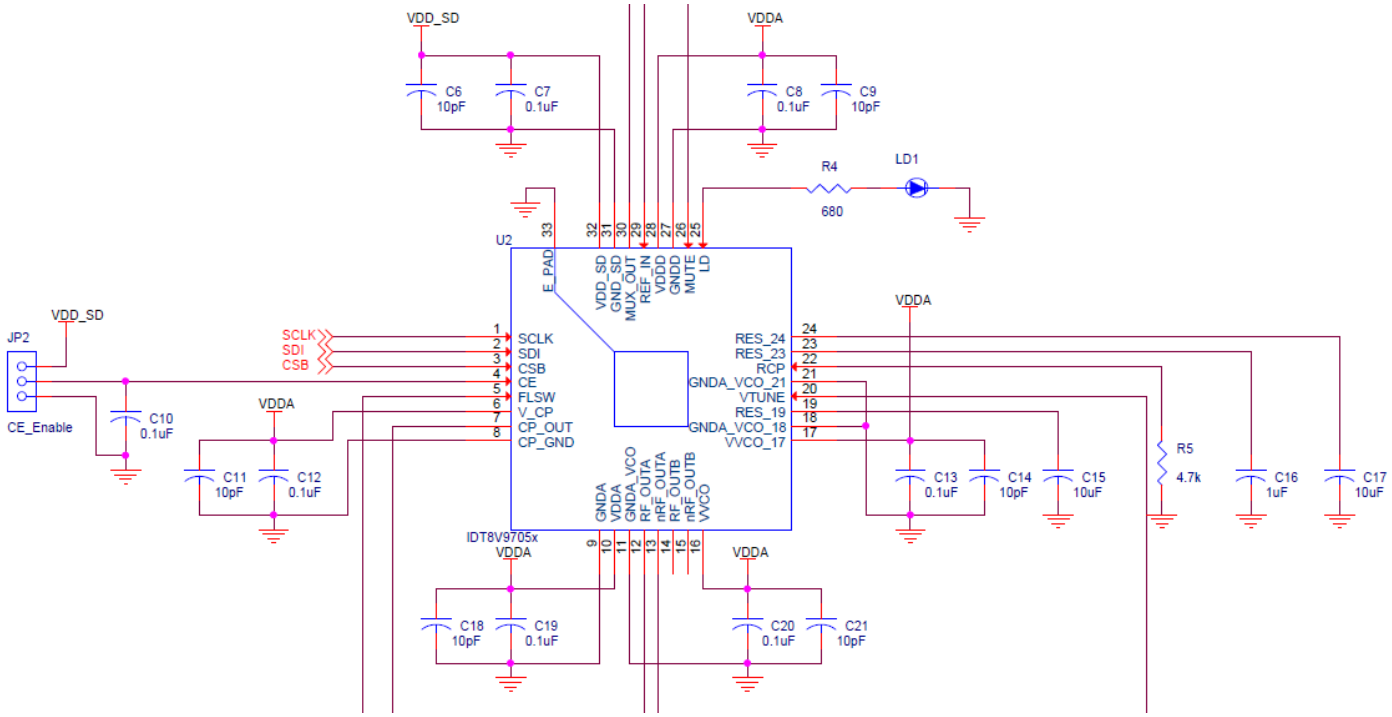
Figure 9. 8V9705x DUT Schematic

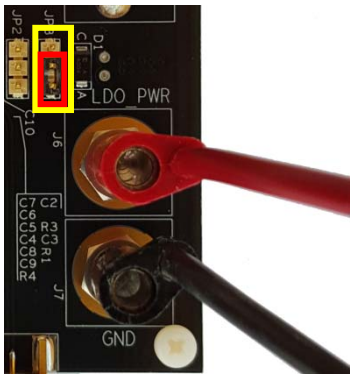


Powering from an External Supply

The evaluation board is by default configured to power through USB. (See JP3 jumper position in Fig. 1). To power the device from an external supply:

1) Set JP3 to the position shown in Figure 9.
2) Connect an external 4V supply to LDO_PWR (J6).
3) Connect the external supply Ground to GND (J7).

Figure 10. External Power Configuration



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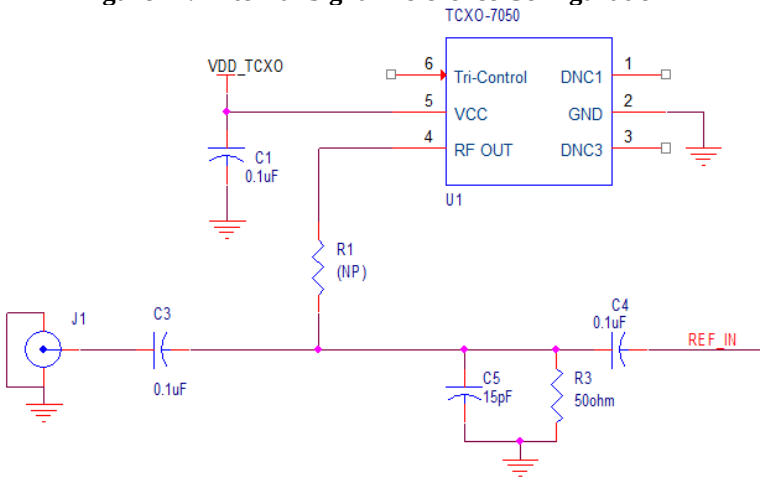
External Signal Reference Configuration

An on-board 25MHz TXCO provides the default source for RF_IN. In order to evaluate the device using an external signal reference, the following changes must be implemented:

1) Remove R20. This powers down the TXCO.
2) Remove R1. This disconnects the TXCO from the input path.
3) If the external signal can be ac-coupled, then populate C3=0.1uF. For dc termination to ground, C3=0ohm.
4) Populate R3=50ohm. This provides a termination for the input signal.
5) Replace C4=0.1uF. The input is ac-coupled into the device, which provides its own internal re-bias.
6) Connect the external signal reference to J1 using a 50-ohm cable.

Figure 11. External Signal Reference Configuration



DC Controls

JP1 MUTE control: RF_OUTA and RF_OUTB Power-Down. A logic low on this pin mutes the RF_OUT outputs and puts them in High-Impedance. This function is also SPI controllable and in this case also allows the power down of either RF_OUTA or RF_OUTB. This jumper can be left floating for normal operation.

JP2 Chip Enable: Powers down the device on logic Low, with charge pump put into a High-Impedance mode. Powers up the device on logic High. This jumper can be left floating for normal operation.

For more questions or support, feel free to contact us at clocks@idt.com

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