

CLK-104a/b Boards Using Renesas RF-PLL and RF-Synthesizer Solutions

Renesas collaborated with AMD to design a version of the CLK-104 board to work with AMD’s platform for RF SoC solutions. The CLK-104 board uses an RF-PLL device to provide a reference for up to 12 RF clocks, including one for an onboard RF-synthesizer device, and the 8V97003 as a reference clock to generate two output clocks up to 18GHz for ADC/DAC applications. Two versions of the CLK-104 boards are available: the CLK-104a uses an RF-PLL device with the 8V19N491-24, and the CLK-104b uses the 8V19N882. The rest of the design is identical for both versions.

The CLK-104 is designed as a plug-in module to the AMD ZCU-1275 (16×16) platform. By plugging in to the mainboard socket, the CLK-104 acquires power supplies, an I2C/SPI interface, and input reference clocks. The following figure shows the bottom of the CLK-104 board with a male connector to match with ZCU-1275 board. For information on how to operate and access the CLK-104 board, see the *ZCU-1275 User Manual*.



Figure 1. Back of CLK-104 Board with Mating Connector with AMD ZCU-1275

The CLK-104 board is designed to function as a standalone testing platform. For more information, see the following sections.

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1. System Overview

The CLK-104 board consists an RF-PLL device (8V19N491-24 or 8V19N882) and two RF-synthesizer devices (2x 8V97003). RF-PLL device can take one of the following three reference clocks as inputs to its CLK0/nCLK0 and CLK1/nCLK1 (both are differential inputs):

- 156.25MHz from AMD RF SoC (ZCU-1275) board through above-mentioned connector
- An onboard 10MHz TCXO
- An external clock connected to SMA connectors

The RF-PLL devices generate the following output clocks:

- A differential output for RF-synthesizer #1
- A differential output for RF-synthesizer #1
- A differential output for RF-synthesizer #2
- A differential output to a pair of onboard SMA connectors for monitoring
- 6 differential outputs connecting to ZCU-1275 board (through the connector)

A diagram of the CLK-104 board is displayed below.

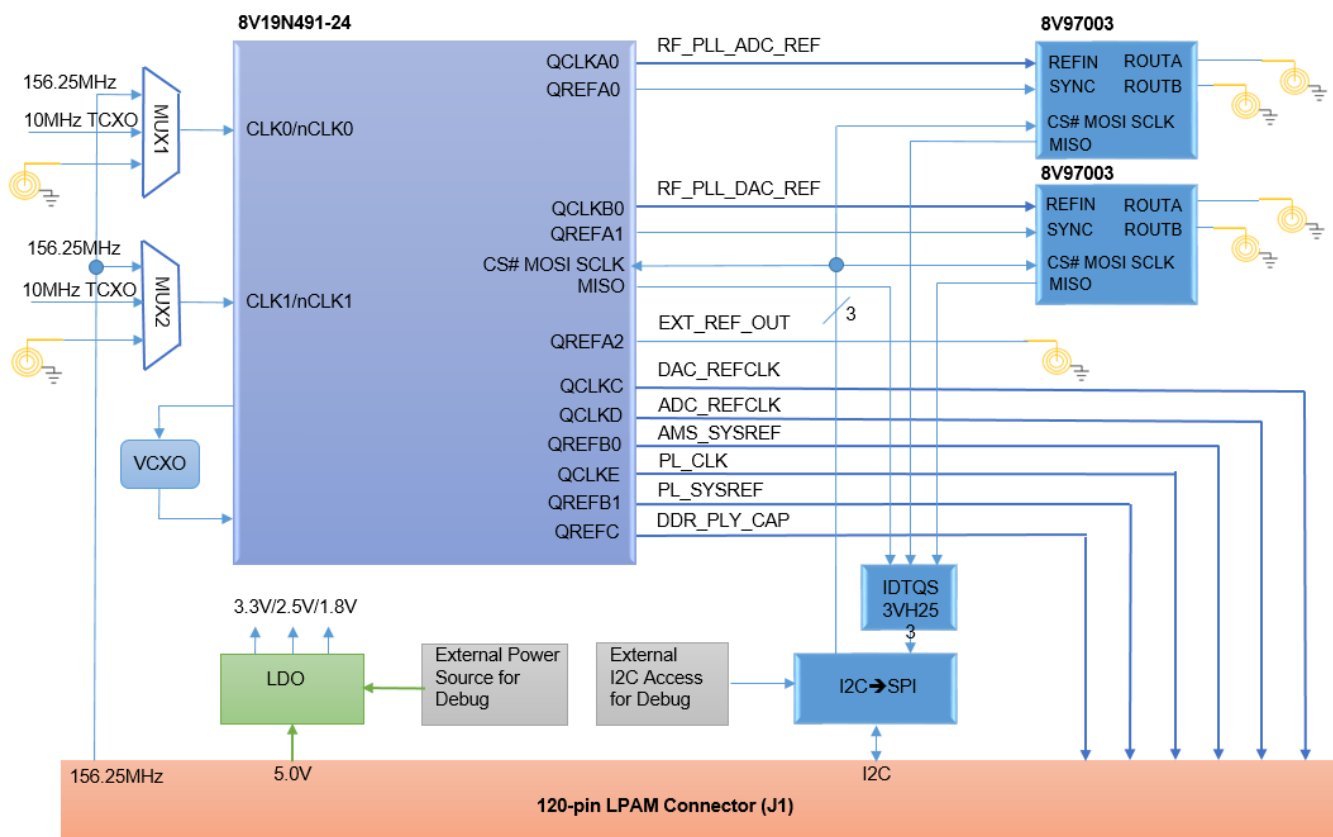


Figure 2. CLK-104 Board Diagram

The RF-PLL device and two RF-synthesizer devices are accessible by an SPI interface. As stated above, they can be accessed by an I2C-to-SPI converter from/to the ZCU-1275 board. The I2C signals are within the mating connector between the two boards. Please note that the SPI port has been connected to an onboard 5 × 2 header by which an external SPI master can access all devices on CLK-104 board.

The CLK-104 board can be powered locally or by plugging it into the ZCU-1275. For more information, see “Standalone Testing.”

2. Standalone Testing

If an AMD ZCU-1275 board is not available, the CLK-104 board can be tested standalone. To conduct a standalone test or evaluation, complete the following steps and information below.

2.1 Power Supply

The connector between the CLK-104 and ZCU-1275 contains +5V, +3.3V, and ground pins that provide power supplies to the CLK-104 board when plugged in. Copper pads are available on the CLK-104 board to facilitate the power supplies coming from a bench power supply. Solder a thick wire on these pads and connect +5V, +3.3V, and GND to a bench power supply. For the locations of these copper pads, see Figure 3.

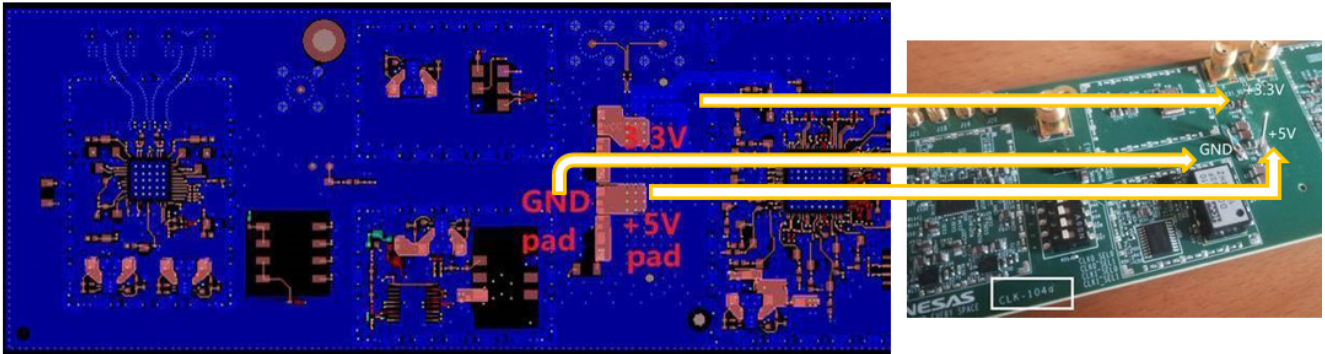


Figure 3. +5V, +3.3V, and GND Copper Pads are Provided for Local Power Supplies

3. SPI Interface

The 5 × 2 header is installed to make connections between an external SPI master to the devices on the CLK-104 board. Use an FTDI dangle (C232HM) to connect the SCLK, SDI, SDO, and nCS signals as labelled in the header below.

Note: Jump J4, J5, or J6 one at a time to access one of three devices on the board.

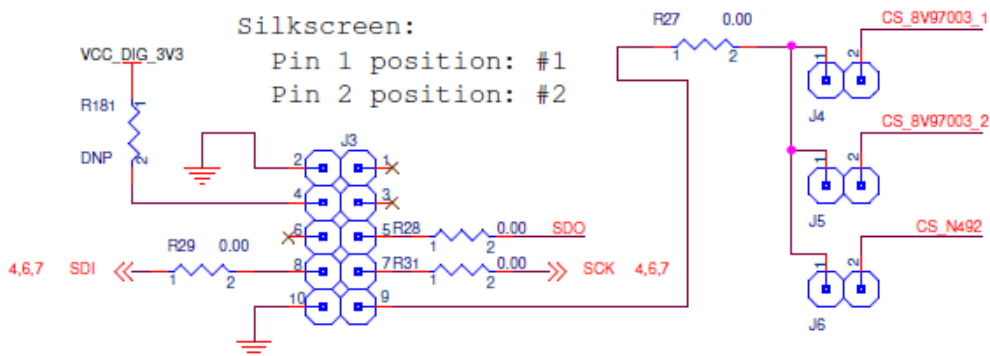


Figure 4. SPI Header for Connecting to 8V19N491-24 or 2x 8V19N882 One at a Time

4. Input Reference Selection

A 4-bit dip-switch (J11) is used to select one of three available reference clocks for the two input clocks of the RF-PLL (8V19N491-24 or 8V19N882). Two mux devices are used so the two input clocks going to the RF-PLL device can be selected individually (see Dipswitch selection pin allocation below).

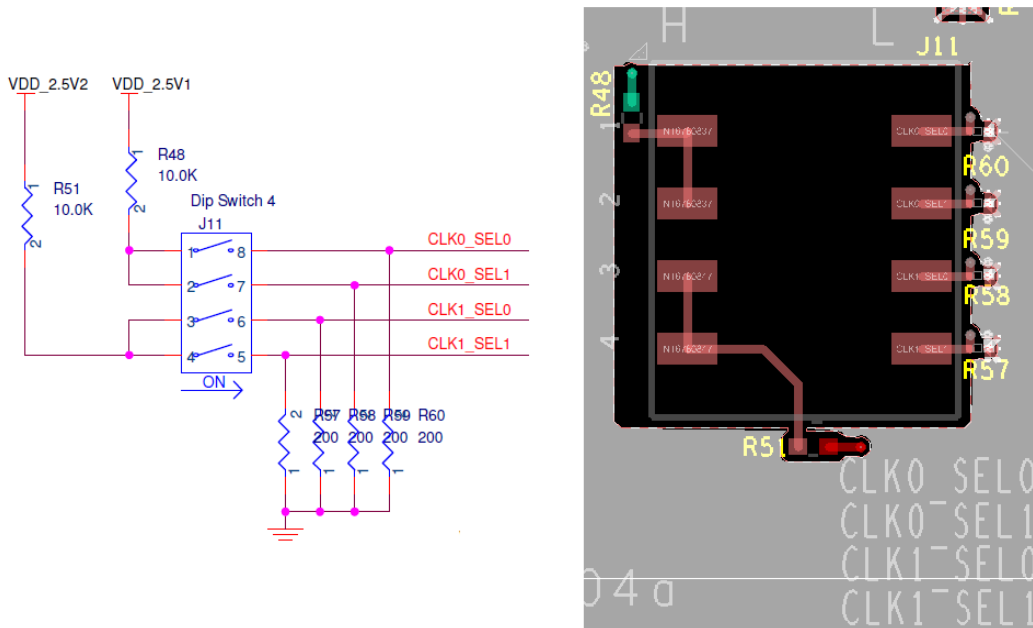


Figure 5. Dip-Switch to Individually Select an Input Reference for CLK0/nCLK0 and CLK1/nCLK1

Follow onboard silkscreen labels for “H” or “L” position (see Figure 5) for the Dipswitch (J11) pins. The reference selection table is as follows.

Table 1. Reference Selections for RF_PLL Inputs (CLK0/nCLK0 and CLK1/nCLK1)

Destination	CLK0_SEL0 Pin	CLK0_SEL1 Pin	Reference Selected
CLK0_P/N	H	H	X
	H	L	SMA_IN
	L	H	TCXO_IN
	L	L	SFP_RCV_CK_P/N
	CLK1_SEL0 Pin	CLK1_SEL1 Pin	
CLK1_P/N	H	H	SFP_RCV_CK_P/N
	H	L	TCXO_IN
	L	H	SMA_IN
	L	L	X

5. Using Timing Commander to Program the Devices

For ease of use, Renesas' free-of-charge software tool – Timing Commander is recommended to configure and program the CLK-104 board/devices (8V19N491-24, 8V19N882, and 8V97003). If you have any questions on the Timing Commander software download or TCP/TCS files, contact Renesas Timing Technical Support via Renesas.com

In the Timing Commander GUI, when the settings file (.tcs) is loaded:

1. Click on the button in the upper-right corner to display the Connection Settings window.



2. Select USB/SPI in the Connection Settings window.

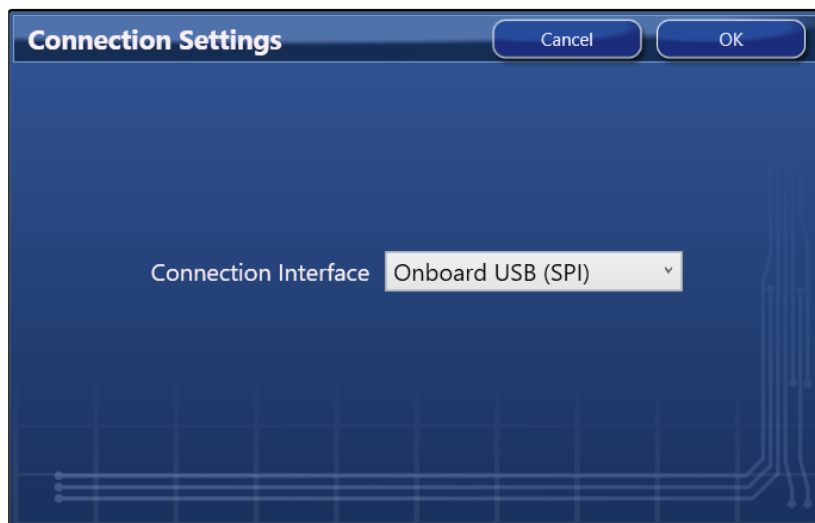


Figure 6. Connection Setting window to select SPI mode

3. Click the chip symbol button in the upper-right corner of the GUI to initiate the connection to the targeted device.

6. Output Clock Monitoring/Measurement

The following SMA connector pairs are available to monitor/measure the output frequencies from devices on the CLK-104 board:

- J15/J16 – 8V97001 #1 Output A
- J14/J17 – 8V97001 #1 Output B
- J19/J20 – 8V97001 #2 Output A
- J18/J21 – 8V97001 #2 Output B
- J12/J13 – 8V19N491-24 Output QREF_A2/nQREF_A2

Other outputs are connected to the connector, and therefore, are not accessible.

6.1 Example 1: Phase Noise Plot from J12/J13 (122.88MHz)

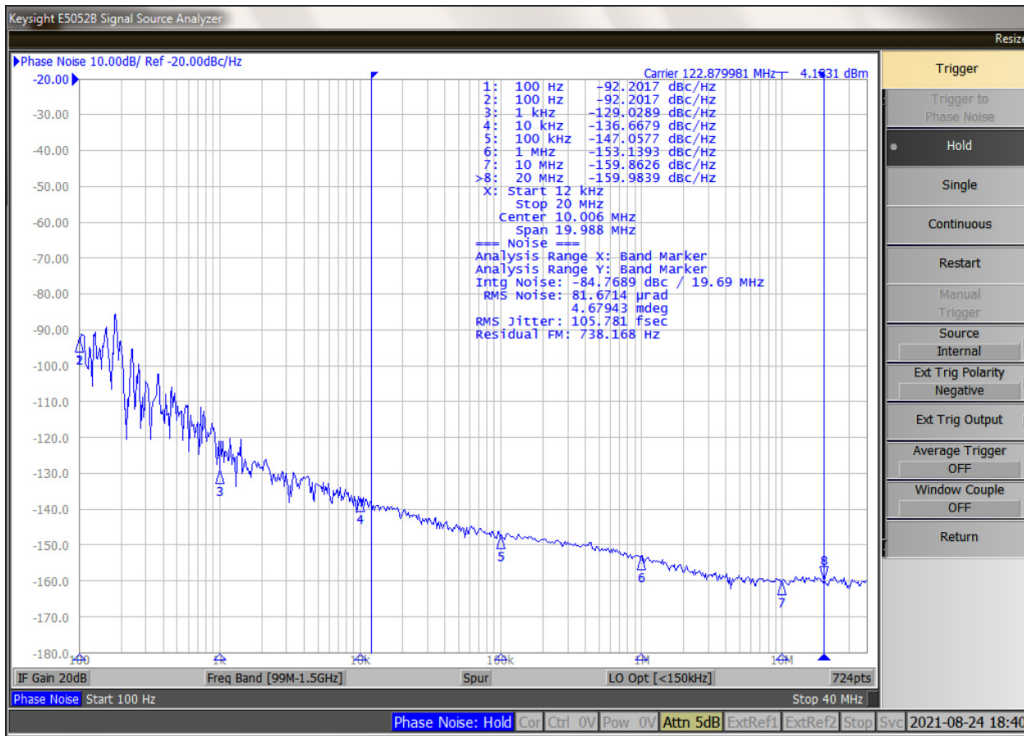


Figure 7. Phase Noise Plot of 122.88MHz Output from 8V19N491-24 QREF_A2/nQREF_A2

6.2 Example 2: Phase Noise Plot from 8V97003 #1 (1GHz)

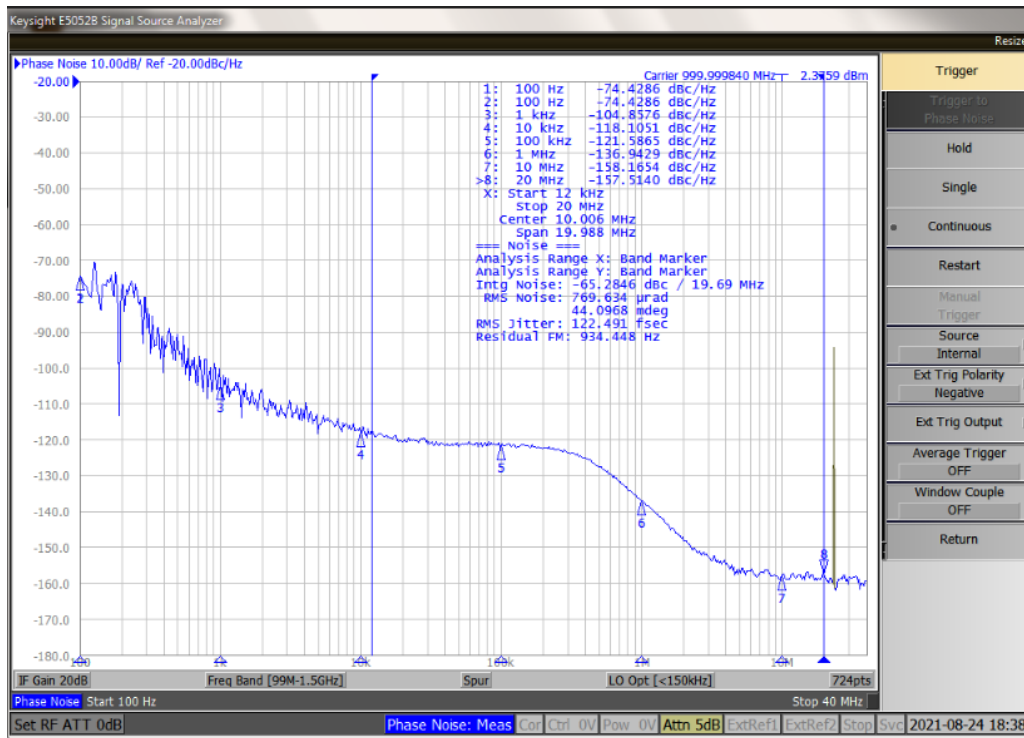


Figure 8. Phase Noise Plot of 1000MHz Output from 8V97002 #1 ROUT_A/nROUT_A

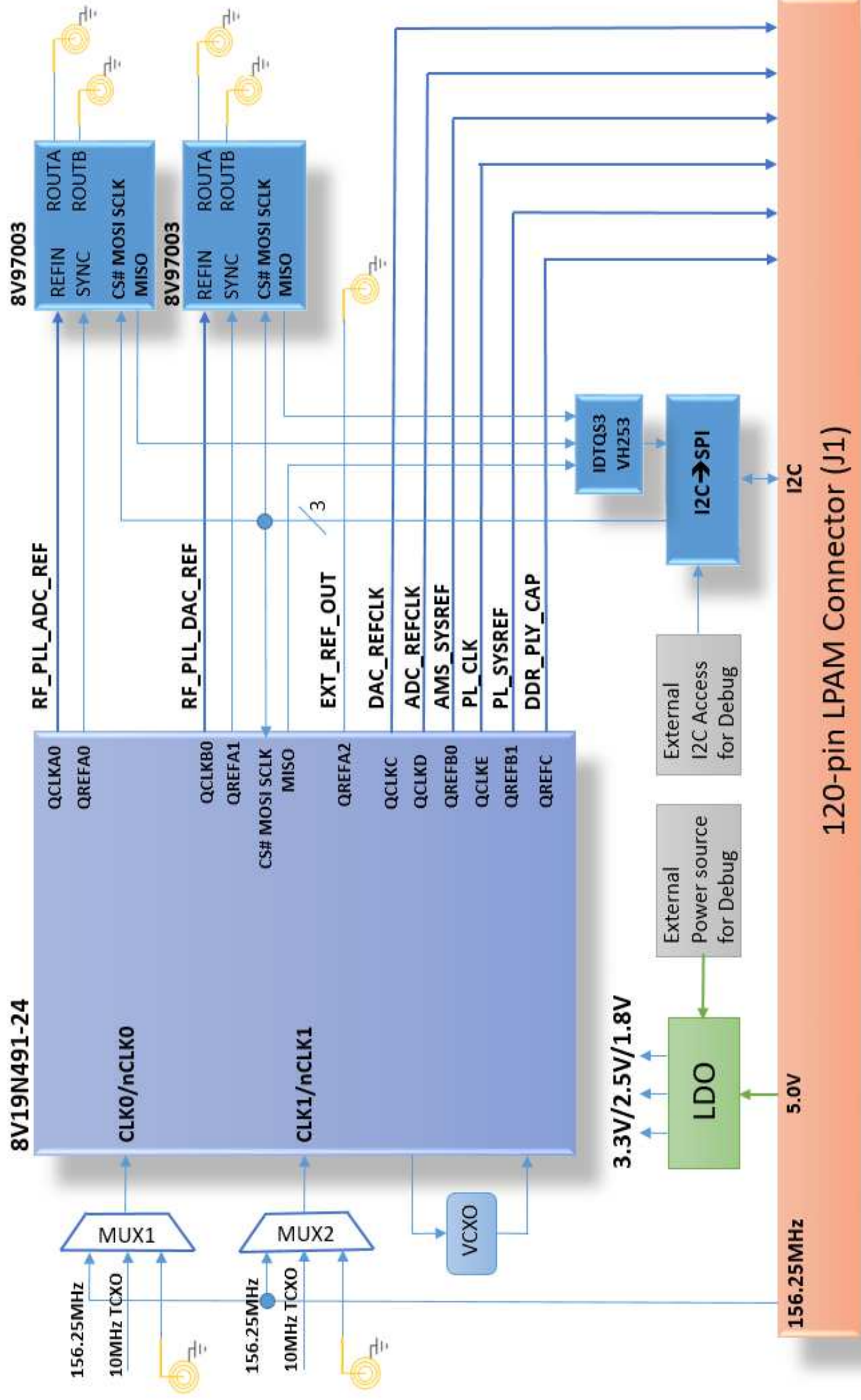
7. Board Schematics

The board schematics are located at the end of this document.

8. Revision History

Revision	Date	Description
1.01	Jul 22, 2024	<ul style="list-style-type: none">▪ Replaced all instances of Xilinx with AMD.▪ Updated schematics.
1.00	Nov 26, 2021	Initial release.

CLK-104 RF CLOCK BLOCK DIAGRAM



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Title: CLK-104

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B	Date: 07/16/2024	Sheet: 1 of 11	A

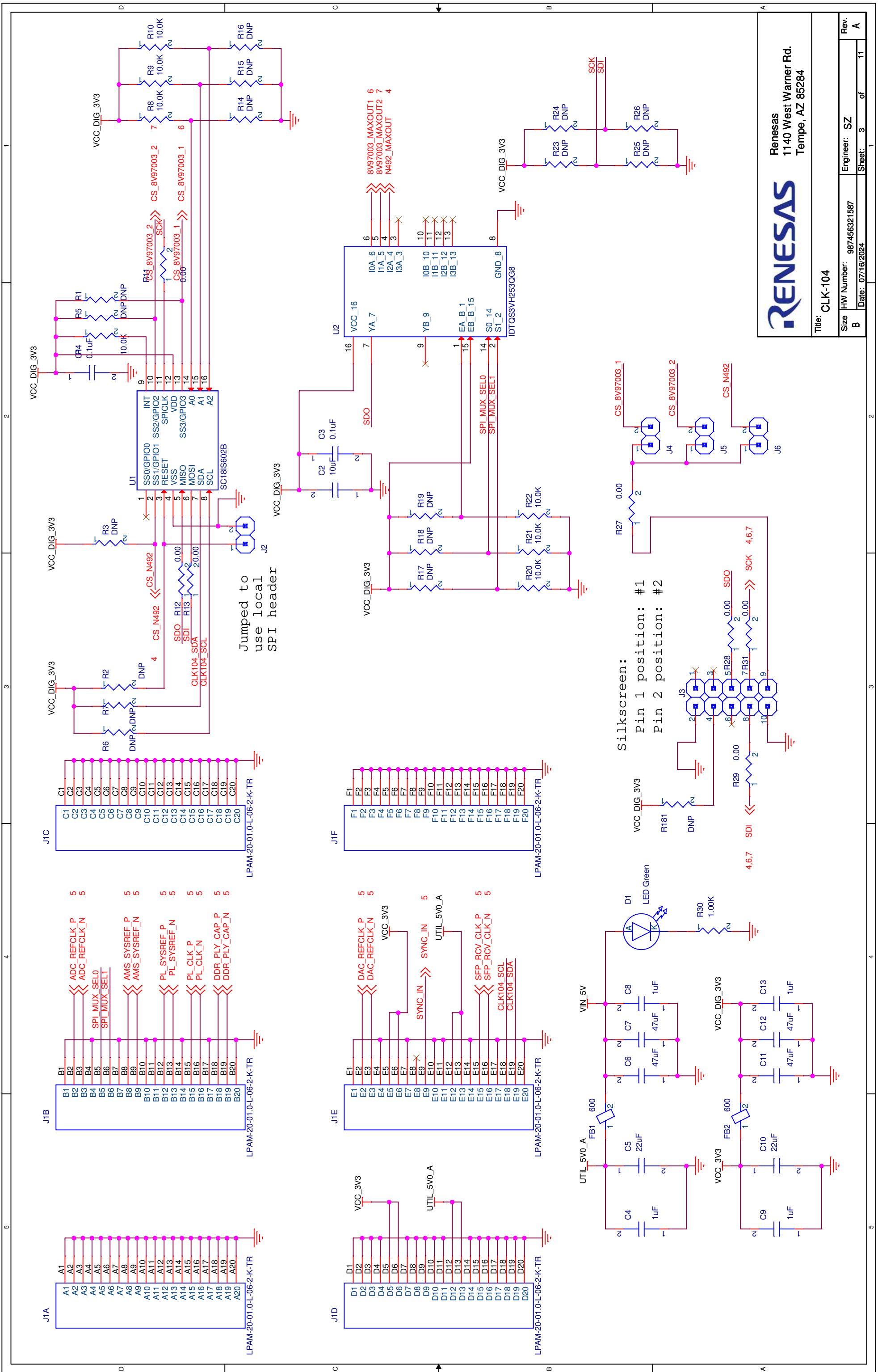
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A	CLK-104 INITIAL DRAFT	12/10/2020	SZ
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Title: CLK-104

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Date: 07/16/2024	Sheet: 2	of 11	A

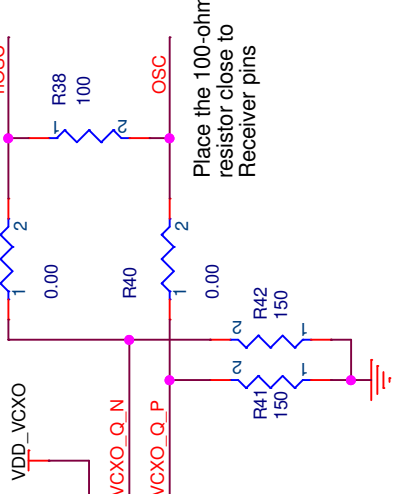
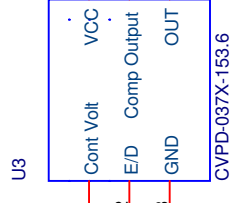
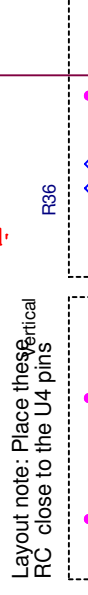
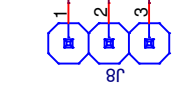
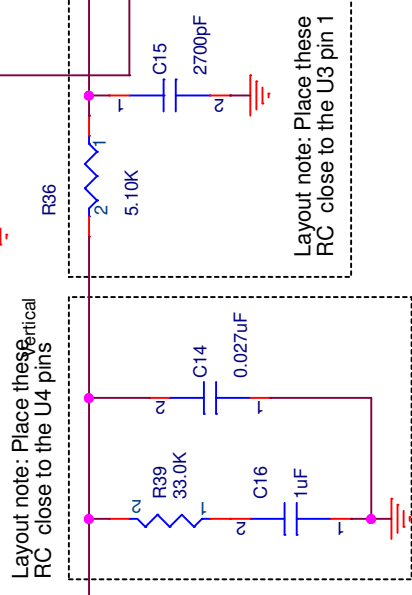
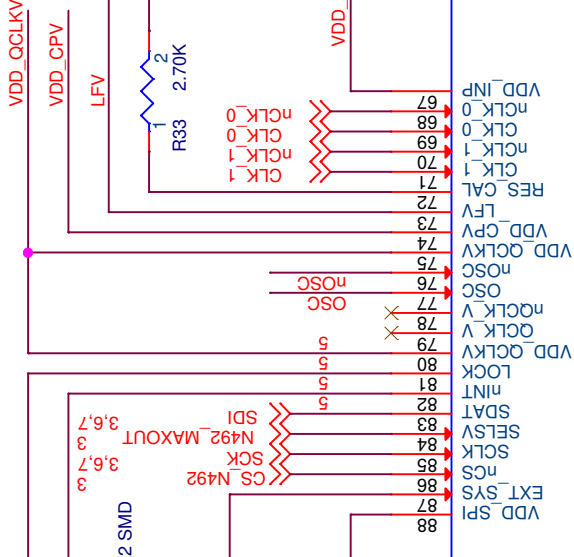
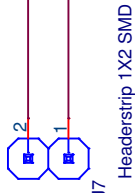


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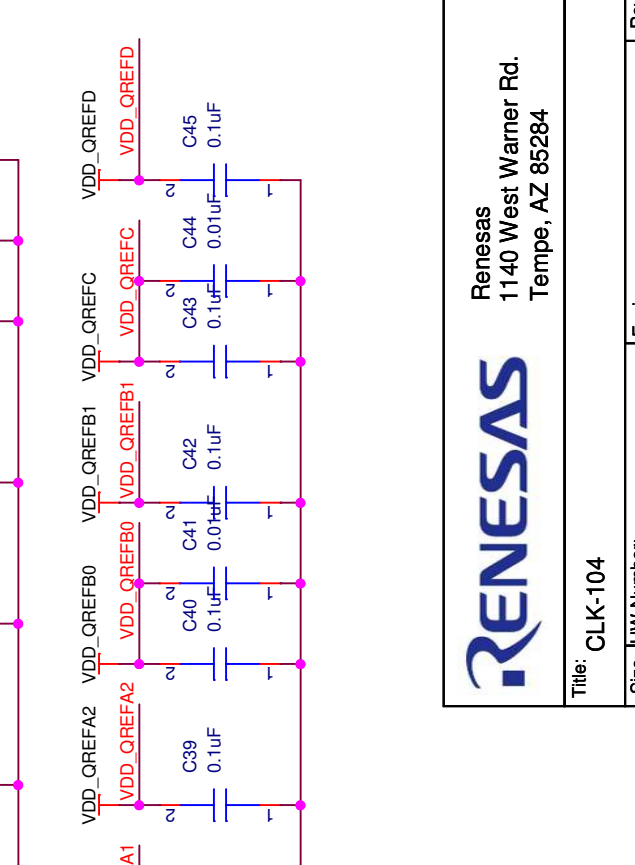
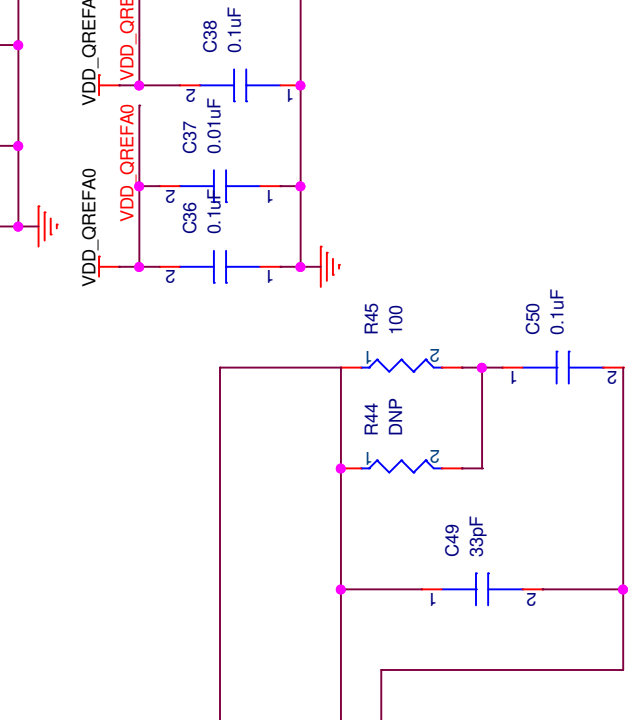
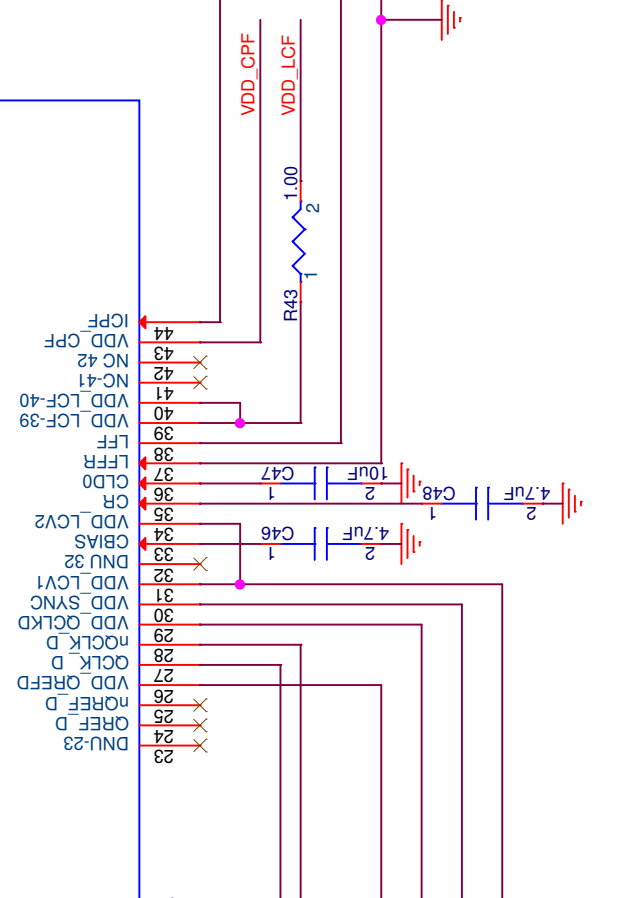
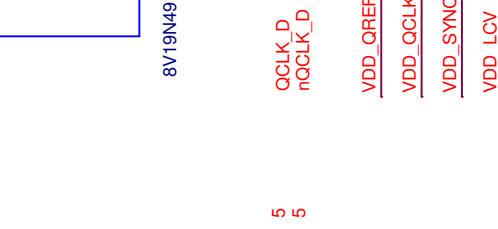
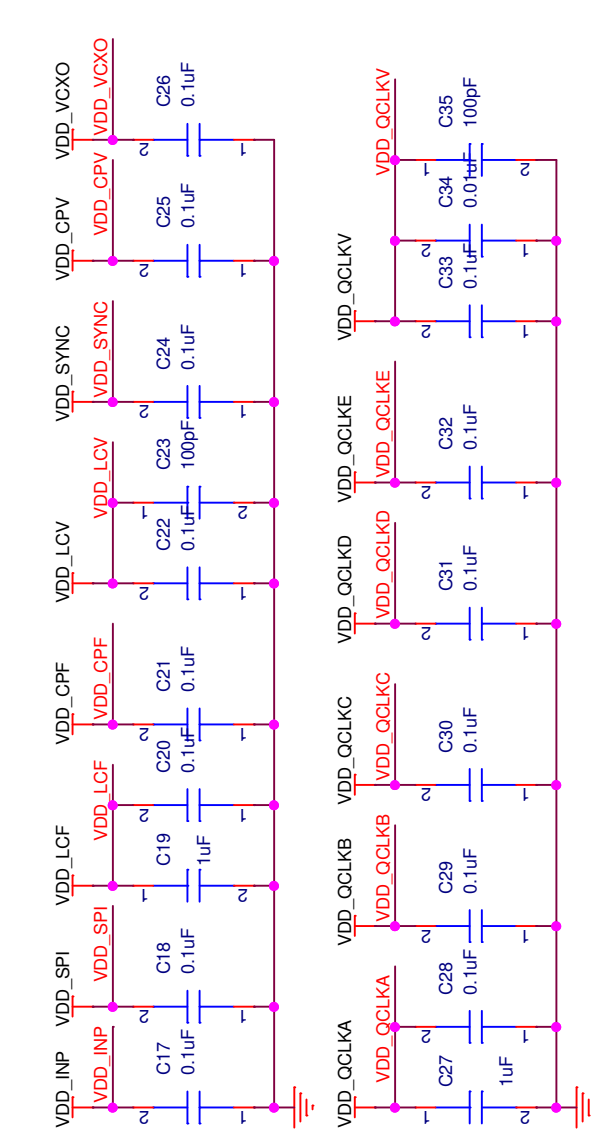
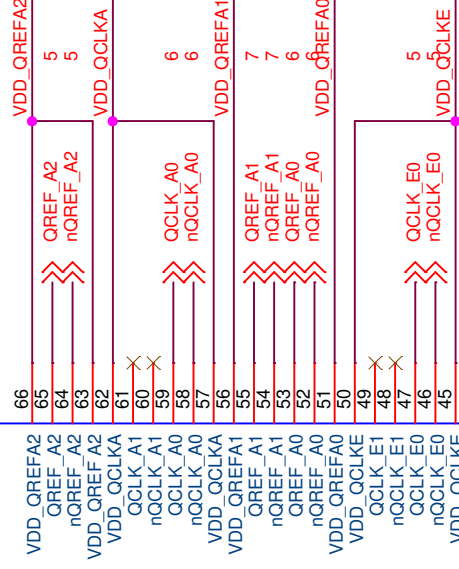
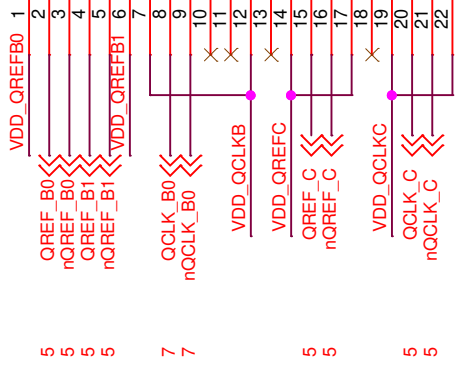
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Rev.	A	Date:	07/16/2024	Sheet:	3 of 11

Silkscreen: LOCK
Silkscreen: nINT



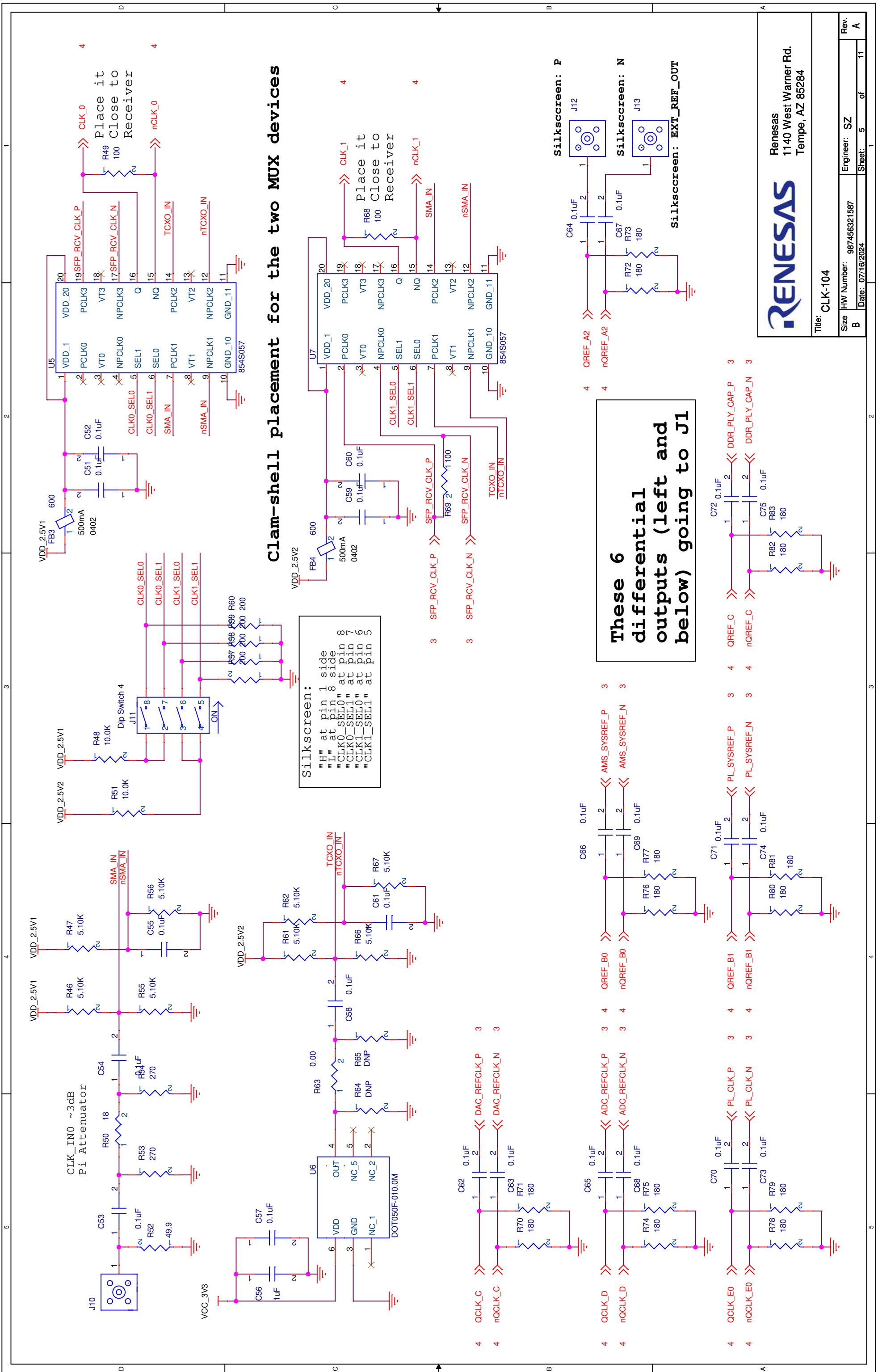
Place the 100-ohm resistor close to Receiver pins



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Clam-shell placement for the two MUX devices

Silkscreen:
 "H" at pin 1 side
 "L" at pin 8 side
 "CLK0_SEL0" at pin 8
 "CLK0_SEL1" at pin 7
 "CLK1_SEL0" at pin 6
 "CLK1_SEL1" at pin 5

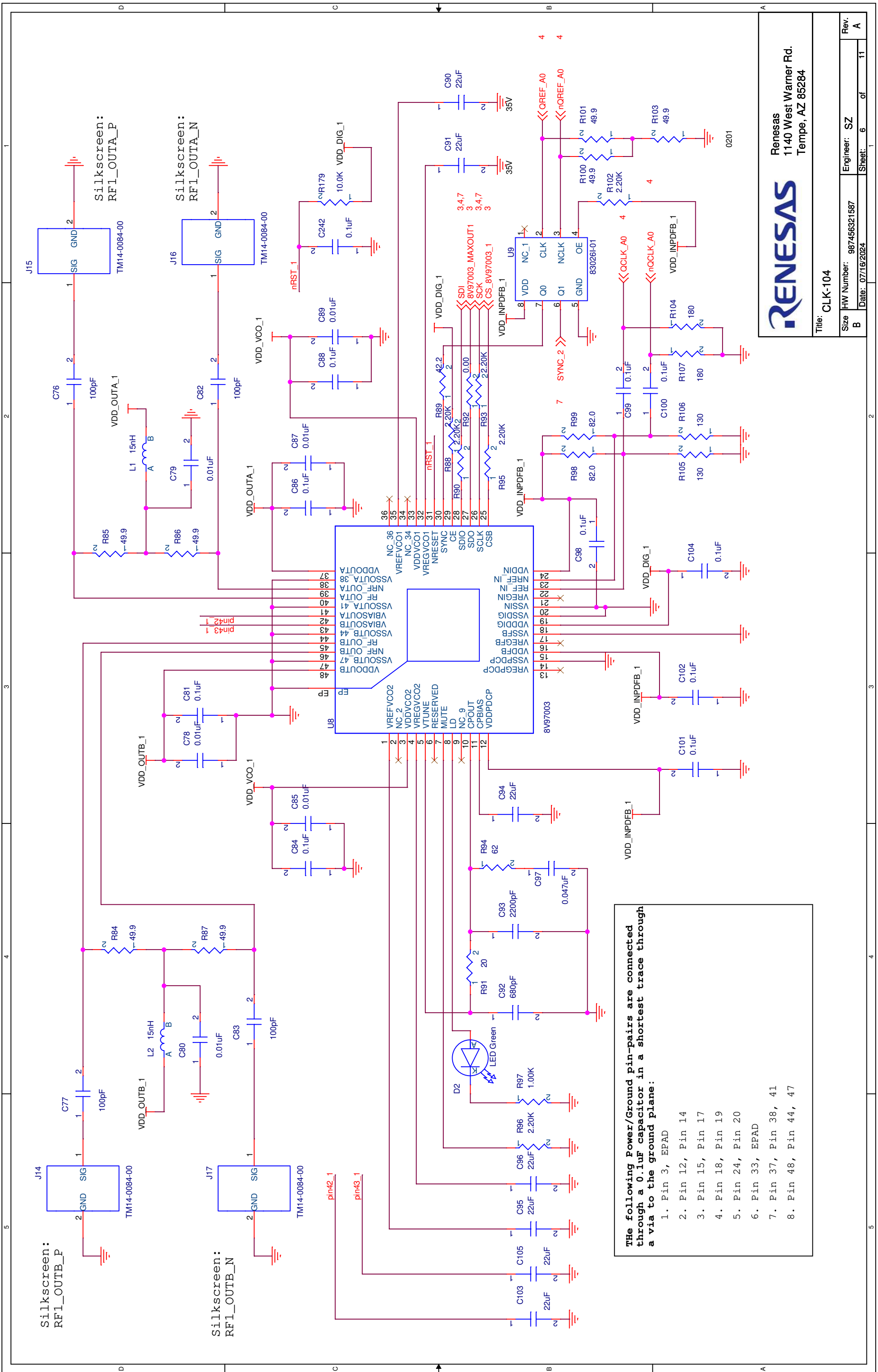
These 6 differential outputs (left and below) going to J1



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The following Power/Ground pin-pairs are connected through a 0.1uF capacitor in a shortest trace through a via to the ground plane:

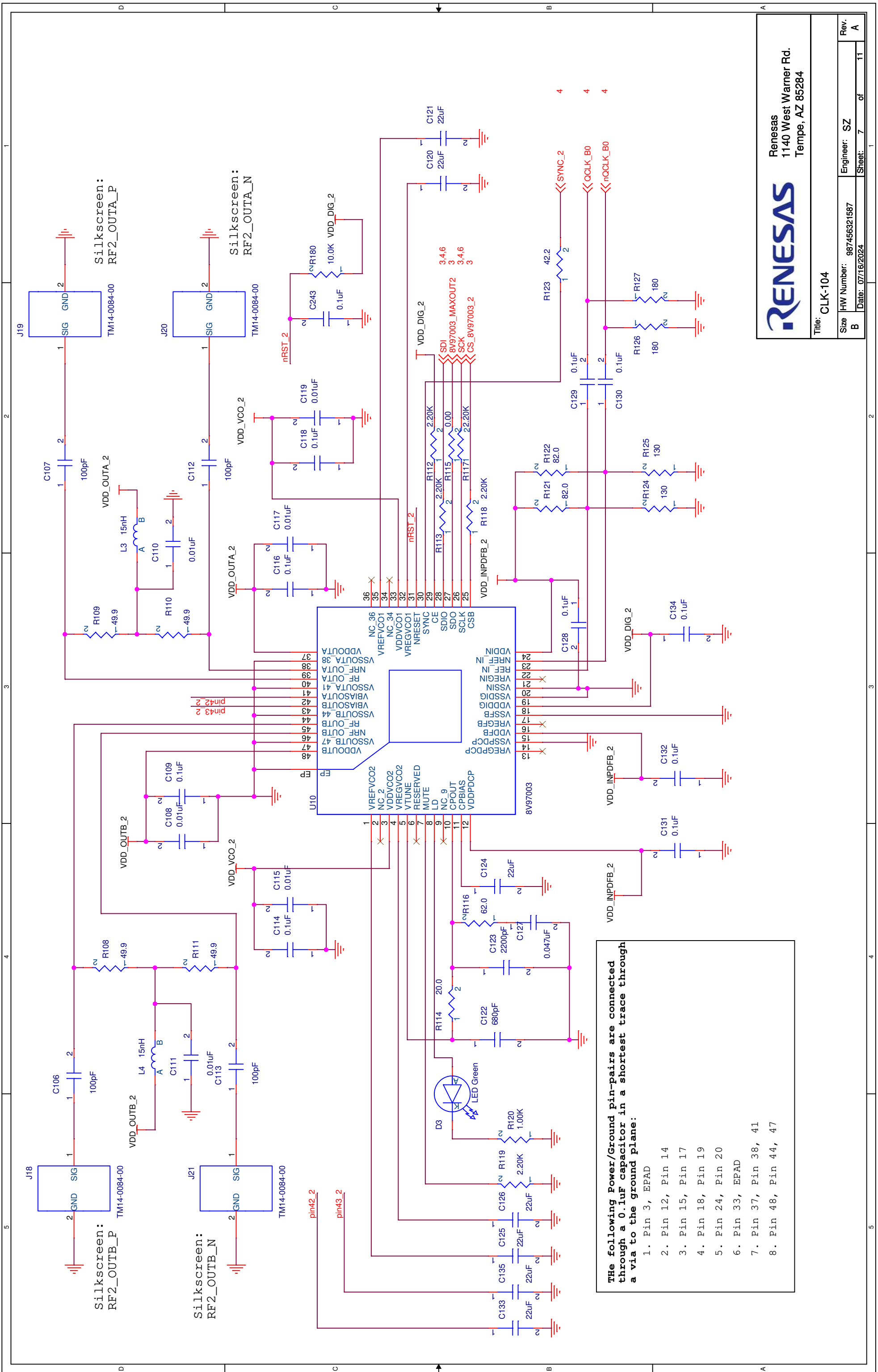
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2. Pin 12, Pin 14
3. Pin 15, Pin 17
4. Pin 18, Pin 19
5. Pin 24, Pin 20
6. Pin 33, EPAD
7. Pin 37, Pin 38, 41
8. Pin 48, Pin 44, 47



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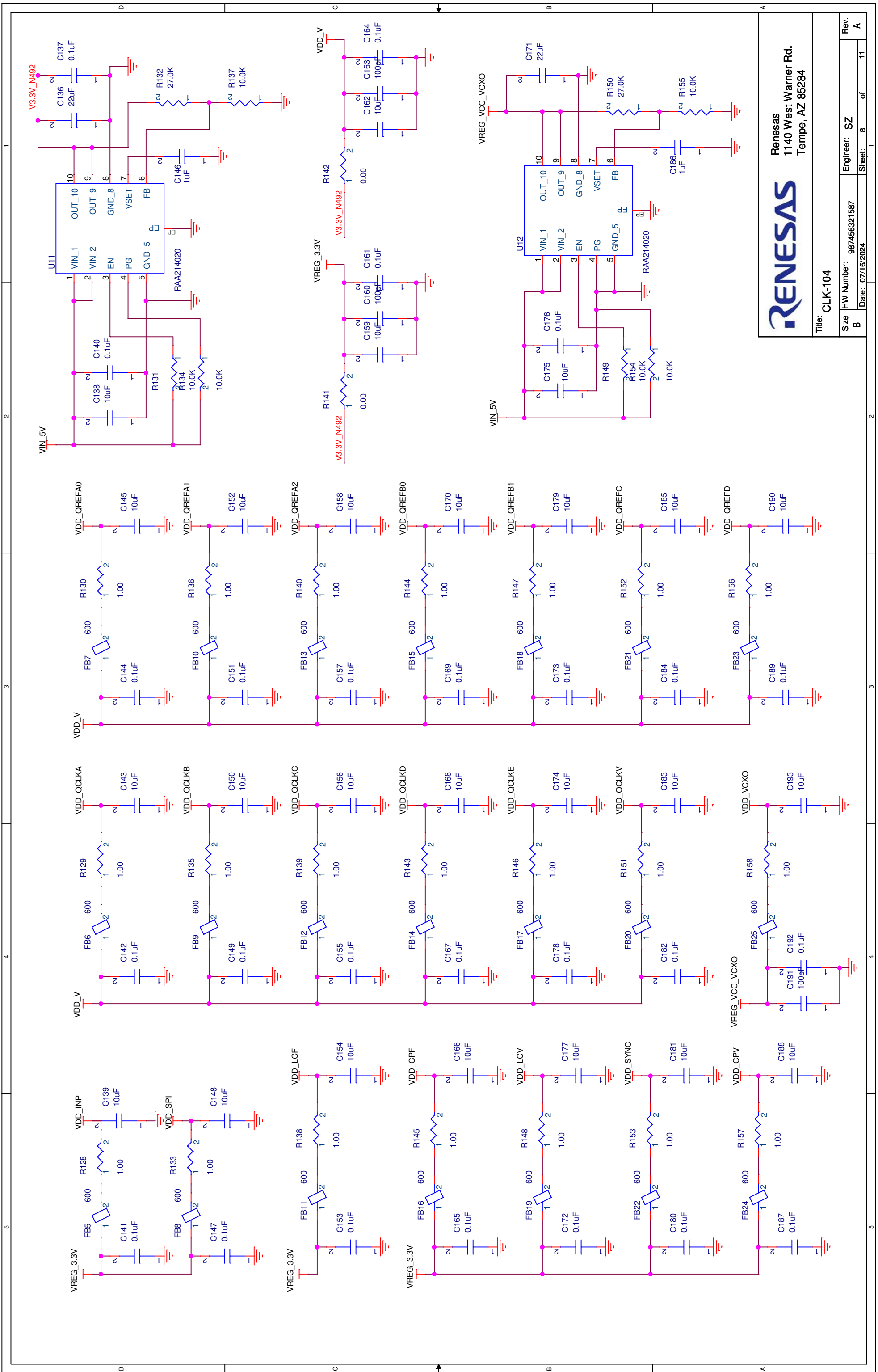
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Date:	07/16/2024	Sheet:	6	of	11		



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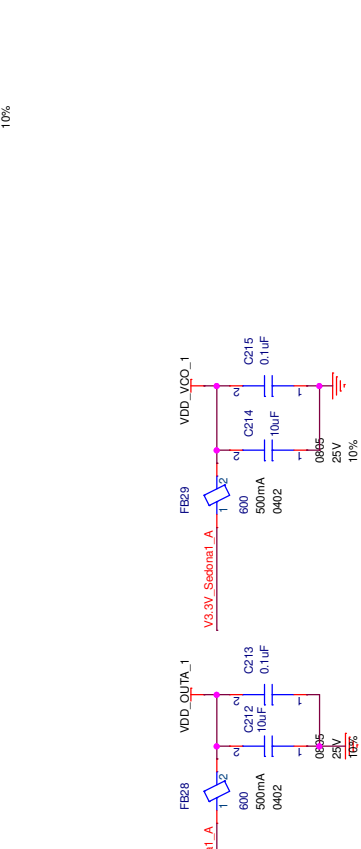
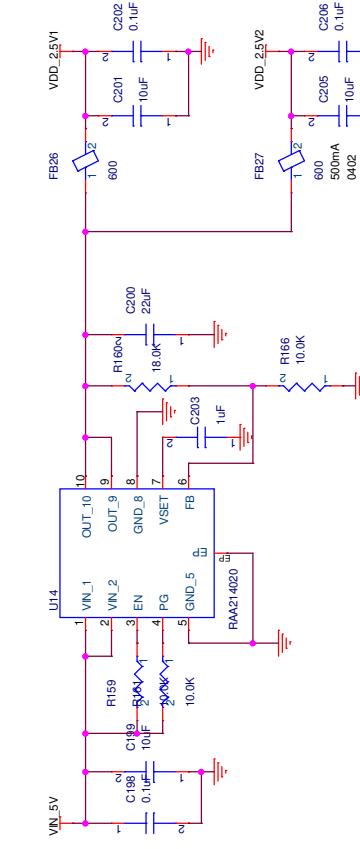
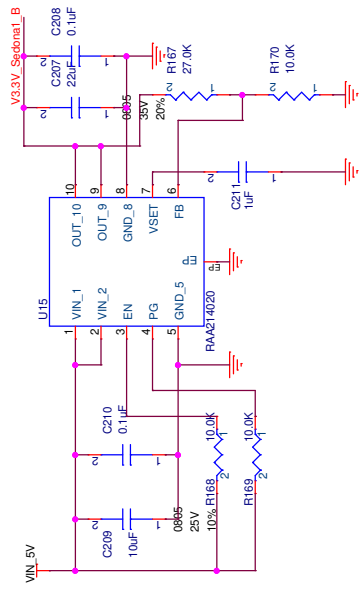
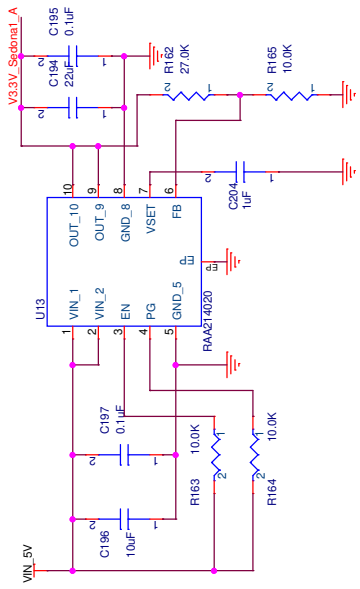
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2. Pin 12, Pin 14
3. Pin 15, Pin 17
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6. Pin 33, EPAD
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8. Pin 48, Pin 44, 47



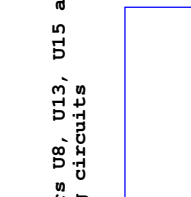
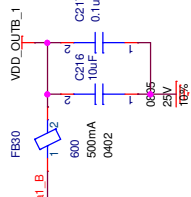
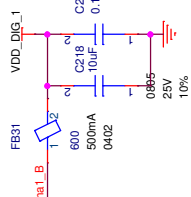
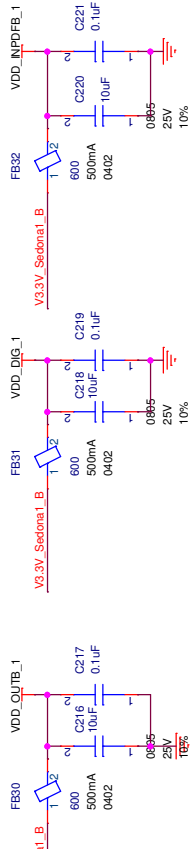
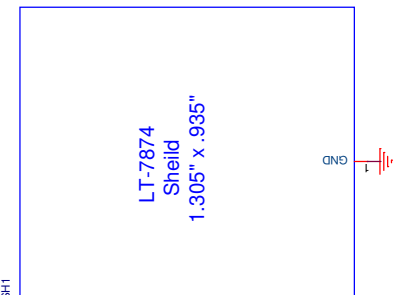
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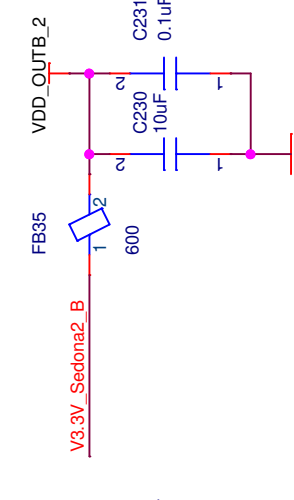
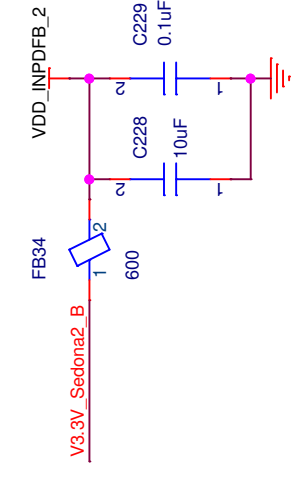
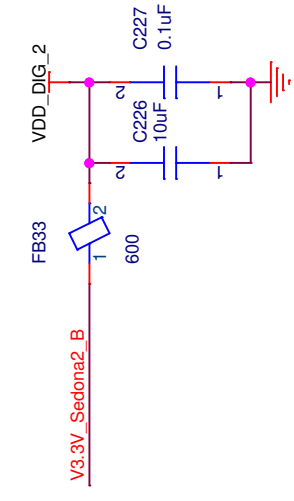
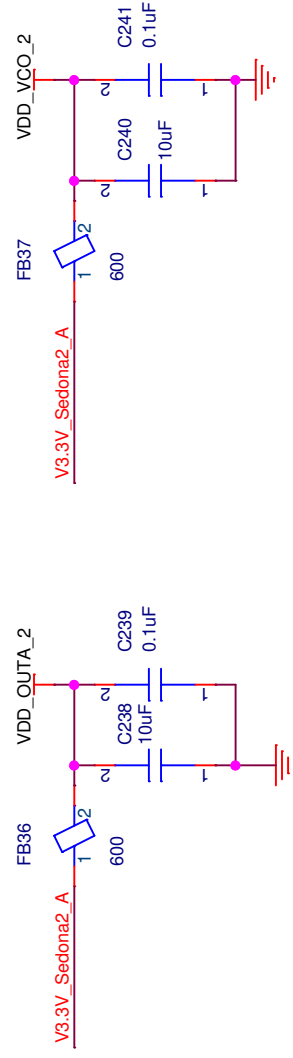
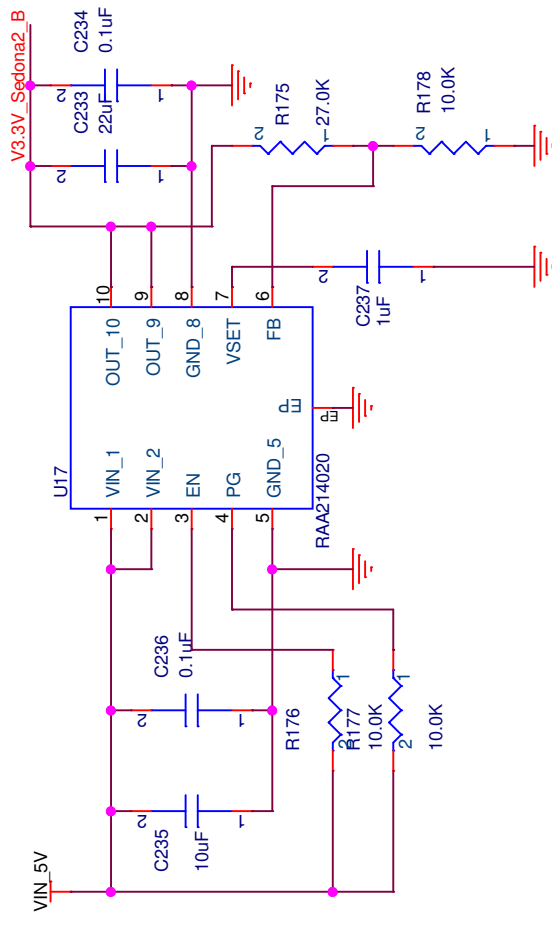
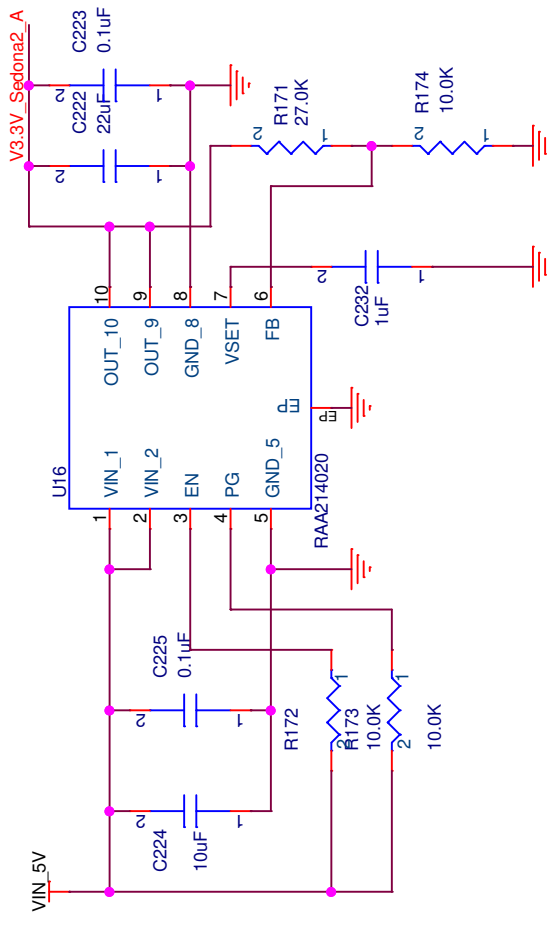
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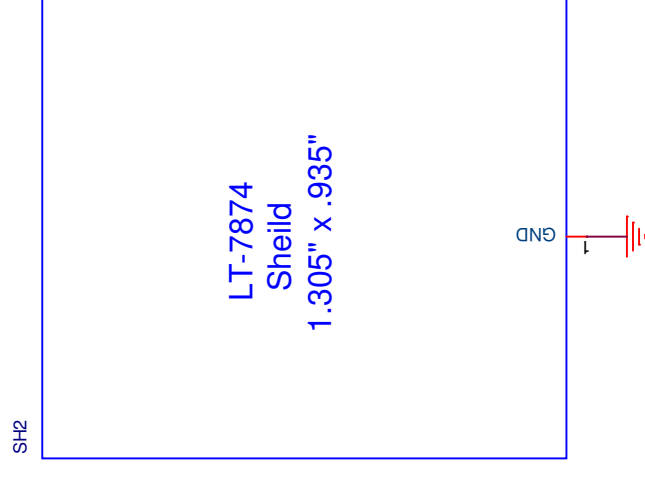


SH1 covers U8, U13, U15 and its filtering circuits





SH2 covers U10, U16, U17 and its filtering circuits

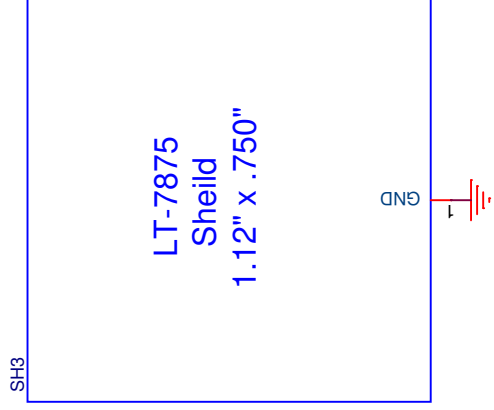


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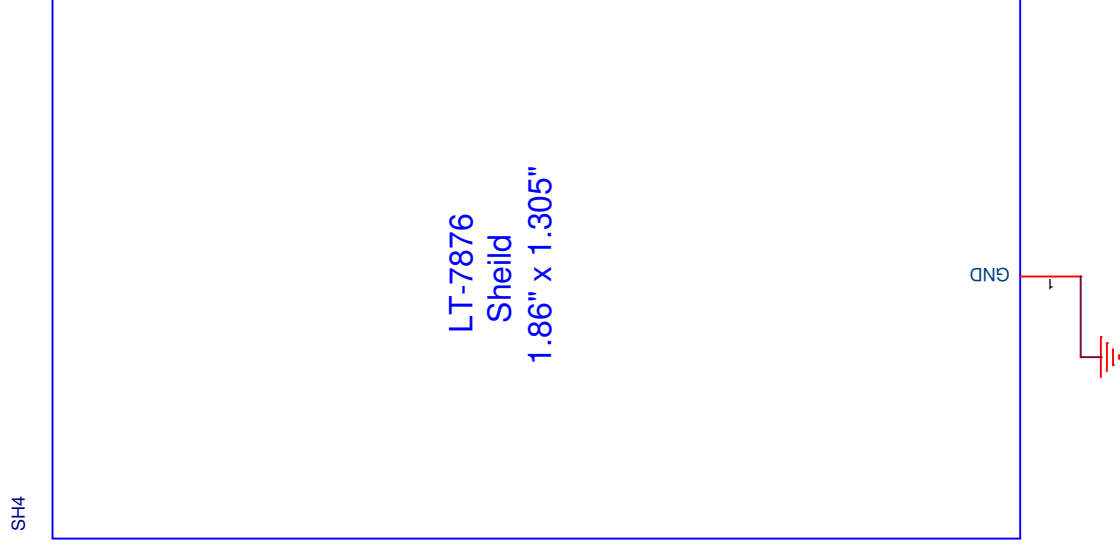
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Date:	07/16/2024	Sheet:	10 of 11

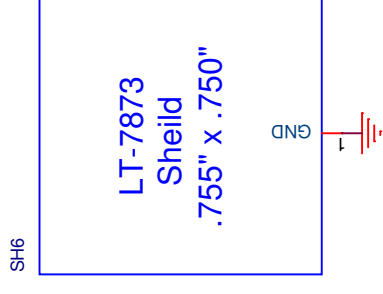
SH3 covers U3, and U12 and its surrounding components and circuits



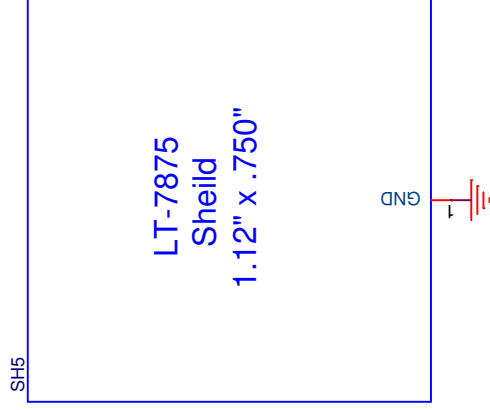
SH4 covers U4, U11 and its respective surrounding circuits



SH6 covers U1 its surrounding components and circuits



SH5 covers U6 its surrounding components and circuits



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