

Quick Start

DEMO DA1x01D Demonstration Board for DAC1401D125

Rev. 2.0 — 2 June 2012

Quick Start

Document information

Info	Content
Keywords	DEMO DA1x01D, PCB2055-1, Demonstration board, DAC, Converter, DAC1401D125
Abstract	This document describes how to use the demonstration board DEMO DA1x01D for the digital-to-analog converter DAC1401D125.

Overview



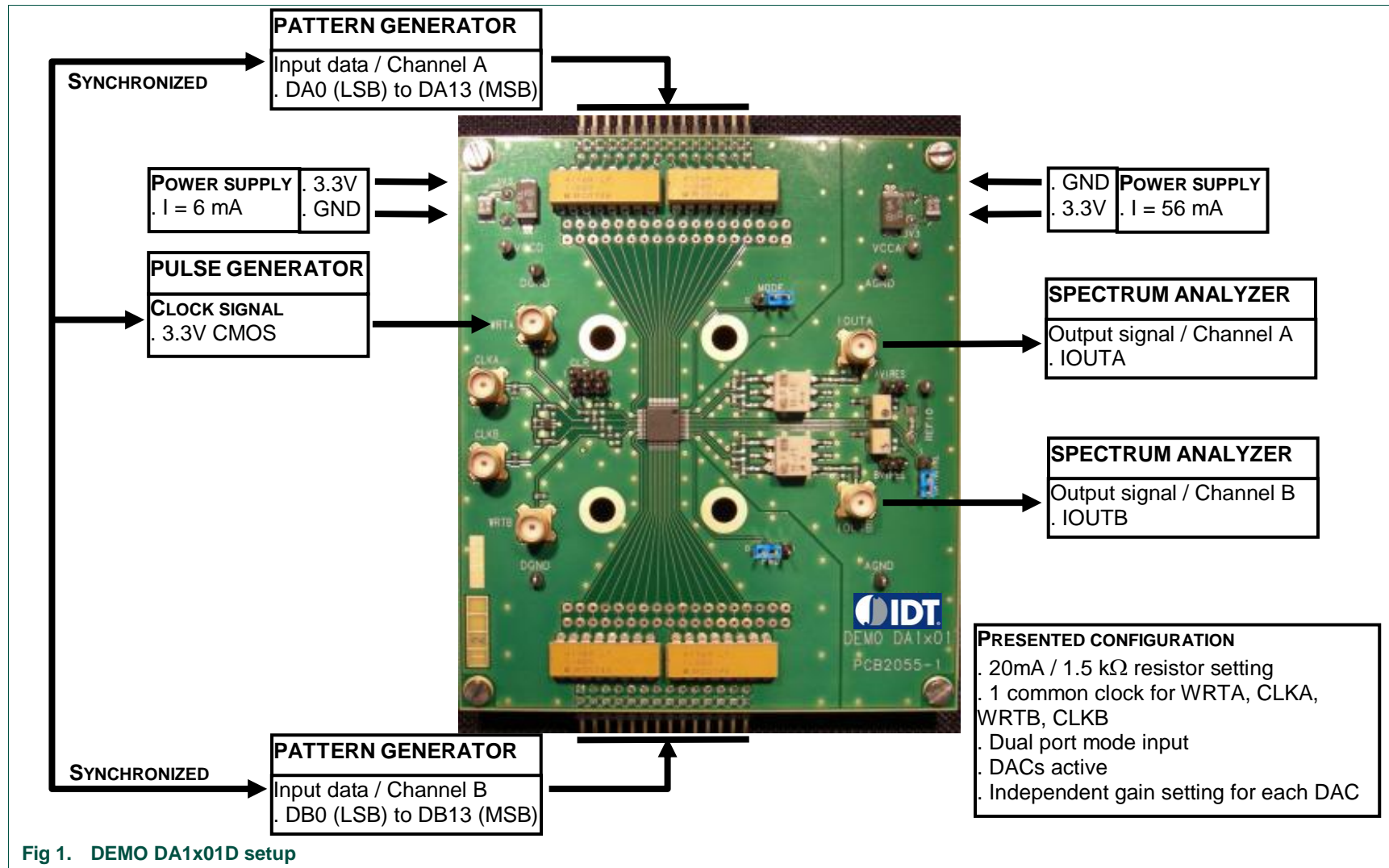
Revision history

Rev	Date	Description
2.0	20120702	Rebranded.
0.1	20081007	Initial version.

1. Quick start

1.1 Setup overview

Figure Fig.1 presents the connections to measure DEMO DA1x01D.



1.2 Power supply

Table 1. General power supply

Name	Function	View	
J1	VDDD connector – Digital power supply 3.3 V _{DC} / 6 mA.		
J2	VDDA connector – Analog power supply 3.3 V _{DC} / 56 mA		
TP1	VDDD test point – Digital power supply		
TP2	VDDA test point – Analog power supply		
TP4, TP5	DGND test point – Digital ground		
TP6, TP7	AGND test point – Analog ground		
TB5	PWD switch – Power down selection		
	DACs active	Power down	

1.3 Output current and gain adjustments

Table 2. Output current and gain adjustments

Name	Function	View	
P1	AVIRES trimmer – Channel A full-scale current setting		
TB8	AVIRES test point – Channel A resistor test point (1.5 k Ω for 20 mA)		
P2	BVIRES trimmer – Channel B full-scale current setting		
TB6	BVIRES test point – Channel B resistor test point (1.5 k Ω for 20 mA)		
TB7	GAINCTRL switch – Gain control selection		
	2 independent resistors for full-scale current setting of both channels		1 common resistor (P1) for full-scale current setting of both channels
J3	REFIO connector – External input for reference adjustment		
TP3	REFIO test point – Reference I/O (typ. 1.25 V)		

1.4 Input/output datas

Table 3. Input/output datas

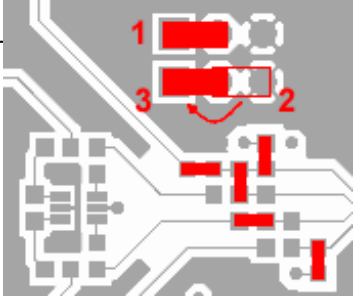
Name	Function	View
TB1	Array connector – Channel A digital inputl (DA0 to DA13)	
J9	IOUTA connector – Channel A analog output signal (100 Ω differential resitor)	
TB2	Array connector – Channel B digital inputl (DB0 to DB13)	
J8	IOUTA connector – Channel B analog output signal (100 Ω differBntial resitor)	
TB9	MODE switch – Mode selection	

Interleaved data input	Dual-port data input

1.5 Clock signals

Table 4. Clock signals

Name	Function	View	
J4	WRTA connector – Write A input		
J5	CLKA connector – Clock A input		
J6	WRTB connector – Write B input		
J7	CLKB connector – Clock B input		
net	Dual-port mode: 1 common clock (WRTA) for WRTA, CLKA, WRTB and CLKB		
	Dual-port mode: 4 clock inputs for WRTA, CLKA, WRTB and CLKB		
	Dual-port mode: 1 common clock (CLKA) with 2 buffers for WRTA, CLKA, WRTB and CLKB		

Name	Function	View
	<p data-bbox="236 203 432 230">Interleaved mode:</p> <ul data-bbox="236 241 501 539" style="list-style-type: none"><li data-bbox="236 241 501 297">- WRTA input for IQWRT and IQCLK<li data-bbox="236 309 501 365">- CLKB input for IQRESET<li data-bbox="236 376 501 432">- IQSEL is generated by the 74LCX112M<ol data-bbox="268 443 437 539" style="list-style-type: none"><li data-bbox="268 443 437 470">1. Put CLR to 1<li data-bbox="268 481 437 508">2. Put PRE to 0<li data-bbox="268 519 437 546">3. Put PRE to 1	

2. Example

2.1 Setup example

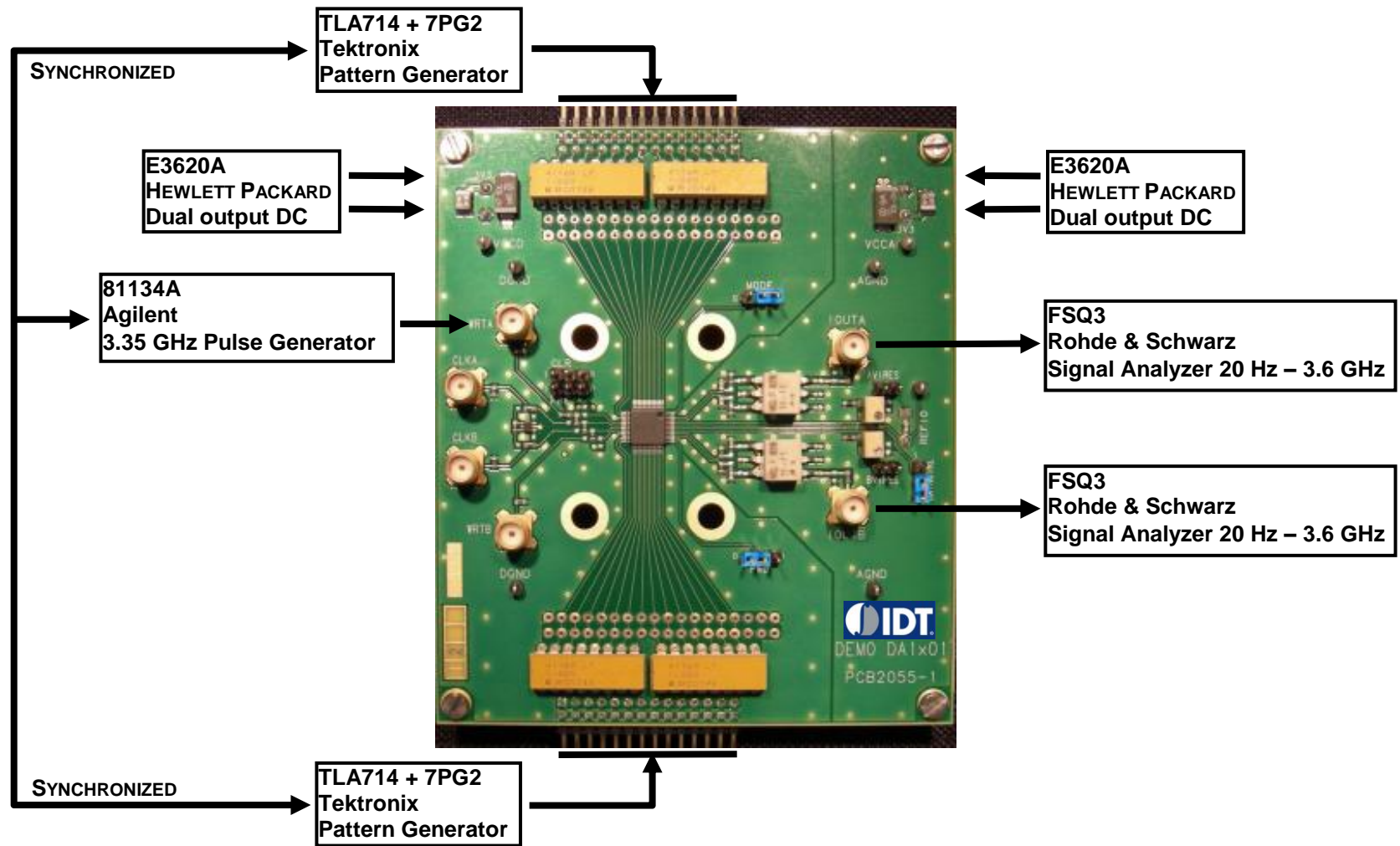


Fig 2. DAC1401D125 hardware setup