F5701

24.25GHz to 29.5GHz RF, 2.5GHz to 6GHz IF Upconverter/Downconverter

The F5701 evaluation kit (EVK) is designed to help users evaluate the F5701 RF upconverter/ downconverter device. This document provides the necessary information and a brief overview of the associated control software Graphical User Interface (GUI). Renesas recommends that you review the corresponding device datasheets and use them as a reference to supplement the information provided in this document.

Features

- RF range: 24.25GHz to 29.5GHz (n257/n258)
- IF range: 2.5GHz to 6GHz
- Two integrated LO frequency doublers
- Analog supply voltage: +2.4V to +2.6V
- Dedicated PA supply voltage: selectable between +2.4V to +2.6V and +3.0V to +3.3V

Evaluation Kit Contents

- F5701 evaluation board (Figure 1, item 1)
- FT2232HL interface board (Figure 1, item 2)
- USB-to-Micro USB cable (Figure 1, item 3)
- 16-pin supply cable (Figure 1, item 4)

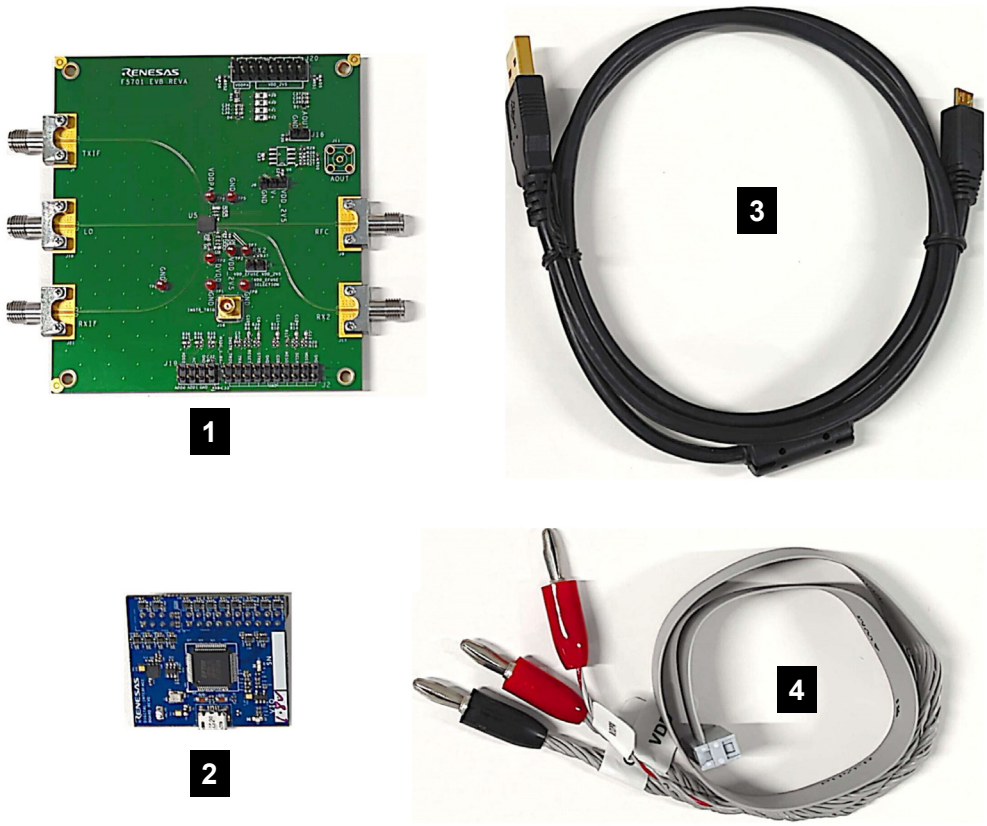

Figure 1. Evaluation Kit Contents

Contents

Figures

Tables

1. Hardware Overview

1.1 Evaluation Board

Figure 2 identifies the locations of RF I/O ports, digital interface and power supply headers, and sensing test points.

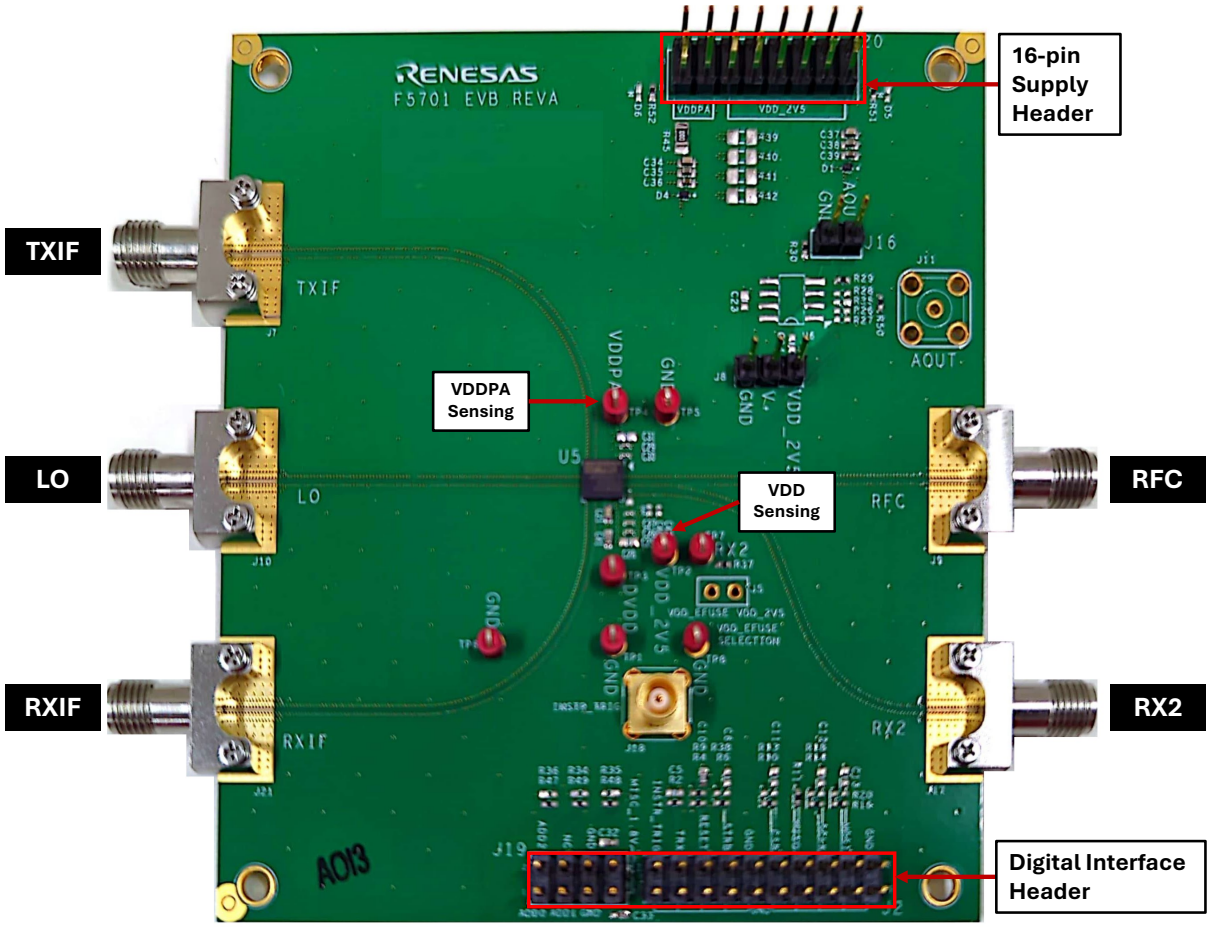

Figure 2. F5701 Evaluation Board Ports and Connectors

Table 1. Connector Descriptions

Connector	Description
J2	Digital interface header (2 × 10) 1, 3, 5, 7 – No connection 2 – Instrument Trigger 4 – TRX control 6 – RESETB control 8 – STRB control 9, 11, 13, 15, 17, 19 – GND 10, 20 – GND 12 – CSB control 14 – MISO control 16 – SCLK control 18 – MOSI control
J7	TXIF port
J9	RFC port
J10	LO port
J17	RX2 port

Connector	Description
J19	Digital interface header (2 × 4) 1 – ADD0 2 – ADD2 3 – ADD1 4 – No connection 5, 6 – GND 7, 8 – MISC_1.8V
J20	16-pin supply header 1, 3, 5, 7, 9, 11, 13, 15 – GND 2, 4, 6, 8, 10, 12 – VDD (Analog) 14, 16 – VDDPA
J21	RXIF port

Table 2. Selector Descriptions

Selector Block	Description	Factory Setting
J5	2-pin EFUSE header 1 – VDD_2V5 2 – VDD_EFUSE	Not connected
J8	AOUT buffer VDD jumper 1 – GND 2 – OPA356 VDD pin (connect to J8.3 to power OPA356) 3 – VDD	Not connected
J16	AOUT reference resistor connection jumper 1 – U6 Op-amp positive signal input 2 – R30 resistor to ground	Not connected

Table 3. Test Point Descriptions

Test Point	Description
TP1, TP5	GND test point
TP2	VDD test point
TP3	DVDD test point
TP4	VDDPA test point

1.2 THRU Reference Fixture

The THRU reference fixture (optional part of the evaluation kit) is used to generate test equipment de-embed files for removing the effects of the EVB RF traces and connectors. AFR (Automatic Fixture Removal) is a commercial product available from test and measurement suppliers to create the de-embed files (**.s2p**) using measurements from the THRU Reference Fixture traces (2x half-fixture lines). The THRU board is laid out symmetrically so that the AFR process can generate two half-fixture s-parameter files. The S-parameter de-embed files are available from the Renesas Application Support or your local field engineer. For information on purchasing the THRU Reference Fixture board in order to create your own de-embed files, contact the Renesas Sales department.

1.3 FT2232HL Digital Interface Board

The FT2232HL digital interface board connects your computer to the F5701 EVB through a USB-to-Micro USB cable.

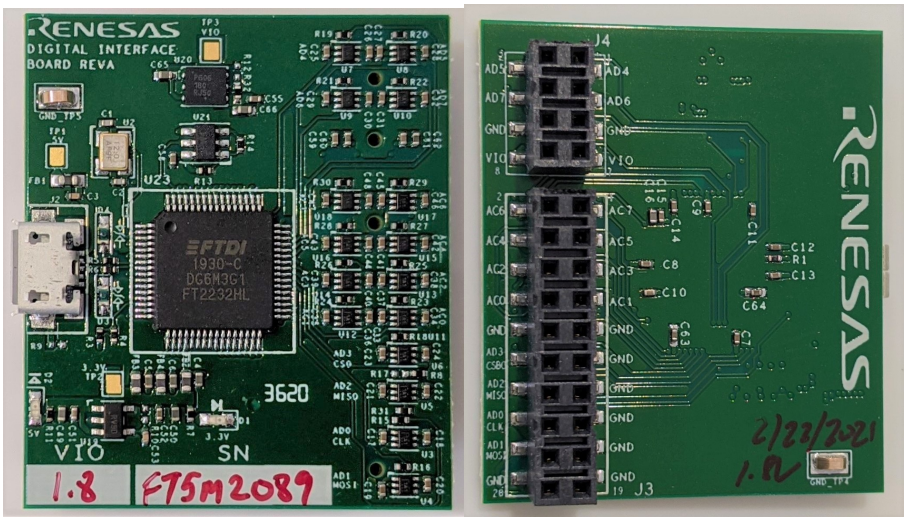

Figure 3. FT2232HL Digital Interface Board – Top (left) and Bottom (right)

2. Quick Start

2.1 Required or Recommended Test Equipment

- Power supplies with banana jack outputs capable of at least 2.5V and 1000mA rating. It is recommended to use a 4-wire remote sensing power supply for V_{DD} and V_{DDPA} when making any measurements for correlation with datasheet parameters. Removing all voltage drops introduced by the conductors and connectors is critical to achieving the datasheet specified performance.
- Vector network analyzer capable of measuring up to 30GHz.

2.2 Computer Requirements and Setup

2.2.1 Computer Requirements

- Renesas F5701 Evaluation System Software installed
- USB 2.0 or 3.0 Interface
- Windows XP SP3 or later
- Processor: Minimum 1GHz
- Memory: Minimum 512MB; recommended 1GB
- Available hard disk space: Minimum 600MB (32-bit OS), 1.5GB (64-bit OS); recommended 1GB (32-bit OS), 2GB (64-bit OS)
- Internet access during installation if the **.NET** framework (4.6.1 or later) is not currently installed on the system

2.2.2 Software Installation and Setup

1. Download the Renesas F5701 Evaluation Software (EVS) from the F5701 webpage. Contact a Renesas field engineer if experiencing any difficulty with the download.
2. Launch the software installation application (**setup.exe**).

   Note: Your account must have administrator privileges to complete the installation.
3. Follow the on-screen prompts to complete the installation.

2.3 EVB Hardware Setup

Connect the EVB as displayed in Figure 4 using the provided power supply cable and USB-to-Micro USB cable. The digital interface board can be attached directly to the F5701 EVB. The typical V_{DD} and V_{DDPA} power supplies are 2.5V. For details on other recommended power supply operating voltages, refer to the F5701 datasheet.

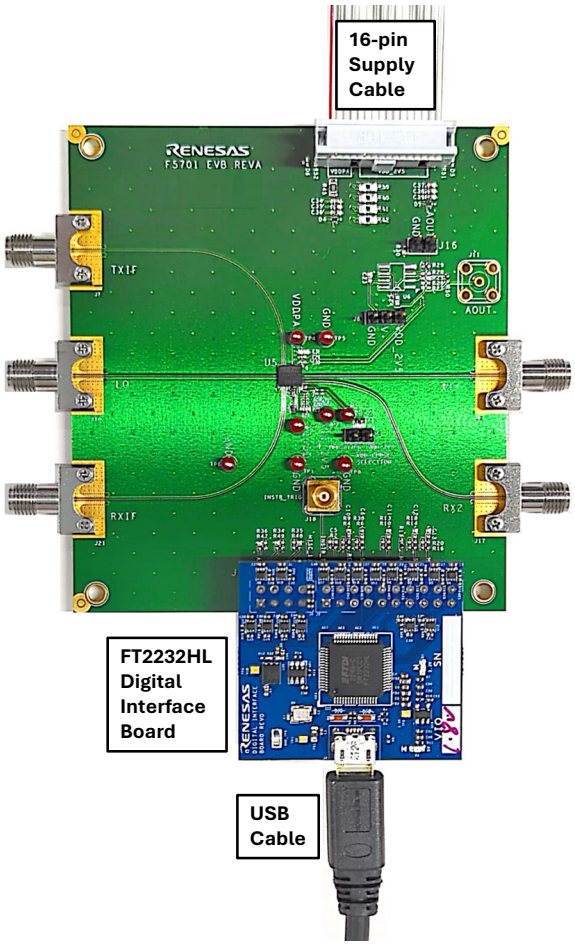

Figure 4. F5701 EVB Hardware Setup

2.4 Software Start-up and Presets

1. Open the application through the Windows Start menu or click on the application icon if saved on the desktop. The application appears as shown in Figure 5. The USB Interface Serial Number (Figure 5, item 1) should be auto-detected if the FT2232HL digital interface board is connected and recognized.
2. Select write speed, read speed, and chip address (Figure 5, item 2), then select **Detect** (Figure 5, item 4) to start the communication with the device. The **Device Selection** drop-down menu (Figure 5, item 3) is automatically selected with the correct device variant (ZL or Y). A subsequent pop-up window will ask if the user would like to program the device with the recommended default values (Figure 6). Click *Yes* to program the default values or click *No* to reset the device.
3. For each device variant, there are five recommended settings to choose from: H8 (5GHz IF / 28GHz RF), H6 (5GHz IF / 26GHz RF), H6H (5GHz IF / 26GHz RF, high linearity), L8 (3GHz IF / 28GHz RF), and L6 (3GHz IF / 26GHz RF). By default, H8 is initially selected and programmed. To program the device to other settings, use the **Device Selection** drop-down menu (Figure 5, item 3) and follow the pop-up window.
4. Users can also program the device with the recommended default values at any time afterward by clicking the *Program Defaults* button (Figure 5, item 8). After the programming, the GUI settings will be in sync with the hardware settings and the device can be controlled in real time.

5. Users can quickly enable/disable the master bias, enable/disable signal paths, set the device standby mode, switch between transmit and receive modes, and control the strobe pin by using the high-level chip control checkboxes at the bottom of the main panel (Figure 5, item 5).
6. To read all bitfield and register values at any given time, click the *Read Values* button (Figure 5, item 6) and the results will be displayed on both **BitField Log** and **Register Log** panels. To view the results, click on either **BitField Log** or **Register Log** panel tabs (Figure 5, item 10).

   Important: The **Enable BitField Log** and **Enable Register Log** checkboxes (Figure 7, items 1 and 2) must be selected beforehand. The **BitField Log** and **Register Log** panels will also keep track of all the SPI write commands.

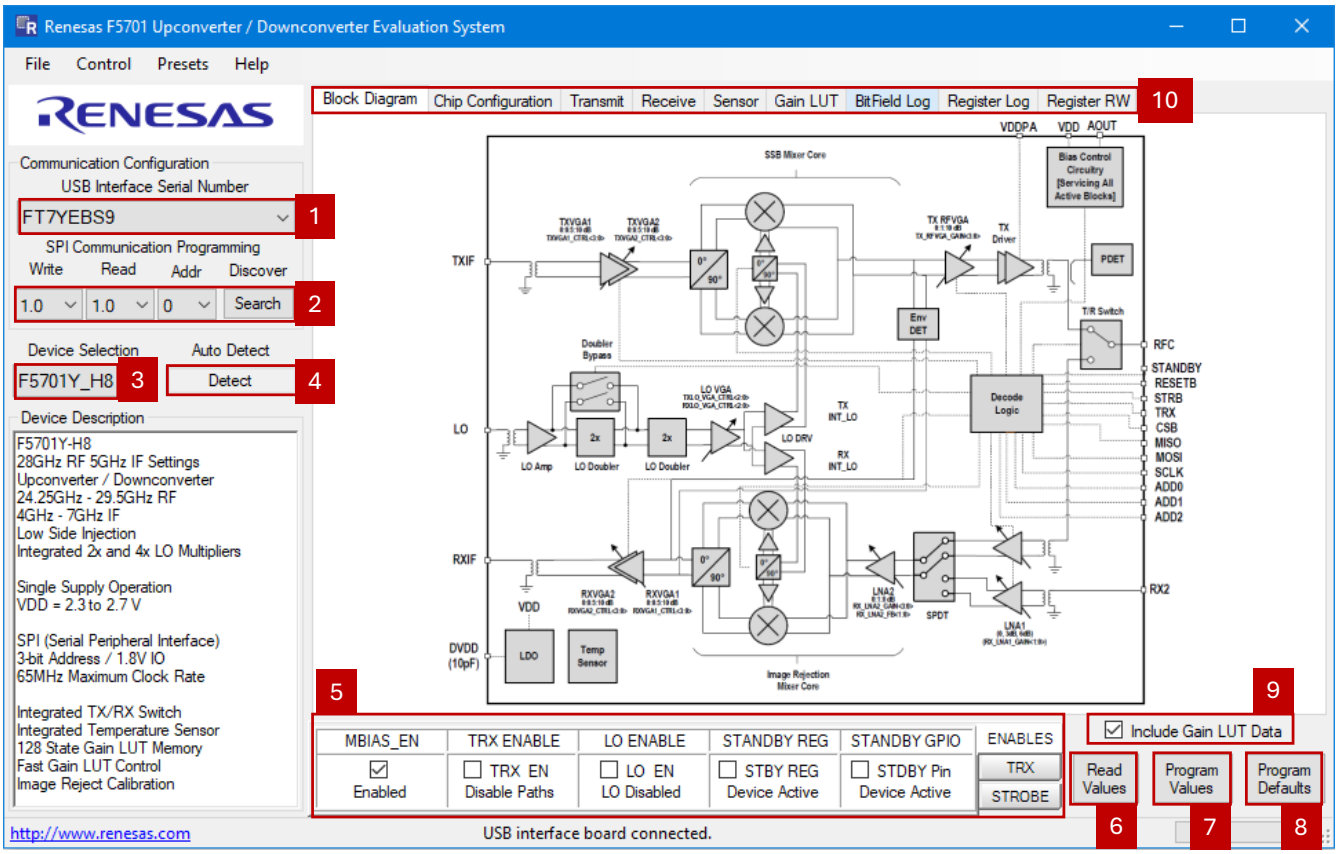

Figure 5. Application Control Panel at Start-up

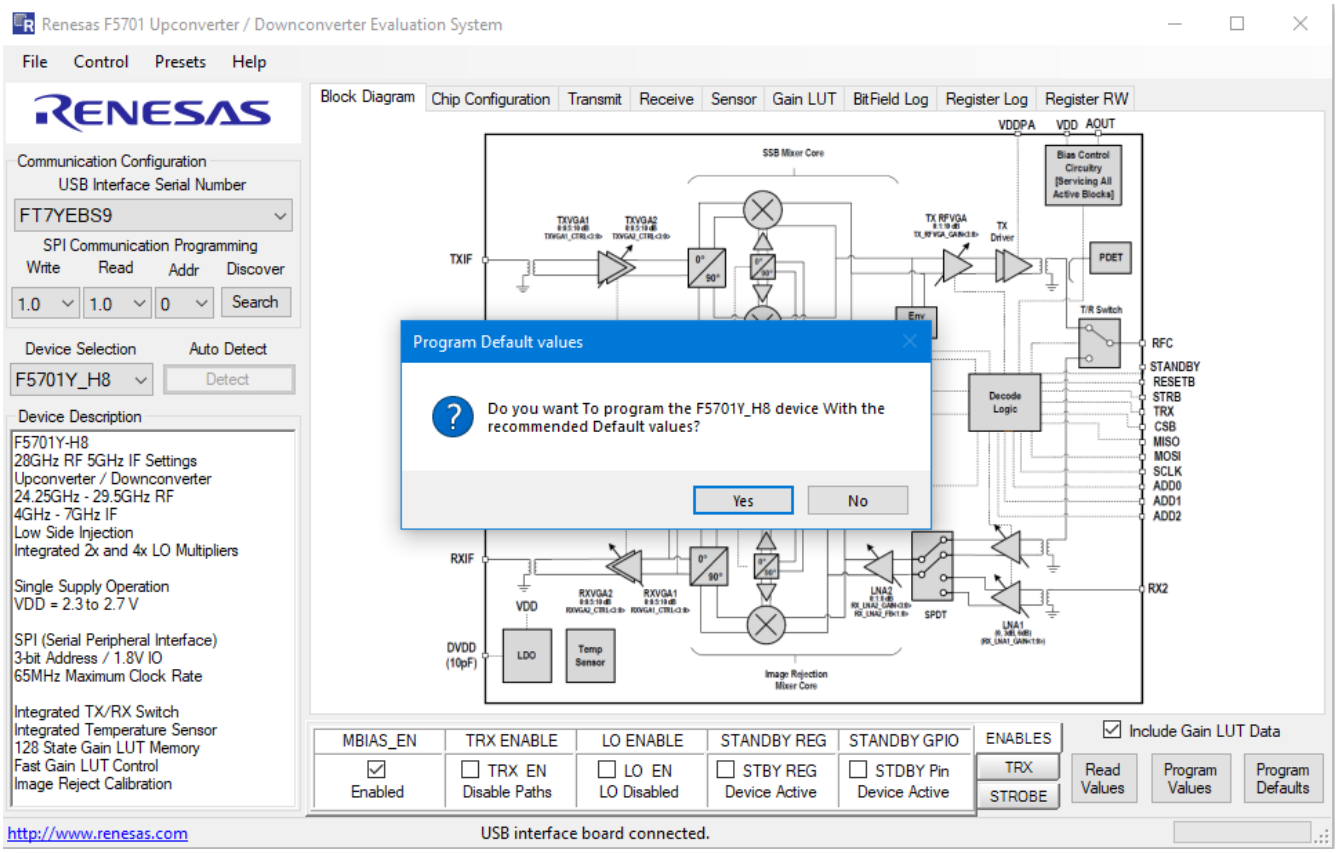

Figure 6. Pop-up Window to Program Default Values

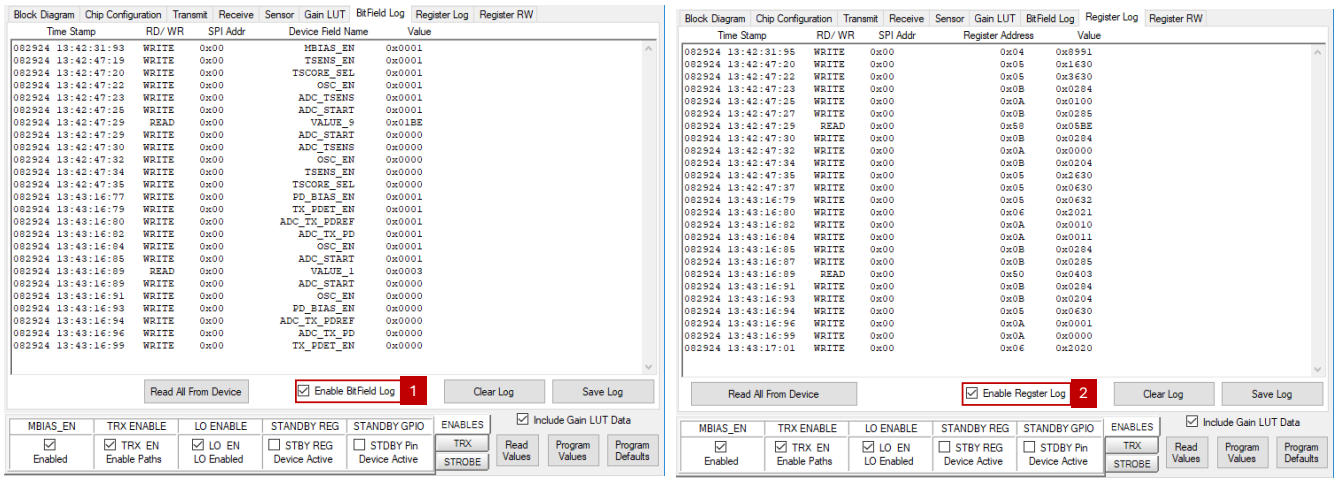

Figure 7. BitField Log and Register Log Panels

7. The File menu shown in Figure 8 provides options to load or save device settings (Figure 8, item 1). Device bitfield settings can be saved to an XML file and loaded back to the software at any given time. To use a Gain Lookup Table (LUT), **Load Gain Lookup Table** (Figure 8, item 2) to load a gain LUT file, then select **Program Gain Lookup Table** (Figure 9, item 3) in the Control menu to program it to the device.

   Note: To use gain LUT, the **Include Gain LUT Data** checkbox (Figure 5, item 9) must be checked. The Control menu also allows users to reset the device (Figure 9, item 1). The software will read back the written register after every SPI write command if item 2 in Figure 9 is selected.

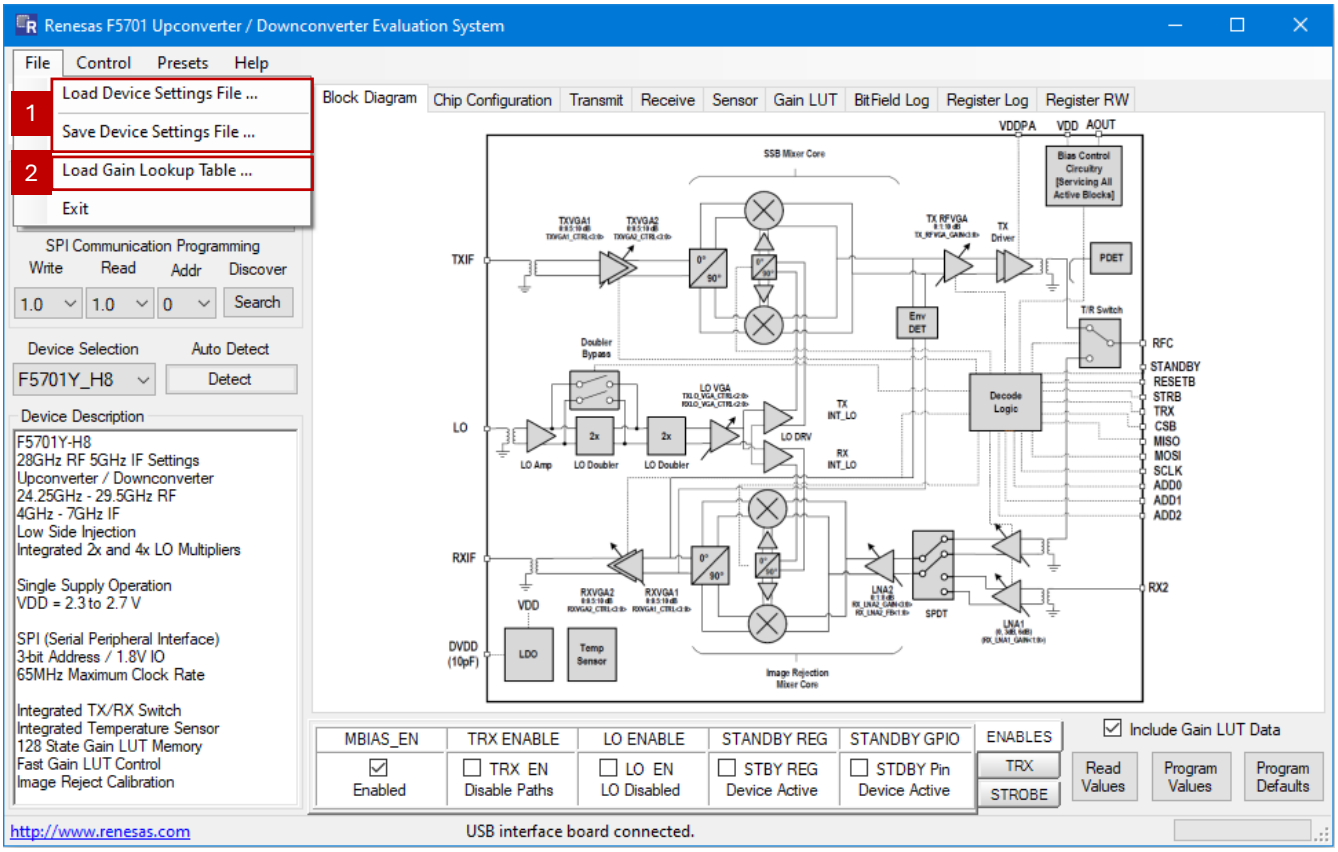

Figure 8. File Menu

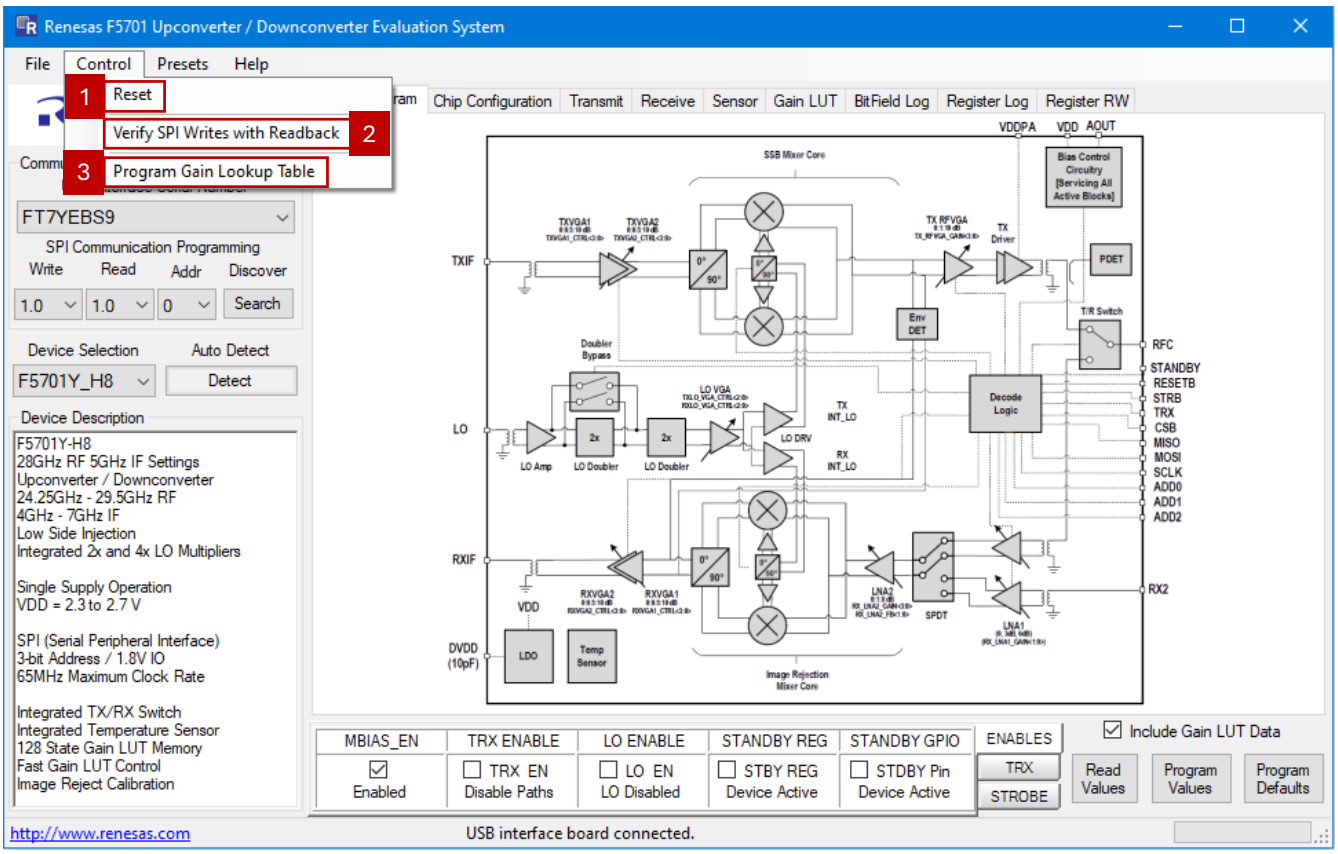

Figure 9. Control Menu

8. For convenience, the Presets menu (see Figure 10) is provided in this software for users to quickly program the device to one of the predefined states for the standby mode, transmit modes, receive modes, and receive-2 modes (RX2 path). For example, by selecting the **Transmit: Transmit LO2X** option, both TRX and LO signal paths will be enabled in the transmit mode with LO_SEL set to 0 for LOx2.

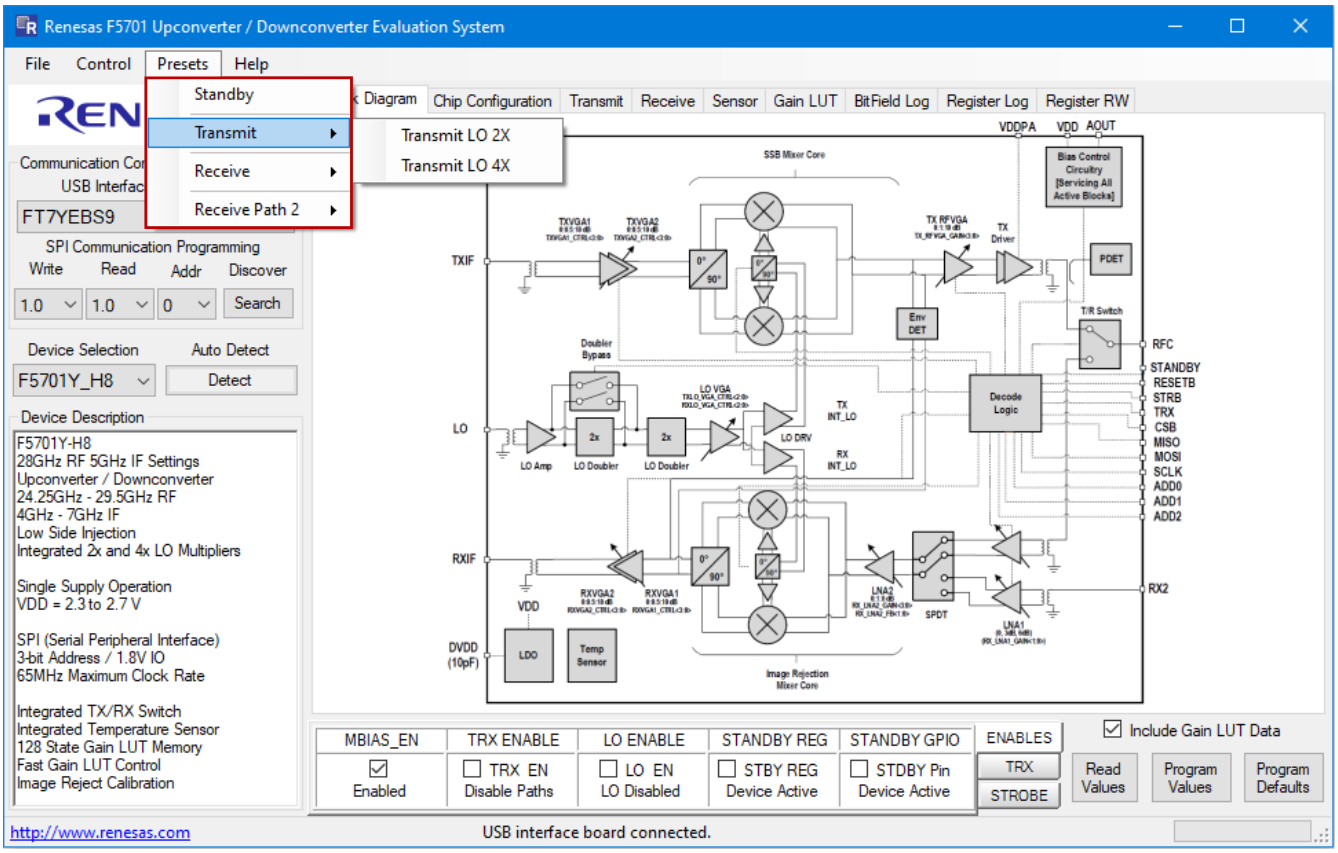

Figure 10. Presets Menu

9. The main configuration control panel can be seen by clicking on the **Chip Configuration** panel tab (Figure 5, item 10). Users can select the corresponding subpanel tab to read chip information (Figure 11), set general device configuration (Figure 12), set/enable master bias (Figure 13), and test the SRAM (Figure 14).

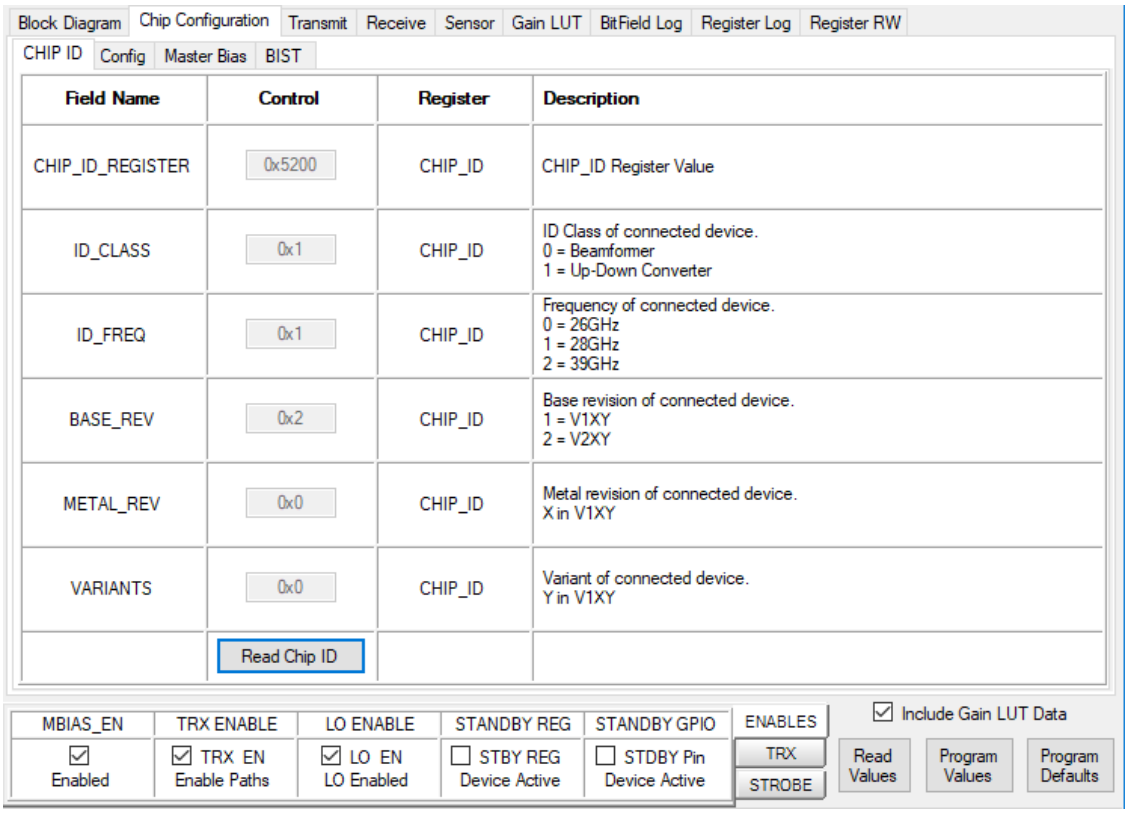

Figure 11. Chip ID Panel

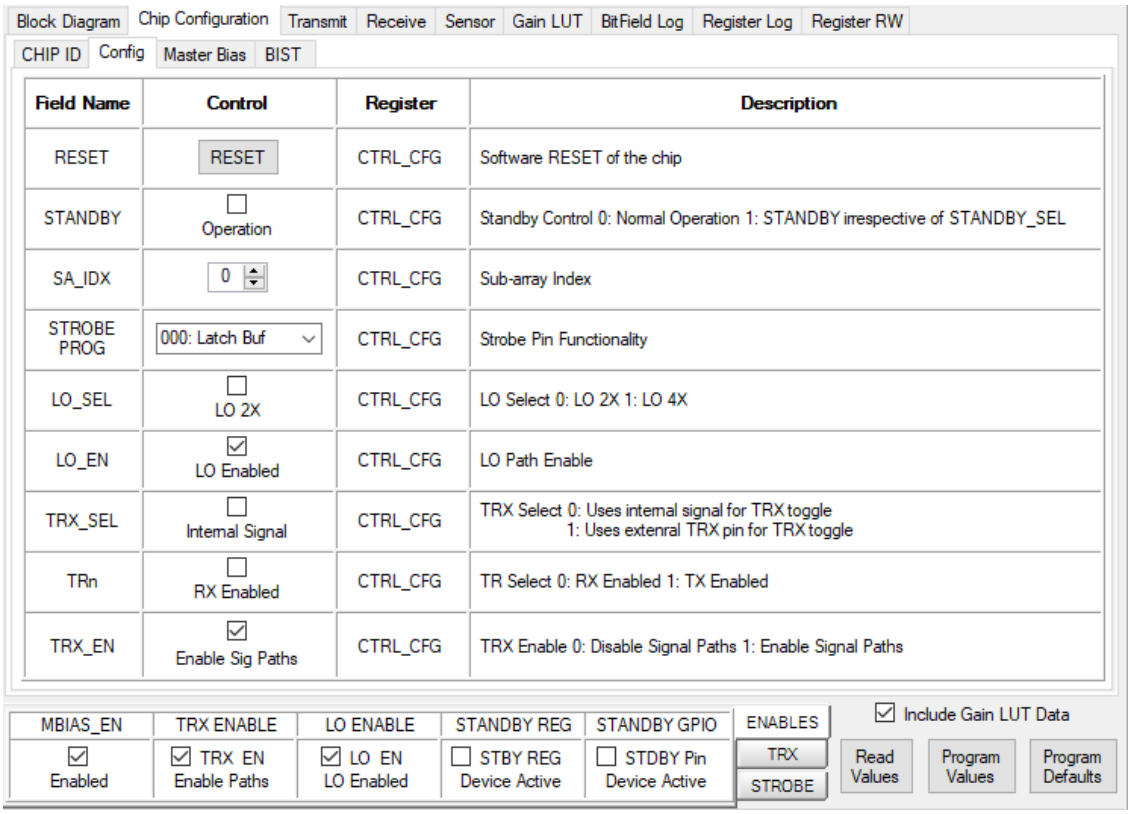

Figure 12. Configuration Panel

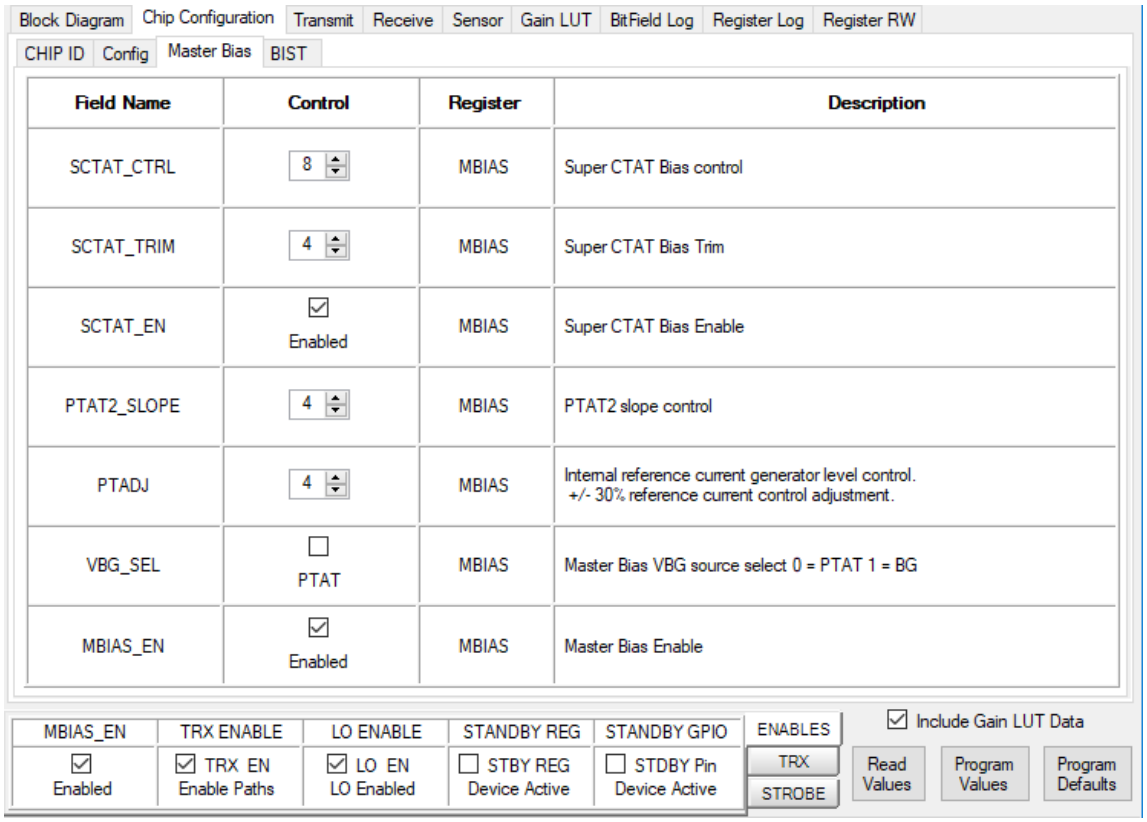

Figure 13. Master Bias Panel

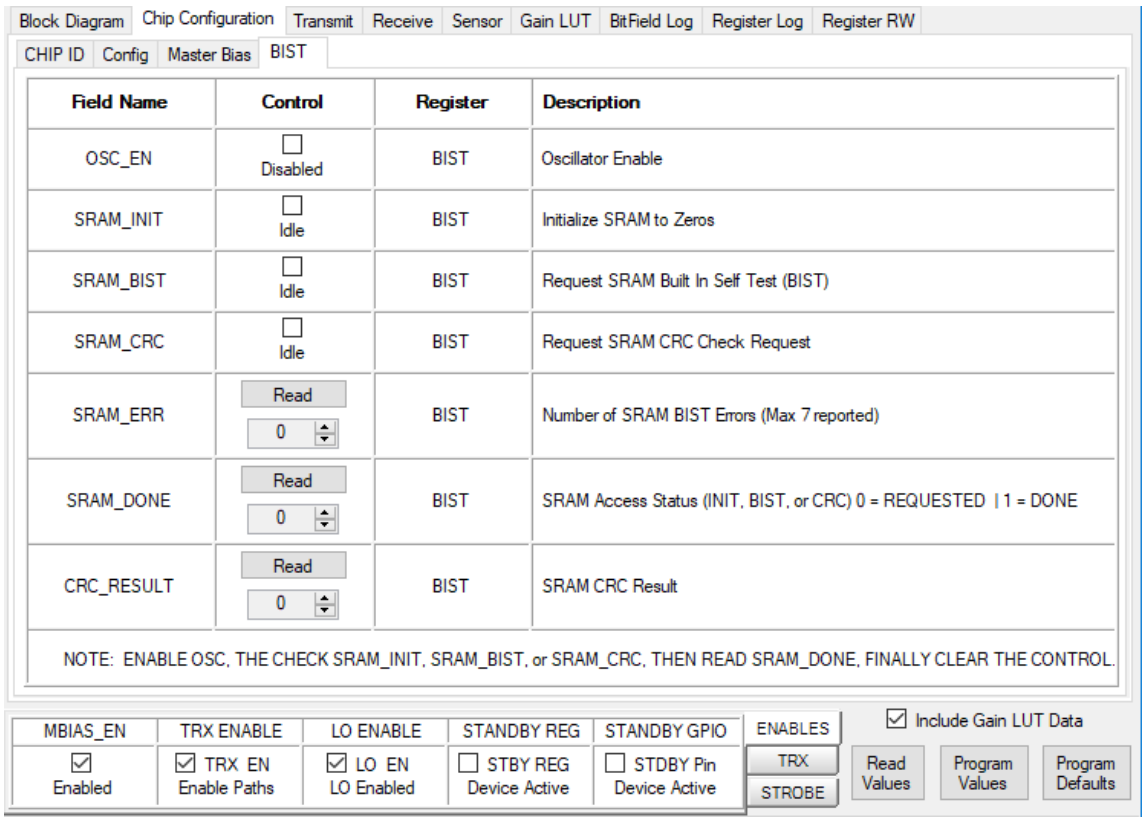

Figure 14. BIST Panel

10. In transmit mode, individual transmit building blocks and their warmup states can be configured by selecting **Transmit panel** tab (Figure 5, item 10) and **Enable / Warmup** subpanel tab as shown in Figure 15.

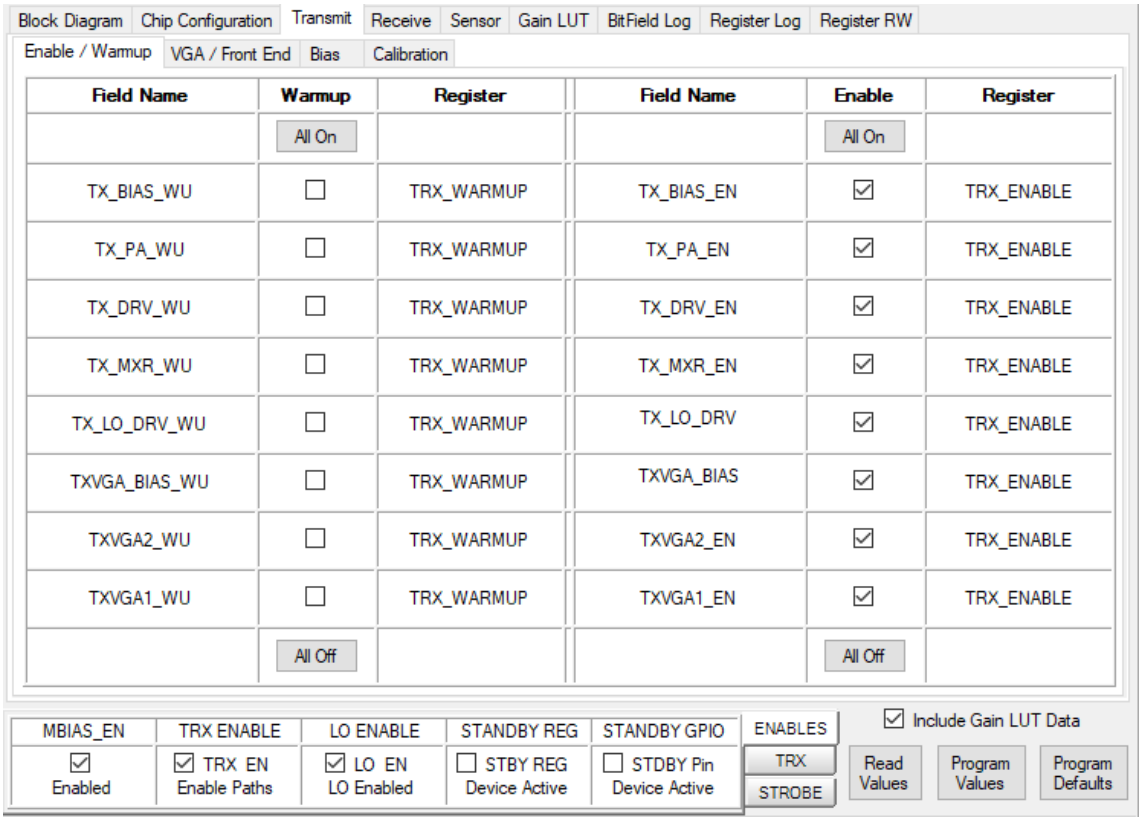

Figure 15. Transmit: Enable / Warmup Panel

11. The **VGA / Front End** panel (Figure 16) allows users to manually adjust TX VGA/FE gain settings. Users can also manually adjust bias settings for individual TX building blocks and calibration parameters by selecting **Bias** and **Calibration** subpanel tabs.

    Important: To manually adjust VGA/FE gain settings (both transmit and receive modes), the **Include Gain LUT Data** checkbox (Figure 5, item 9) must be unchecked, otherwise, the gain settings will be dictated by the gain LUT control feature.

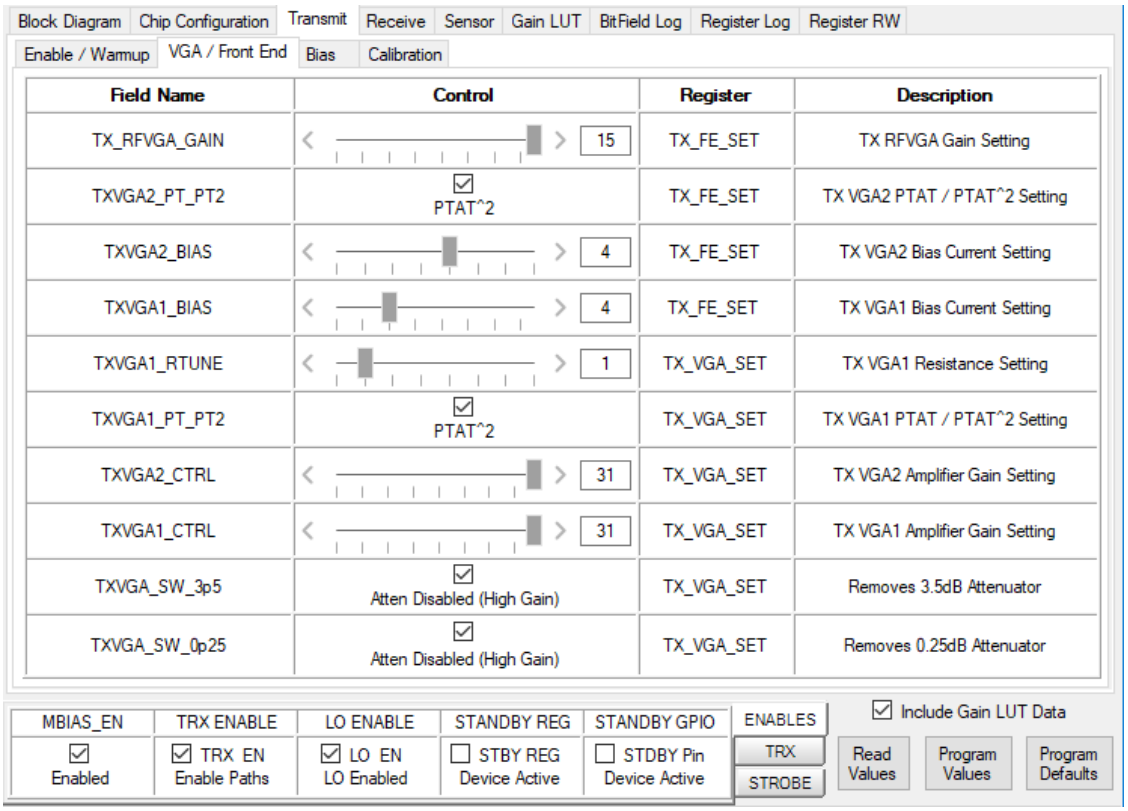

Figure 16. Transmit: VGA / Front End Panel

12. Similarly, in receive mode, individual receive building blocks and their warmup states can be configured by selecting **Receive panel** tab (Figure 5, item 10) and **Enable / Warmup** subpanel tab as shown in Figure 17.

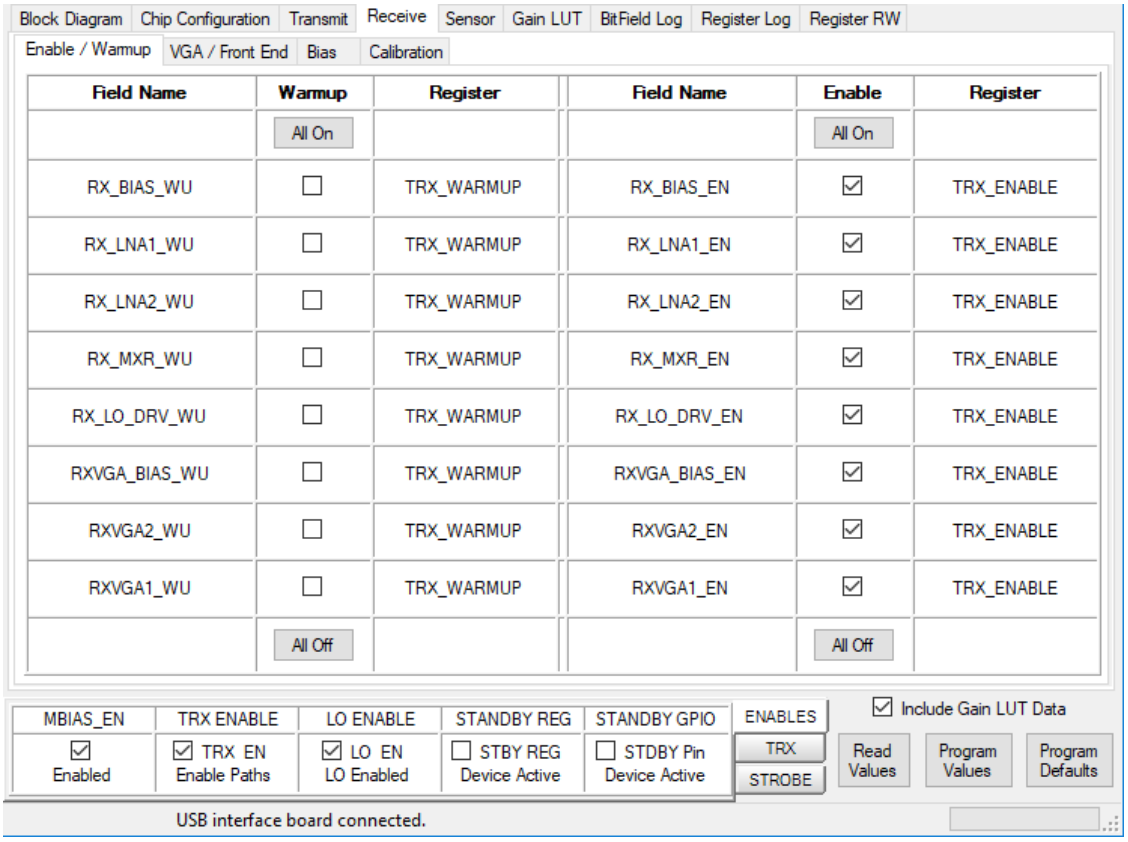

Figure 17. Receive: Enable / Warmup Panel

13. The **VGA / Front End** panel (Figure 18) allows users to manually adjust RX VGA/FE gain settings. Users can also manually adjust bias settings for individual RX building blocks and calibration parameters by selecting **Bias** and **Calibration** subpanel tabs.

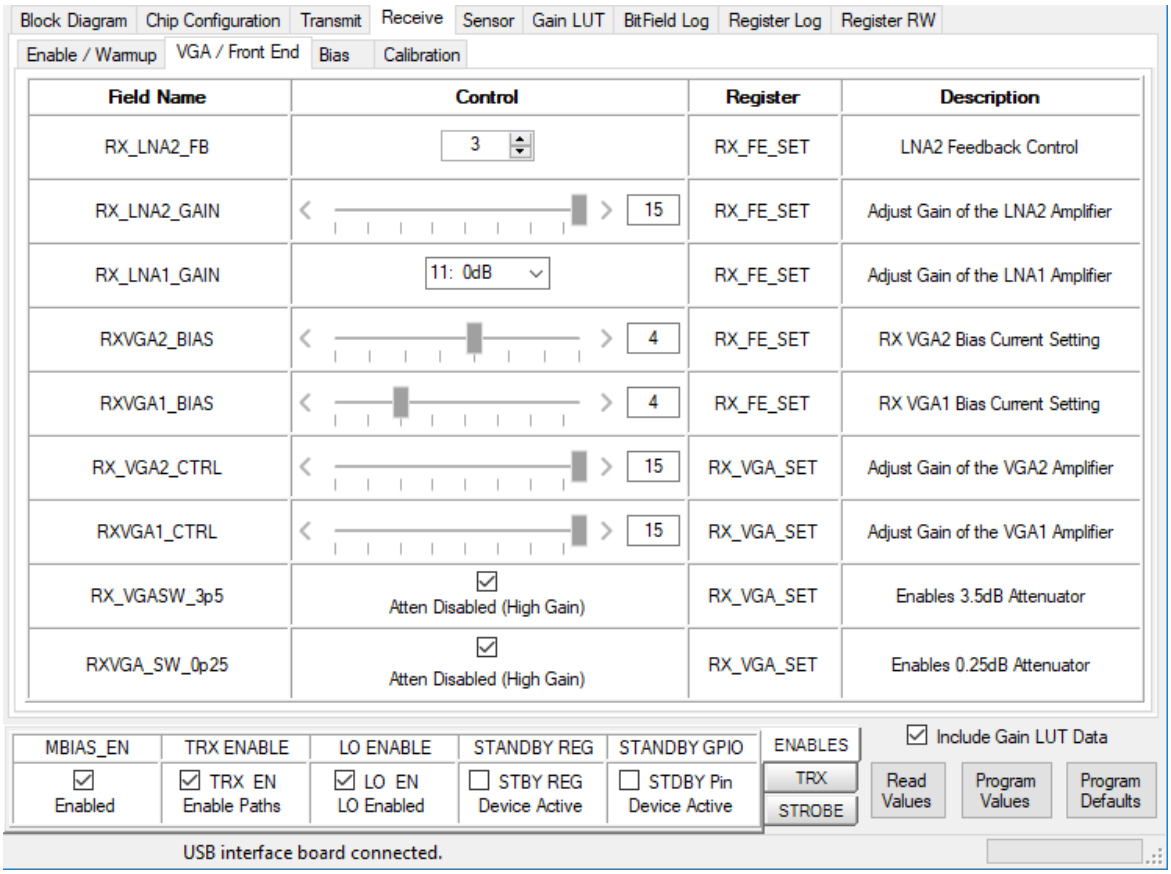

Figure 18. Receive: VGA / Front End Panel

14. Sensor control panel can be accessed by selecting **Sensor** panel tab (Figure 5, item 10). While individual settings relating to temperature sensor and power detector (PDET) can be controlled, a **Macros** panel (Figure 19) is provided for quick evaluation.

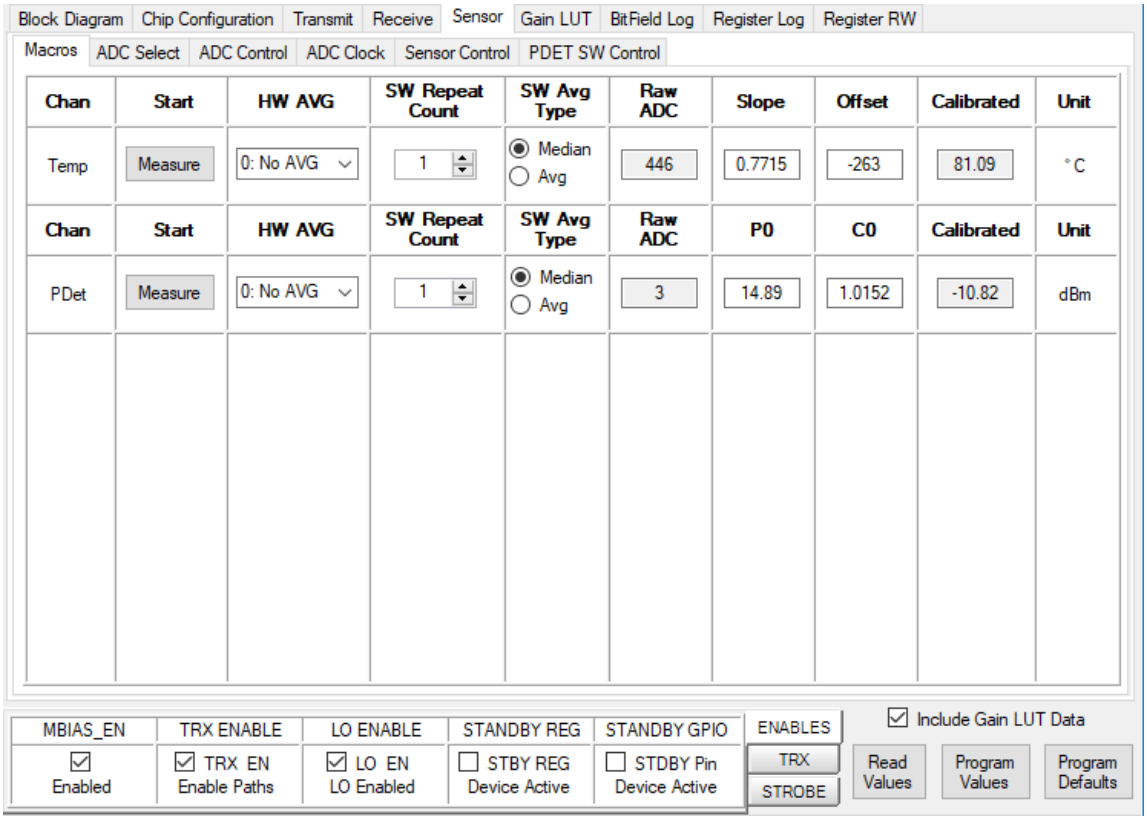

Figure 19. Sensor: Macros Panel

15. TX/RX VGA/FE gain can be controlled by a predefined gain LUT. For gain control mapping and typical performance at nominal settings, please consult the datasheet. An example gain LUT CSV file is included with the evaluation software and can be loaded and programmed (Figure 8, item 2 to load and Figure 9, item 3 to program). The **Include Gain LUT Data** checkbox (Figure 5, item 9) must be checked beforehand. Select **Gain LUT** panel tab (Figure 5, item 10) to see the LUT control panels.

16. Figure 20 shows the **SRAM LUT Entry Select** panel. Use the slider to select any gain LUT index loaded on the SRAM, or similarly on the **Direct LUT Entry Select** panel (Figure 22) without accessing the SRAM.

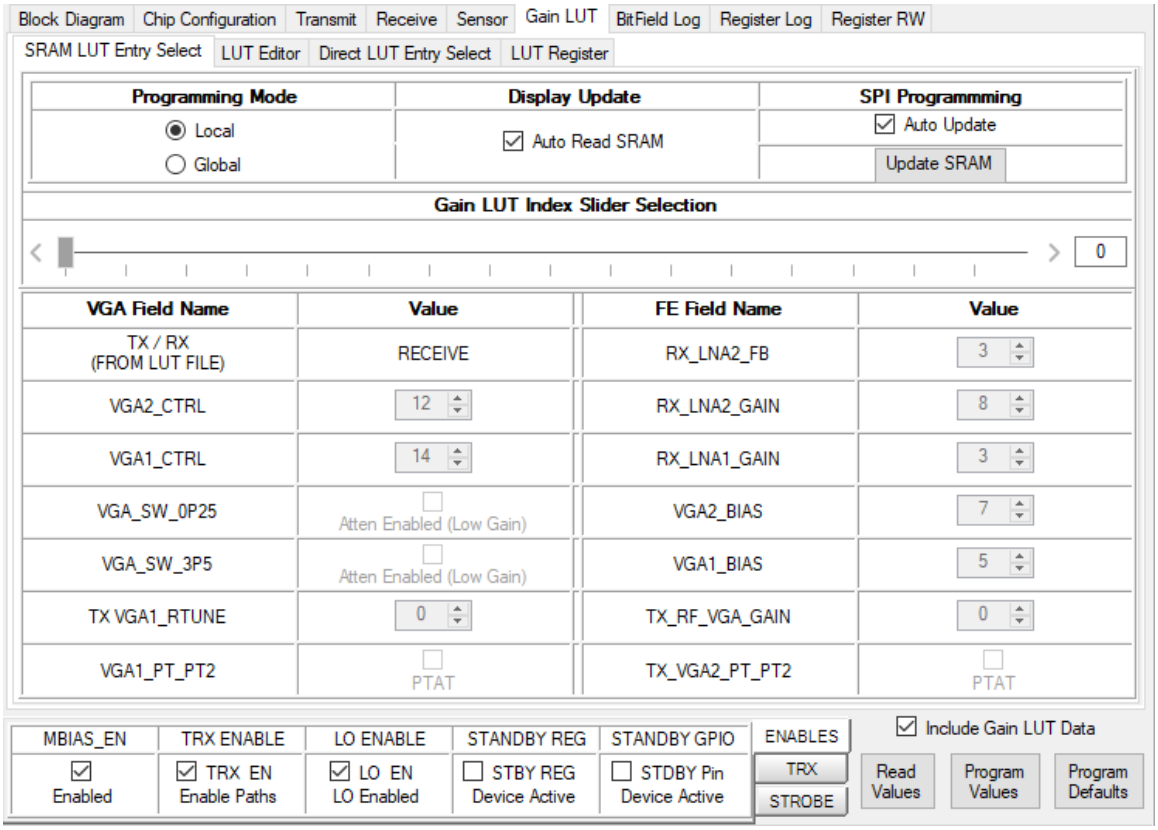

Figure 20. Gain LUT: SRAM LUT Entry Select

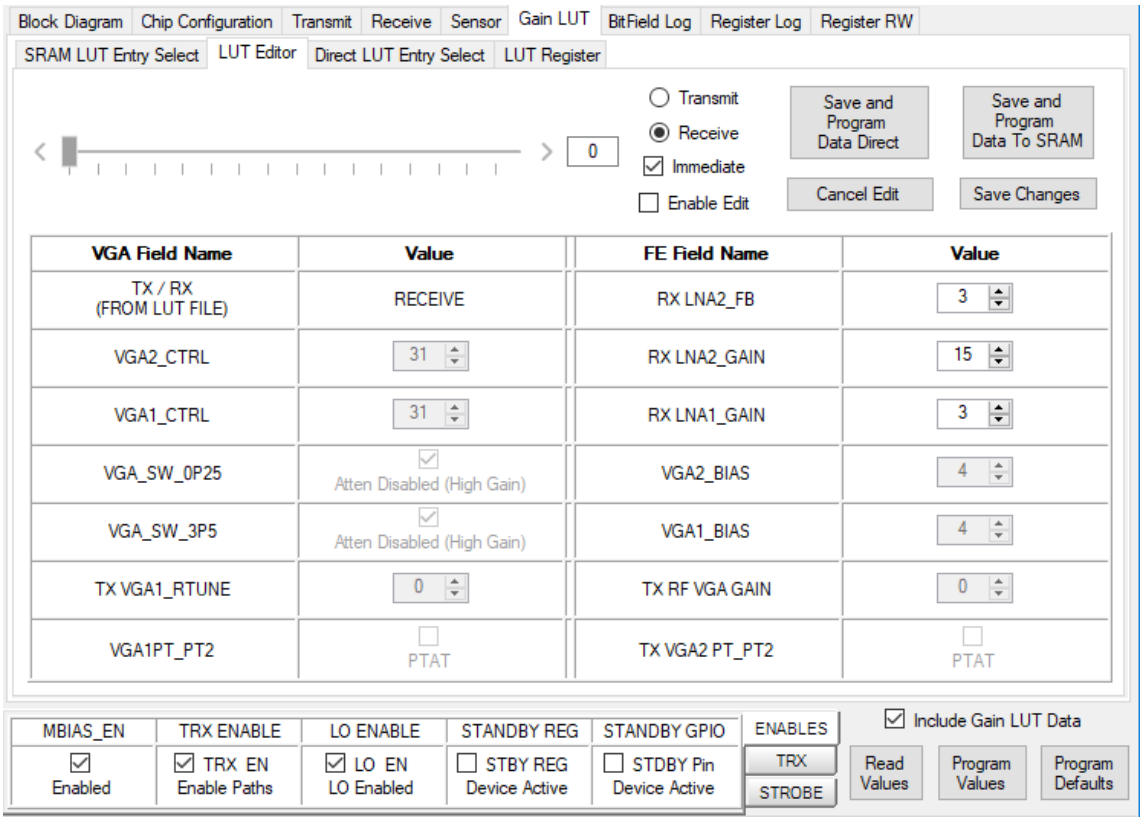

Figure 21. Gain LUT: LUT Editor

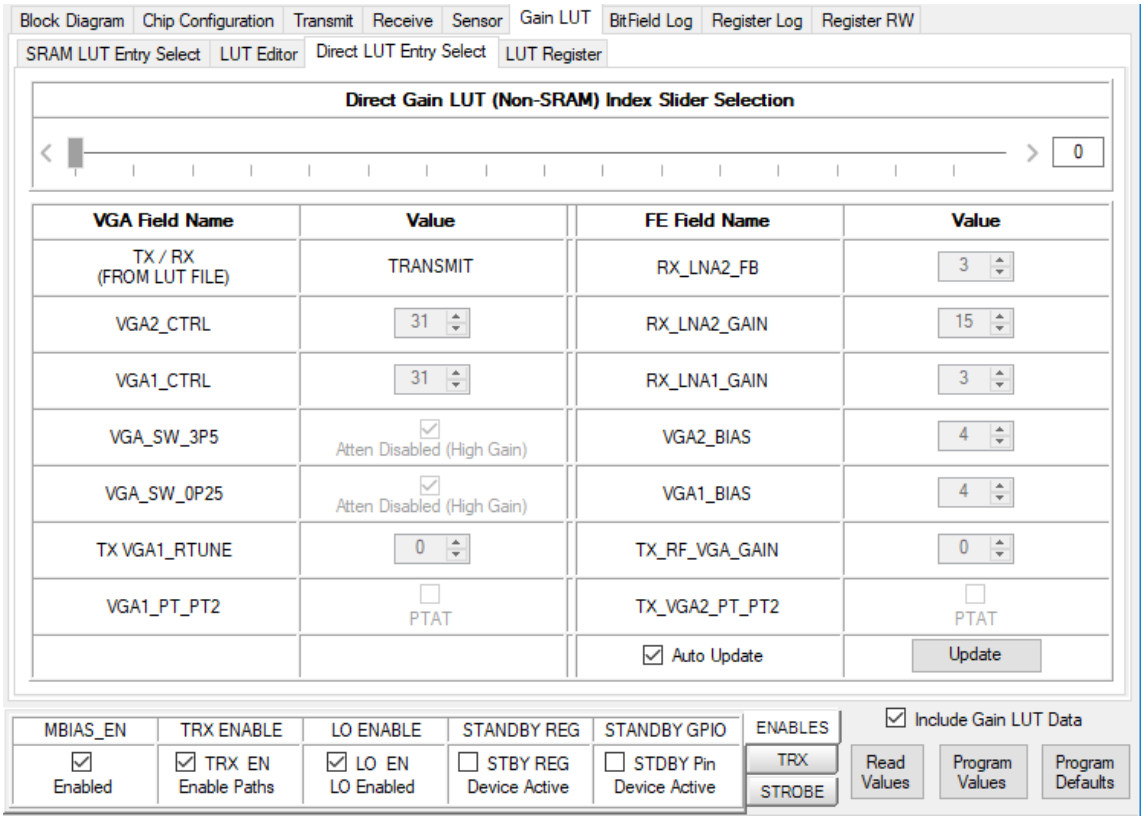

Figure 22. Gain LUT: Direct LUT Entry Select

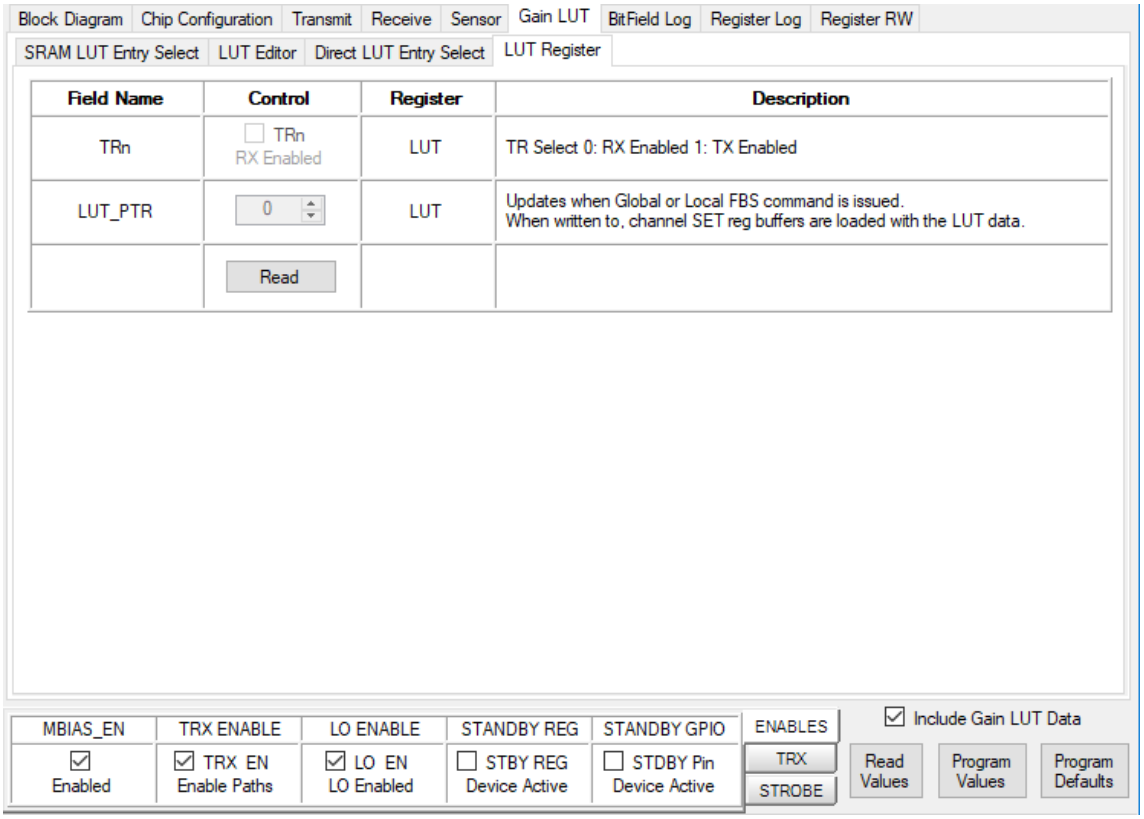

Figure 23. Gain LUT: LUT Register

17. Users can read or write directly to any writable register using the **Register RW** panel shown in Figure 24. Select the register name from the drop-down menu (Figure 24, item 1). The register address (Figure 24, item 2) will be automatically updated. Click *Read* to read the register value. To write to the register, enter the new value in the **Register Value (0x)** box and click *Write*.

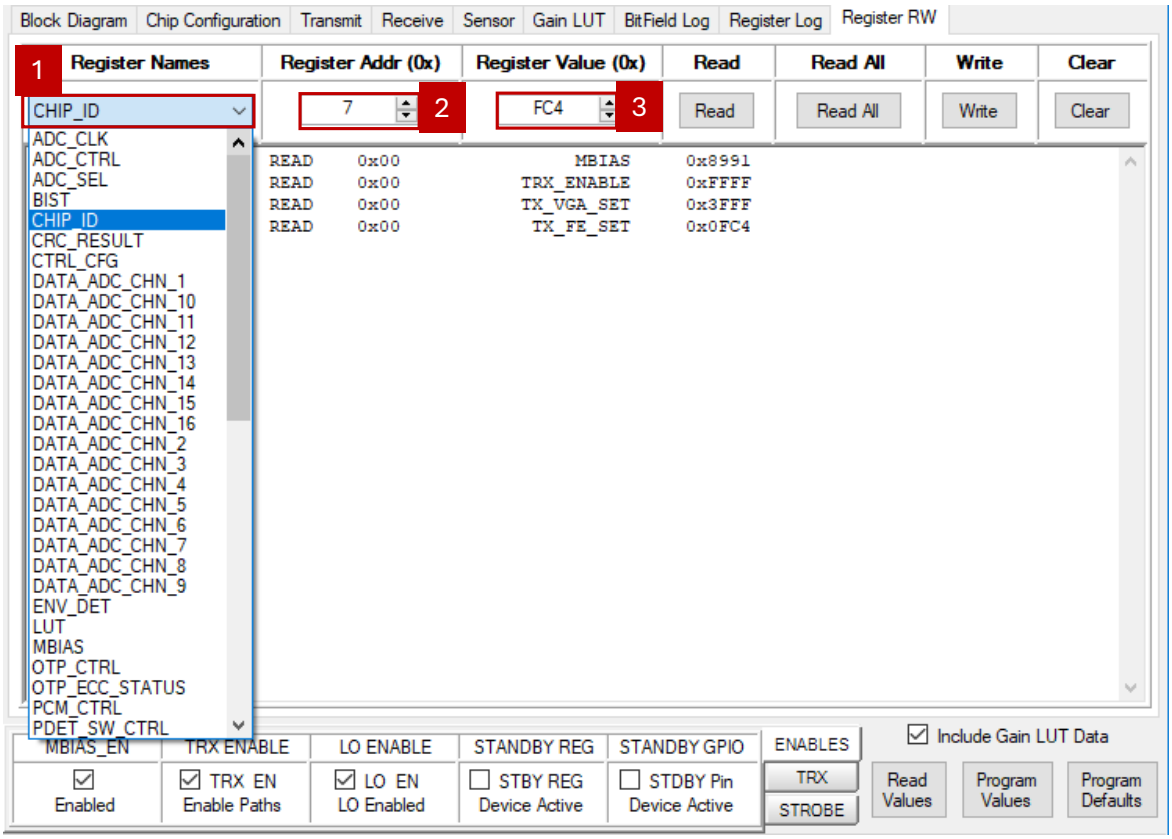

Figure 24. Register RW Panel

3. Board Design

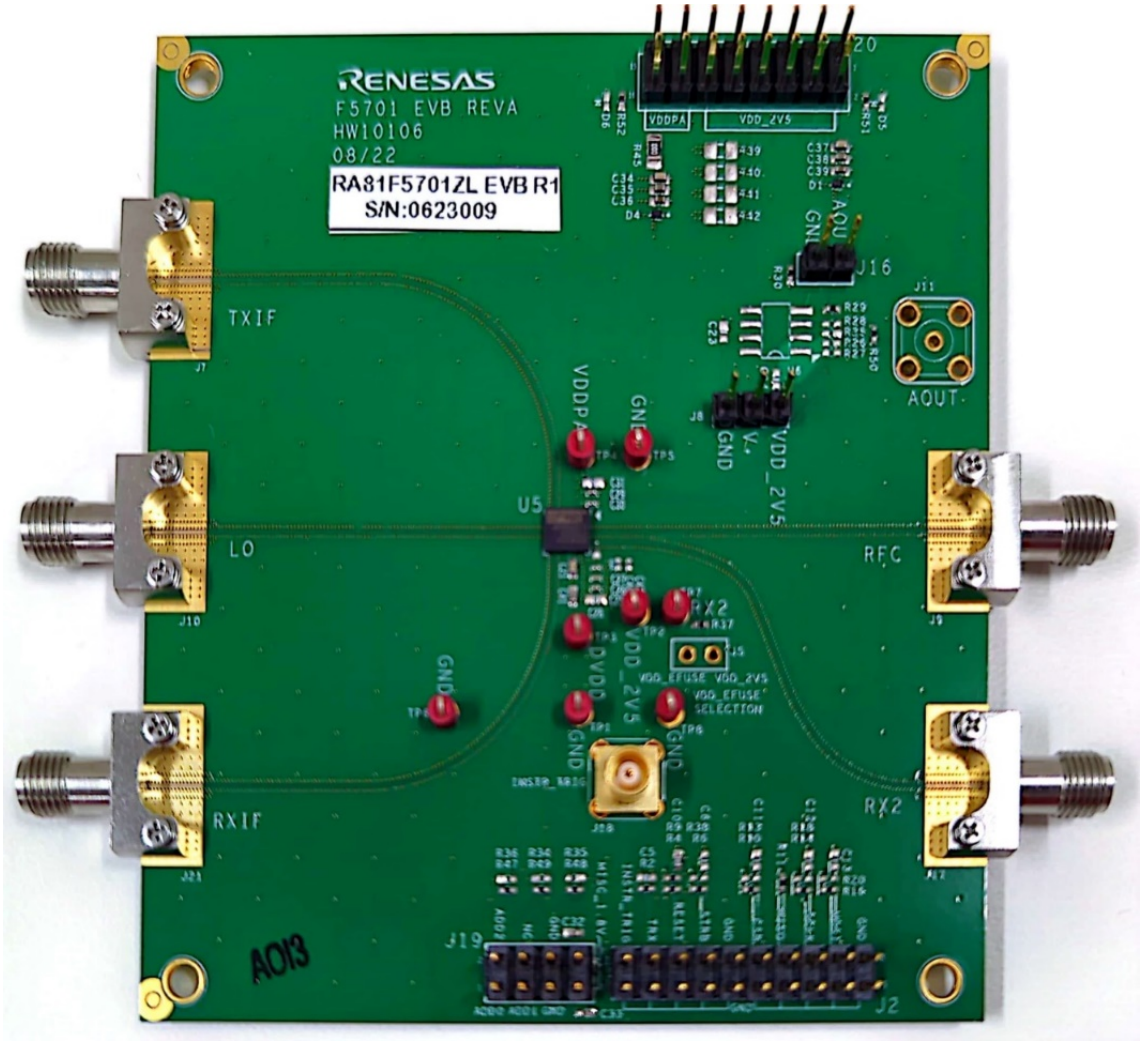

Figure 25. F5701 Evaluation Board Image (Top)

3.1 Schematic Diagrams

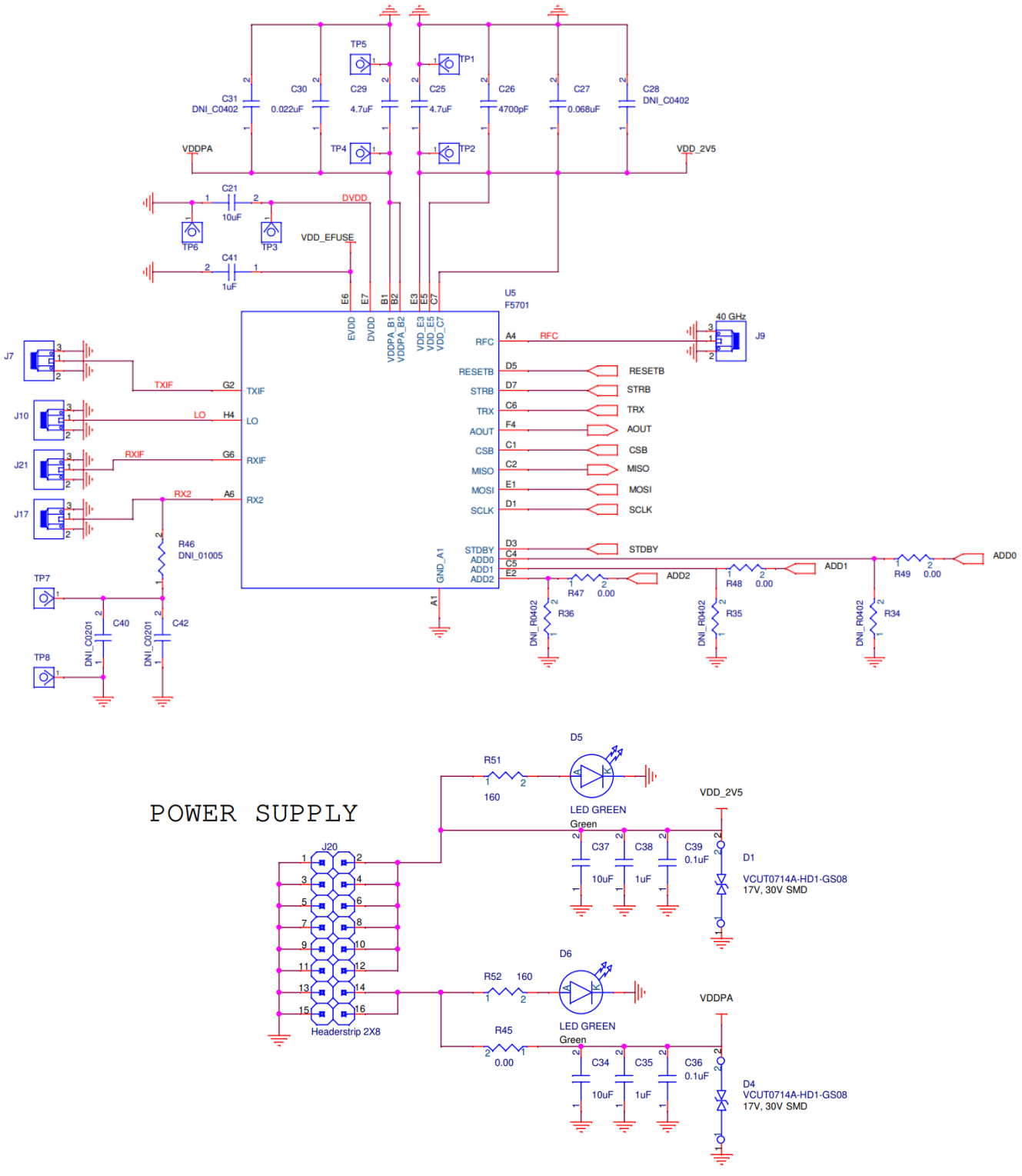

Figure 26. F5701 Evaluation Board Schematic – Part 1

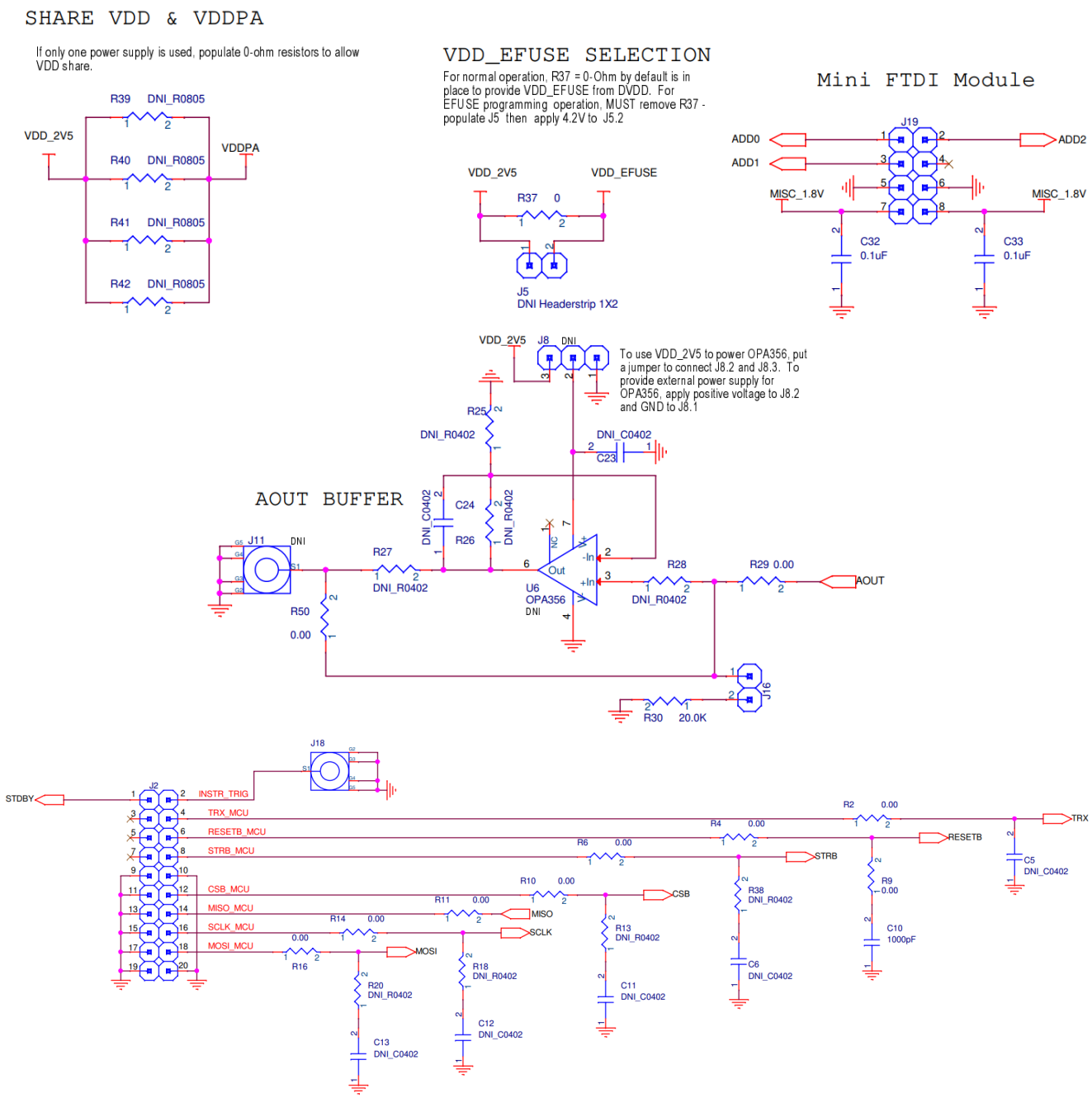

Figure 27. F5701 Evaluation Board Schematic – Part 2

3.2 Bill of Materials (BOM)

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C5, C6, C11, C12, C13, C23, C24, C28, C31	9	TBD Surface Mount Capacitor	DNI	
C10	1	COG Surface Mount Capacitor, 1000pF	GRM1555C1E102J	Murata
C21, C34, C37	3	X5R Surface Mount Capacitor, 10µF	GRM155R60J106M	Murata
C25, C29	2	X5R Surface Mount Capacitor, 4.7uF	GRM035R60J475ME15D	Murata
C26	1	X7R Surface Mount Capacitor, 4700pF	GRM033R71E472K	Murata
C27	1	X5R Surface Mount Capacitor, 0.068µF	GRM033R61C683K	Murata
C30	1	X5R Surface Mount Capacitor, 0.022µF	GRM033R61C223K	Murata
C32, C33, C36, C39	4	X7R Surface Mount Capacitor, 0.1µF	GRM155R71C104KA88D	Murata
C35, C38, C41	3	X5R Surface Mount Capacitor, 1µF	CL05A105KA5NQNC	Samsung
C40, C42	2	TBD Surface Mount Capacitor	DNI	
D1, D4	2	Surface Mount Diode	VCUT0714A-HD1-GS08	Vishay
D5, D6	2	Green LED, SMD	APHHS1005CGCK	Kingbright
J2	1	Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240-inch contact mating length	10-89-7200	Molex
J5	1	Header, 2 × 10 Vertical	DNI	
J7, J9, J10, J17, J21	5	2.92mm edge launch, Female Standard Profile	ELF40-002	Signal Microwave
J8	1	Header, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240-inch contact mating length	22-28-4033	Molex
J11	1	SMB Connector Jack, Male Pin 50Ω Through Snap Connect	1-1337482-0	TE Connectivity
J16	5	Header, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240-inch contact mating length	22-28-4023	Molex
J18	1	MCX Connector Jack, Female Socket 50Ω Through Hole Solder	0733660061	Molex
J19	1	C-Grid Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch	10-89-7080	Molex
J20	1	Header Dual, Gold, Unshrouded, 100mil pitch, 0.062-inch contact mating length	68602-116HLF	Amphenol FCI
R2, R4, R6, R9, R10, R11, R14, R16, R29, R47, R48, R49, R50	13	Surface Mount Resistor	ERJ-2GE0R00	Panasonic
R13, R18, R20, R25, R26, R27, R28, R34, R35, R36, R38	11	Surface Mount Resistor	DNI	-

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
R30	1	Surface Mount Resistor	RCG040220K0FK	Vishay
R37	1	Surface Mount Resistor	ERJ-2GE0R00	Panasonic
R39, R40, R41, R42	4	Surface Mount Resistor	DNI	-
R45	1	Surface Mount Resistor	CRCW08050000Z0EA	Vishay
R46	1	Surface Mount Resistor	DNI	-
R51, R52	2	Surface Mount Resistor	CRCW0402160RFK	Vishay
SO1, SO2, SO3, SO4	4	Hex Standoff Threaded M3 Nylon 0.984" (25.00mm) Natural	25506	Keystone Electronics
TP1, TP2, TP3, TP4, TP5, TP6	4	Phosphor Bronze Wire Loop	5000	Keystone Electronics
U5	1	mmWave Upconverter/Downconverter 24.25GHz to 29.5GHz RF, 2.5GHz to 7GHz IF	F5701	Renesas
U6	1	Voltage Feedback Amplifier 1 Circuit Rail-to-Rail SOIC8	OPA356AID	TI

4. Ordering Information

Part Number	Description
RTKA81F5701000RU	F5701 24GHz to 30GHz Evaluation Board

5. Revision History

Revision	Date	Description
1.00	Sep 4, 2024	Initial release.

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