User's Manual

RENESAS

ISL91301AII-L-EV1Z, ISL91301AII-H-EV1Z
User's Manual: Evaluation Boards

Core Power Solutions

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1. Overview

The ISL91301AII-L-EV1Z and ISL91301AII-H-EV1Z platform allows quick evaluation of the high performance features of the ISL91301A multi-output PMIC, which has three controllers capable of configuring its power stages for 2+1+1 channel outputs. Each channel can deliver up to 4A per phase continuous output current for 2.8V ~ 5.5V supply voltage, or 3A per phase current for wider 2.5V ~ 5.5V supply voltage.

The ISL91301A uses the Renesas proprietary R5 modulator technology to maintain accurate voltage regulation, while providing excellent efficiency and transient response. It also supports the standard I^2C and SPI communication protocols, ideal for systems using a single-cell battery.

1.1 Key Features

- Small, compact design
- Supports both I^2C and SPI bus communication protocols
- Adjustable V_{OUT} and independent DVS control for all three channels
- Real-time fault protection and monitor (OC, UV, OV, OT)
- Six layer board design optimized for thermal performance and efficiency
- Connectors, test points, and jumpers for easy measurements
- Built-in load transient circuits for each output channel

1.2 Specifications

The board is designed to operate at the following operating conditions:

- ISL91301AII-L-EV1Z (VIN_SEL = GND)
  - Input voltage rating from 2.5V to 5.5V
  - 2+1+1 configuration with 3A maximum load current/phase
- ISL91301AII-H-EV1Z (VIN_SEL = AVIN)
  - Input voltage rating from 2.8V to 5.5V
  - 2+1+1 configuration with 4A maximum load current/phase
- Programmable output voltage range of 0.3V to 2V
- 4MHz default switching frequency
- DVS slew rate of 2.5mV/µs
- Power-up sequence: Buck1→Buck2→Buck3, 1ms delay between each rail
- Power-down sequence: Buck1, 2, and 3 power down at the same time
- Operating temperature range: -40°C to +85°C
- VOUT1, 2, and 3 = 0.9V

1.3 Related Literature

- For a full list of related documents, visit our website
  - ISL91301A product page

1.4 Ordering Information

Part Number	Description
ISL91301AII-L-EV1Z	Evaluation board. VIN_SEL = GND, V_{IN} = 2.5V to 5.5V, max current = 3A per phase
ISL91301AII-H-EV1Z	Evaluation board. VIN_SEL = AVIN, V_{IN} = 2.8V to 5.5V, max current = 4A per phase

1.5 Contents

- ISL91301AII-L-EV1Z or ISL91301AII-H-EV1Z evaluation board
- Evaluation software
- Mini USB I^2C dongle with USB cable (ISLUSBMINIEVAL1Z)
- Documentation

1.6 Recommended Equipment

- 0V to 10V power supply with at least 10A current sourcing capability (V_{IN} supply bias)
- 0V to 10V power supply with at least 1A current sourcing capability (VCC_6V supply bias)
- Electronic loads capable of sinking current up to 10A
- Digital multimeter
- 500MHz quad-trace oscilloscope
- Dual edge slew rate controllable signal generator
- Differential probe (for load transient current measurement)

1.7 Block Diagrams

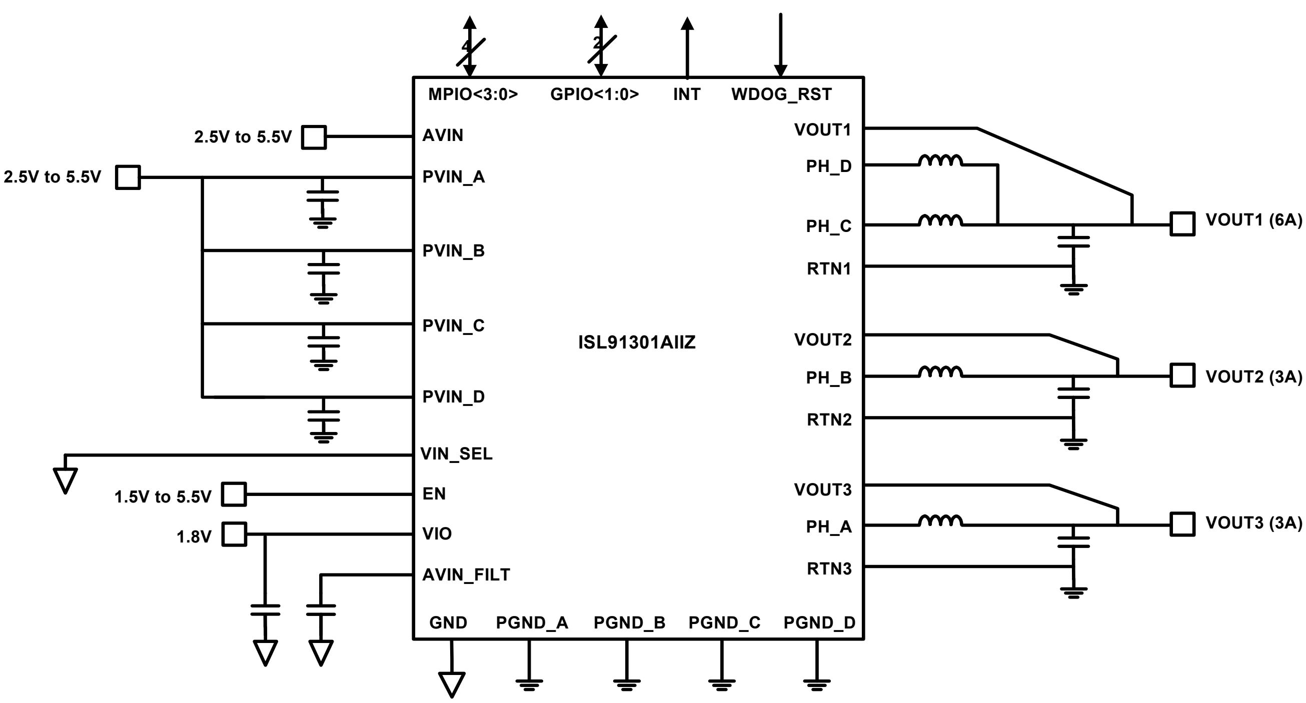


Figure 1. ISL91301A 2+1+1 Block Diagram (3A/Phase, VIN_min = 2.5V)

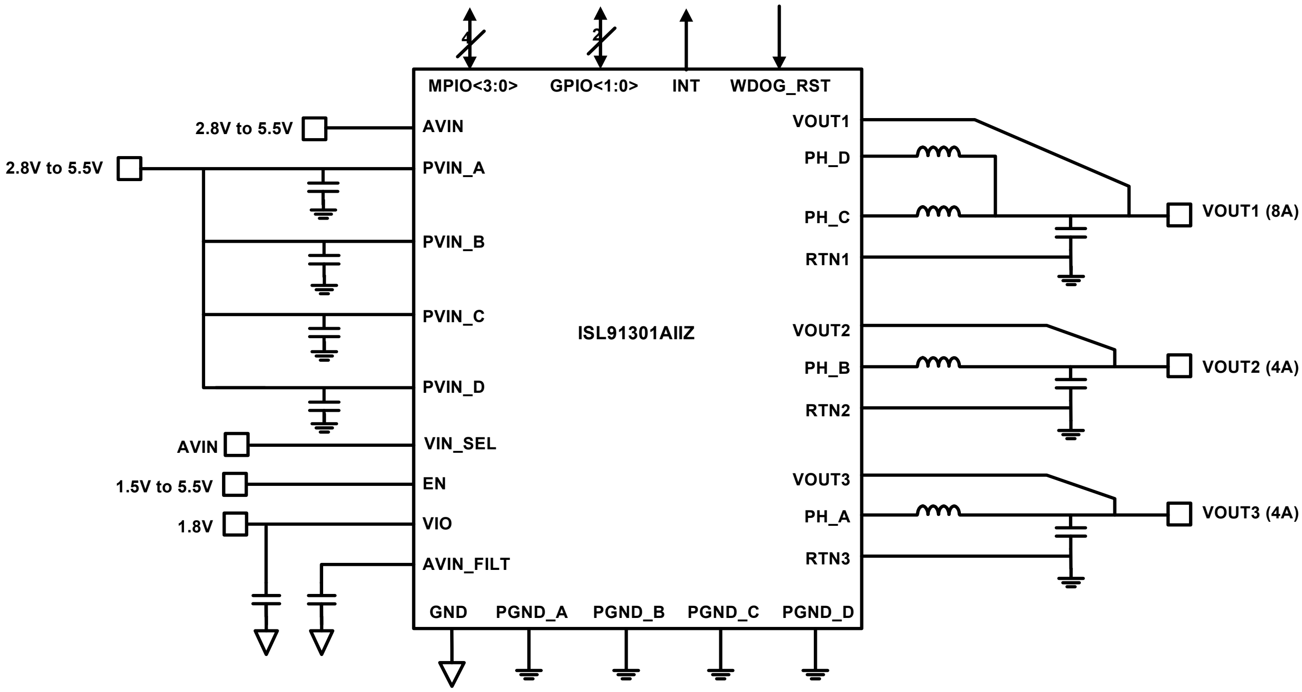


Figure 2. ISL91301A 2+1+1 Block Diagram (4A/Phase, VIN_min = 2.8V)

2. Functional Description

The ISL91301AII-L-EV1Z and ISL91301AII-H-EV1Z evaluation boards provide a simple platform to demonstrate the functionality of the feature-rich ISL91301A PMIC. It has a 0.9V output (default) on each of its output channels after start-up and each output voltage can be programmed by I^2C/SPI. The evaluation board has been functionally optimized for best performance, working harmoniously with the factory default tuning on the ISL91301A. The input power and load connections are provided through multi-pin connectors for high current operations.

The ISL91301AII-L-EV1Z and ISL91301AII-H-EV1Z evaluation boards are shown in Figure 10. Table 1 lists the evaluation board's key test points and jumpers. The ISL91301A's internal registers can be accessed by the I^2C/SPI through the on-board header J24 (SPI), J42 (I^2C), and J42B (I^2C).

Table 1. Description of Important Test Points and Jumpers

Test Point	Description
J6(+), J7(-)	Header for connecting V_{IN} supply
J35(+), J38(-)	Buck1 Header for connecting external load
J37(+), J58(-)	Buck2 Header for connecting external load
J57(+), J36(-)	Buck3 Header for connecting external load
J3	V_{IN} Kelvin connection for efficiency measurements
J15	Buck1 V_{OUT} Kelvin connection for efficiency measurements
J18	Buck2 V_{OUT} Kelvin connection for efficiency measurements
J56	Buck3 V_{OUT} Kelvin connection for efficiency measurements
TP1	VCC_6V SUPPLY for VIO LDO and load transient circuits
J60	Buck1 driver input for load transient circuit
J61	Buck2 driver input for load transient circuit
J62	Buck3 driver input for load transient circuit
J52	Load transient current sense, 1A/10mV
J55	Load transient current sense, 1A/10mV
J59	Load transient current sense, 1A/10mV
J24	Header for connecting to SPI interface
J42, J42B	Header for connecting to I^2C interface
SW1	Enable/disable IC

The evaluation software GUI for the ISL91301A is shown in Figure 9 on page 11. The schematic of the ISL91301AII-L-EV1Z and ISL91301AII-H-EV1Z evaluation boards are shown in Figure 14 on page 15. The PCB layout images for all layers are shown in Figures 19 through 26. The bill of materials of the ISL91301AII-L-EV1Z and ISL91301AII-H-EV1Z boards are shown in Table 3.5 on page 22.

2.1 Operating Range

The V_{IN} range of the board is 2.5V to 5.5V for the ISL91301AII-L-EV1Z with 3A per phase I_{OUT} range and 2.8V to 5.5V for the ISL91301AII-H-EV1Z with 4A per phase I_{OUT} range. The adjustable V_{OUT} range for both versions are from 0.3V to 2.0V. The operating ambient temperature range is -40°C to +85°C.

2.2 Quick Start Guide

For the ISL91301AII-L-EV1Z and ISL91301AII-H-EV1Z evaluation boards, the default output voltage is set at 0.9V for all three outputs. No jumper configurations are needed to power up the part into its default state, and all the settings and features are instead loaded through the one-time programmable memory inside the IC after the minimum bias conditions are met. Refer to the "Setup Guide" on page 6 on how to power up the board for proper operation.

2.2.1 Setup Guide

(1) Place scope probes on the V_{OUT} test point and other test points of interest.

(2) Connect a power supply to J6 (VIN SUPPLY), with voltage setting between 2.5V and 5.5V. This will bias the PVIN and AVIN pins, but not initiate the startup sequence, and the quiescent current should be less than 1mA.

(3) Connect a second power supply to TP1 (VCC_6V), with voltage set to 6V. This will bias the VIO and Chip Enable pin as well as the on-board load transient circuits. The ISL91301A will boot up its internal reference, load the default register settings, and then initiate the power-on sequence by toggling SW1 to the “ENABLE” position. All three outputs should turn on in Pulse Skipping mode if there are no external loads present, and V_{OUT} should default to 0.9V.

(4) During the startup sequence, all three outputs should turn on sequentially, from Buck1 to Buck2 and then Buck3. Buck1 will turn on with a 1.4ms delay from the Chip Enable pin going high, and the other buck regulators will turn on 1ms apart.

(5) To initiate a shutdown sequence, toggle SW1 to the “DISABLE” position. The ISL91301A will turn off all the buck regulators at the same time.

2.2.2 I^{2}C/SPI Communication

The ISL91301A supports I^{2}C communication by default. A USB to I^{2}C communication dongle (ISLUSBMINIEVAL1Z) is included with each ISL91301AII-L-EV1Z or ISL91301AII-H-EV1Z board, and the Renesas Graphical User Interface (GUI) supports this tool across all operating systems.

To communicate with ISL91301A using I^{2}C, connect the USB to I^{2}C dongle to J42B. Ensure R_{93} is present on the board, because it provides the pull-up from SPI_SS to 1.8V VIO supply.

Note: For the SPI communication option using the GUI, contact Renesas support.

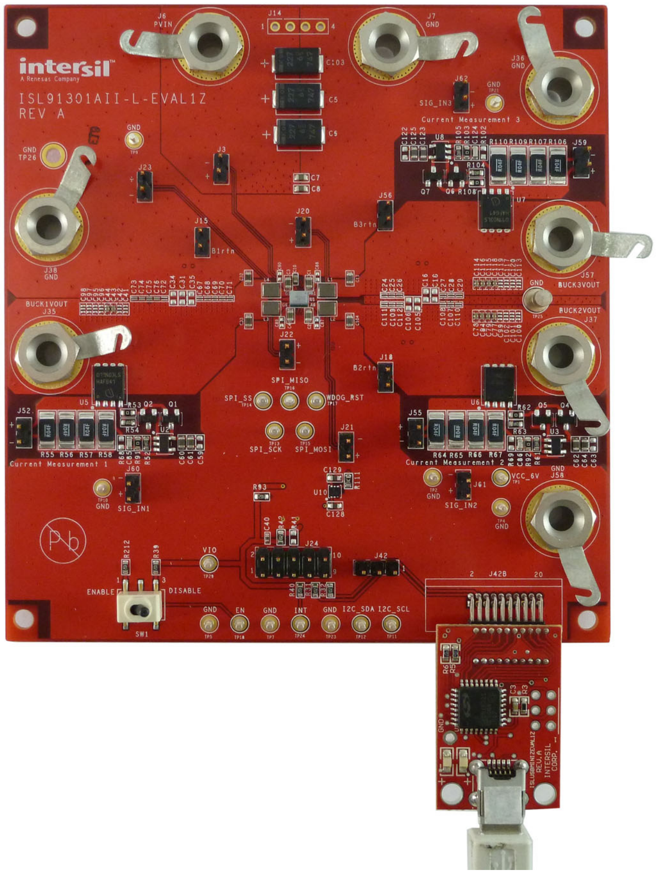


Figure 3. Communication Dongle Connection

2.2.3 Efficiency Measurement

(1) Connect a power supply at J6 (VIN supply), with the voltage setting between 2.5 and 5.5V for the ISL91301AII-L-EV1Z and between 2.8 and 5.5V for the ISL91301AII-H-EV1Z. The current limit should be set high enough to support the maximum load current with additional headroom. If the power supply supports remote sense lines, use a Kelvin connection on J3. Otherwise, connect a multimeter at J3.

(2) Apply 6V to TP1 (VCC_6V) to initiate the startup sequence and all three outputs will turn on. To get an accurate single channel measurement, disable the other two outputs using the GUI.

(3) Turn on the electronic load at VOUTx. The connection should be made at J35 (VOUT1), J37 (VOUT2), or J57 (VOUT3). Make sure the load current does not exceed 3A per phase for the ISL91301AII-L-EV1Z and 4A per phase for the for the ISL91301AII-H-EV1Z. Use the correct wire size when attaching the electronic load.

(4) Measure the output voltage with a multimeter. The voltage should regulate within datasheet spec limits.

(5) To determine efficiency, measure input and output voltages at the Kelvin sense test points (S+ and S-), which are located at J3 (VIN SENSE) and J15 (BUCK1 SENSE), J18 (BUCK2 SENSE), or J56 (BUCK3 SENSE) headers. Measure the input and output currents from the VIN power supply and the electronic load. Calculate efficiency based on these measurements. For detailed setup information, refer to Figure 12 on page 14.

2.2.4 Load Transient Measurement

(1) Go through the quick setup procedure (see "Setup Guide" on page 6). The ISL91301AII-L-EV1Z or ISL91301AII-H-EV1Z should already be powered up with 2.5 to 5.5V for the ISL91301AII-L-EV1Z and 2.8 to 5.5V for the ISL91301AII-H-EV1Z at J6 (VIN supply) and 6V at TP1 (VCC_6V).

(2) Connect a slew rate controllable signal generator to the transient load circuit input, J60 (TRANSIENT 1 PULSE GEN), J61 (TRANSIENT 2 PULSE GEN), or J62 (TRANSIENT 2 PULSE GEN).

(3) Program the signal generator to pulse mode, set the frequency to 100Hz, ON duration to 200µs, and signal amplitude from 0V to 2V. The load transient circuit starts to turn on when the input is ~2.6V. When in doubt, connect the signal generator output to an oscilloscope set to 1MΩ termination. The slew rate of the pulse, both rising and falling, should be conservatively slow, such as 1µs.

(4) Connect a differential probe to monitor load current across the sense resistors J52 (ISENSE1), J55 (ISENSE2), or J59 (ISENSE3). The load current can be accurately converted to a voltage at 1A/10mV. Make sure the vertical scale of the oscilloscope is set properly to display the full amplitude of the load profile.

(5) Connect a second differential probe at the VOUT sense points connected to the VOUT decoupling capacitors, J15 (BUCK1 SENSE), J18 (BUCK2 SENSE), or J56 (BUCK3 SENSE).

(6) Set the oscilloscope to measure the rise and fall times and maximum level of the load current. Slowly increase the signal generator amplitude and slew rate until the desired load profile is a achieved. For detailed setup information, refer to Figure 13 on page 14.

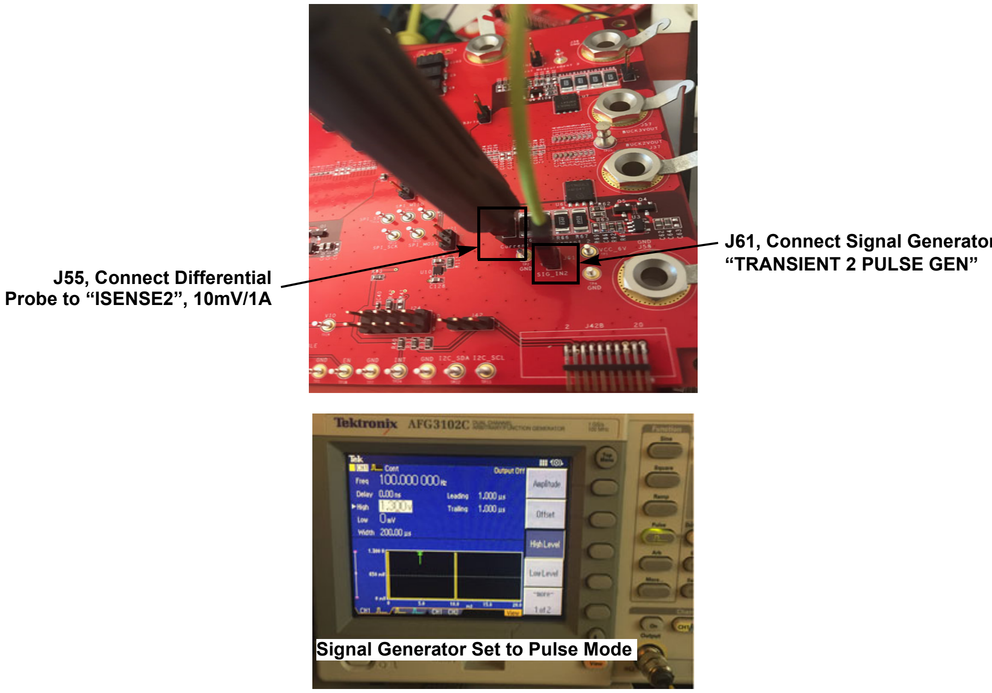


Figure 4. BUCK1 Transient Load Connection Example

2.3 Evaluation Software Installation and Use

(1) On the ISL91301AII-EV1Z evaluation CD, double-click AutoRun.exe. Follow the instructions to install the Multiphase PMIC I2C Control Tool software..

(2) Attach the USB-I2C interface (ISLUSBMINIEVAL1Z) dongle to the computer using the supplied USB cable.

(3) Attach the USB-I²C interface dongle to J42B on the ISL91301AII-EV1Z evaluation board. Following the instructions in "Setup Guide" on page 6, connect the power supplies, DC load, and other test equipment to the ISL91301AII-EV1Z evaluation board, then apply power.

(4) Start the Multiphase PMIC Control Tool software. Select Start > Programs > Renesas -> Multiphase PMIC I2C Control Tool.

(5) Select ISL91301 from the "Select Product" menu. Click "Connect" button ton the GUI to establish a connection between the GUI and the dongle. If the USB-I²C connection is established, the LED on the dongle will light up, and the "I2C Communication" check box in the GUI will show a green check mark. If a connection is not detected, the "I2C Communication" check box will show a red X. To troubleshoot, check the connections and ensure that the ISL91301AII-EV1Z is powered up.

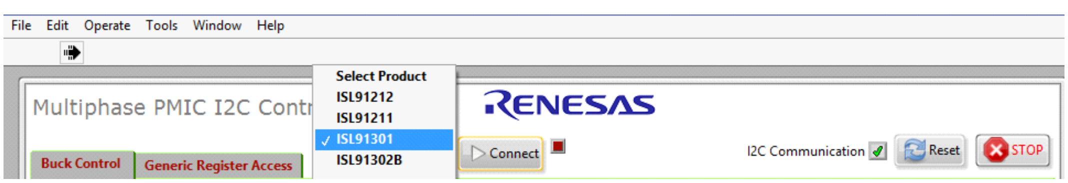


Figure 5. Product Selection Menu and I²C Communication OK Indicator

(6) After the evaluation software establishes a connection to the USB-I²C interface dongle, the software reads and updates the DVS registers and pointers to the programmed values.

(7) The user should see Buck1, Buck2, and Buck3 enabled, and the default DVS0 values should be 0.9V. If no fault conditions occurred during the board power-up, all the fault indicators (UV, OV, OC) should be clear rather than red.

(8) To change the output voltage, enter the desired value in voltages in the DVS0 control. There are also four default DVS values that are loaded as part of ISL91301A one-time programmable memory space. The user can go to any of them and activate a DVS command by clicking on the DVS Pointer.

Figure 6. DVS Pointer Selection

(9) Changing the ‘Max Voltage’ controls changes the internal feedback divider between ratios of 1x, 0.8x, and 0.6x. This will change the maximum output voltage ISL91301A can support, with the maximum being 2V. Keep in mind the smallest DVS resolution the IC and the software can support is no less than the maximum voltage divided by 1024.

(10) After the evaluation software is up and running without hiccup, it polls all the registers at 2s intervals by default. The user can disable this feature by clearing the “Continuous Read” option. Alternatively, the user can click “Read All Once” to perform a one-time read of all the registers.

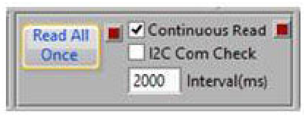


Figure 7. Continuous Read and Manual Read All Options

(11) The fault indicators self clear when the software reads the register through the Continuous Read or the “Read All Once” function. Three additional replica fault indicators (UV, OV, and OC) latch the faults so they will only clear after the user clicks “Push To Clear” in the event of a spurious fault condition.

Figure 8. Fault Indicators

Note: The default switching frequency of the ISL91301A is set to 4MHz and the slew rates for both DVS and power-up/down are set to 2.5mV/µs. These settings, along with many other features, are programmable only through OTP request or a Startup Script, not supported by the evaluation software. For more information, contact Renesas support.

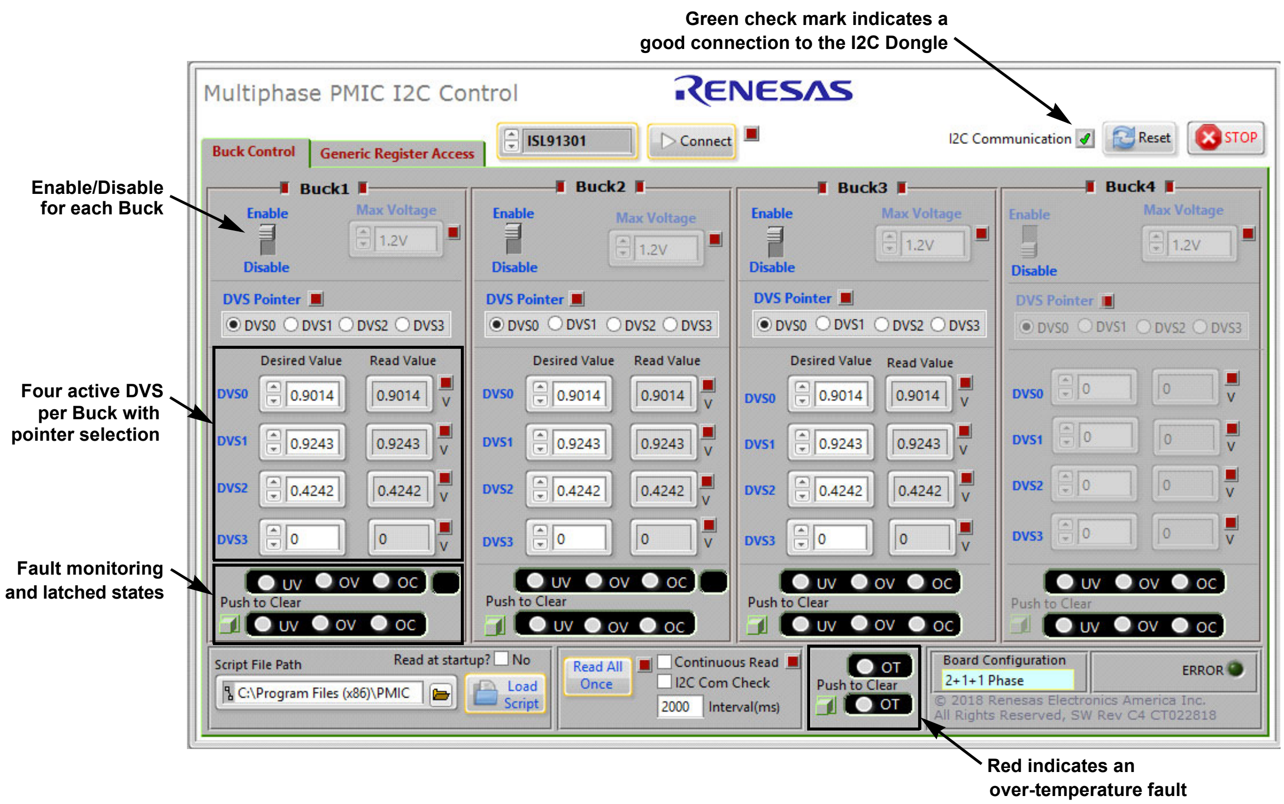


Figure 9. Multiphase PMIC (ISL91301A) I2C Control Tool Interface

3. PCB Layout Guidelines

The ISL91301AII-L-EV1Z and ISL91301AII-H-EV1Z boards are a 6-layer FR4 board. The main components are the ISL91301A, its passive filter components, test points, and connectors. A 220nH inductor is located close to each phase node of the ISL91301A, and 3x22µF plus 4x4.3µF capacitors are populated at the output of each inductor. PVIN is distributed using a power plane on an inner layer with a 10µF capacitor placed in close proximity to the PVIN and PGND balls of the power stage. In addition, there is a 10µF AVIN filter capacitor placed next to the ISL91301A referenced to a quiet ground plane.

The PCB layout is a critical design step to ensure that the designed converter works under optimum conditions. For the ISL91301A, the power loop is composed of the inductor, output capacitors, phase node, and PGND pins. It is necessary to keep this loop as short as possible and the connecting traces among them should be direct, short, and wide. The phase nodes of ISL91301A are very noisy, so keep remote sense signals away from traces coming out of the phase nodes, and do not route them under the inductor in an adjacent layer. The input capacitor should be placed as close as possible to the PVIN and PGND pins, and there should be a large unbroken ground plane that should connect all the decoupling capacitors together.

The heat of the ISL91301A is mainly dissipated through the GND and PHASE plane vias under the IC. To maximize thermal performance, use as much copper area as possible connecting to these vias. In addition, a solid ground plane is helpful for better EMI performance.

3.1 Summary of Key Layout Strategies

- Place input capacitors as close as possible to their respective PVIN and PGND pins to minimize parasitic loop inductance.
- Route phase nodes with short, wide traces and avoid any sensitive nodes.
- Route the remote sense lines directly to the load using small, low inductance capacitors at the load for bypassing.
- Output capacitors should be close to the inductors and have a low impedance path to the PGND pins.
- Keep digital and phase nodes from intersecting AVIN_FILT, VOUT, and RTN lines.
- Create a PGND plane on the 2nd layer of the PCB below the power components and bumps carrying high switching currents.

3.2 ISL91301AII-L/H-EV1Z Evaluation Board

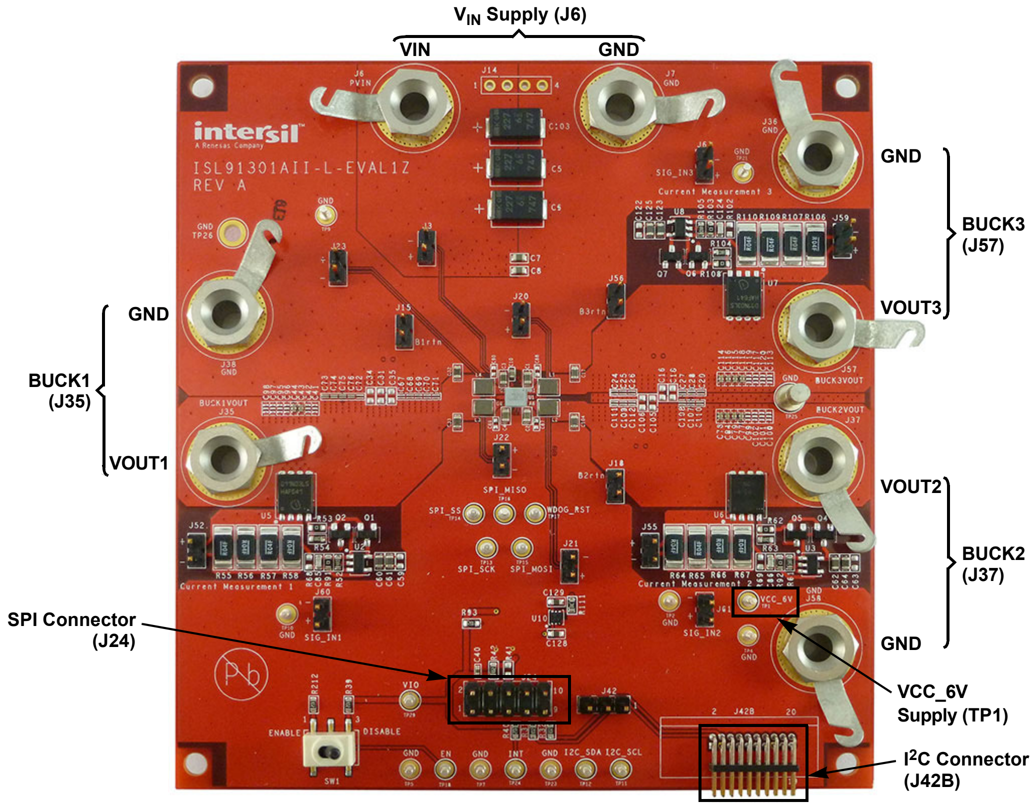


Figure 10. ISL91301AII-L/H-EV1Z Top View

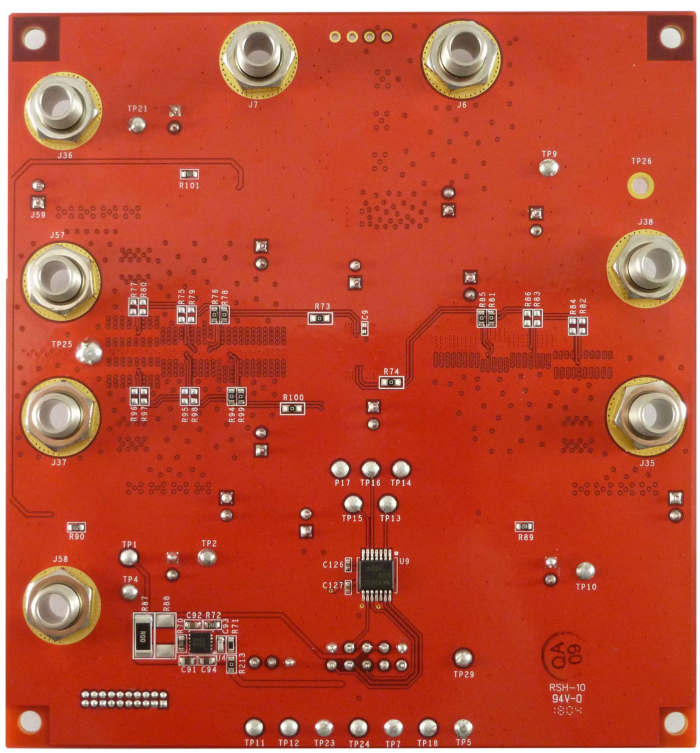


Figure 11. ISL91301AII-L/H-EV1Z Bottom View

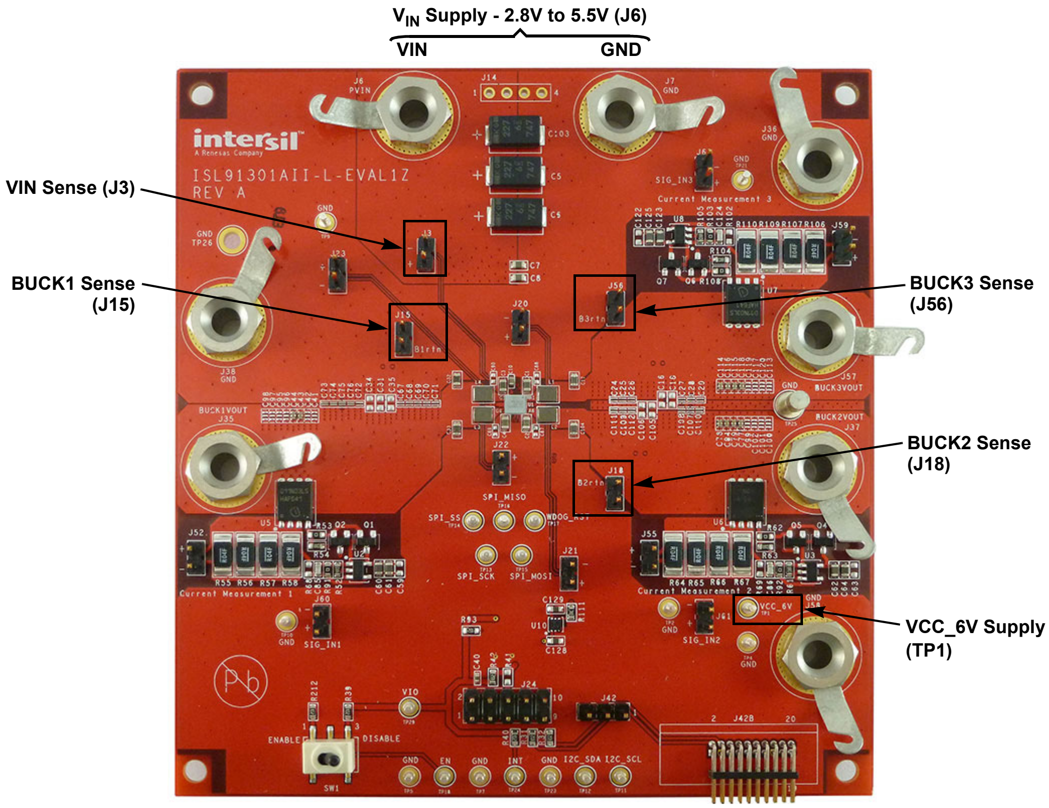


Figure 12. ISL91301AII-L/H-EV1Z Efficiency Measurement Connections

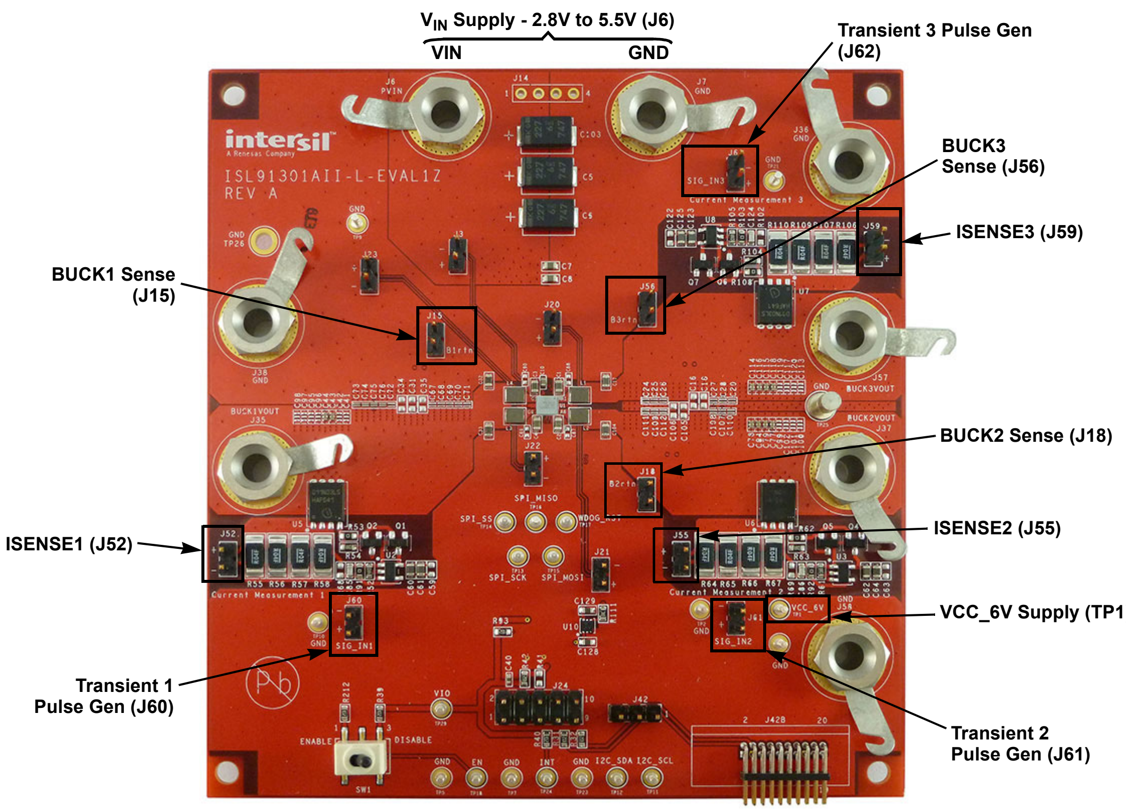


Figure 13. ISL91301AII-L/H-EV1Z Load Transient Measurement Connections

3.3 ISL91301AII-L/H-EV1Z Schematics

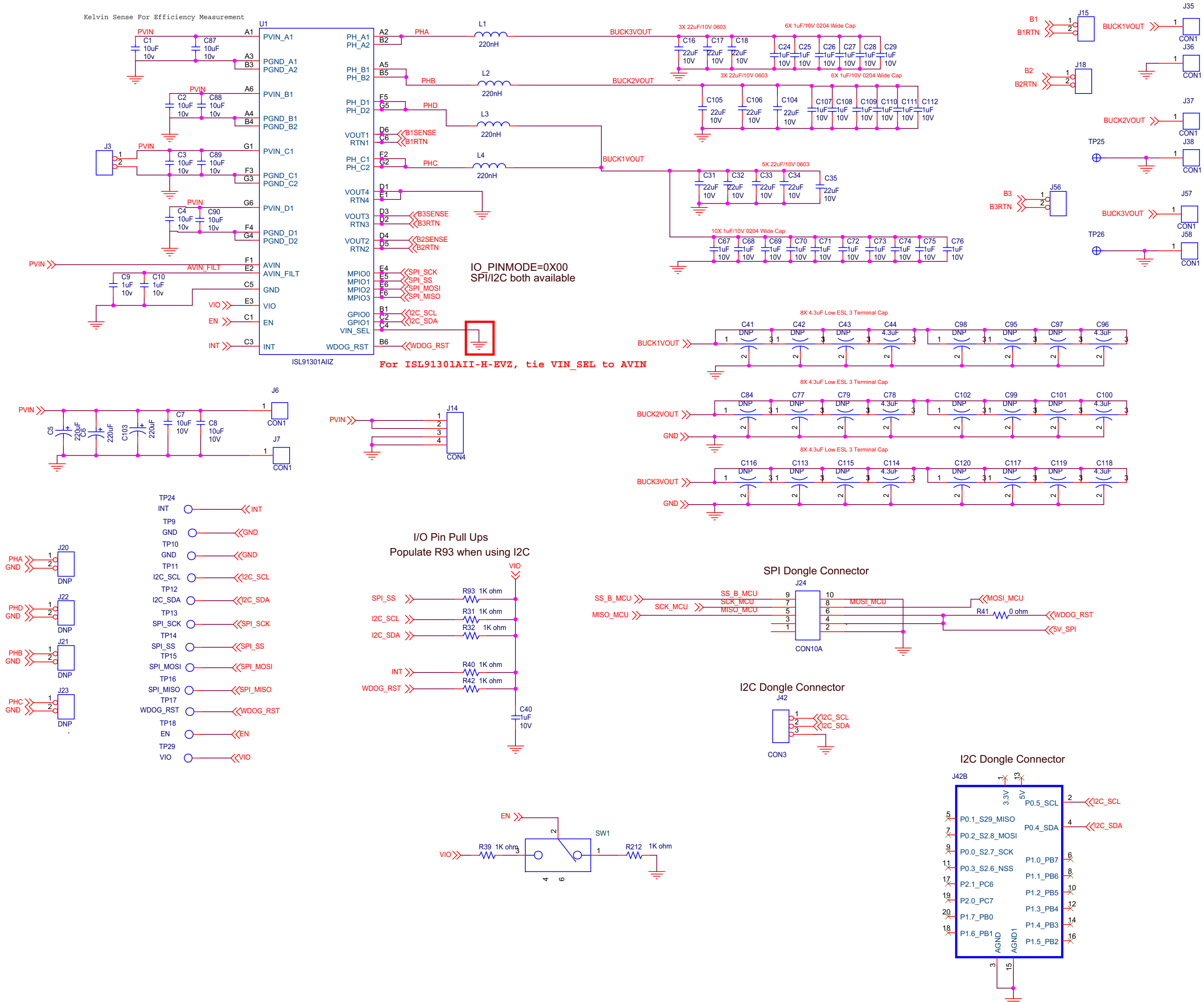


Figure 14. ISL91301AII-L/H-EV1Z Schematic - Page 1

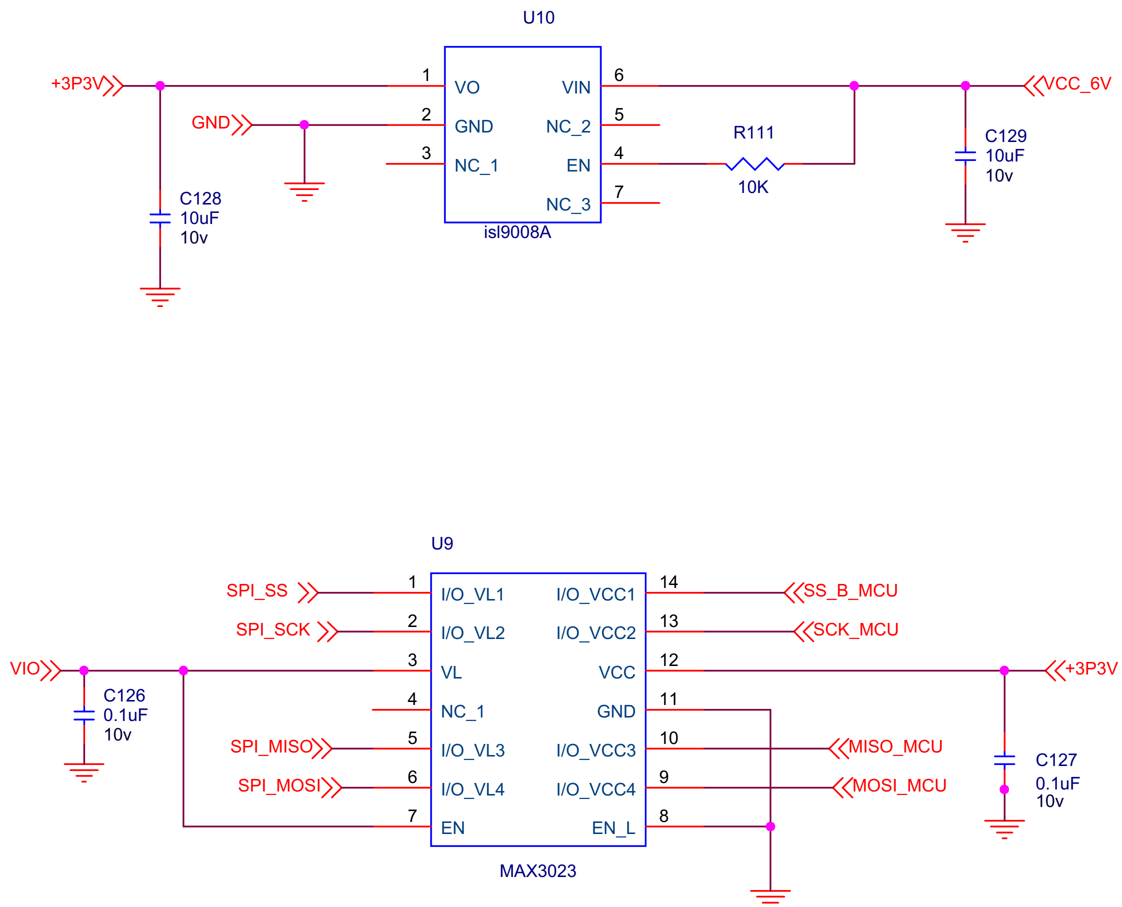


Figure 15. ISL91301AII-L/H-EV1Z Schematic - Page 2

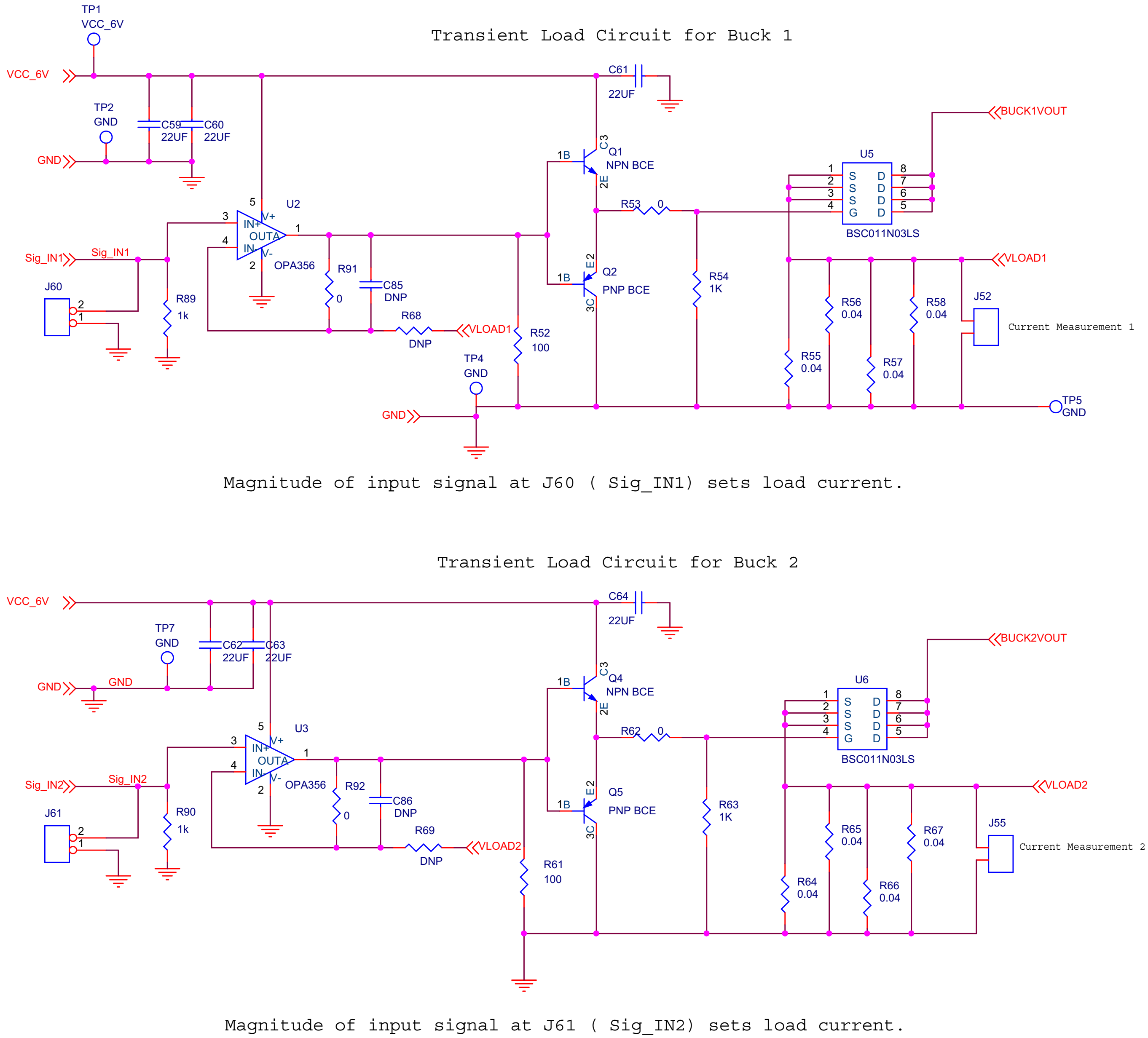
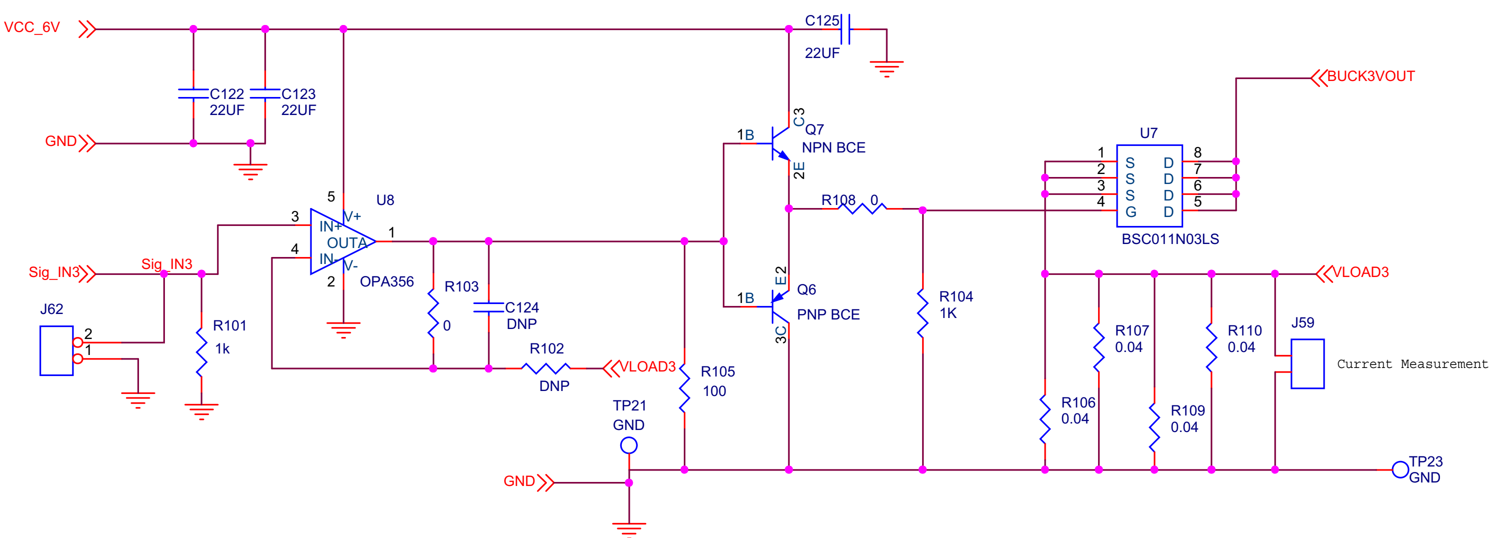


Figure 16. ISL91301AII-L/H-EV1Z Schematic - Page 3

Transient Load Circuit for Buck 3



Magnitude of input signal at J62 (Sig_IN3) sets load current.

Figure 17. ISL91301AII-L/H-EV1Z Schematic - Page 4

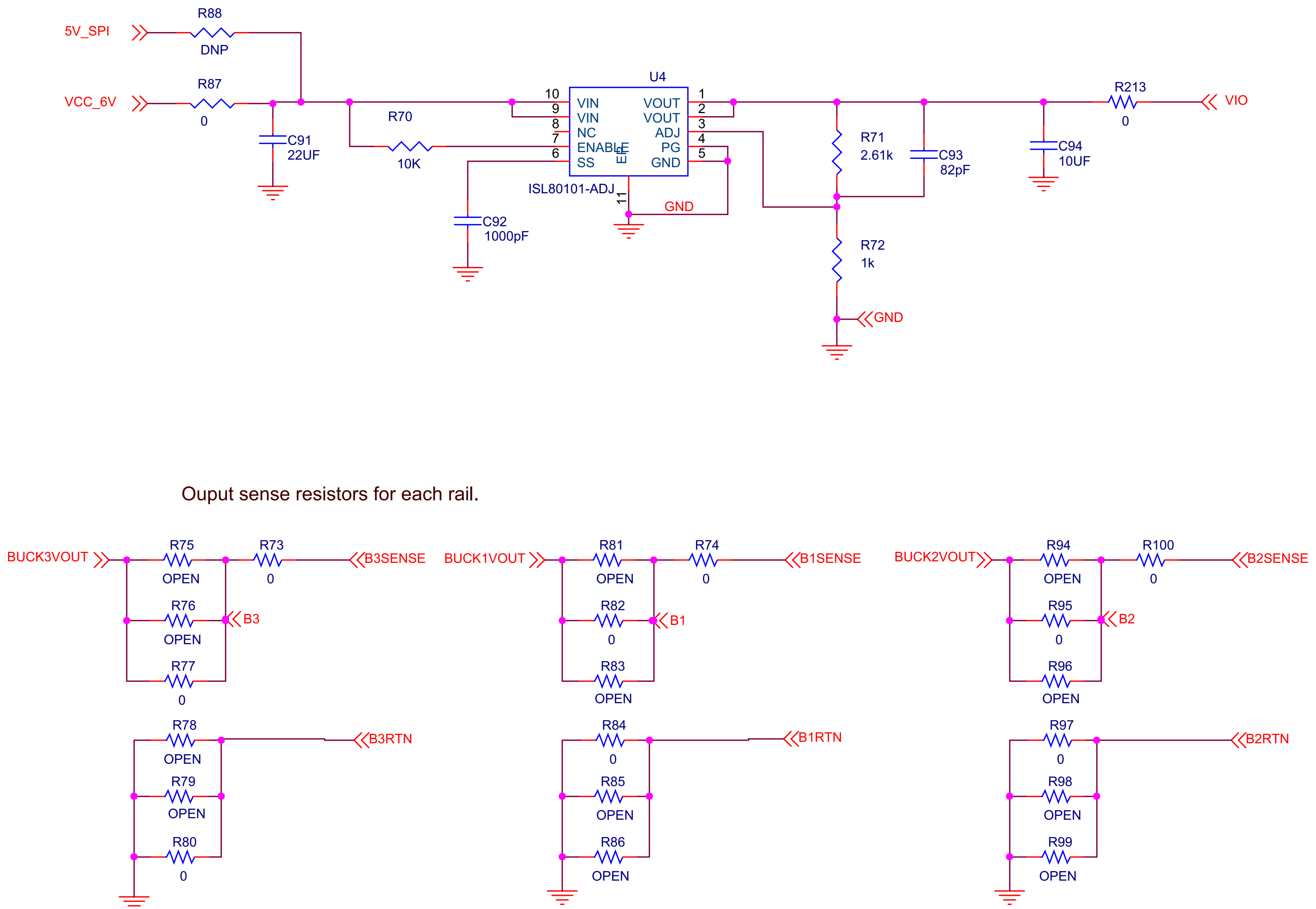


Figure 18. ISL91301AII-L/H-EV1Z Schematic - Page 5

3.4 ISL91301AII-L/H-EV1Z PCB Layout

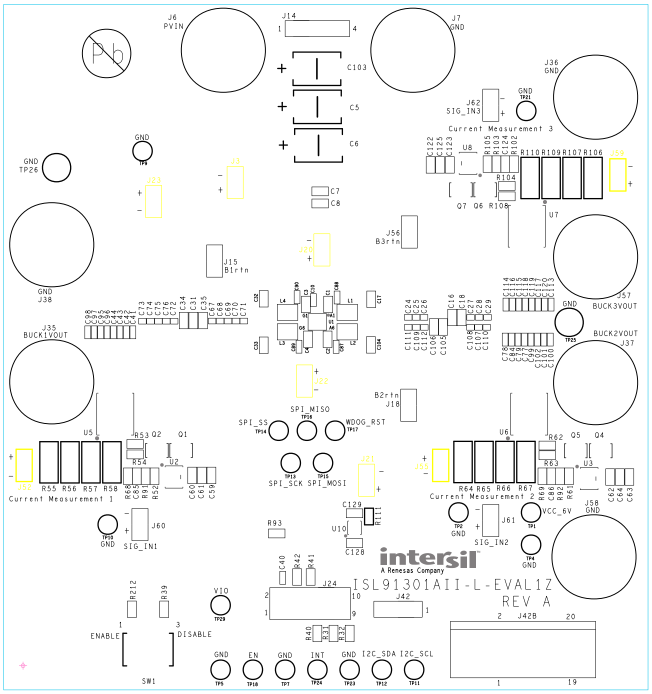


Figure 19. Top Silkscreen Layer

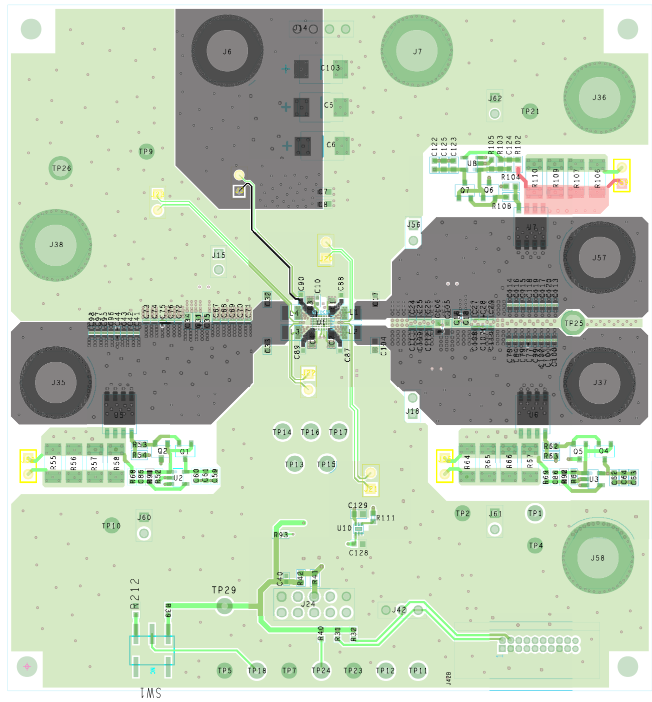


Figure 20. Top Layer

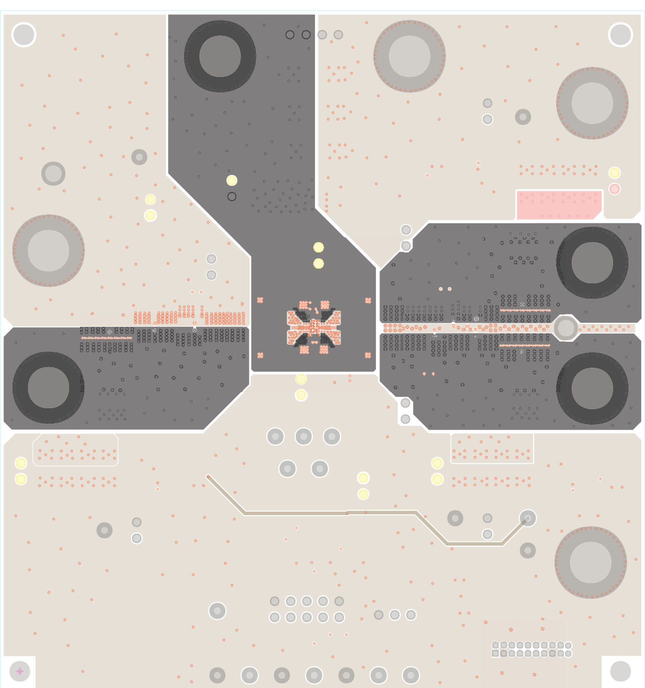


Figure 21. Layer 2 (PVIN Plane)

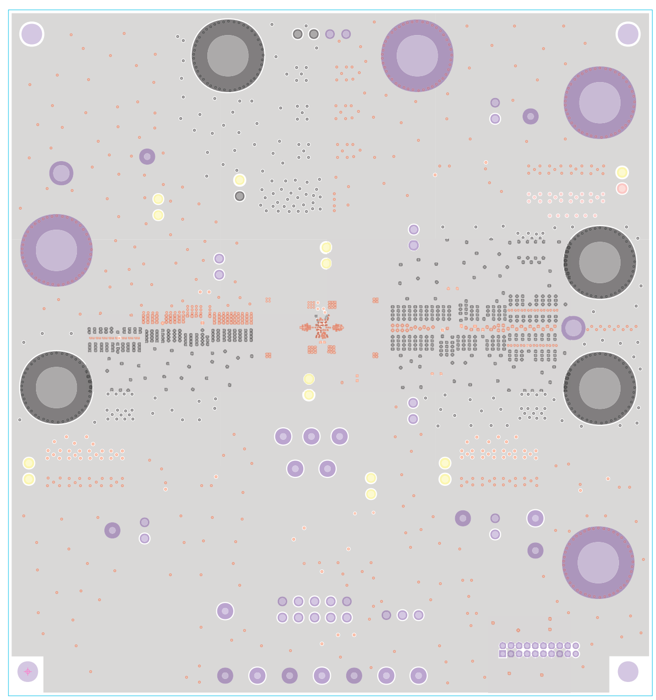


Figure 22. Layer 3 (GND Plane)

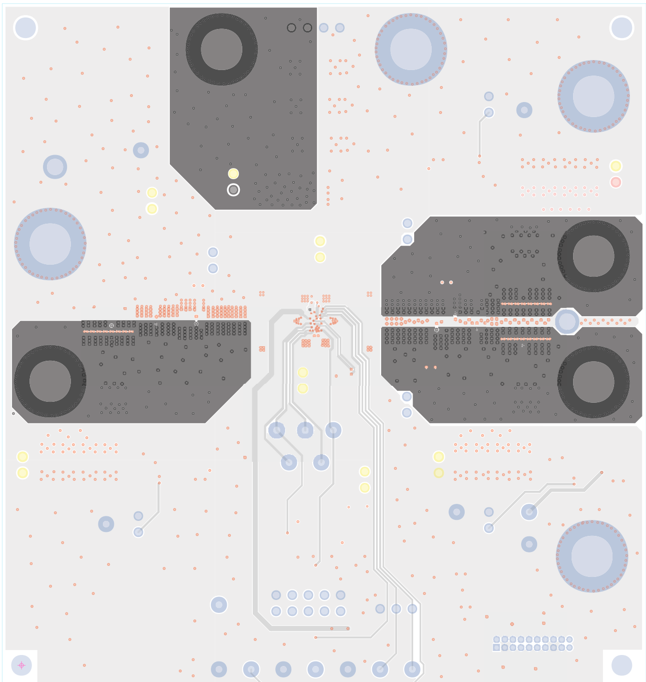


Figure 23. Layer 4 (IO Communications)

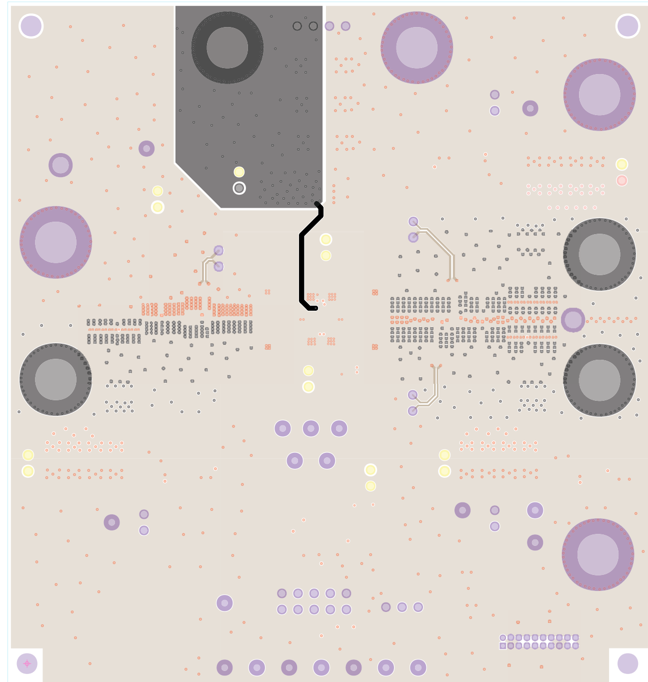


Figure 24. Layer 5 (GND Plane)

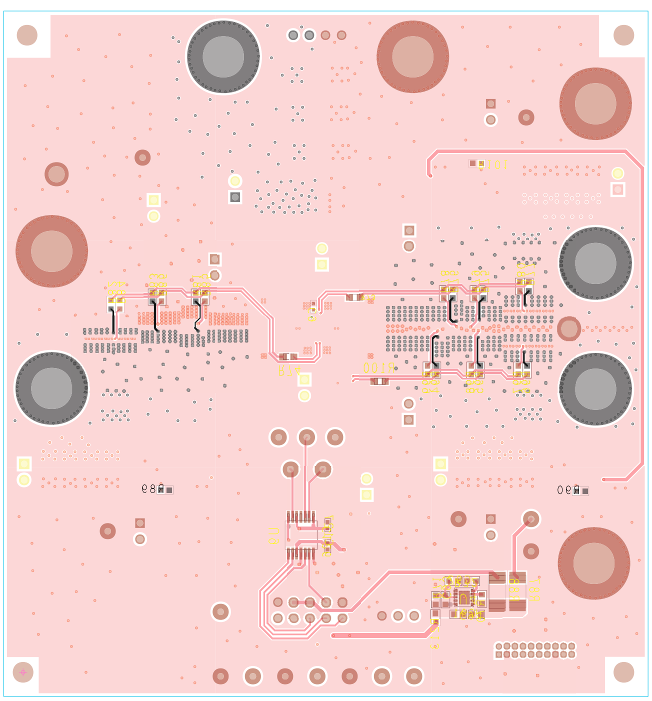


Figure 25. Bottom Layer (Remote Sense Lines)

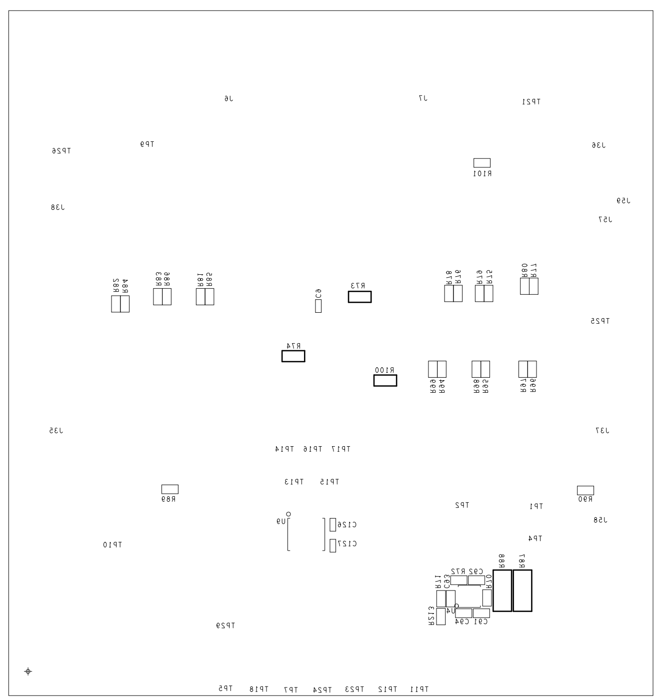


Figure 26. Bottom Silk Screen Layer

3.5 ISL91301AII-L-EV1Z and ISL91301AII-H-EV1Z Bill of Materials

Qty	Reference Designator		Description	Digi-Key Part Number	Manufacturer	Manufacturer Part Number
	Top Components	Bottom Components				
1		C92	1000pF, 100V, X7R, 0603	587-1445-1-ND	Taiyo Yuden	HMK107B7102KA-T
2		C126, C127	0.1µF, 10V, X5R, 0402	587-1227-1-ND	Taiyo Yuden	LMK105BJ104KV-F
1	C40		1µF, 10V, X5R, 0402	587-1454-1-ND	Taiyo Yuden	LMK105BJ105KV-F
2	C128, C129		1µF, 10V, X5R, 0603	587-4281-1-ND	Taiyo Yuden	LMK107BJ105KA-T
4	C73, C74, C75, C76		1µF, 6.3V, X5R, 0204	587-3107-1-ND	Taiyo Yuden	JWK105BJ105MP-F
10	C43, C44, C77, C78, C79, C84, C114, C115, C116, C118		4.3µF Multi-Terminal, 4V, X5R, 0402	n/a	Murata	LLD154R60G435ME01
7	C1, C2, C3, C4, C7, C8	C94	10µF, 10V, X5R, 0603	587-3412-1-ND	Taiyo Yuden	LMK107BBJ106MAHT
1	C10		10µF, 10V, X5R, 0402	1276-1450-1-ND	Samsung Electronics	CL05A106MP5NUNC
13	C17, C32, C33, C60, C61, C62, C64, C104, C123, C125	C91	22µF, 10V, X5R, 0603	445-9077-1-ND	TDK	C1608X5R1A226M080AC
3	C5, C6, C103		220µF, 6.3V, Polymer Tant, D Case	399-4043-1-ND	KEMET	T520D227M006ATE040
16	R53, R62, R108, R91, R92, R103	R73, R74, R78, R76, R85, R81, R99, R94, R100, R213	0Ω, 1/10W, 0603	P0.0GCT-ND	Panasonic	ERJ-3GEY0R00V
1		R87	RES SMD 0.0Ω JUMPER 3/4W 2010	RMCF2010ZT0R00CT-ND	Stackpole	RMCF2010ZT0R00
12	R55, R56, R57, R58, R64, R65, R66, R67, R106, R107, R109, R110		0.04Ω, 1%, 1W, 2010	WSLF-.04CT-ND	Vishay	WSL2010R0400FEA18
3	R52, R61, R105		100Ω, 1%, 1/10W, 0603	P100HCT-ND	Panasonic	ERJ-3EKF1000V
14	R31, R32, R39, R40, R42, R93, R212, R54, R63, R104	R72, R89, R90, R101	1.0kΩ, 1%, 1/10W, 0603	P1.00KHCT-ND	Panasonic	ERJ-3EKF1001V
1		R71	2.61kΩ, 1%, 1/10W, 0603	P2.61KHCT-ND	Panasonic	ERJ-3EKF2611V
1		R70	10kΩ, 1%, 1/10W, 0603	P10.0KHCT-ND	Panasonic	ERJ-3EKF1002V
1	R111		10kΩ, 1%, 1/10W, 0603	P10.0KLCT-ND	Panasonic	ERJ-2RKF1002X
4	L1, L2, L3, L4		0.22µH, 10mΩ, 6.6Asat, 2520 Inductor	n/a	Cyntec	PIFE25201T-R22MS
3	Q1, Q4, Q7		TRANS NPN 40V 0.2A SOT-23	MMBT3904FSCT-ND	Fairchild	MMBT3904

Qty	Reference Designator		Description	Digi-Key Part Number	Manufacturer	Manufacturer Part Number
	Top Components	Bottom Components				
3	Q2, Q5, Q6		TRANS PNP 40V 0.2A SOT-23	MMBT3906FSCT-ND	Fairchild	MMBT3906
8	J6, J7, J35, J36, J37, J38, J57, J58		CONN BANANA JACK THREADED 12AWG	J10138-ND	Cinch Connectivity	108-0740-102
19	TP1, TP2, TP4, TP5, TP7, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP21, TP23, TP24, TP29		Conn-Gen, Compact Test Point, Vertical, White	36-5007-ND	Keystone	5007
14	J3, J15, J18, J20, J21, J22, J23, J52, J55, J56, J59, J60, J61, J62		2 Pin Header, 100 mil spacing	609-4434-ND	FCI	77311-118-02LF
1	J24		2x5 Pin Header, 100 mil spacing	952-2380-ND	Harwin Inc	M20-9980545
1	J42		3 Pin Header, 100 mil spacing	952-1312-ND	Harwin	M22-2510305
1	J42B		Right angle connector	952-1398-ND	Harwin Inc.	M50-3901042
1	J24		2x5 Pin Header, 100 mil spacing	952-2380-ND	Harwin Inc	M20-9980545
1	SW1		SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-NONE-ON, ROHS	CKN1784CT-ND	ITT INDUSTRIES/ C&K DIVISION	GT11MSCBE
1	TP25		Turret Binding Post	36-1514-2-ND	Keystone	1514-2
1	U1		ISL91301AIIZ, 0.4mm Pitch WLCSP	n/a	Renesas	ISL91301AIIZ
3	U2, U3, U8		IC OPAMP VFB 200MHZ RRO SOT23-5	296-32191-1-ND	Texas Instruments	OPA356AIDBVR
1		U4	IC REG LDO ADJ 1A 10DFN	ISL80101IRAJZ-TKCT-ND	Renesas	ISL80101IRAJZ
3	U5, U6, U7		MOSFET N-CH 30V 100A 8TDSON	BSC011N03LS	Infineon	BSC011N03LSCT-ND
1		U9	IC TRANSLATOR LVL 100MBPS 14TSSO	MAX3023EUD+	Maxim	MAX3023EUD+-ND
1	U10		IC REG LDO 3.3V 0.15A SC70-5	ISL9008AIENZ-TCT-ND	Renesas	ISL9008AIENZ-T
1	J14		4 Pin Header, 100 mil spacing		any	any
5	C87, C88, C89, C90	C9	Capacitor, 0402, DNP		any	any
18	C24, C25, C26, C27, C28, C29, C67, C68, C69, C70, C71, C72, C107, C108, C109, C110, C111, C112		Capacitor, 0204, DNP		any	any

Qty	Reference Designator		Description	Digi-Key Part Number	Manufacturer	Manufacturer Part Number
	Top Components	**Bottom Components**				
14	C41, C42, C95, C96, C97, C98, C99, C100, C101, C102, C113, C117, C119, C120		Capacitor, Multi-terminal		any	any
13	C16, C18, C31, C34, C35, C59, C63, C105, C106, C122, C85, C86, C124		Capacitor, 0603, DNP		any	any
13	R41, R68, R69, R102	R75, R77, R79, R80, R82, R83, R84, R86, R95, R96, R97, R98	Resistor, 0603, DNP		any	any
1		R88	Resistor, 2010, DNP		any	any

Note: Components highlighted in red are DNP.

4. Typical Performance Curves

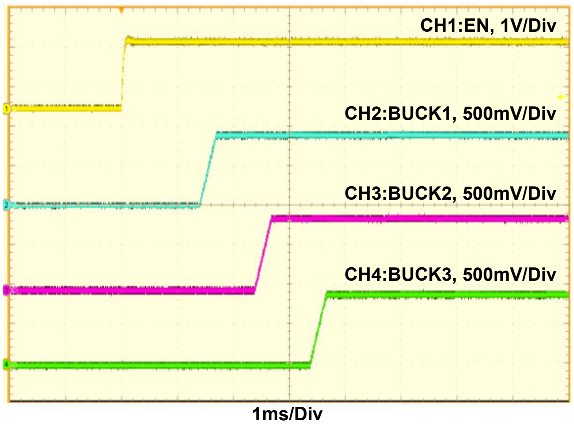


Figure 27. Startup-Up by EN, VOUT1, 2, 3 = 0.9V

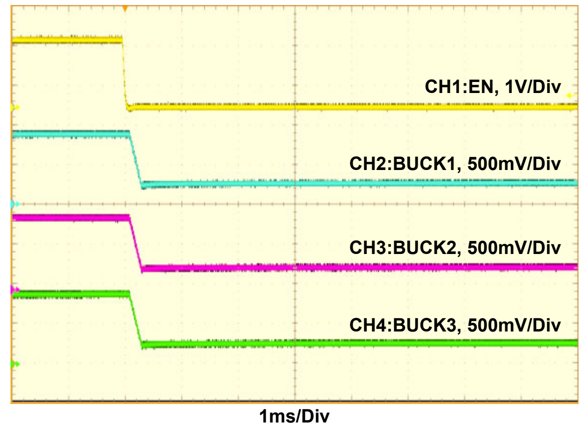


Figure 28. Shutdown by EN, VOUT1, 2, 3 = 0.9V

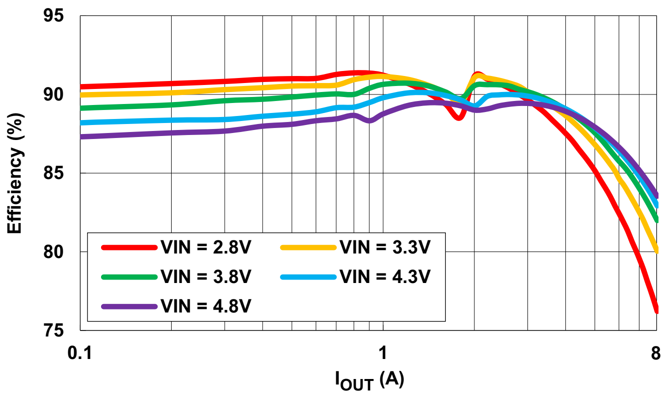


Figure 29. Dual-Phase Efficiency (V_{OUT} = 1V), Continuous Load Sweep (0.1A to 8A), Switching Frequency = 4MHz

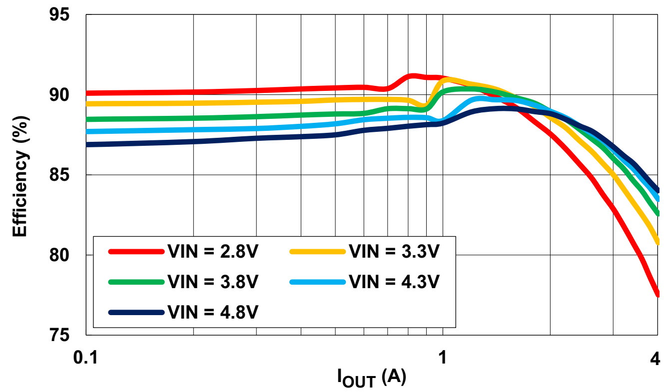
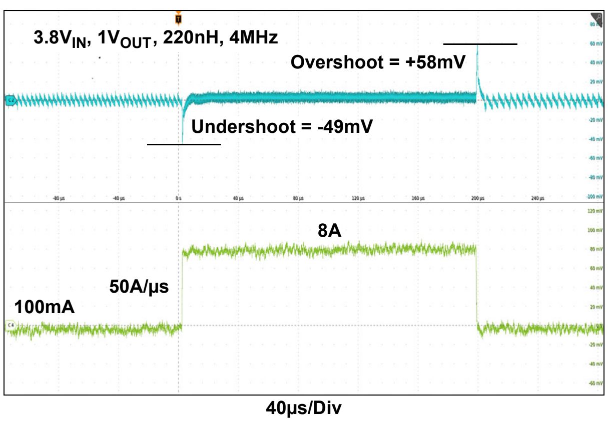
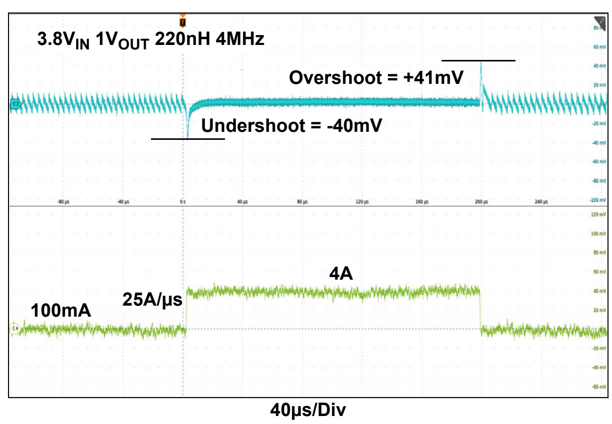


Figure 30. Single-Phase Efficiency (V_{OUT} = 1V), Continuous Load Sweep (0.1A to 4A), Switching Frequency = 4MHz



Load Step Slew Rate: 50A/µs, 0.1A to 8A
220nH Inductor (Cyntec PIFE25201T-R22MS)
2x22µF Capacitor (0603 6.3V Murata)
2x4.3µF Capacitor (0402 Low ESL Murata)
4x1µF Capacitor (0204 Taiyo Yuden)

Figure 31. Dual-Phase Load Transient (8A/160ns)



Load Step Slew Rate: 25A/µs, 0.1A to 4A
220nH Inductor (Cyntec PIFE25201T-R22MS)
2x22µF Capacitor (0603 6.3V Murata)
2x4.3µF Capacitor (0402 Low ESL Murata)

Figure 32. Single-Phase Transient (4A/160ns)

5. Revision History

Rev.	Date	Description
0.00	Apr 6, 2018	Initial release

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