PTX105R-EB-ST-QFN56-POS_IoT (v2.0)

This document describes how the PTX105R demonstration (demo) board can be operated with two selectable voltage settings by moving the jumper from JMP_VBUS to JMP_DCDC. The board also provides easy interfacing options to a PC via USB or to a microcontroller board via PMOD.

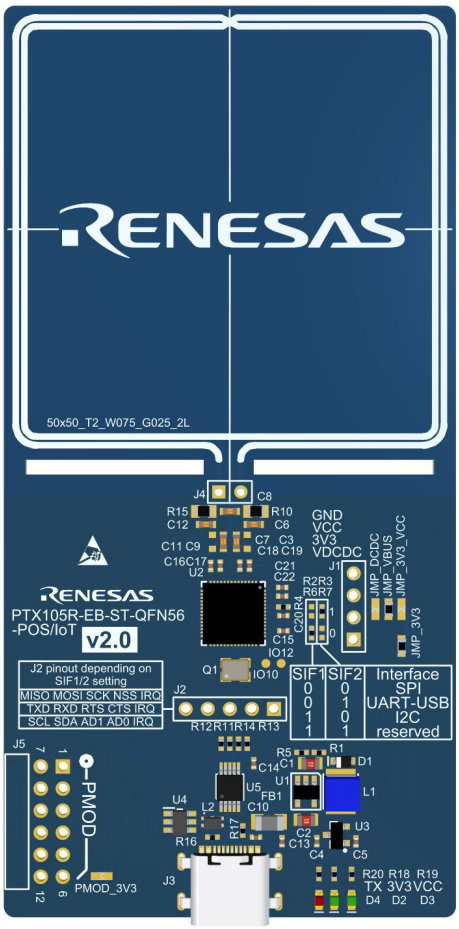


Figure 1. PTX105R-EB-ST-QFN56-POS_IoT Demo Board

Contents

1. Power Supply

The board is powered via a USB-C connection.

The PTX105R can be operated in two voltage settings which can be selected by moving the jumper from JMP_VBUS to JMP_DCDC:

- VBUS (5V)

or

- VDCDC (5.4V)

The board's default is VBUS which is also the setting that the compliance tests were performed in.

Current consumption in continuous field mode is ~360mA with VBUS and ~450mA with VDCDC.

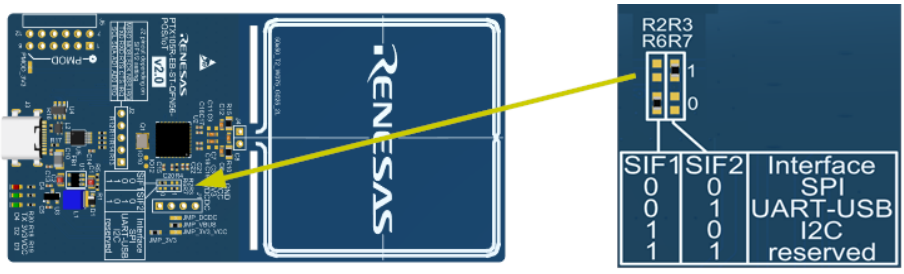
2. USB Interface

The USB Interface is handled by a CH340E USB to UART bridge.

Drivers can be downloaded from the manufacturer's webpage.

3. Interface Switching

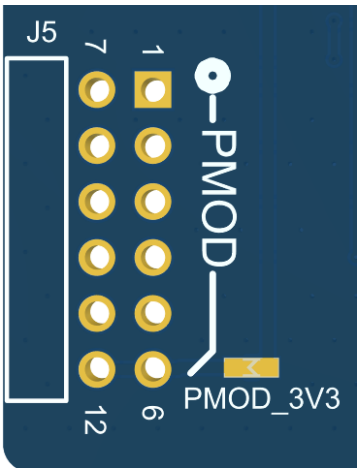
The evaluation board allows the user to switch between three interfaces supported by the PTX105R IC using the SIF1 / SIF2 jumpers:

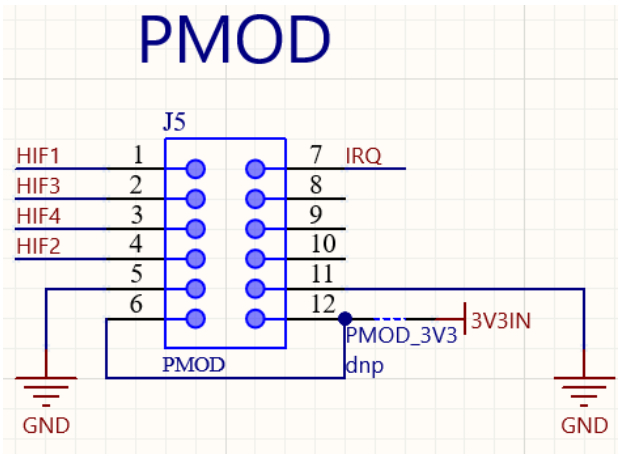
SIF1	SIF2	Interface	Jumpers Used
0	0	SPI	
0	1	UART to USB	
1	0	I^2C	

The UART Interface is connected to the USB bridge and can be accessed via the USB-C plug.

4. PMOD

All interfaces are also available via a PMOD 2 × 6 pin connector (must be soldered manually). The pinout follows the PMOD recommendation for an SPI Interface. The PMOD connector allows connecting to a multitude of MCU demo boards. Example firmware is available for the Renesas TB-S3A1 board.





The 3.3V supply for the host MCU can also be provided by the demo board if jumper PMOD_3V3 is placed

5. Clocking

The PTX105R device's default clock source is a 27.12MHz crystal (Q1).

6. Debugging

The PCB has three debug LEDs:

- Two for supply (green)
- One for UART communication (red)

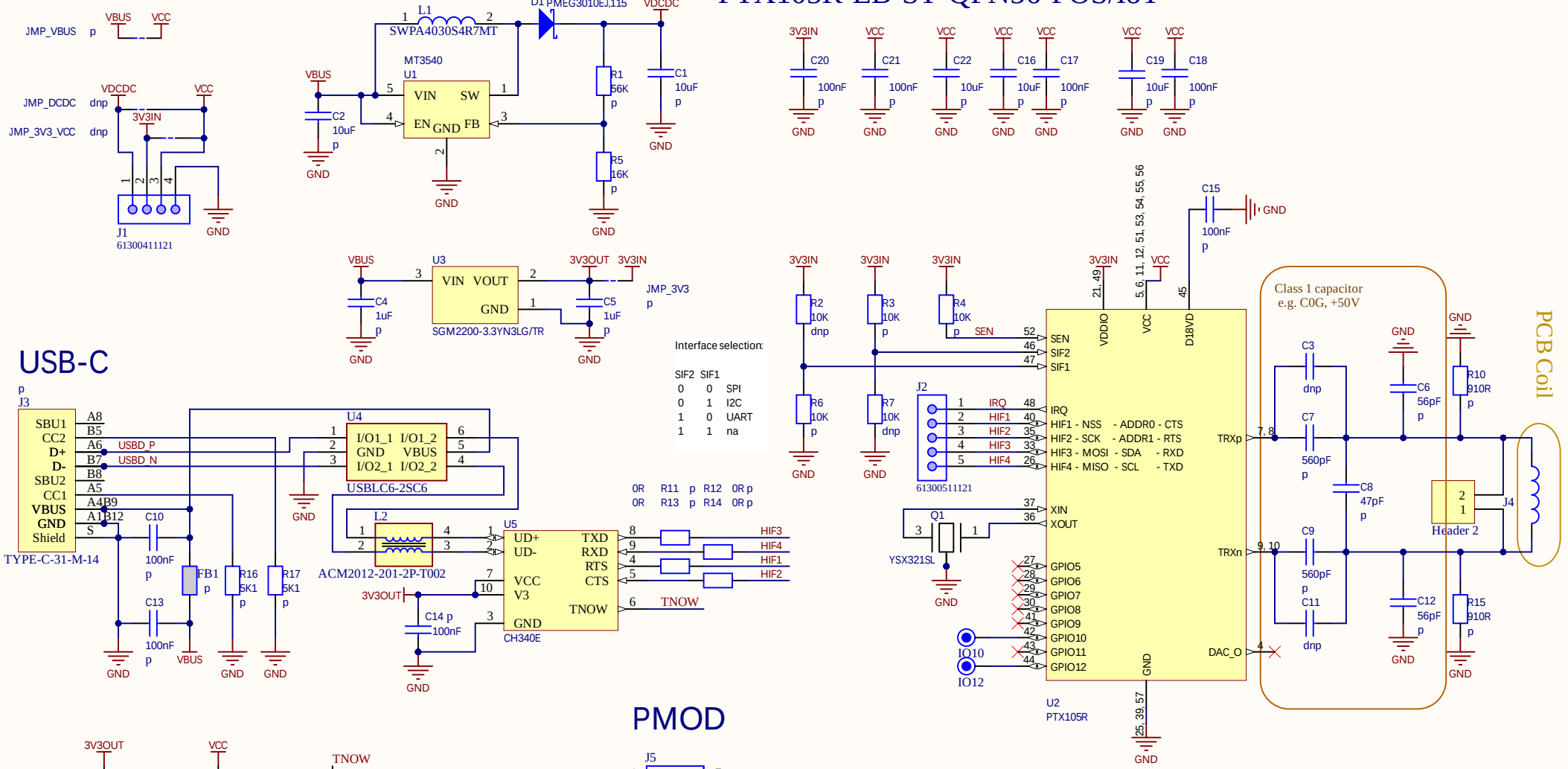
7. Schematics

The PTX105R-EB-ST-QFN56-POS_IoT schematics and layout diagrams are located at the end of this document.

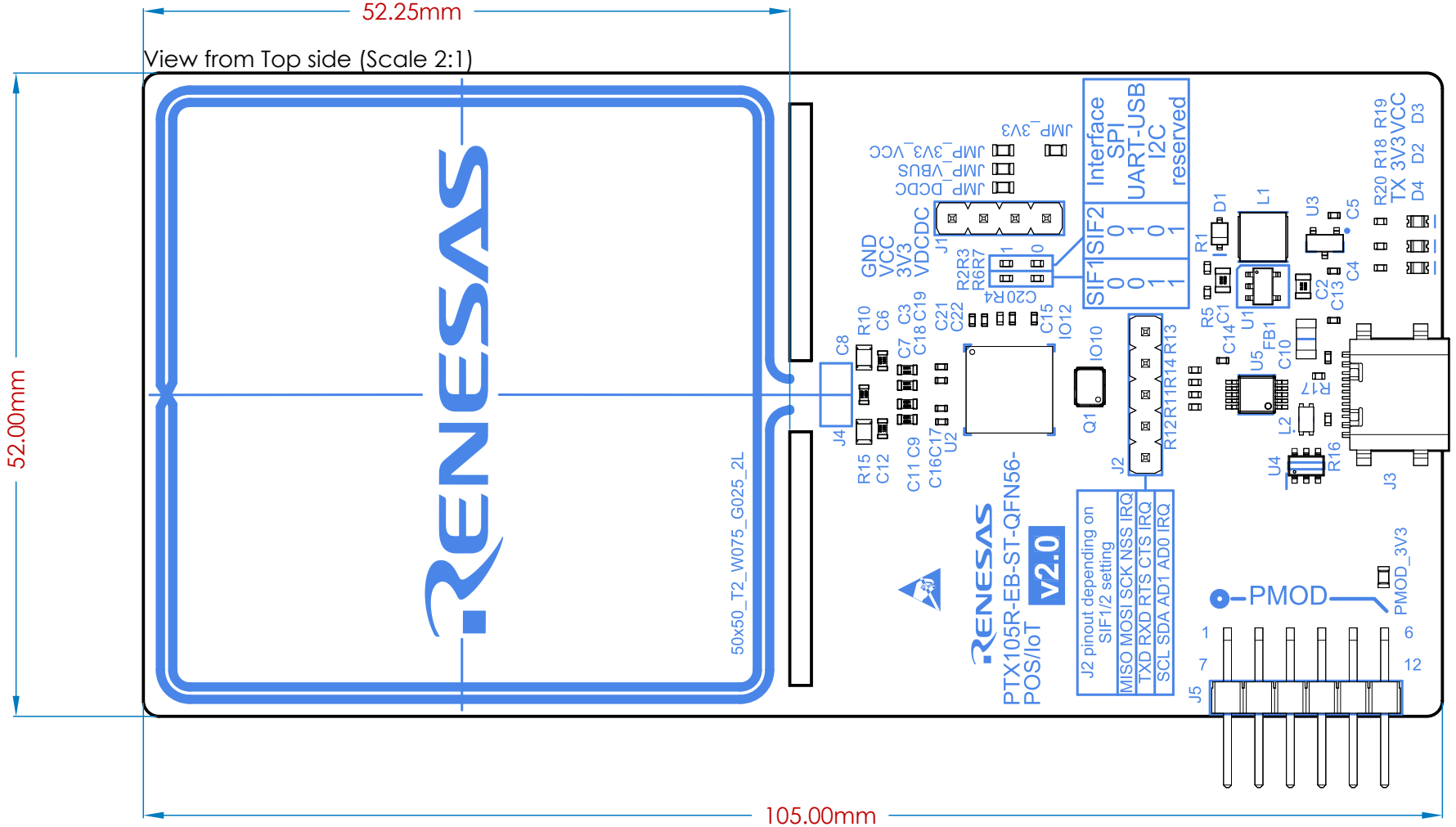
8. Revision History

Revision	Date	Description
1.00	Apr 9, 2024	Initial release.

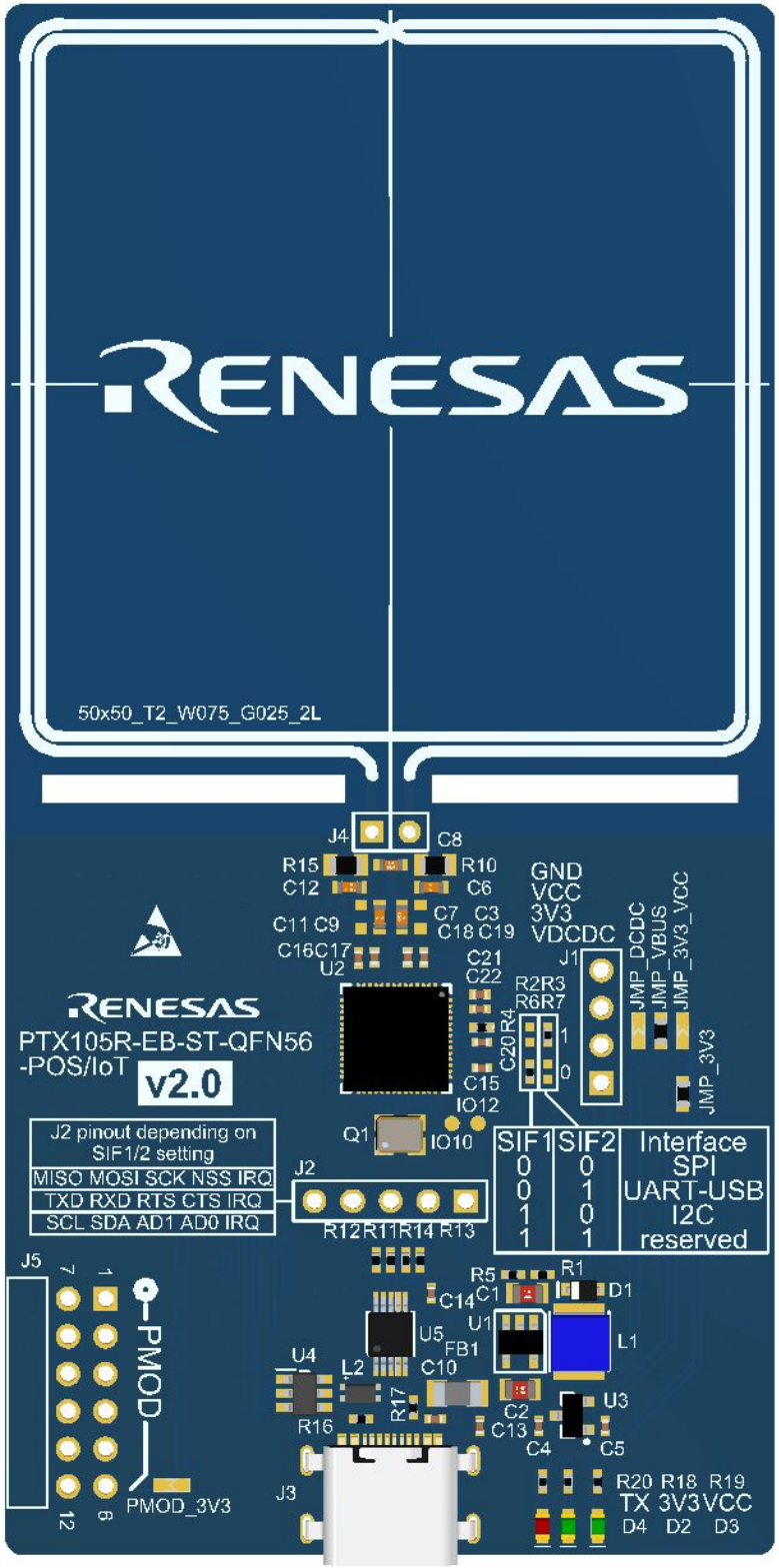
PTX105R-EB-ST-QFN56-POS/IoT

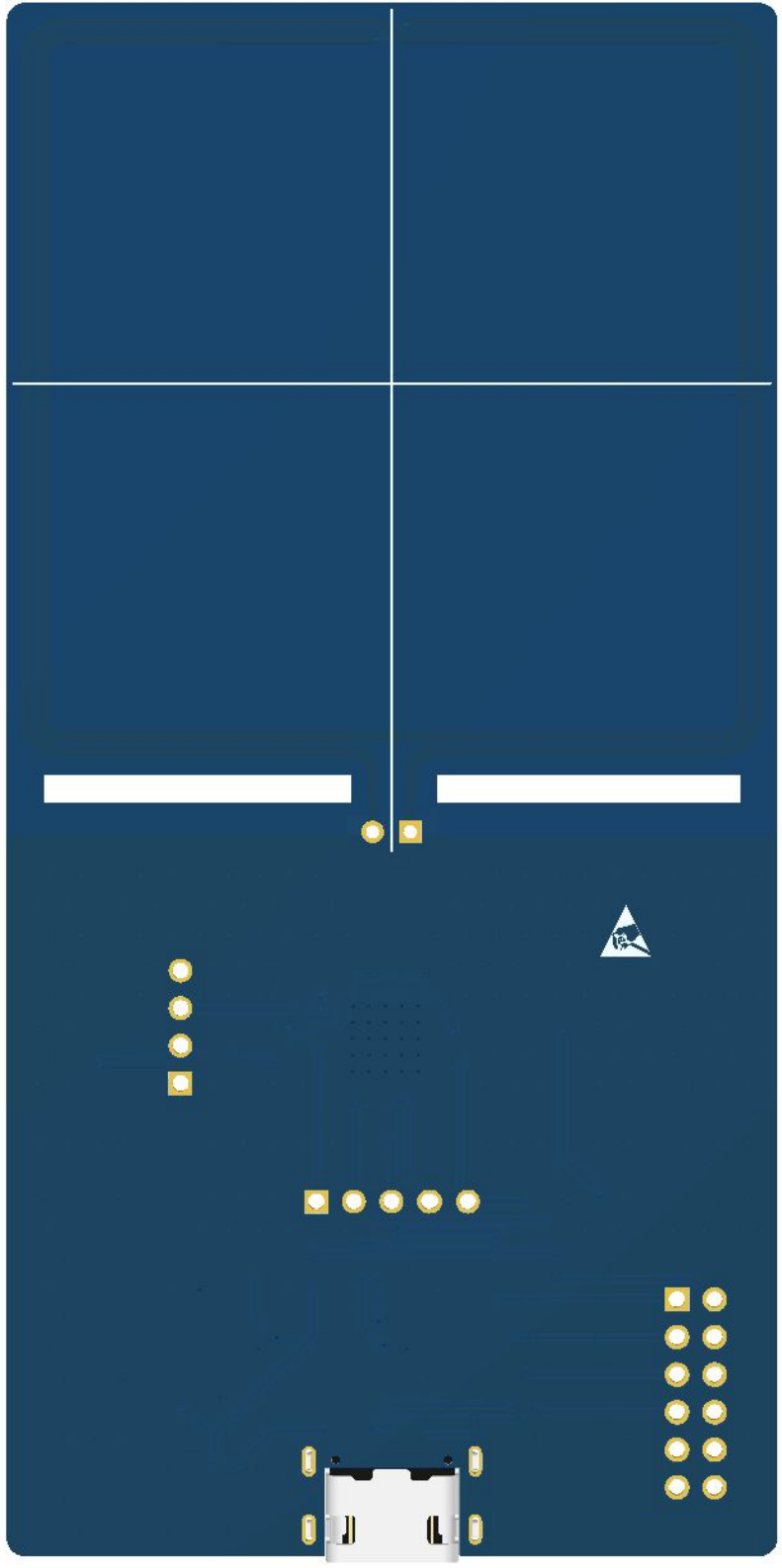


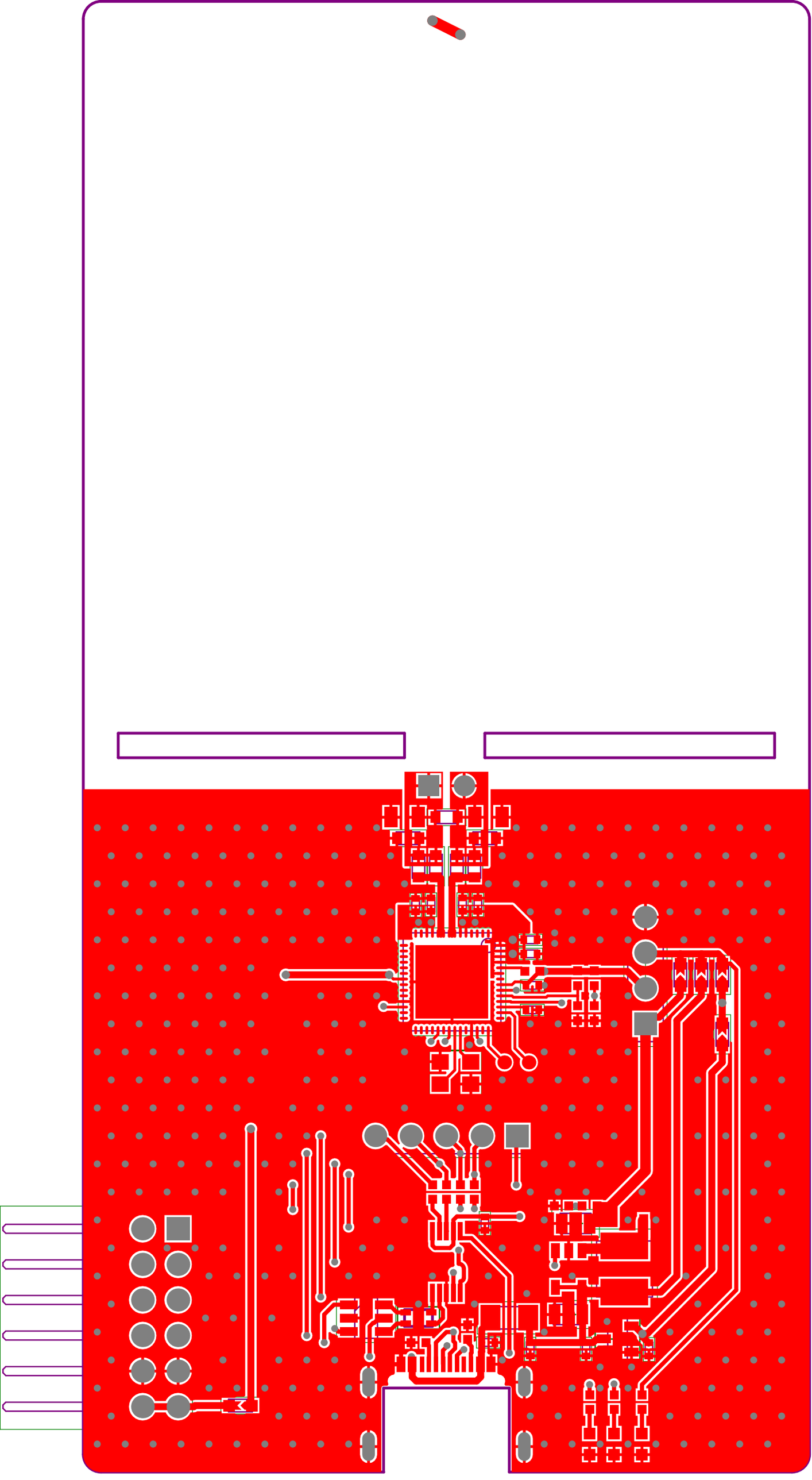
Title	*PTX105.SchDoc*		
Size: A4	Drawn by: gheh	Revision: v2.0	EPSG/CSD
Date: 23/11/2023	Time: 15:47:54	Sheet 1 of 1	RENESAS www.renesas.com
File: PTX105.SchDoc			

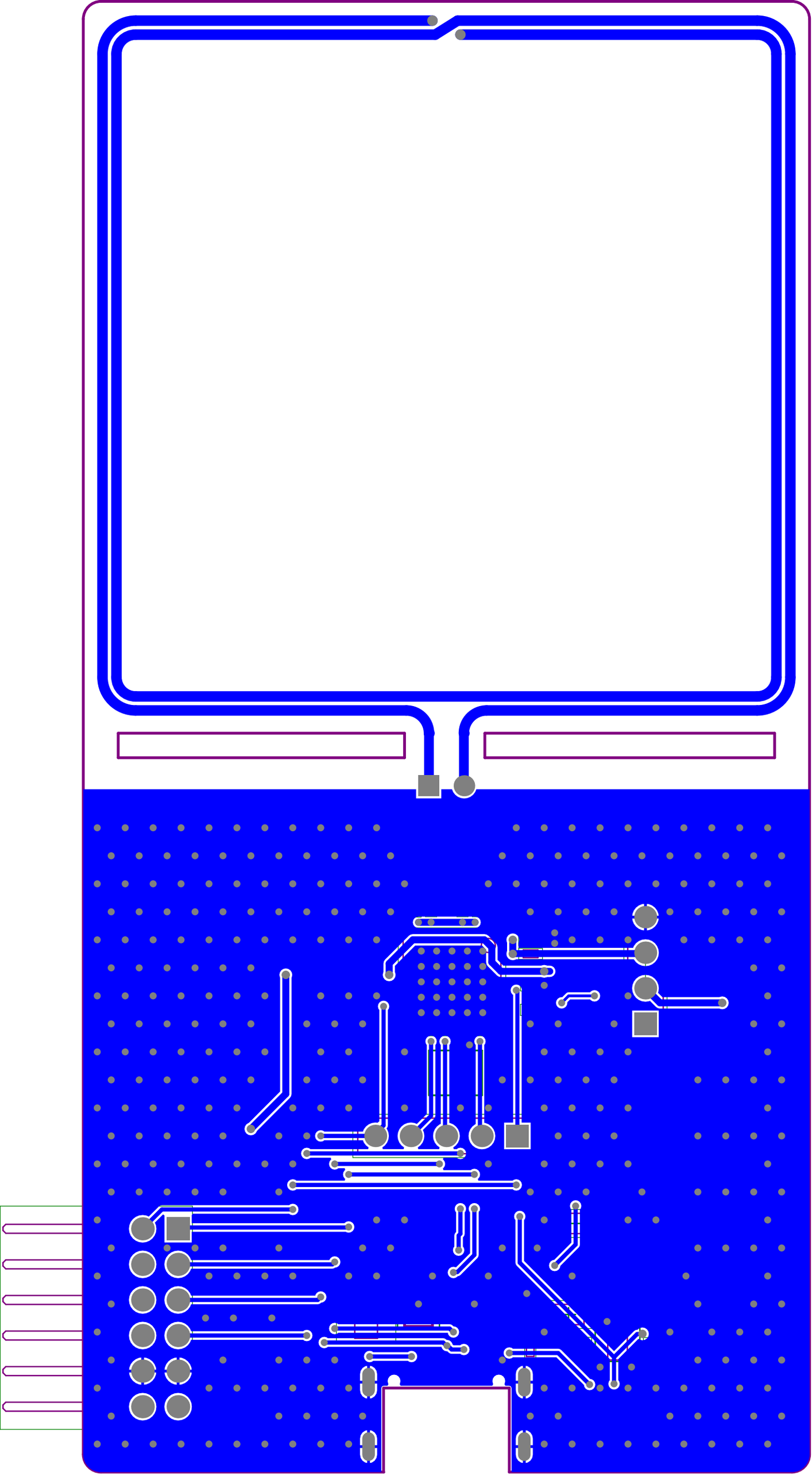


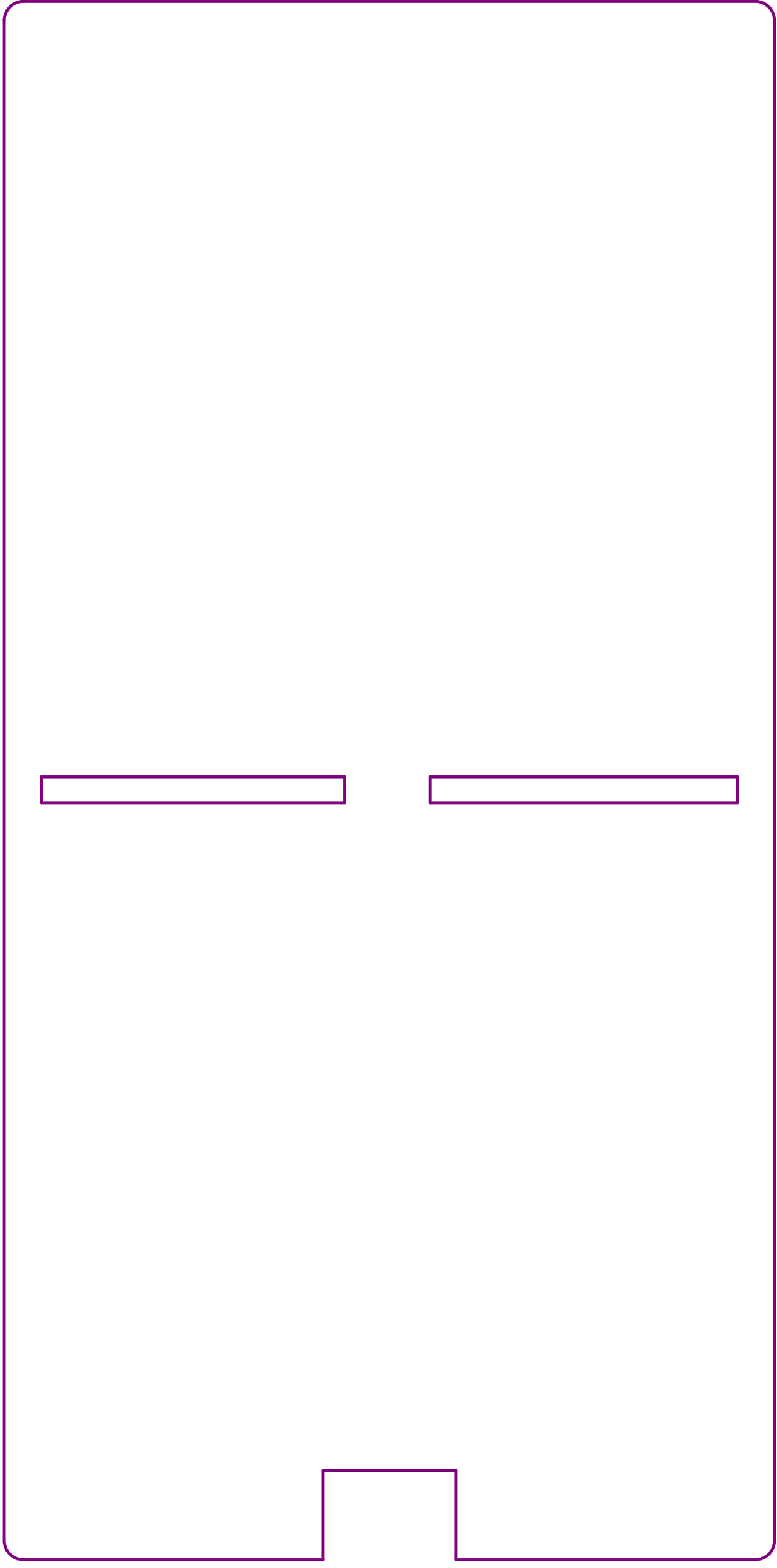
Title: **Assembly Top**	Size: A4	EPSG/CSD	RENESAS
Project: Eval_Board_PTX105.PrjPcb			www.renesas.com
Date: 23/11/2023 Time: 15:47	Sheet 1 of 1		
File: Assembly.PCBDwf			

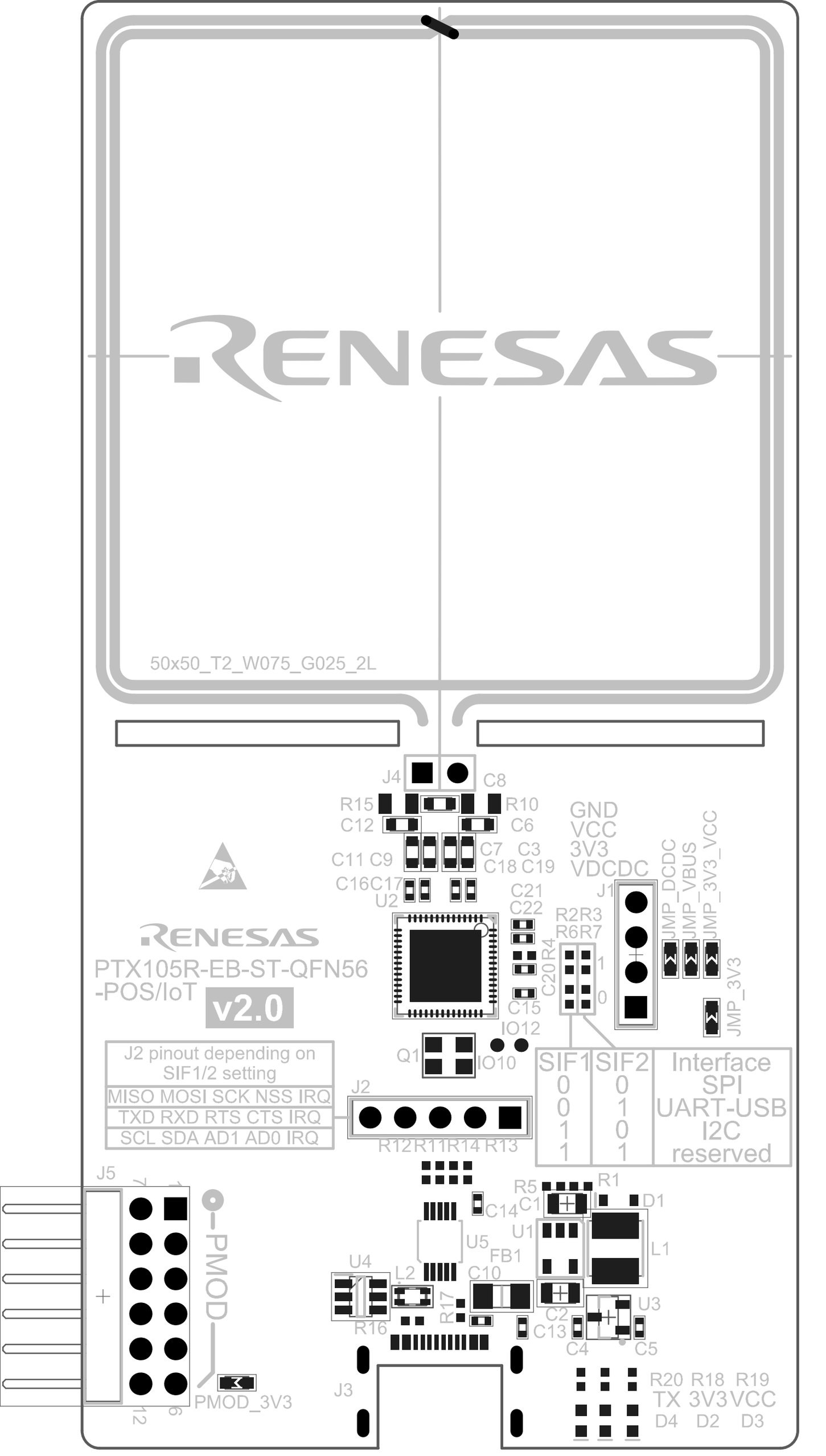

RENESAS
50x50_T2_W075_G025_2L
J4
C8
R15
R10
C12
C6
C7
C3
C11
C9
C18
C19
C16
C17
U2
C21
C22
R2
R3
R6
R7
R4
C20
C15
IO12
Q1
IO10
J1
GND
VCC
3V3
VDCDC
JMP_DCDC
JMP_VBUS
JMP_3V3_VCC
JMP_3V3
RENESAS
PTX105R-EB-ST-QFN56
-POS/IoT
v2.0
J2 pinout depending on SIF1/2 setting
MISO MOSI SCK NSS IRQ
TXD RXD RTS CTS IRQ
SCL SDA AD1 AD0 IRQ
J2
R12
R11
R14
R13
SIF1 SIF2 Interface
0 0 SPI
0 1 UART-USB
1 0 I2C
1 1 reserved
J5
PMOD
PMOD_3V3
R5
R1
C14
C1
D1
U1
U5
FB1
L1
U4
L2
C10
R17
R16
C2
C13
C4
C5
U3
J3
R20
R18
R19
TX
3V3
VCC
D4
D2
D3

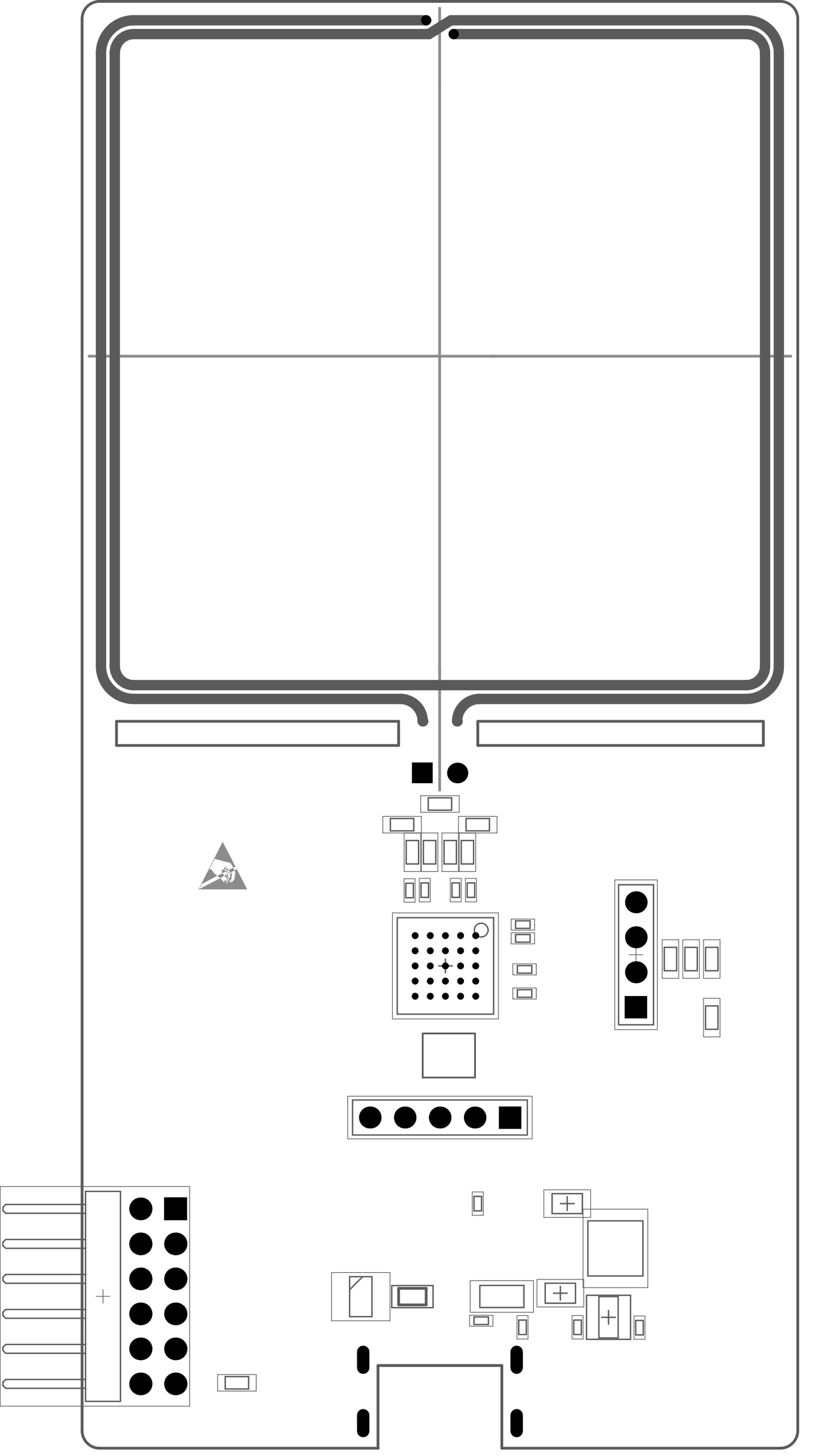









50x50_T2_W075_G025_2L
PTX105R-EB-ST-QFN56
-POS/IoT
v2.0
J4
C8
R15
R10
C12
C6
C11 C9
C7
C3
C18 C19
C16C17
U2
C21
C22
R2R3
R6R7
C20 R4
C15
IO12
IO10
Q1
J1
GND
VCC
3V3
VDCDC
JMP_DCDC
JMP_VBUS
JMP_3V3_VCC
JMP_3V3
1
0
J2 pinout depending on SIF1/2 setting
MISO MOSI SCK NSS IRQ
TXD RXD RTS CTS IRQ
SCL SDA AD1 AD0 IRQ
J2
R12R11R14 R13
SIF1 SIF2 Interface
0 0 SPI
0 1 UART-USB
1 0 I2C
1 1 reserved
J5
PMOD
PMOD_3V3
R5
R1
C1
D1
C14
U1
L1
U5
FB1
U4
L2
C10
R17
R16
C2
U3
C13
C4
C5
J3
R20 R18 R19
TX 3V3 VCC
D4 D2 D3



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