PTX130W/PTX30W Hardware Integration

This manual describes the hardware integration and development of an NFC wireless charging system using Renesas' PTX130W and PTX30W.

Contents

Figures

1. Introduction

This manual describes the hardware integration and development of an NFC wireless charging system using Renesas' PTX130W and PTX30W. It is recommended that the user familiarize themselves with the PTX130W and PTX30W products prior to proceeding with the procedures in this manual.

This manual is structured into the following sections:

- Explanation of PTX130W and PTX30W typical application schematics and guidelines for the layout design
- Antenna design guidelines
- Configuring the low power card detection function for the PTX130W

A system using NFC charging is divided into two sides: **Poller** and **Listener**. The Poller converts DC power to RF power and generates a reactive near field through a coil. The Listener harvests RF energy out of this reactive field through its coil and rectifies it to DC power to perform work – specifically, the charging of a battery, or generally, the powering of an application. The NFC link is used to transmit power from Poller to Listener while simultaneously negotiating the power transfer or even exchanging data.

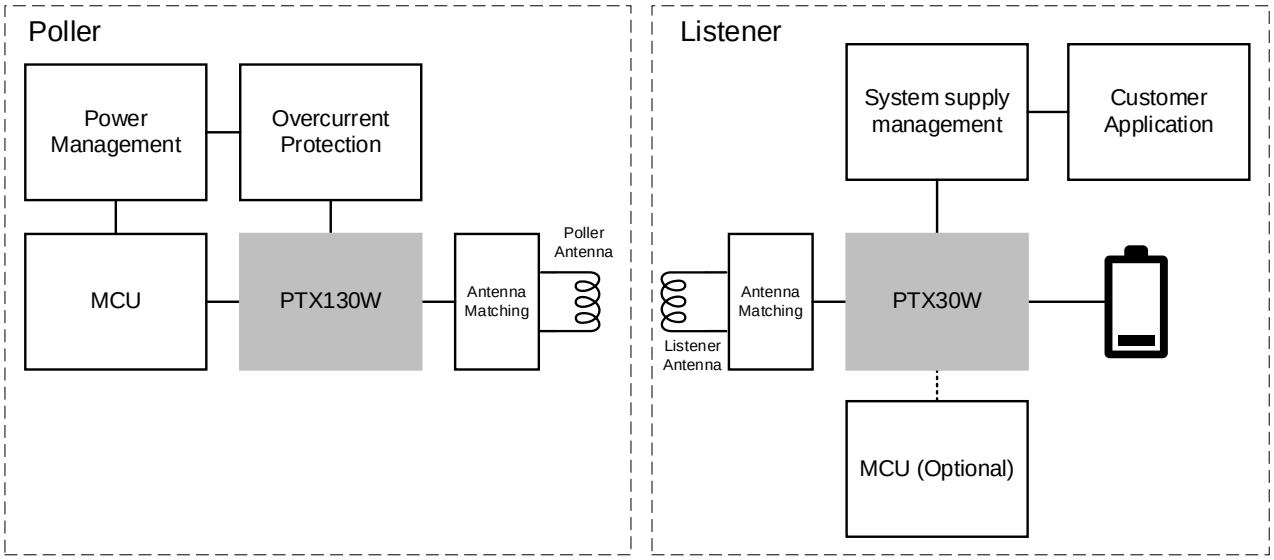


Figure 1. PTX130W/PTX30W Application Block Diagram

The main components in the Renesas NFC charging system are shown in Figure 1.

The PTX130W requires an MCU to control it. For high-power applications driving up to 1W of harvested power on the Listener side, it is recommended to consider overcurrent protection circuitry on the Poller. The system's supply is either regulated by a power management unit or could also be driven directly by a battery or other power source.

The PTX30W does not require an MCU for operation and is shown as optional in the application diagram. The PTX30W internal core contains firmware with all the necessary functions to operate the charging protocol, but if the MCU is present, it can be used to reprogram certain charging parameters during runtime and read-out status information. It can also use the PTX30W as a transparent channel to communicate with the Poller via the NFC interface.

2. PTX130W Typical Application Schematics

The figure below shows the application schematic as given in the PTX130W datasheet. This schematic does not contain details about the power management or overcurrent protection but focuses on the components around the PTX130W such as the supply decoupling capacitors. It also shows the connection to the host microcontroller needed for operation. Details on the overcurrent protection and antenna matching topology and design guideline will be discussed later in this document.

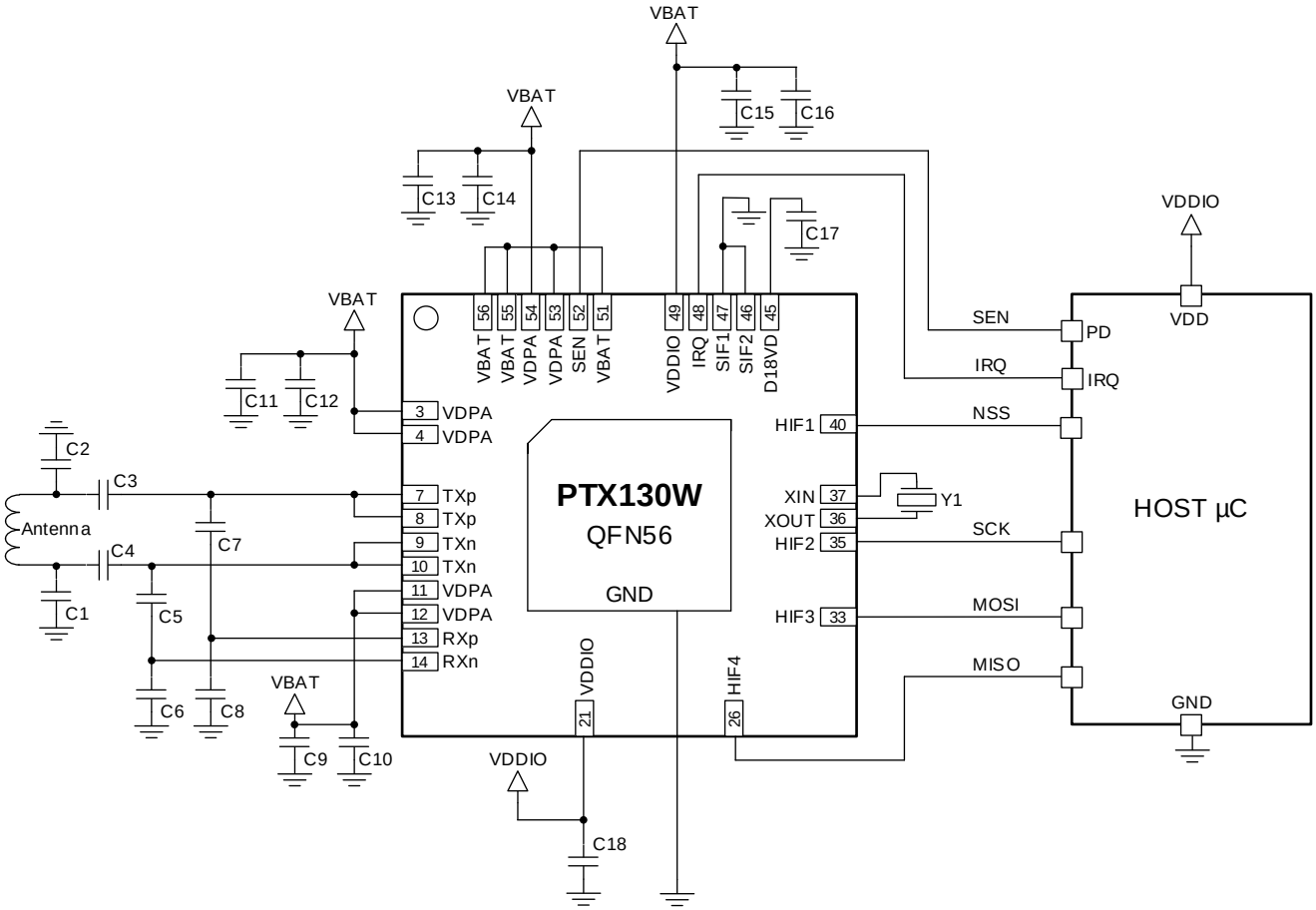


Figure 2. Typical PTX130W Application Schematic

The values for the decoupling capacitors are specified in the datasheet. As shown in the above schematic, it is recommended to have one 10µF and one 100nF supply decoupling capacitor per pin-pair of VDPA (in other words, pins 03 and 04, 11 and 12, and pins 53 and 54). To decouple the VDDIO supply, a 100nF supply decoupling capacitor on each pin is typically sufficient.

2.1 MCU Minimum Requirements for Poller SDK

The minimum requirements to run the PTX130W SDK on the host microcontroller are:

- >= 16 MHz MCU Clock
- ~ 4–5K RAM
- ~70K Flash Memory
- 1x SPI Master
- 2x GPIO:
  - 1 for IRQ for SPI
  - 1 for HW-Reset (SEN-pin)
- 2x general-purpose Timer

Optional:

- I^2C Master
  - Temperature Sensor, if used
  - Power Sensor, if used

2.2 Poller Matching Topology

The following topology is recommended for the initial prototype using the PTX130W. The ending-result of required specific components will be determined during the matching and compliance testing process.

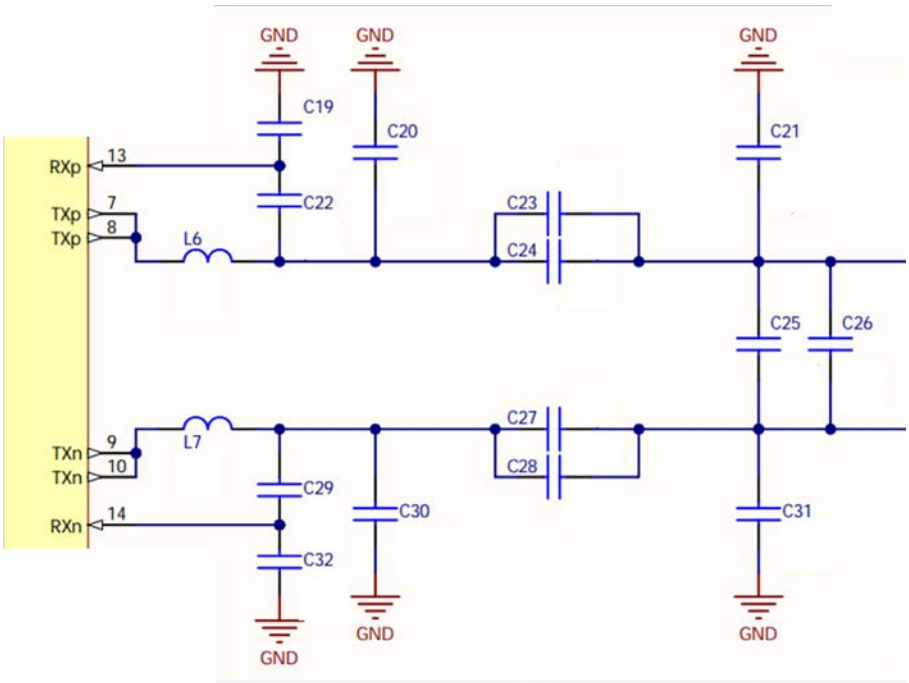


Figure 3. PTX130W Initial Matching Topology

The components L6, L7, C20, C30, C21 and C31 are recommended in the initial design since they may be needed for EMC compliance purpose. For applications targeting higher power levels (for example, 1W power harvesting), it is especially recommended to consider values around 56pF for either C20 and C30, or C21 and C31, depending on the antenna inductance and overall matching. L6 and L7 can typically be shorted (in other words, replaced by 0 Ohm resistors) and are considered mainly in case of noise sources on the design couple into the NFC antenna and used as a radiation path. If inductors are needed, they are most effective when L6 and L7 are placed at 90° with respect to each other. It is also recommended to use the smaller 0603 size inductors. Smaller size inductors will typically show higher losses at these frequencies.

C19, C22, C29 and C32 are used to connect the receiver to the antenna and typical values can be taken from the hardware description found in the datasheet. The rest of the components (C23 to C28) are used to match the system to 13.56MHz resonance.

For all capacitors in the matching network, it is recommended to use Class 1 type capacitors (for example, C0G/NP0 capacitors) with minimum 50V rating for the ones on the single-ended, and 100V for the ones on the differential lines. Typically, the required capacitance will be below 1nF for which this type of dielectric is usually available.

2.3 PTX130W Power Supply Considerations

The power management on the Poller needs to be able to supply at least two domains: V_{DDIO} and V_{BAT}. V_{DDIO} is a shared supply between the PTX130W I/O circuitry and the host microcontroller's supply. The SPI and IRQ, as well as all of the PTX130W GPIOs, will be supplied by V_{DDIO}. V_{BAT} is the main power supply for the PTX130W and is also used to supply VDPA.

Note: V_{BAT} must always be the same or higher than VDPA.

It may be necessary to implement an overcurrent protection for the PTX130W driver stage that is supplied by VDPA, especially when the device is used at the higher end of its specified power levels. The NFC charging systems work with the Listener coupled closely with the Poller to maximize the power transfer and its efficiency.

The antennas and matching are designed to present an overall load impedance of around 5 Ohm +j*0 Ohm to the output driver. This design approach, even though it maximizes output power and efficiency, can result in overcurrent conditions on the output driver when it drives an RF signal without a Listener present in the field. For instance, removing the Listener from the field during an ongoing charging cycle will cause the load on the driver's output to drop and the driver to draw more current than its specified rating.

There are two ways to mitigate this effect:

1. Option A: Overcurrent Protection Using a Current Limiter

   Introduces a current limitation between V_{BAT} and VDPA that automatically limits the current at a set value.

2. Option B: Overcurrent Protection Using a Current Sense Amplifier

   Uses a current sense amplifier via which the PTX130W can measure its supply current.

Both approaches protect the PTX130W from overcurrent events.

Whether the power level is sufficiently high to require overcurrent protection can be tested only once the antennas have been designed and the matching optimized. The Poller can then be operated in continuous wave mode with a constant RF field and no Listener as load. Measuring the current into VDPA will give an indication of how close it is to the limits specified in the datasheet.

2.3.1. Option A: Overcurrent Protection Using a Current Limiter

Using a current limiter to implement the overcurrent protection requires an extra component in between V_{BAT} and VDPA that limits the current. Important in the component selection is that it can limit the current at the maximum specified value of the PTX130W as given in the datasheet. Furthermore, its On-Resistance is to be as low as possible to limit power loss and voltage drop between V_{BAT} and VDPA and have an enable control pin with an active-high logic and short setup time.

Below is a summary of the parameters and criteria to observe during component selection:

- Current limit value
- Low On-Resistance
- On/Off control pin with active high logic
- Fast response time (in other words, short setup time) between enable and operational status

The PTX130W automatically drives the enable control pin of the current limiter via GPIO5. This is needed specifically while the PTX130W operates in the low power detection mode (in other words, LPCD). The PTX130W then automatically enables the current limiter with sufficient setup time for it to be active during the LPCD pulses and disable afterwards (in other words, during stand-by time). This minimizes the current consumption of the overall system while the Poller is waiting for a Listener to enter the field. The longer the limiter's setup time, the higher the current consumption in LPCD will be due to the PTX130W needing to wake-up and enable it before the LPCD pulse is transmitted.

2.3.1.1. PTX130W SDK Configuration for Current Limiter Implementation

When using the current limiter option to protect the PTX130W driver stage from overcurrent conditions, the parameter "**init_param.ExternalProtection.Type**" in "**ptxWLC_Poller_Main.c**" will need to be set to **ProtType_CurrentLimiter**. Only one more setting needs to be adjusted in the SDK when using the current limiter – the parameter "**init_param.ExternalProtection.Settings.Limiter.GuardTime**" which controls the enable/disable via GPIO5 and needs to be adjusted according to the current limiter components setup time.

2.3.2. Option B: Overcurrent Protection Using a Current Sense Amplifier

The PTX130W features an integrated ADC that can be used to measure the current on the VDPA supply. The Renesas ISL28005-50 can be used for this functionality. The PTX130W can again automatically control the mechanism. The output of the current sense amplifier is to be connected to ATEST1 and needs a low shunt resistance of 50mΩ on its input and an enable control. The enable control can be handled by GPIO5, which limits the selection to devices operating at the same supply level as VDDIO since that is GPIO5's supply domain. At 1.8V it can become especially challenging to find suitable devices. Therefore, ATEST3 can be used as an alternative to supply the current sense amplifier from the V_{BAT} domain.

Below is a summary of the parameters and criteria to observe during component selection:

- Gain 50V/V
- Low quiescent current
- ±1% gain error (maximum)
- 50mΩ sense resistor

The advantage of using a current sense amplifier is that it typically has very low resistive losses and can stay disabled during off-time (in other words, it fits well with the LPCD mechanism).

2.3.2.1. PTX130W SDK Configuration for Current Sense Amplifier Implementation

When using the current limiter option to protect the PTX130W driver stage from overcurrent conditions, the parameter "**init_param.ExternalProtection.Type** in **ptxWLC_Poller_Main.c**" needs to be set to "**ProtType_CurrentSensor**".

The current sense amplifier requires additional parameters to configure the application (see below). It is recommended to use a component with the same type of parameters as described above and not change the attenuation setting or threshold.

- **init_param.ExternalProtection.Settings.Sensor.Attenuation**

  It is recommended to not change this setting and use a component with parameters as described in the previous section.

- **init_param.ExternalProtection.Settings.Sensor.Supply**

  This setting defines which PTX130W pin is used to supply the current sense amplifier. It can be supplied either by a V_{DDIO} supply domain through GPIO5 by defining the parameter as "**SupplyPad_GPIO5**", or the current sense amplifier can be supplied by the V_{BAT} supply domain by setting the value to "**SupplyPad_ATEST3**".

- **init_param.ExternalProtection.Settings.Sensor.Threshold**

  It is recommended to not change this setting and use a component with parameters as described in the previous section.

3. PTX130W Layout Guidelines

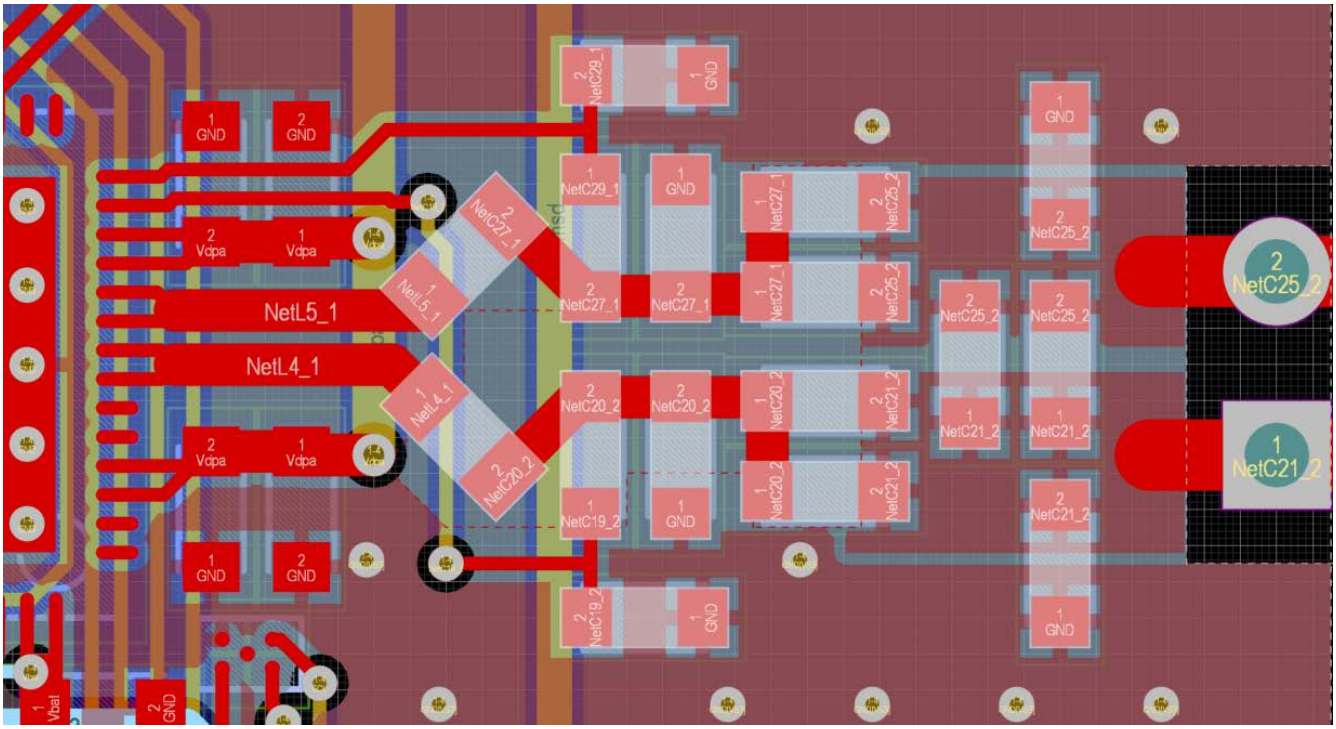
This guideline provides basic paths and recommendations to mitigate unwanted emissions and help create a layout that minimizes the radiation in order to comply with the specific EMC (Electromagnetic Compatibility) regulation.

3.1 General Recommendations

- Consider the return path of the current flow
  - Use a solid GND (in other words, ground and supply planes) wherever possible
  - Dedicate at least one layer of the board(s) as GND plane
  - Do not route signals over gaps in the GND plane
  - Keep GND and supply planes split-free
  - Keep in mind that adjacent lines over a plane can couple via the plane
- Route RF signals as symmetrical as possible and as short as possible
  - Keep loops as small as possible
  - Keep matching components close to the PTX IC and space them symmetrically
- Capacitors are needed to buffer and reduce the noise injected back into the supply
  - Place decoupling capacitors as close to the IC as possible
  - Effective decoupling often requires a set of different value capacitors
- Consider the LF and HF behaviour of decoupling caps separately
  - At LF, the nominal value is more determining
  - At HF, the parasitics are to be considered (refer to the models and graphs provided in the respective datasheet)

3.2 RF Routing

One of the main sources of radiation is the transmit signal from the PTX IC to the antenna. Since this signal carries a significant amount of power over longer traces (including the antenna itself), special care has to be taken to filter out unwanted spurious signals so they won't get broadcasted into the field via the antenna. The signal itself is differential so a good layout should be as symmetric as possible to benefit from the cancellation effect differential signals have in common.



However, component tolerances and manufacturing differences can impact that effect. To that end, the matching network should also be created in a way that allows unwanted HF signal components to be dissipated to GND. A recommended matching network configuration to start with is shown in Figure 4.

Note: Not all components are necessary for every design.

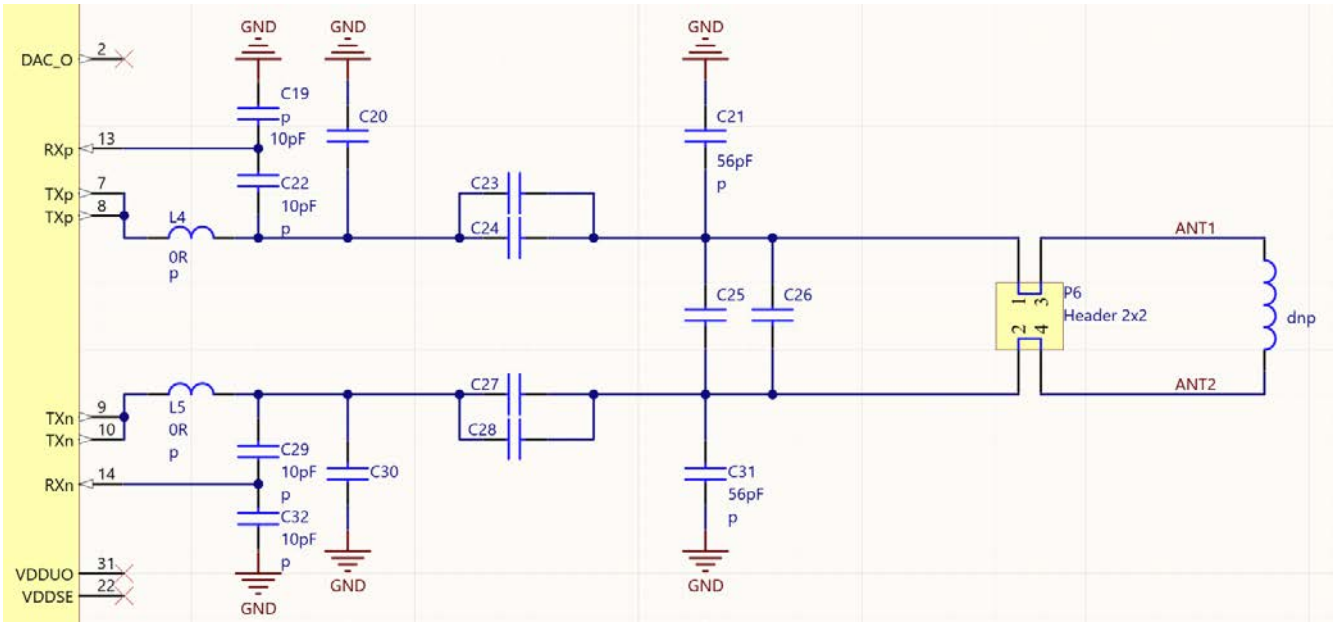


Figure 4. Recommended Matching Network

- The capacitors C19, C22, C29, and C32 are meant to build a capacitive voltage divider in order to attenuate the antenna signal before it enters the receive chain. A default value of 10pF for each capacitor is recommended.
- L4 and L5 are EMI suppression inductors. They might be necessary to achieve higher damping on critical EMC frequencies. By default, it is recommended to keep these as placeholders in the development phase but place 0Ω resistors for initial testing.
- The capacitors C20, C30, C21,and C31 are used to shunt high frequency harmonics to GND:
  - Depending on antenna and matching impedance, either the combination of C20/C30 or C21/C31 has a better effect
  - Values ranging from 20–100 pF, with 56pF being a good starting point, have proven results of offering the best reductions
- C20, C30, C23, C24, C27, and C28, together with C25 and C26, are used to match the antenna impedance to the output of the PTX chip. This is described in more detail here in the datasheet.
- Part of the capacitance of C25 and C26 can be transferred to C21 and C31 (*Note*: multiply by 2x because of the single-ended vs. differential conversion)

The trace width, as well since the current running between the antenna, should be considered and the PTX chip can be as high as 1A. At the frequency of operation, the skin depth in copper is only 17.7µm. This means that using a copper thickness > 35µm shows decreasing improvements because a lesser amount of the conductor cross-section will be used to transport current. To stay below a 20°C rise of temperature, Renesas recommends a minimum trace width of 0.5mm for high power applications.

3.3 Power Supply Considerations

The PTX chip has four power supply domains:

- VBAT1
- VBAT2
- VDPA
- VDDIO

Each of the domains needs decoupling capacitors placed as close to the respective pins as possible.

The recommended capacitors for the pins are as follows:

- VBAT1 and 2: Connected together with a 100nF capacitor close to each pin and one 10µF capacitor on the trace connecting the pins
- VDPA: One 100nF and 10µF capacitor on each pin pair (3/4, 11/12, 53/54) with the 100nF positioned closest
- VDDIO: One 100nF capacitor on pin 21 and 49

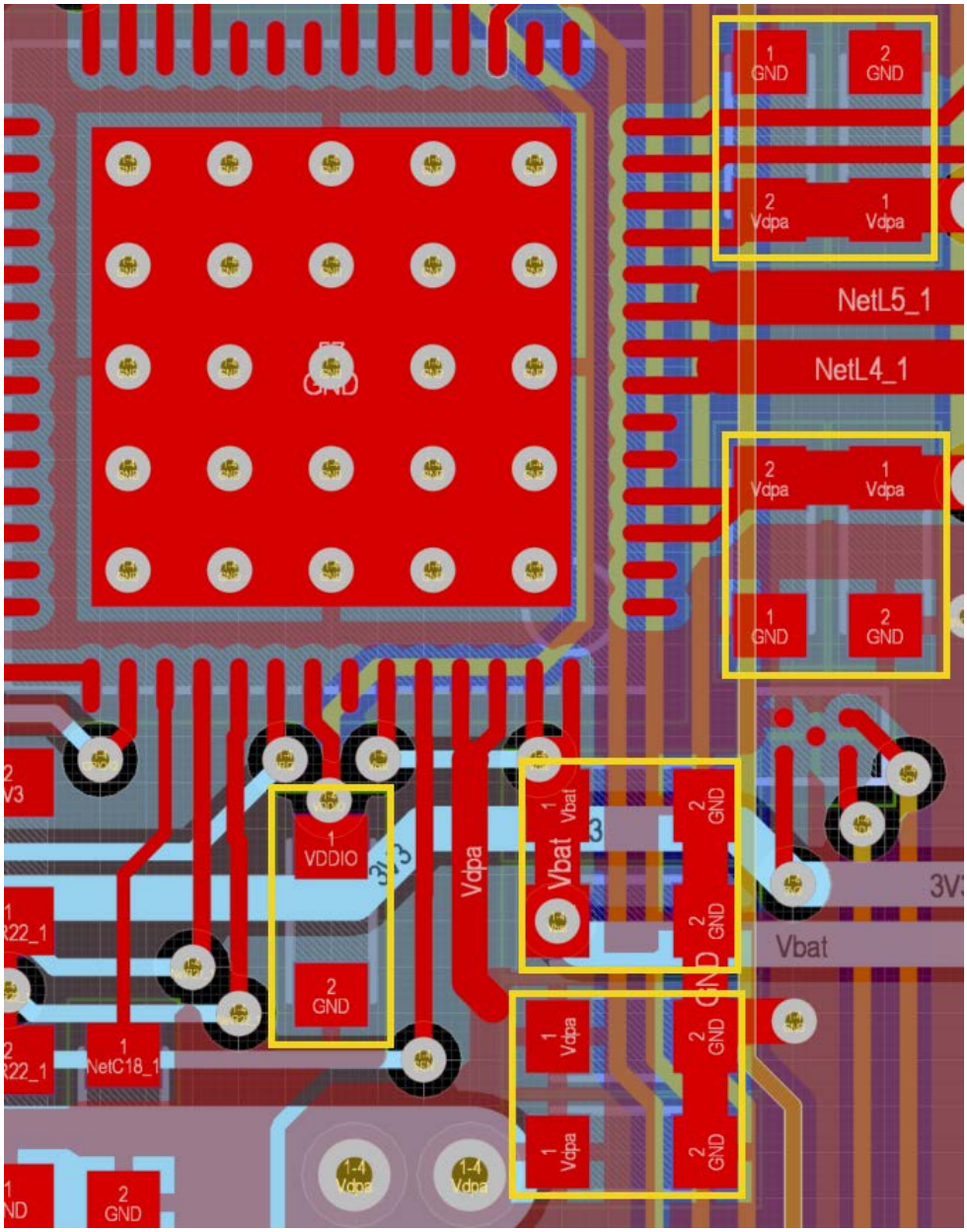


Figure 5. Power Supply Domains

3.4 Clocking

The reference for the clock is typically provided by a 27.12MHz crystal. The crystal should be close to the XIN/XOUT pins of the chip to avoid long traces radiating the clock signal.

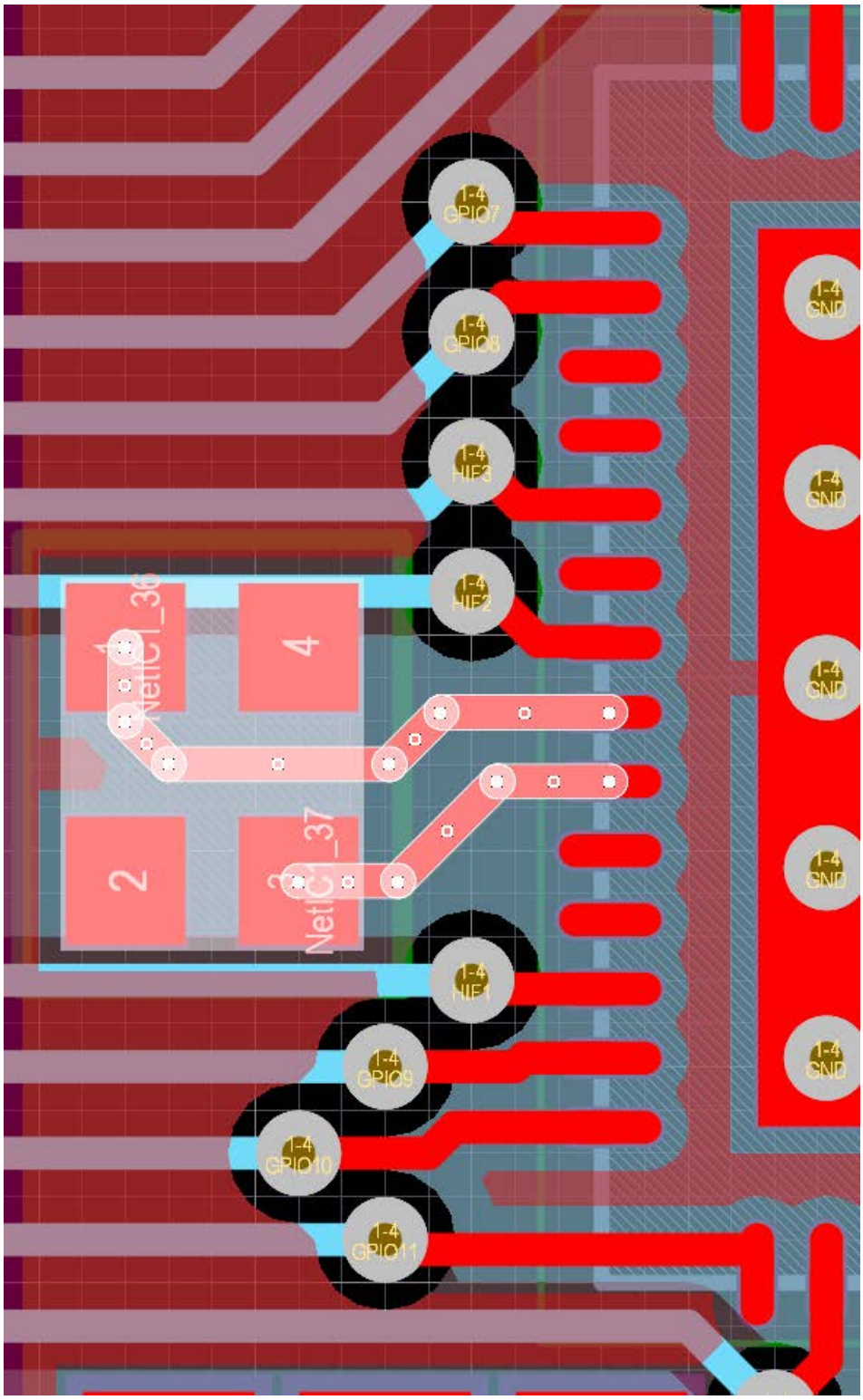


Figure 6. Clocking – Crystal Reference

3.5 Exposed Pad

The PTX130W exposed pad acts as both the thermal connection to the PCB as well as the GND connection. Therefore, a good electrical and thermal connection is important for correct functionality. Renesas recommends a 5.2 × 5.2 mm pad with multiple vias connecting directly to the GND plane. This decreases parasitic inductance and creates a good thermal coupling to the GND plane which dissipates most of the heat.

Measurements with different PCB sizes have shown that the following thermal coefficients and temperature increase at maximum power output can be expected for different PCB sizes:

Table 1. Thermal Coefficients for Different PCB Sizes

PCB Size [mm²]	tk [K/W]	Δt [°C]
5500	28	35
2600	33	43
1400	57	66

3.6 Digital Interface

The PTX chip is connected via SPI. To avoid radiating the harmonics of the fast switching digital signal lines, keep the traces short and the return path unbroken. Keeping the trace lengths equal should also be a priority to avoid signal disturbances.

Important: Avoid crossing the signals with the crystal oscillator signals or any analog lines.

4. PTX30W Typical Application Schematics

The figure below shows a reference schematic with mandatory, optional and design related components.

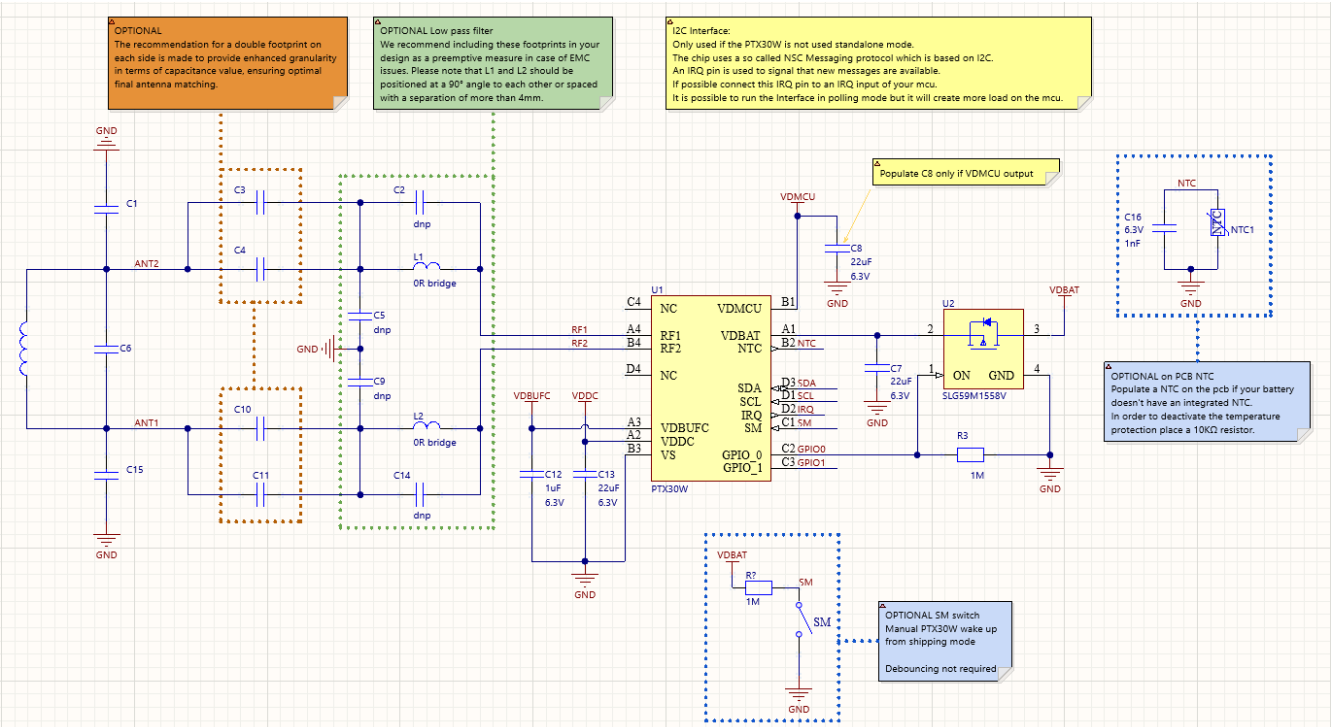


Figure 7. Typical PTX30W Application Schematic

- The minimum components necessary for operating the PTX30W are the decoupling capacitors C12, C13 and C8.
  - C8 values are necessary only if VDMCU is used as an output. Otherwise, it may be replaced with a typical 100nF capacitor.
- C3/4, C10/11, C6/1/15 allows several matching topologies as explained in the following sections

  Note: Class 1 capacitor (in other words, C0G dielectric capacitors with 50V rating) is highly recommended for the matching network.
- L1,L2,C3,C8 and C2/C14 serve as placeholders for a potential low-pass filter. In other words, they are designed to suppress emissions and counteract the efficiency loss inherent in such a circuit.

  Note: Renesas suggests keeping these in your layout until the EMC pre-compliance test
- The **NTC** is typically inside the LiPo battery but can also be placed on the PCB. If not used, connect it to a 10KΩ resistor to GND. The parallel capacitor (C16) is required to stabilize the signal on this node.
- GPIO0,1 offer several signaling functionalities like field detection and charging active. GPIO0 is required to implement the Start-up circuit.
- The SM pin is used to wake the chip from shipping mode, and it could be connected to a mechanical switch
- The Load Switch (U2) is necessary to implement a functioning Start-up circuit. For more details, see section 4.1.

4.1 Start-up Circuit

When a battery is deeply discharged (< 2.4V) the system gets stuck in reset state with the charge regulation transistor conducting. If an RF field is present in that situation, the battery is charged with an undefined (unregulated) charging current, although trickle charge should be applied. This happens for as long as the RF field is present. The effect is due to incorrect biasing of the pass transistor on V_{BAT} when the system is not booted. To remedy this incorrect charger behavior, add a load switch in between the battery and the PTX30W.

4.1.1. Operating Conditions

The added circuitry places limitations on the following operating conditions:

- **Start-up via the SM pin**:
  - Start-up via the SM pin is only possible if the PTX30W is supplied with a V_{BAT} > 3V. Since V_{BAT} has to go through the body diode of the load switch while the system is in shipping mode, the forward voltage drop of that diode has to be added to V_{BAT} for the circuit to start. For this load switch, a V_{BAT} of 3.4V is required for start-up.
- **Current draw from VDDC**:
  - Since the battery is completely disconnected from the PTX30W in shipping mode, the initial power delivered at the beginning of the charging cycle (defined by the Polling Power Level setting and the coil arrangement) has to be more than the current demand of the circuitry connected to VDDC
  - This can be tested by setting the initial minimum and maximum power level the same as the Polling Power Level and observing the charge current without a load at VDDC. This observed charge current is the upper limit of current draw allowed on VDDC.

4.2 PTX30W Power Supply Considerations

The application on the listener side can be connected to the battery via two nodes on the PTX30W (for more details, see the PTX30W datasheet). Powering the system this way has the benefit that the ship mode of the PTX30W can be used to disconnect the system from the battery and keep it in an ultra low power state. It is also possible to connect the system supply directly to the battery but then the PTX30W ship mode cannot disconnect the battery from the system supply anymore.

The system can be supplied on the VDMCU node by the integrated LDO or on the VDDC node, or even by both. The internal LDO configuration is described in greater detail in the datasheet. In case the application requires more than 50mA, it cannot be supplied by the internal LDO itself since this is its limit.

Using the VDDC node to supply the system requires power management on that node. The voltage present on the load is either directly the battery voltage when there is no RF field present, or a voltage roughly 300mV higher than the battery voltage, up to a maximum of 5.2V while it is charging. The limits on the VDDC current capability when driving the system are given in the datasheet.

Note: During charging, any energy required to power the system will be provided by the RF field as long as enough energy is available. However, this reduces the power available to charge the battery.

4.3 Listener Matching Topology

The following describes the recommended listener matching topology for a prototype design.

The specific components that will be needed for the final prototype design will be determined during the matching and compliance testing process. An EMI filter using components C3, C8, L1 and L2 is included in this matching topology since the non-linear components of the rectifier could cause emissions that need to be filtered. This needs to be determined by performing pre-compliance testing. Renesas recommends using the minimum 0603 components for L1 and L2 and placing the two components at 90° towards each other.

For the medium to high charging current ranges (> 50mA), a series or series-and-parallel matching using C5, C2 and C7 is required on the Listener to achieve the highest efficiencies possible in the specific antenna system. The target is to tune the system to 13.56MHz, where typically the capacitance in parallel to the antenna is much smaller than the capacitance in series. Consider using two capacitors in parallel for C2 and C7 to achieve more flexibility in matching the antenna.

For low charging currents (< 50mA) and medium to low coupling, a parallel matching approach has proven to be beneficial. The benefit of using a parallel matching in this application space is that the maximum performance can be achieved with lower antenna inductances of around 200nH–300nH.

For all capacitors in the matching network, Renesas recommends using C0G/NP0 type capacitors with a minimum voltage rating of 50V. Typically, the capacitor values will be below 1.5nF and are usually available for this type of dielectric.

5. PTX30W Layout Guidelines

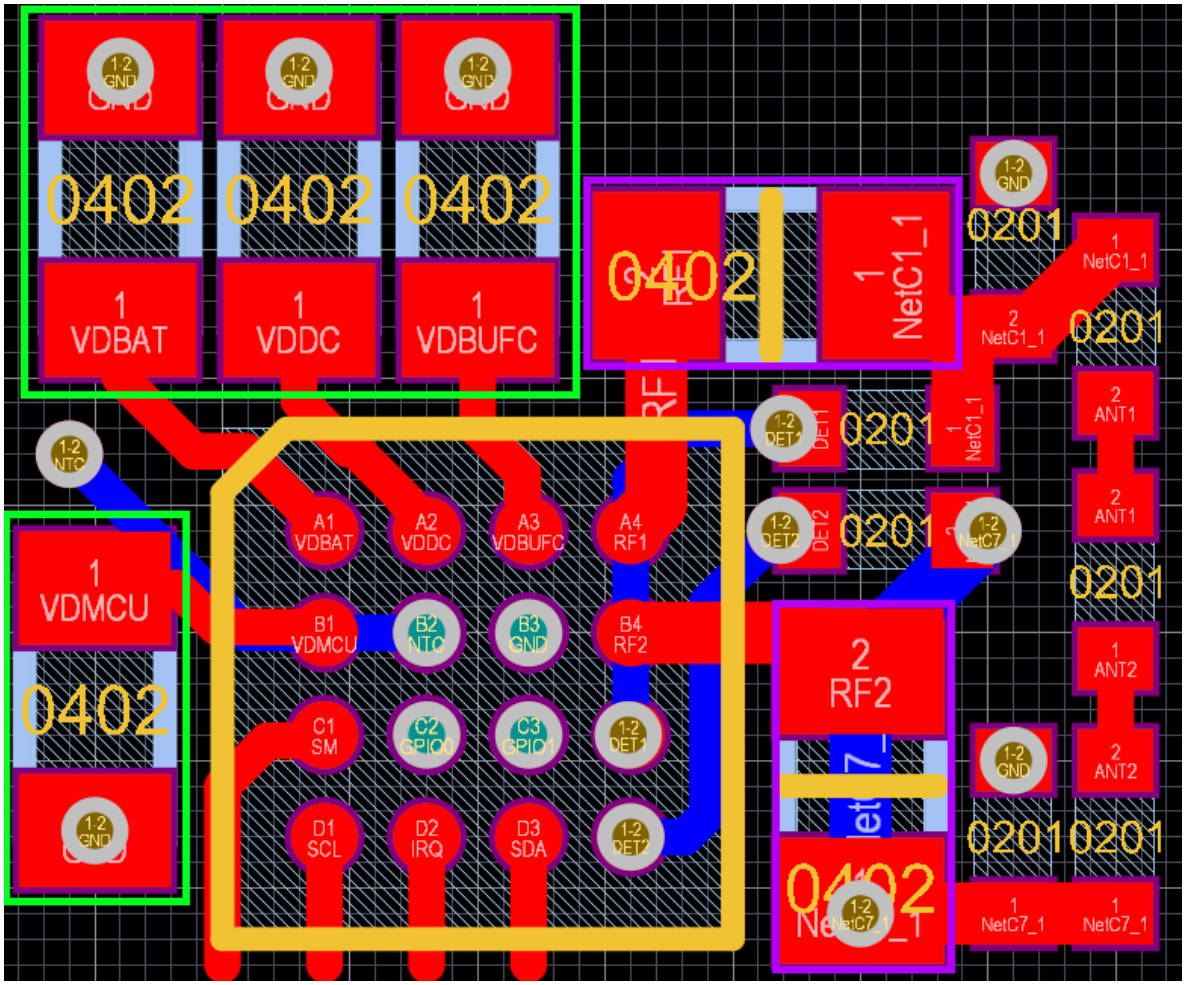


Figure 8. PTX30W Layout Component Sizes

5.1 Power Supply

- Place the decoupling caps (C4, C6, C10 and C11 – enclosed in green) as close to the PTX30W as possible
- Recommended component sizes: 0402 or 0603

5.2 Antenna Connection

- Keep the traces to the antenna as short as possible
- L1 and L2 (marked in magenta) are EMI suppression inductors. They may be necessary to achieve higher damping on critical EMC frequencies. By default, it is recommended to keep these as placeholders in the development phase, but place 0Ω resistors for initial testing.
- C3 and C8 work together with L1 and L2. Keep them unpopulated for the first testing.
- Keep C1 and C9 unpopulated for the first testing

6. Antenna Matching Guideline

This section describes how to design antennas for the PTX130W and PTX30W systems. With NFC charging, a lot of flexibility in the design is possible since the antennas can be designed to fit the application, and not vice versa. Instead of giving exact design dimensions, this section focuses on what the target antenna characteristics should be dependent on the application.

6.1 Required Tools

To perform the antenna matching, a vector network analyzer is required to measure the antenna parameters and fine tune the matching components. To simulate the circuit, the freeware QucsStudio is used (for more information, see the datasheet). To optimize the matching, the PTX130W-N/PTX30W-N Config Tool (referred to as Config Tool) is used. The Config Tool is available from the knowledge base on the support portal. In order to use the Config Tool, the Renesas evaluation boards can be used. The evaluation board's antennas can be broken off the PCBAs and custom antenna prototypes can be connected via wires to the evaluation boards.

6.2 Matching Workflow

The following workflow has shown to work well when designing antennas for a new system and matching them to optimize the performance. In a first step, the antennas are designed based on the application requirements and prototypes manufactured. The prototypes are measured with the VNA and fixed in the application. The setup will mimic the final product as close as possible but, as a minimum, needs to consider all metal components in the antennas vicinity. In this position the coupling factor between the two antennas from the Poller and Listener is measured. The antenna's parameters and coupling factor are then used in a simulation to determine the initial matching values. The Config Tool is used to optimize the performance.

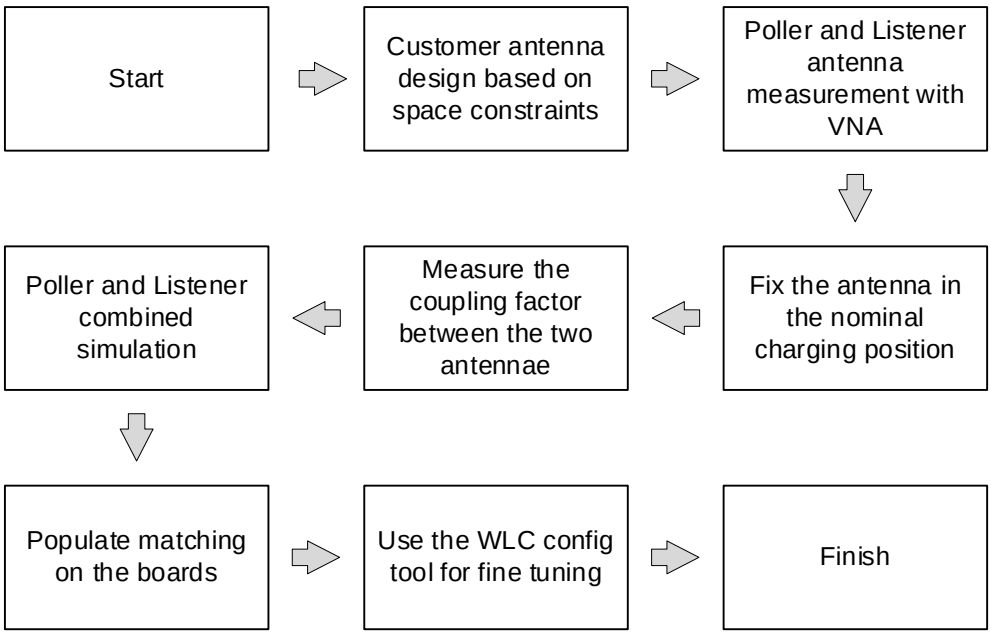


Figure 9. Antenna Matching Workflow

6.3 Application Requirements

The following NFC charging application requirements are to be considered and are needed before starting the antenna design. These are:

- Harvesting power requirements – voltage and current
- Available antenna area on Poller device
- Available antenna area on Listener device
- Placement of the antennas within the respective environment, especially with regards to proximity to metal surfaces (battery, PCB planes, frames, connectors, etc.)
- Required charging volume (in other words, the volume in which a Listener needs to be able to harvest a minimum amount of power)

The power harvesting requirements depend on the battery that needs to be charged and the desired charge time. This will define the required charging current. The PTX30W can handle a current range up to 250 mA (as defined in the datasheet). Besides the power needed to charge the battery, any additional load in the system also needs to be supplied by the harvested RF power and considered in the requirements.

Any metals near the antennas need to be shielded using ferrites. The ferrites used need to be suited for NFC applications and the losses in the ferrite kept to a minimum.

6.4 Antenna Design – Poller

The inductance range for the Poller antenna should be in the range of 300nH to 550nH. Typically, between 3 to 4 turns for the antenna have shown to be sufficient to achieve an inductance in this range. This of course depends on the available area, whether ferrites are used, and if metal surfaces are in close proximity. The traces should be made wide enough to achieve a low real impedance at 13.56MHz. A good starting point for the trace width for the Poller antenna has shown to be 0.8mm – 1.0mm, and a gap between traces of 0.15mm or 0.2mm – all dependent of course on the available area.

6.5 Antenna Design – Listener

The inductance range for the Listener antenna depends on the application requirements, especially the required charging current and the coupling between the Poller and Listener antenna. The required charging current is given by the battery itself and the time within which the battery shall be charged. The coupling between the antennas is influenced by several factors, such as:

- Antenna geometry
- distance between the antennas
- Antenna surrounding

The coupling between the antennas in NFC charging is typically lower than for other wireless charging technologies, where 30% is already quite high for this technology. For the purpose of designing antennas with the PTX130W and PTX30W, the coupling is divided into the following ranges.

- High coupling range will be defined at around 30% coupling between antennas
- Mid coupling range will be defined at around 20% coupling
- Low coupling range will be defined at 10% coupling

Determining the coupling between the antennas requires either 2-port VNA measurements or 3D full-wave simulation. An estimate can be measured using the 1-port VNA approach described in the section “Coupling Factor Measurement Method”.

The charging current can be roughly divided into greater than 150mA being high current, between 50mA and 150mA medium range and 50mA and below low current. This applies to power classes typically seen in NFC charging of around 1W and below harvested power.

Table 2. Coupling Factor and Charging Current between Antennas

Range	Coupling Factor	Charging Current
High	~30%	150mA – 250mA
Medium	~20%	50mA – 150mA
Low	~10%	< 50mA

The reason why the charging current and the coupling between the antennas is important in the antenna design for the Listener is because of how the driver's output impedance is impacted by these factors. Through the mutual inductance between the Poller and the Listener antennas, the Listener system presents an impedance to the output driver. Both the Poller's and Listener's antenna inductance, and the coupling factor **k**, determine the value of the mutual inductance (**M)**.

A high mutual inductance and a high charging current will result in a high impedance on the driver's output, thereby limiting its maximum output power. Since the charging current is given by the application requirements and the coupling factor is strongly dependent on the geometry and charging volume, one way to lower the driver's output impedance is by lowering the antenna inductances. Conversely, for low coupling factors due to the separation between the antennas, the inductance can be increased to increase the mutual inductance. The effect mentioned here can be explored in the QUCSStudio model shared below.

The following example from an investigation performed with the PTX130W/PTX30W demo illustrates this behavior where both charging current and coupling factor are varied. The Listener antenna inductance was varied to achieve the highest efficiency for each application case. The Poller antenna is the evaluation board antenna for all measurements.

Table 3. Listener Antenna Inductance Example

Listener antenna inductance needed to achieve maximum efficiency when using the Renesas evaluation kit with antennas in free air.

100mA Battery Load

Listener Antenna Inductance	Distance between Poller and Listener Antennas	Coupling (k)
480nH	4mm	0.3
900nH	7mm	0.2
1600nH	10mm	0.17

Listener antenna inductance needed to achieve maximum efficiency when using the Renesas evaluation kit with antennas in free air.

220mA Battery Load

Listener Antenna Inductance	Distance between Poller and Listener Antennas	Coupling (k)
200nH	4mm	0.3
480nH	7mm	0.2
900nH	10mm	0.17

In the design, start with a trace width of 0.6mm – 0.8 mm and a gap between traces of 0.15mm or 0.2mm (all dependent on the available area). Typically, two to six turns are sufficient for the Listener antenna. The required number of turns depends on the available area. Smaller antennas typically require more turns to achieve an inductance in the desired range. Having three turns on two layers each to achieve six turns in total has proven to be more beneficial, rather than having all six turns on the same layer. Other factors that need to be considered in the design are ferrites and metal areas in close proximity to the antenna, as these will have an impact on the antenna's characteristics.

6.6 Antenna Technology Considerations

The technology used to fabricate the antennas can have an impact on the antenna's performance. Especially the trace thickness, as this will influence losses in the antenna's performance. Using a thicker metal process lowers the antenna's resistance and reduce these losses. However, with a skin depth of 17.7µm for copper at 13.56MHz, the benefit of increasing the metal thickness will diminish the thicker it gets. A good technology to use is 35Ωm thick copper (1oz.) which allows the signal to penetrate the complete conductor cross-section.

6.7 Parameter Measurement

The following sections describe how to measure the antenna parameters, as well as a measurement method to determine the coupling factor.

6.7.1. Antenna Measurement

To measure the antenna parameters, a network or impedance analyzer is used and set up according to the procedure detailed below:

- Set the measurement mode of the network analyzer to S11 reflection measurement
- Use the Smith Chart format (R + jX) to display the impedance curve
- Set the start frequency at 1MHz and the stop frequency at 1500MHz
- Connect a short SMA cable to the RF port of the network analyzer and start the calibration using **OPEN**, **SHORT** and **50Ω LOAD** as the load resistance
- Connect the SMA cable to the antenna to be measured with one pin soldered to the HOT terminal of an SMA connector, and a second pin soldered to one of its ground connections

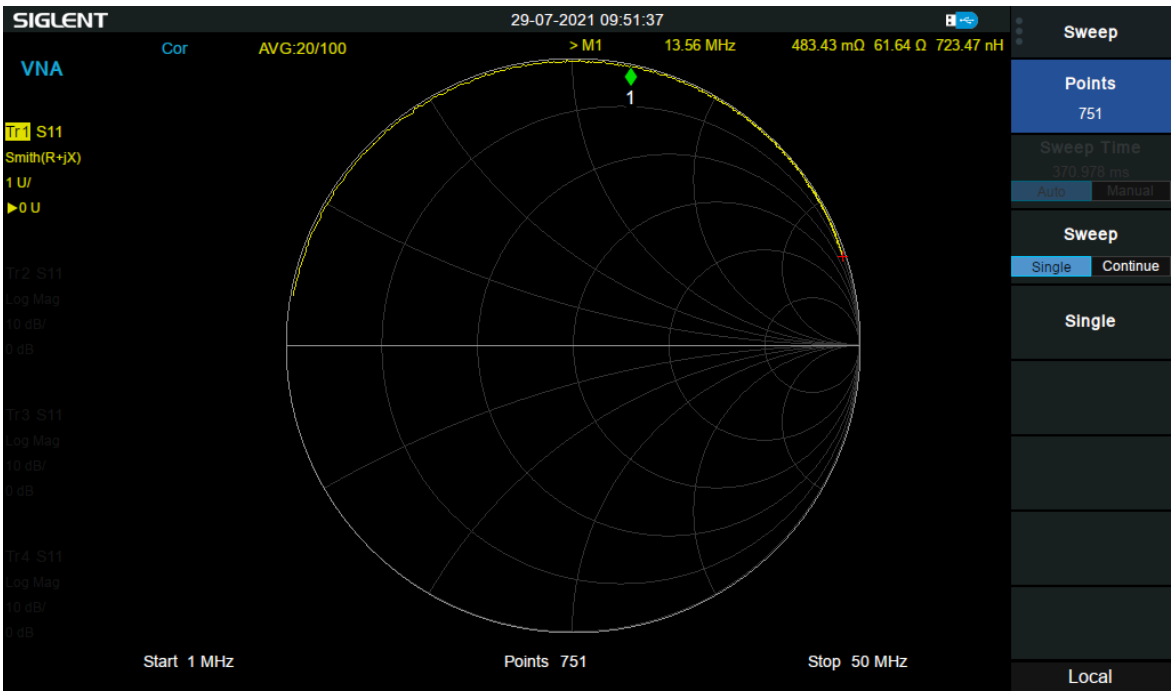
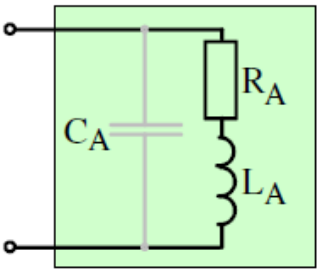


Figure 10. Smith Chart – Loop Antenna Measurement with VNA

To retrieve the loop antenna impedance, a marker needs to be set at 13.56MHz and the real (Rs) and imaginary parts (Xs) converted to resistance R_A and inductance L_A.

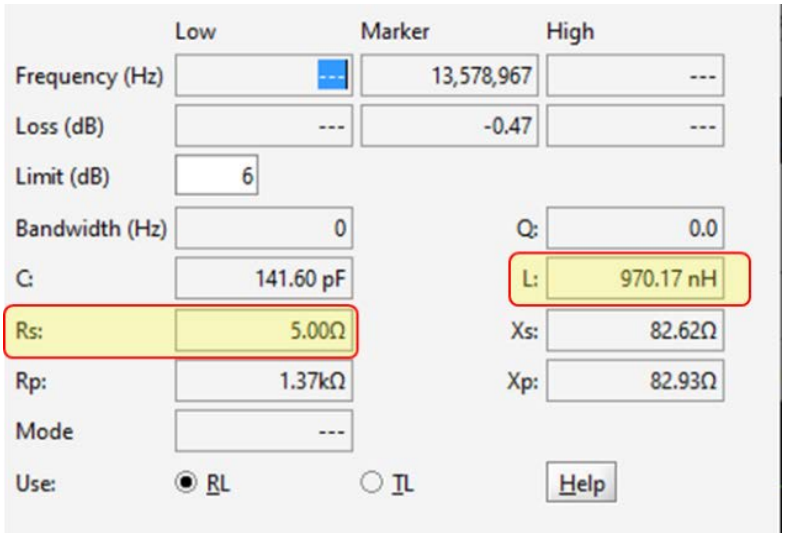


R_A = Rs; LA = XS/2πf

The parasitic capacitance C_A is relatively low and can be omitted in the matching network calculation. The formula to calculate this to completeness is:

$$f_0 = \frac{1}{2\pi\sqrt{L_A C_A}} \quad => \quad C_A = \frac{1}{4\pi^2 L_A f_0^2}$$

In most of the network analyzers, the impedance value is internally processed and the values are already available, as shown below.



Based on this measurement, it is possible to extrapolate the electrical parameters of the antenna.

6.7.2. Coupling Factor Measurement Method

This method requires only a 1-port VNA capable of measuring in the frequency range around 20MHz.

6.7.2.1. Measurement Procedure

1. Switch on the VNA and let it warm up (ca 30 min). Then set the frequency range to 10MHz – 17MHz, linear sweeping with at least 201 measurement points.
2. Calibrate the device using an appropriate calibration kit.
3. Connect the VNA probe to coil 1 (whichever from the two coils) and align the coils to achieve their required mutual position.

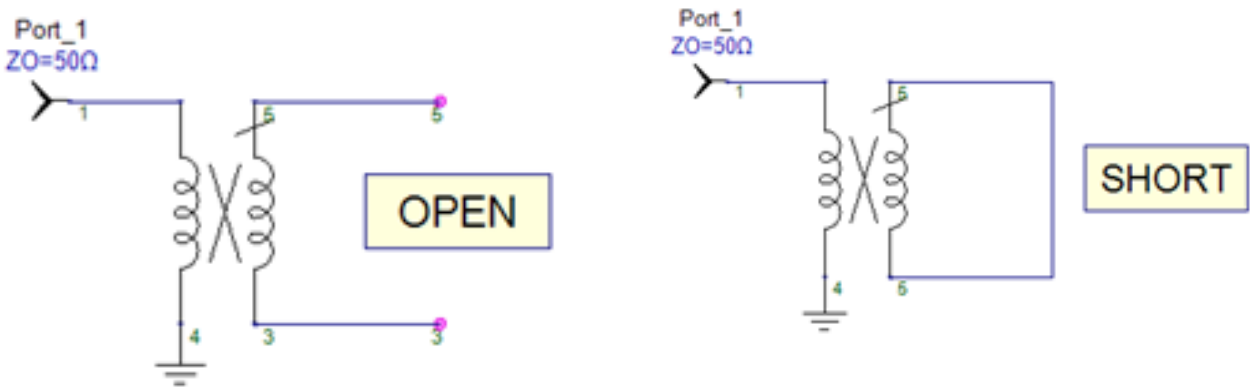


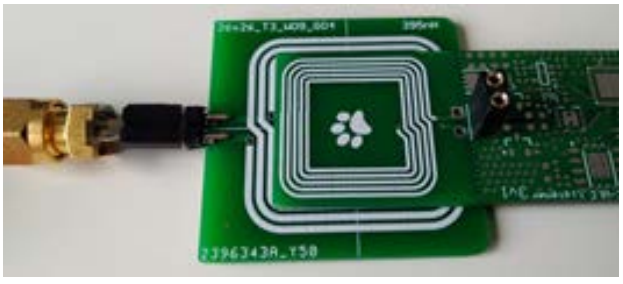
Figure 11. Coupling Factor Measurement

4. Measure the inductance of coil 1 at a frequency of 13.56MHz while leaving coil 2 open. This achieves a value of L1o.
5. Measure the inductance of coil 1 at a frequency 13.56MHz while shorting coil 2. This achieves a value of L1s.
6. Calculate the coupling between the two coils using the following formula:

$$coupling = \sqrt{((L1o - L1s)/L1o)}$$

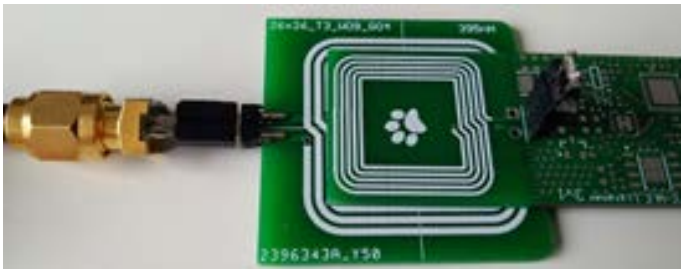
Example:

Open



L1o = 370.5nH

Short



L1s = 328nH

Despite the fact that the source impedance of VNA is not included in the formula, the overall results correlate well with the results gained by a more precise 2-port measurement method.

6.8 Matching Simulation

The following sections describe how to use the QucsStudio model used in the simulation. An example simulation using the evaluation board antennas is given in the evaluation board hardware descriptions of the datasheet.

6.8.1. Qucs Studio Model

- QucsStudio version 4.3.1
- PTX130W/PTX30W Matching Simulation Template

6.8.2. Renesas Matching Model PTX130W/PTX30W

The matching model system using the PTX130W and the PTX30W is shown below. This is a simplified model.

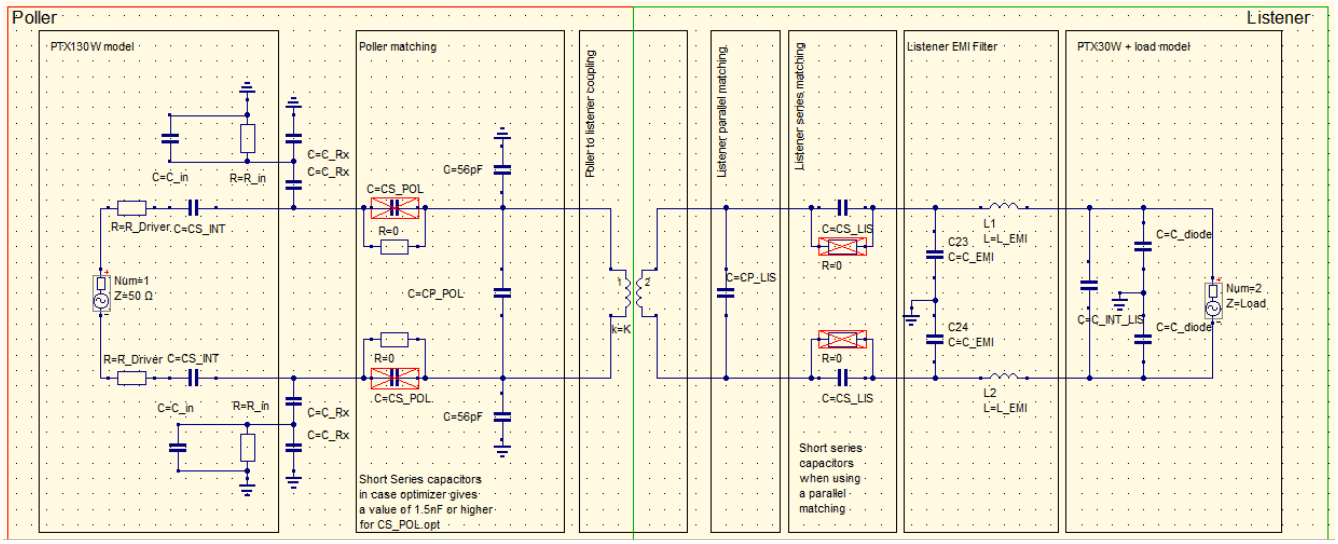


Figure 12. PTX130W/PTX30W Matching Model System

6.8.2.1. Input Parameters

The input parameters for this model are:

- **RS_POL**

  Real part of the Poller antenna impedance at 13.56MHz.
- **XS_POL**

  Imaginary part of the Poller antenna impedance at 13.56MHz.
- **RS_LIS**

  Real part of the Listener antenna impedance at 13.56MHz.
- **XS_LIS**

  Imaginary part of the Listener antenna impedance at 13.56MHz.
- **XS_short**

  Imaginary part of the Poller antenna impedance at 13.56MHz when measured with the Listener antenna in nominal charging position and the antenna terminals shorted.
- **XS_open**

  Imaginary part of the Poller antenna impedance at 13.56MHz when measured with Listener antenna in nominal charging position and the antenna terminals open.
- **L_EMI**

  Series inductor needed for EMI filter on Listener side.

- **R_EMI**
  Series resistance of EMI filter inductor.
- **C_EMI**
  Parallel capacitance needed for EMI filter on Listener side.
- **K**
  Coupling factor calculated from XS_short and XS_open.
- **Load**
  This mimics the loading on the Listener side.

6.8.2.2. Output Parameters

The output parameters of the simulation are:

- **CS_POL**
  Series matching capacitor Poller.
- **CP_POL**
  Parallel matching capacitor Poller.
- **CP_LIS**
- Parallel matching capacitor Listener.
- **CS_LIS**
- Series matching capacitor Listener.

6.8.2.3. Model Parameters

- **R_Driver**
  Output driver impedance.
- **CS_INT**
  Internal series capacitance.
- **C_in**
  Capacitive loading due to receiver stage.
- **R_in**
  Resistive loading due to receiver stage.
- **C_INT_LIS**
  Internal capacitance of Infineon SLC36 tag.
- **CS_T**
  Decoupling capacitance for Infineon SLC36 tag.
- **C_diode**
  Parasitic capacitance of rectifier diodes.
- **CS_POL.opt**
  Series capacitance on the Poller – output from optimizer.
- **CP_POL.opt**
  Parallel capacitance on the Listener – output from optimizer.

6.8.3. Target Impedance

The PTX130W operates most efficiently when the output driver's load is a real impedance of around 5Ω. This is the target impedance for achieving optimum efficiency when matching the antennas, and includes all the components in the RF circuit, the internal resistances and capacitances. Also included is the load on the Listener side.

6.8.4. Simulation Procedure

1. Set the coupling factor **K** to 0; Poller and Listener are decoupled. Enable and run the optimization function. The optimizer will tune the Poller antenna to 13.56MHz while minimizing the impedance. Depending on the antenna inductance, the external series capacitance "**CS_Reader**" may be shorted to not include it in the simulation.
2. Copy the values from "**CS_Reader.opt**" and "**CP_Reader.opt**" to "**CS_Reader**" and "**CP_Reader**" respectively. Deactivate the optimizer.
3. Set the coupling factor to the measured value and the load as defined by the charging requirements.
4. Tune the Listener to 13.56MHz with either the series capacitance or series parallel combination. For applications with a low charge current and medium to low coupling, a parallel matching may be more suitable. For this case, it may be necessary to tune the Listener antenna to a higher frequency to prevent detuning of the Poller. Detuning of the Poller can be observed when the driver's load impedance moves away from the real axis at 13.56MHz in the Smith Chart.
5. The impedance on the driver side (S11) is to be as close as possible to 5Ohm + j*0Ohm.

6.9 Matching Optimization

Using the Config Tool and evaluation boards is an easy way to test and optimize custom antenna setups. Therefore, the evaluation board antennas can be detached and the custom antenna setup connected. Using the Config Tool easily enables the supply voltage and wave amplitude setup for the PTX130W, and the runtime configuration of the PTX30W as well. A detailed description of the functionality and settings can be found in the Config Tool's user manual. The performance can be directly measured with the onboard power settings.

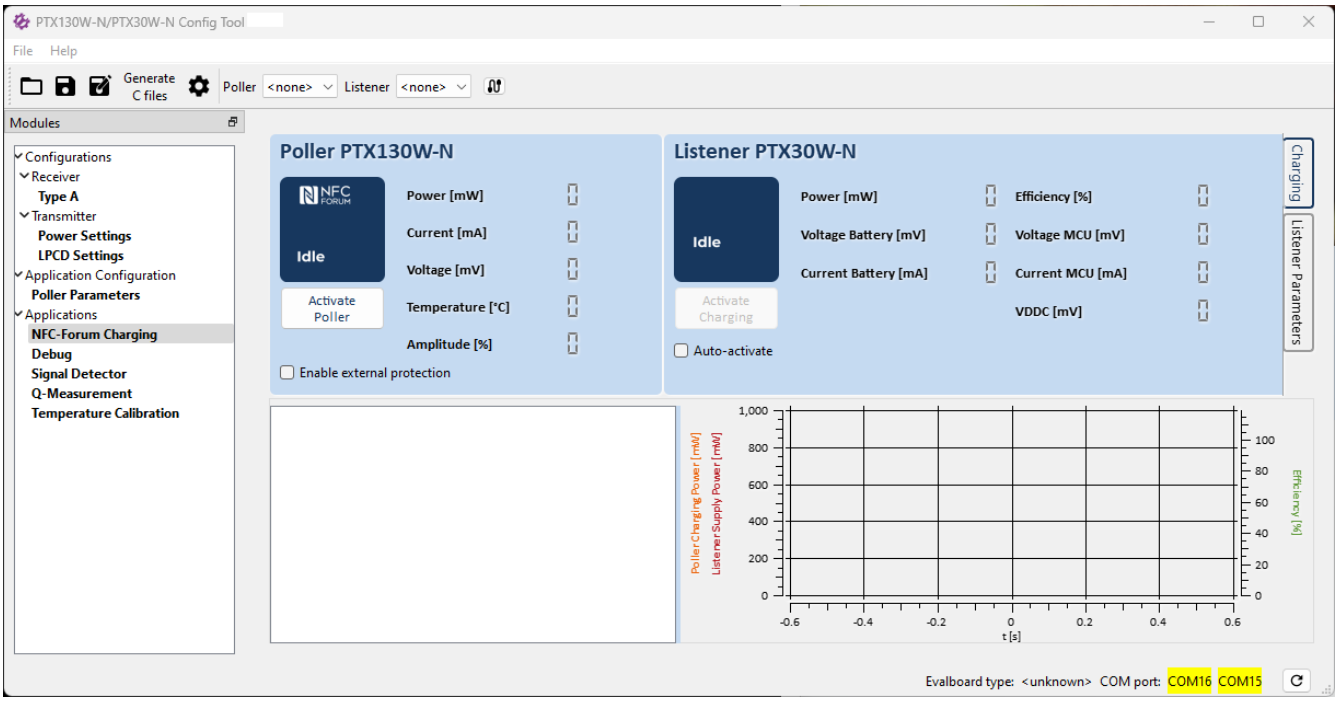


Figure 13. PTX130W/ PTX30W Config Tool Window

6.9.1. Config Tool Q-Factor Measurement

The Config Tool includes a function to measure the Q-factor and resonance frequency at the resonance plane of the output driver. In case of high coupling between the Poller and Listener antenna, it can be seen that the resonance will be lower than 13.56MHz, even if each system itself is tuned to 13.56MHz. In that case, match the Listener at a higher frequency as explained in section 6.8.4.

7. PTX130W Low Power Card Detection Configuration

7.1 Overview

The Low Power Card Detection (LPCD) reduces the amount of current consumed by the PTX during Reader mode. With LPCD enabled, the device can be in active or battery mode for an extended period of time.

The PTX achieves reduced current consumption by using only a small set of analog/digital blocks during this mode, and for a shorter time as compared to the default polling mode.

The following blocks are used during LPCD:

- Transmitter on with Continuous Wave (CW)
- Rx Frontend (configured during Start-up)
- PREDAC (configured during Start-up)
- PGA2 (user-specific configuration – Detection Range)
- ADC
- Digital Evaluation (user-specific configuration – Sensitivity)

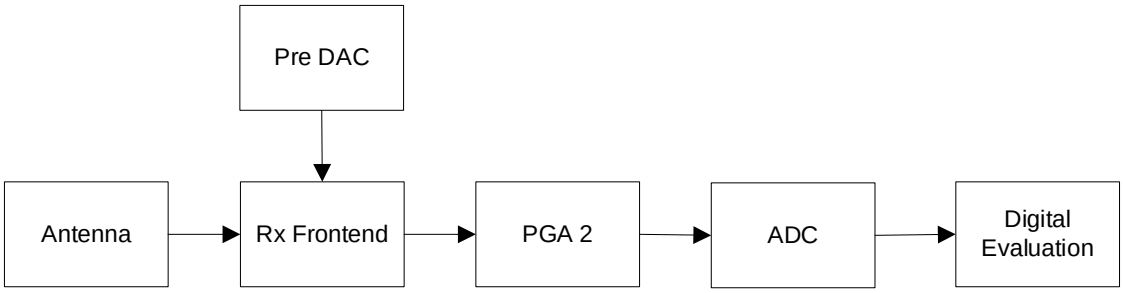


Figure 14. Blocks Used During LPCD

Compared to a normal polling procedure as shown in the figure below, LPCD polls only once the LPCD is triggered. Otherwise, the system remains in stand-by in between LPCD pulses.

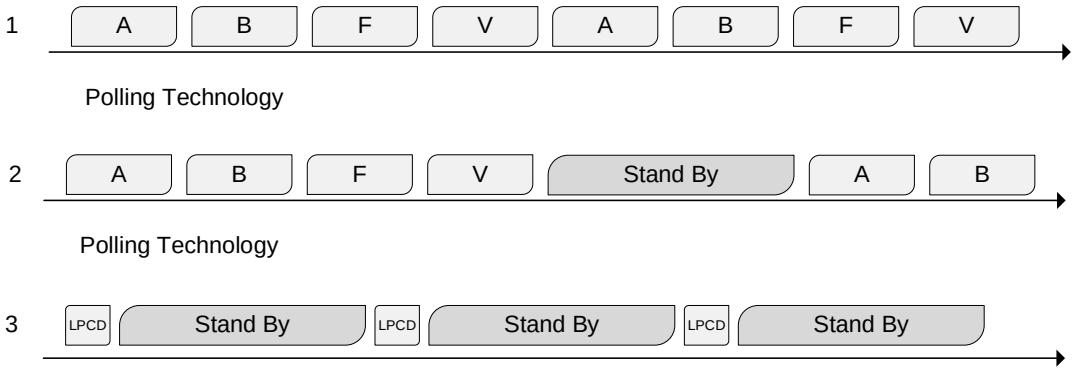


Figure 15. Normal Polling Procedure

7.2 Normal LPCD Behavior

When the host starts the LPCD routine (Mode 3), an initial polling sequence is called to ensure no card is within the field and to prevent false initial LPCD calibration. If no card was detected, the system starts the initial LPCD calibration (PRE-DAC). Directly after that, the recalibration is called which sets the ADC to a desired starting value (center). During the first few LPCD calls, the recalibration is performed several times to compensate for thermal and noise drifts due to the cooling down of the DUT. After a couple of cycles, and once a stable state is reached, the device gets powered up from the stand-by periods only for the short LPCD pulses (~75µs). This dramatically reduces the current consumption.

7.3 Configuration

The configuration of the key parameters of the LPCD is done via the "**RF_configuration**" in the Transmitter section. The following parameters can be adjusted and are explained in greater detail in section 7.3.1:

- Wave amplitude – LPCD
- LPCD_SAMPLING_INTERVAL
- LPCD_PGA2_GAIN
- LPCD_I_LIMIT
- LPCD_Q_LIMIT
- DCC Settling Time
- Average Sample Count

7.3.1. Parameter Details

- **Wave amplitude – LPCD**

  The transmit signal's wave amplitude can be adjusted using the "**Wave amplitude - LPCD**" slidebar to limit the detection range and further reduce the current consumption.

- **LPCD_SAMPLING_INTERVAL**

  To reduce the influence of distortion over the RF field/Supply, the sampling interval between LPCD ADC samples can be increased from 0µs (default) up to 255µs. The resulting LPCD pulse width increases by 32 * LPCD_Sampling_Interval + ~75µs.

- **LPCD_PGA2_GAIN**

  This parameter specifies the gain setting for I- and Q-branch. These goes hand-in-hand with the detection range. Values can be set between 0dB and 30dB.

- **LPCD_I_LIMIT and LPCD_Q_LIMIT**

  The I and Q Limits are used to adjust the sensitivity, where the Q value should be lower than the I limit due to different balanced detection paths. Values can be set between 0x00 (0) and 0xFF (255).

- **DCC Settling Time**

  DC compensation for the internal signal before the digital detection block. Value can be set from 20µs to 255µs.

- **Average Sample Count**

  This register defines the number of measurements for the averaging sample count. Value can be set from 1 to 32.

7.3.2. Configuration Procedure

Use the Config Tool to set up and fine-tune the device.

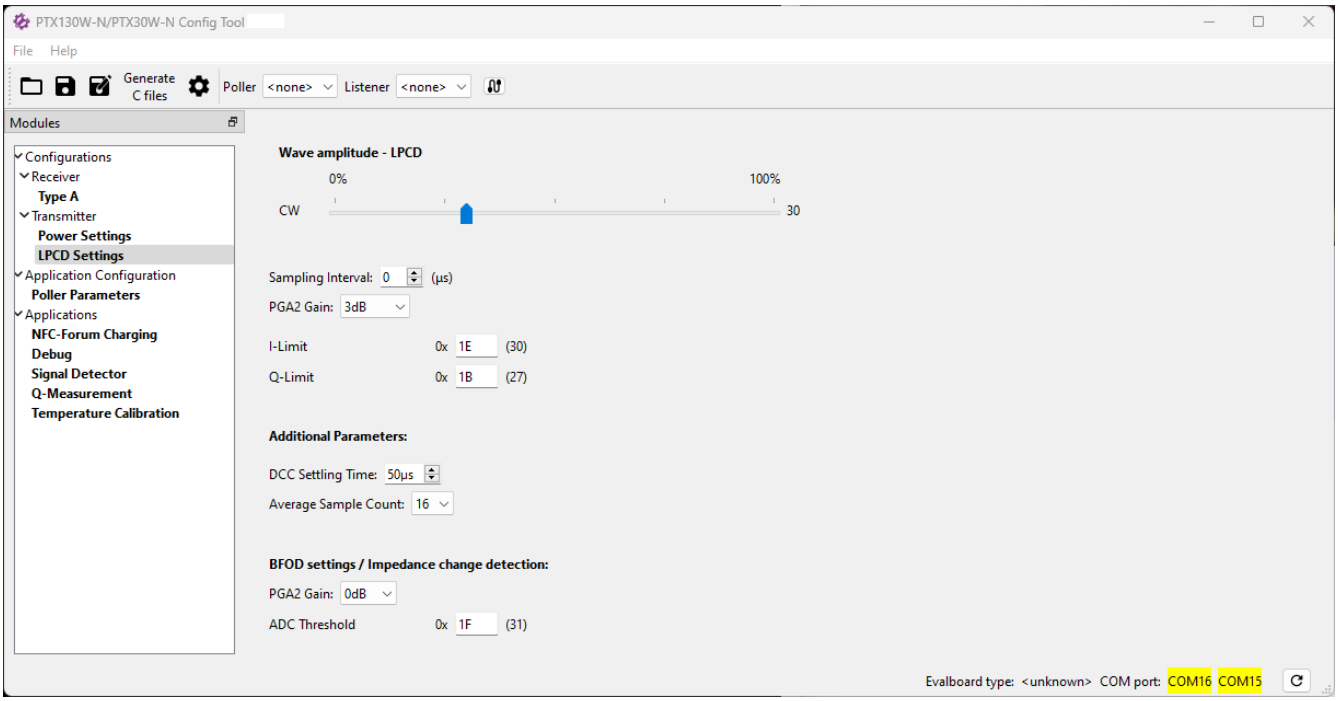


Figure 16. Config Tool LPCD Settings Window

1. **Desired Sine Amplitude**

The following table shows the current consumption behavior for different amplitude and stand-by time settings.

Relative Current Consumption (%)		Sine Amplitude (%)				
		100	**80**	**60**	**50**	**40**
Discovery Stand-by Time(s)	**0,1**	100	84	71	65	59
	0,33	32	27	23	21	19
	0,5	22	18	16	15	13
	0,75	16	13	11	11	9
	1	12	10	9	8	8

The higher the value of the sine wave amplitude, the higher the LPCD pulse amplitude and the detection distance will be at the cost of higher current consumption.

2. **LPCD_SAMPLING_INTERVAL Setting**

Set sampling interval to 0µs for the lowest current consumption.

Increasing the sampling interval will increase the pulse duration, making the LPCD more robust against false card detection.

3. **LPCD_PGA2_GAIN**

Increase the PGA2 Gain setting incrementally to increase the detection range and to view the false alarms. The value for PGA2 should start at 0dB, with its highest at 30dB. The higher the value, the higher the receiver sensitivity.

4. **LPCD_I_LIMIT and LPCD_Q_LIMIT**

If the detection range from previous steps is already acceptable, continue with the fine-tuning by adjusting the Limits. To establish wanted asymmetry in the I and Q branches, the I-branch should be held higher than the Q-branch.

Start by setting both branches to a value where no false alarm occurs. Then start decreasing the Q branch limit. The last step will be the I branch adjustment.

Parameter Adjustments

Depending on current consumption behavior, if the previous steps result in an undesirable detection performance, the parameters can be adjusted as follows:

Behavior	Suggested Change in the CFG	Impact On
High false alarm rate; within wanted detection range.	Lower PGA 2 gain.	Lower noise; lower field change impact; decreases detection distance.
	Lower Q-limit.	Increases sensitivity on amplitude change.
	Lower I-limit.	
High false alarm rate; outside wanted detection range.	Increase Q-limit.	Higher ADC fluctuations are tolerated.
	Increase I-limit.	
	Increase SAMPLING_INTERVAL.	More robust against distortions.
	Increase PGA2 gain.	Higher field change impact; increases detection distance.
	Increase sine amplitude.	Higher field change impact.
Good false alarm rate but short detection distance.	Increase PGA2 gain.	Higher sensitivity.
	Decrease Q- and I-limit.	Faster detection response; higher sensitivity.
	Increase sine amplitude.	Higher field change impact.

LPCD Notification in the Config Tool

The LPCD can be enabled in the *Poller Parameters* section of the Config Tool. By default, a hybrid between regular polling and LPCD is used, where after a set number of LPCD pulses, a regular polling function is performed.

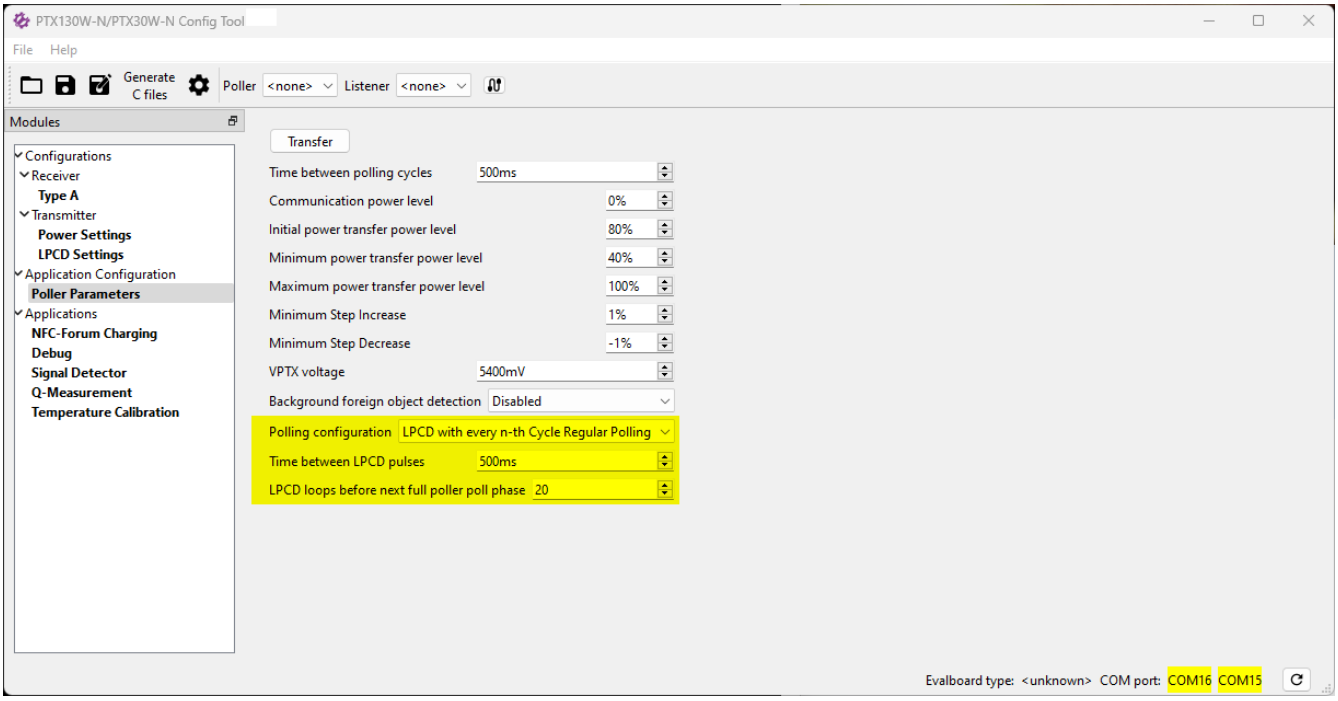


Figure 17. Config Tool Poller Parameters Window

In the *Debug* section of the Config Tool, an LPCD counter can be started. This will count detections of the LPCD and can be used to fine tune its sensitivity.

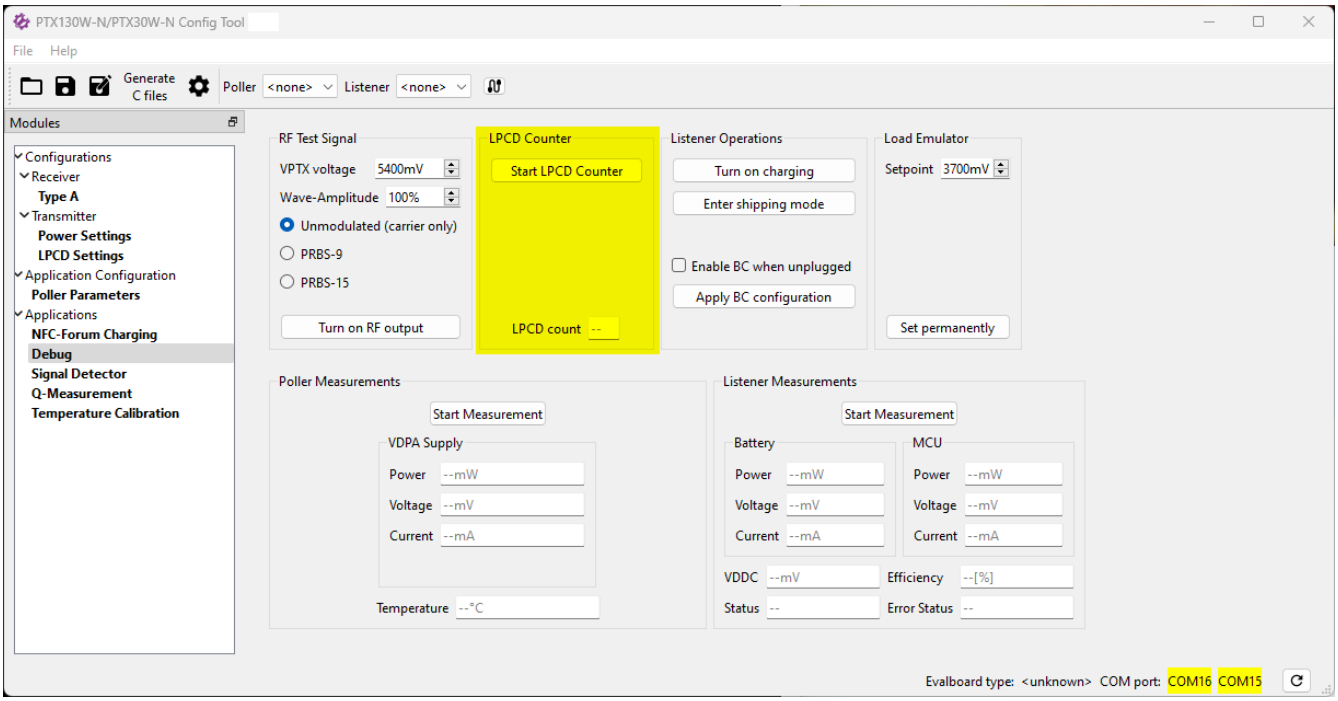


Figure 18. Config Tool Debug Window

The LPCD notification should indicate 0 when no NFC card is in proximity of the reader. This is the condition when there are no false detections. The counter starts increasing if a conductive object is moved closer to the reader antenna.

If the counter number is increasing without having an object on top of the antenna, this means that the LPCD parameters need to be adjusted. For example, reducing the sine wave amplitude or reducing the sensitivity of the receiver.

8. References

PTX130W datasheet

PTX30W datasheet

Hardware Description PTX130W-NFC-WLC-Poller-EB

Hardware Description PTX30W-EB-ST-CSP16-LISTENER

Hardware Description PTX30W-NFC-WLC-MCU-EB

QucsStudio

PTX130W-N/PTX30W-N Config Tool

PTX130W-N/PTX30W-N Config Tool User Manual

9. Revision History

Revision	Date	Description
1.00	Nov 22, 2023	▪ Updated to Renesas template ▪ Added Startup circuitry ▪ Updated reference schematics and Qucs model

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