QCIOT-5APWRPOCZ

The QCIOT-5APWRPOCZ power board enables quick prototyping of the RAA211651 60V 5A Low Quiescent Current Integrated Switching Regulator in a custom system design. The ISL28023 Precision Digital Power Monitor is designed to measure and control the regulator output of the RAA211651 with margining.

The board provides a standard Pmod™ Type 6A (extended I^2C) connection for the on-board sensor to plug into any required MCU evaluation kit with a matching connector. The QCIOT-5APWRPOCZ features Pmod connectors on both sides of the board to allow additional Type 6/6A boards to connect in a daisy-chained solution with multiple devices on the same MCU Pmod connector.

The software support that is included with the Renesas IDE (e^2 studio) provides code generation to connect the device and the MCU so that development time is significantly reduced. With its standard connector and software support, the QCIOT-5APWRPOCZ is ideal for the Renesas Quick-Connect IoT to rapidly create an IoT system.

Features

- 4.5V to 60V input supply range
- Adjustable output voltage (0.8V to 3.3V)
- Variable load current, up to 5A
- ΔΣADC, 16-bit native resolution
- System voltage/current monitoring with efficiency reporting
- Overvoltage/undervoltage and current fault monitoring with 500ns detection delay
- Standardized type 6A Pmod connector supports I^2C extended interface
- Dual connectors allow pass-through signals for daisy-chained solutions
- Software support in e^2 studio minimizes development time with one-click code generation

Board Contents

- QCIOT-5APWRPOCZ

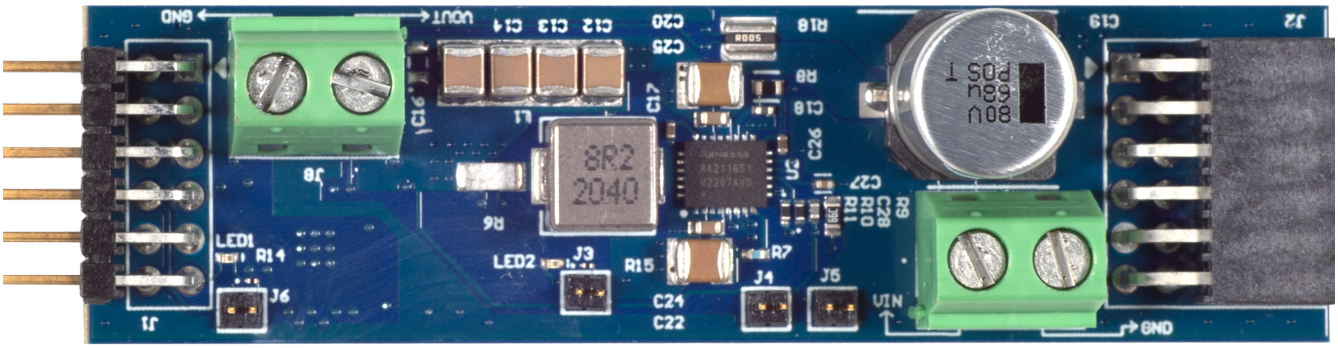


Figure 1. QCIOT-5APWRPOCZ Image

Contents

1. Functional Description

The QCIOT-5APWRPOCZ is intended as a quick connect prototyping solution for a switching buck regulator and digital power monitoring. This board can enable the designer to quickly evaluate applications where higher voltage and current supply from USB power is required. The QCIOT-5APWRPOCZ takes external voltages between 4.5V to 60V and can deliver up to 5A to an external load. A digital power monitor can monitor both input and output voltage and current, and it can report diagnostics like power efficiency, peaks, and faults.

The block diagram below highlights the main parts of the system:

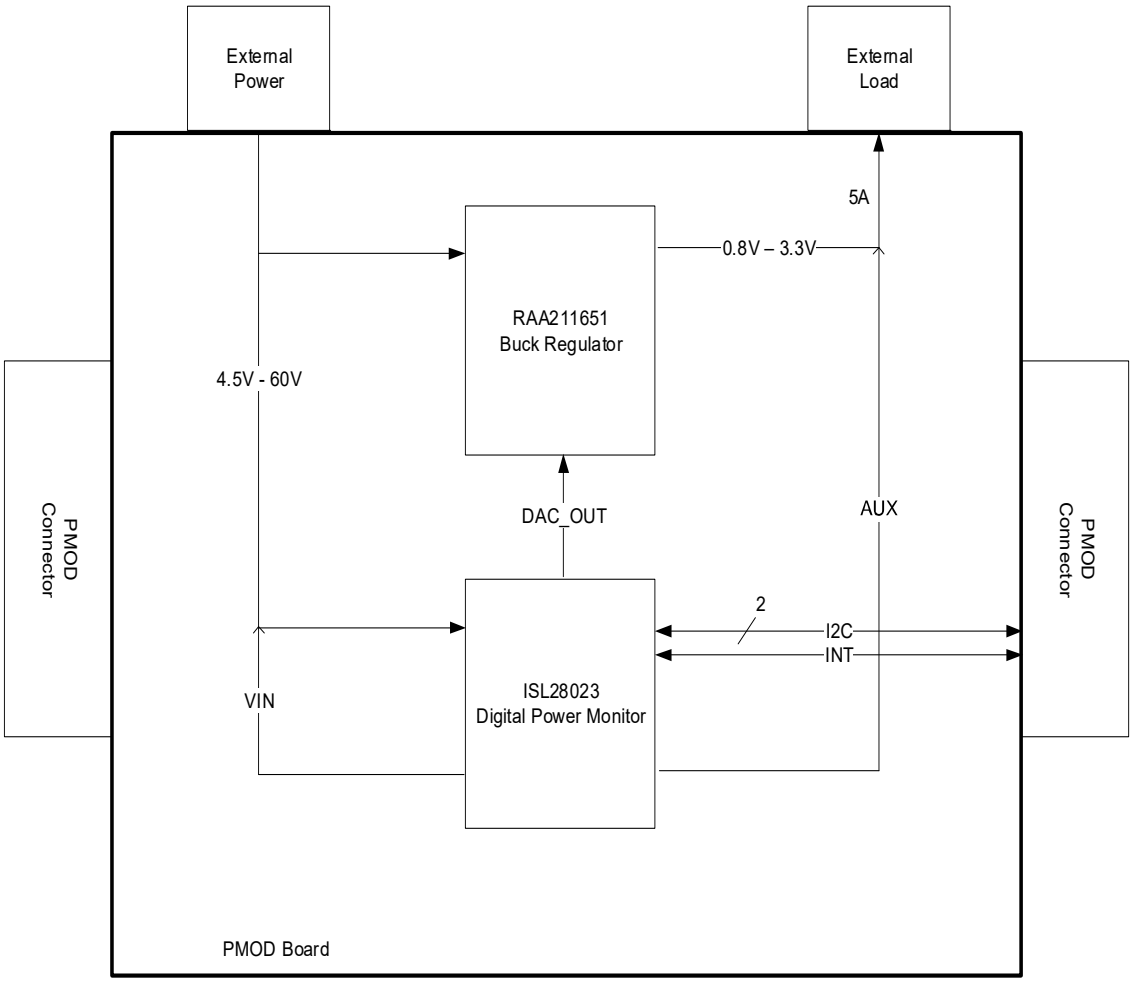


Figure 2. QCIOT-5APWRPOCZ Block Diagram

The building blocks of QCIOT-5APWRPOCZ and their functionality are as listed:

- RAA211651 – Integrated 60V, 5A synchronous buck regulator with the Constant On-Time (COT) control scheme. It supports a wide range of input voltage from 4.5V to 60V and adjustable output voltage (0.8V to maximum duty cycle × VIN). It also features a very low quiescent current, typically 19µA at 24V input. The modulation scheme used allows for high efficiency at all output load levels, especially at light-load conditions.
- ISL28023 – Bidirectional high-side and low-side digital current sense and voltage monitor with a serial interface. The device monitors power supply current, voltage and provides the digital results along with calculated power. The ISL28023 provides tight accuracy of 0.05% for both voltage and current monitoring.

1.1 Operational Characteristics

The QCIOT-5APWRPOCZ can be used as a starting point for DC power distribution, whether in high voltage industrial or battery powered applications.

The board has been designed to the following specifications:

- Input voltage range = 4.5V - 60V
- Output voltage range = 0.8V - 3.3V
- Output current = 0A - 5A
- Maximum output voltage ripple: 3%

While the RAA211651 is capable of outputting higher voltages, as much as max duty cycle × VIN, the range is constrained to be up to 3.3V to optimize output filtering. The minimum output voltage is 0.8V and is set by the internal reference voltage of the RAA211651.

(EQ. 1) $$VOUTmax = \left[\frac{0.8}{R11}\right]R10 + 0.8$$

The output range is set by resistors R10 and R11 on the board, which forms a resistor divider in a feedback loop between the output voltage and reference voltage. Users who wish to change the output range can change the values of these resistors, but also must consider the values for the output filter components. Renesas provides a spreadsheet to help calculate these parameters.

1.1.1 Adjusting Output

While the output voltage range is set by resistors R10 and R11, the output voltage can be changed within the range by adjusting the voltage applied across R9. This can be done using the voltage margining feature of the IS28023, where the user can program the margin DAC output voltage using I^2C.

The RAA211651 output voltage is in a feedback loop with its FB pin, which is compared to a reference voltage of 0.8V. The feedback loop attempts to make the FB pin match 0.8V, and thus the current across R11 equals 0.8V divided by R11.

Applying a voltage across R9 and injecting a current into the node results in lowering the output voltage required to maintain 0.8V at the FB pin. The output voltage change is in proportion to R9 and R10.

(EQ. 2) $$VOUT = \left[\frac{0.8}{R11} - \frac{VDAC - 0.8}{R9}\right]R10 + 0.8$$

1.1.2 Fault Monitoring

The QCIOT-5APWRPOCZ features fault monitoring circuitry to detect when power exceeds thresholds. The digital power monitor ISL28023 can set thresholds for overvoltage, undervoltage, and overcurrent. In addition, RAA21651 provides a power-good signal that communicates whether the regulator is operating normally. The following signals are available for fault monitoring:

- SMBALERT1
- SMBALERT2
- Power Good

1.1.2.1 SMBALERT1

SMBALERT1 pin on the ISL28023 is an open-drain pin that requires an external pull up. During normal operation, SMBALERT1 is pulled high to 3.3V using R13 if jumper J3 is in place. The user can set overvoltage, undervoltage, and overcurrent levels that would trigger SMBALERT1 to pull down.

SMBALERT1 signals the host MCU on any threshold cross event through pin 7 of the Pmod interface. In addition, LED2 on the board turns on.

When the user is ready, SMBALERT1 can be reset through clearing the fault status registers.

1.1.2.2 SMBALERT2

SMBALERT2 pin of ISL28023 is a push-pull output that is high on normal operation, and low after threshold cross detection. This pin is triggered by the same overvoltage, undervoltage, and overcurrent levels that trigger SMBALERT1.

SMBALERT2 is connected to the enable pin of RAA211651, and it is used as a failsafe shutoff to the power regulator. This pin is not connected to the host MCU.

1.1.2.3 Power Good

RAA211651 provides a power-good (PG) pin to signal normal operation. This is an open-drain pin that is pulled up by R12 if jumper J6 is in place.

PG asserts high when both the regulator soft-start completes and the FB pin voltage exceeds 91% of VREF. When the buck regulator is in normal operation, PG is remains high. PG goes low if EN is driven low or the FB pin voltage exceeds the ±12% PG tolerance or any fault conditions exists.

PG signals the host MCU using Pin 10 of the Pmod interface, and it turns on LED3(RED) when pulled down during a fault.

1.2 Setup and Configuration

Required or Recommended User Equipment – The following additional lab equipment is required for using the board (and is sold separately):

- FPB-RA4E1

1.2.1 Software Installation and Usage

Visit the Renesas website for the latest version of the e^2 studio installer. Renesas recommends version 2024 or later. The minimum FSP version supporting the QCIOT-5APWRPOCZ is FSP 5.1.0. For the latest sensor support, ensure that the latest release is used.

Visit the Renesas Quick-Connect IoT site for more information about creating your customized system solution.

1.2.2 Kit Hardware Connections

Follow these procedures to set up the kit (see Figure 3).

1. Ensure that the MCU evaluation kit in use has a Pmod connector set to Type 6A (refer to the kit hardware manual for details). Renesas recommends using FPB-RA4E1.
   a. If no Type 6A Pmod is available, ensure that the MCU evaluation kit can use the US082-INTERPEVZ interposer board. Insert the board into the MCU connector before adding any sensor boards.
2. Plug in the QCIOT-5APWRPOCZ to the Type 6A connector. Be careful to align Pin 1 on the sensor board and MCU kit.
3. Connect the J3 and J6 jumpers to place 4.7kΩ pull-up resistors on the IRQ and PG bus lines resp. Also, if the MCU doesn't have internal pull-up, connect J4 and J5 to place 4.7kΩ pull-up resistors on I^{2}C. RA4E1 has internal pull-ups.
   a. Only one set of I^{2}C pull-up resistors should be used on the bus. If multiple Pmod connected boards are used, only one board should have the jumpers present.
   b. If multiple modules use the IRQ# line on the PMOD, only one pull-up jumper should be present.
   c. MCU kits typically do not have pull-up resistors present on the bus lines, but ensure to check for them.

4. Connect power source to VIN and GND of screw terminal connector J7, and load to VOUT and GND of J8 using wires or terminal pins. If using wires, ensure the wire gauge is a sufficient thickness to carry the operating current load. Apply VIN between 4.5V to 60V.
5. The device is now ready to be used in the system. Follow the MCU kit instructions for connecting and powering up the evaluation kit.

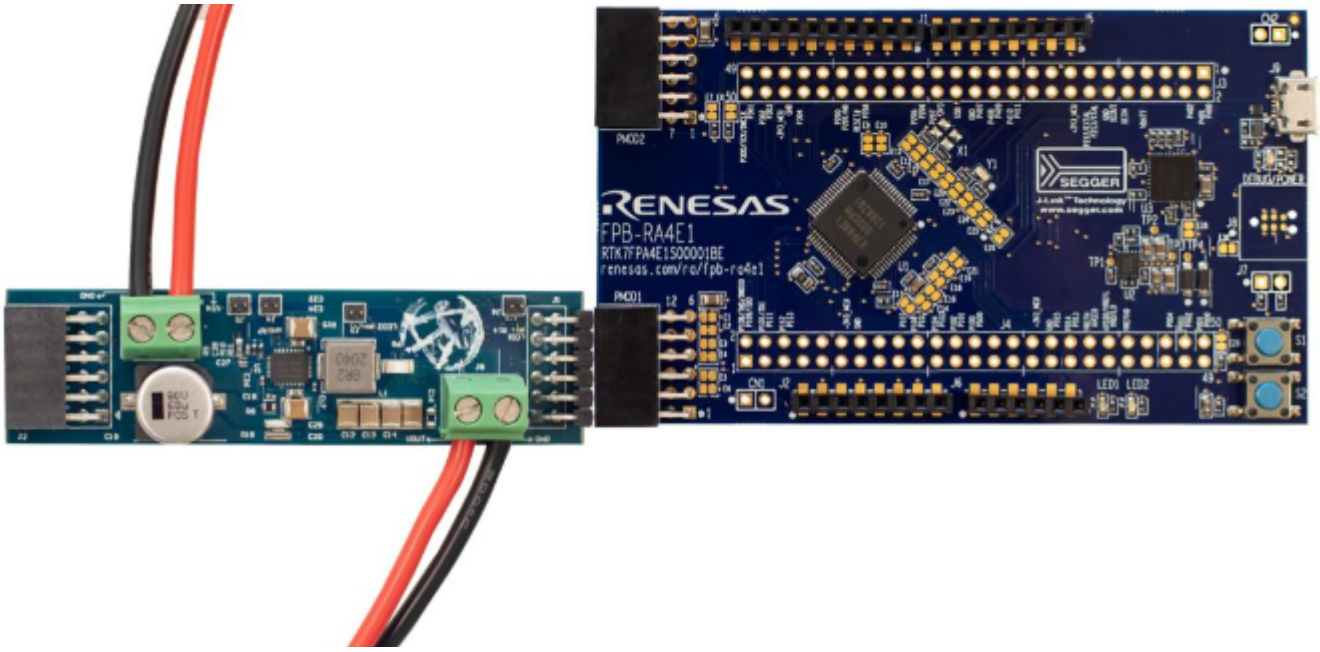


Figure 3. QCIOT-5APWRPOCZ with FPB-RA4E1 MCU Kit

1.2.3 I²C Address Select

The QCIOT-5APWRPOCZ has a default I²C address of 1011 111 for binary, 0x5F for the 7-bit address, or 0xBE/F for the 8-bit address. If this is in conflict with another device on the I²C line, the user can change the I²C address by removing the 0Ω resistor R3 on the board. To change the address, connect A2 to GND or SDA. A1 and A0 are connected to SCL, so changing A2 gives an option for three I²C addresses.

For details on I²C addresses, see the table, *I²C Slave Addresses,* in the *ISL28023 datasheet*.

2. Board Design

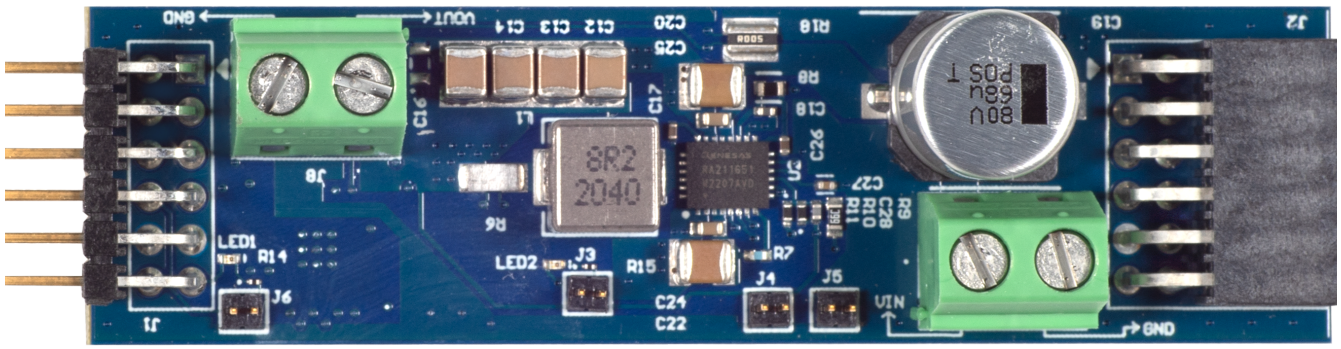


Figure 4. QCIOT-5APWRPOCZ Image (Top)

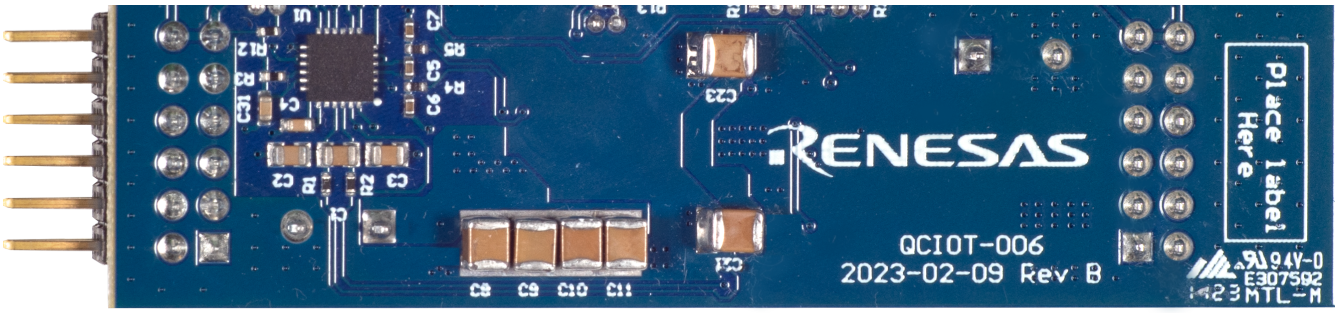


Figure 5. QCIOT-5APWRPOCZ Image (Bottom)

2.1 Schematic Diagrams

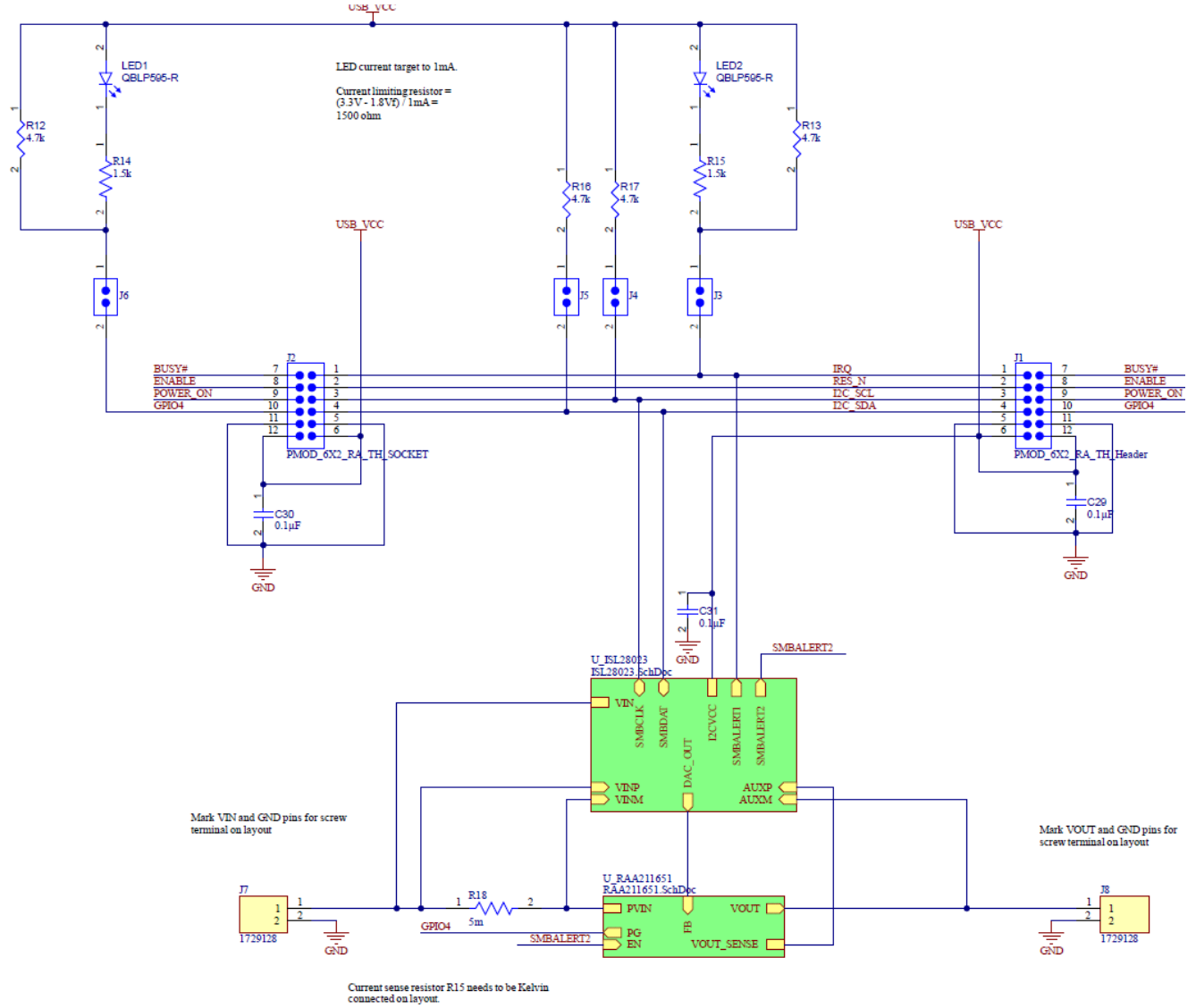


Figure 6. CIOT-5APWRPOCZ Schematic

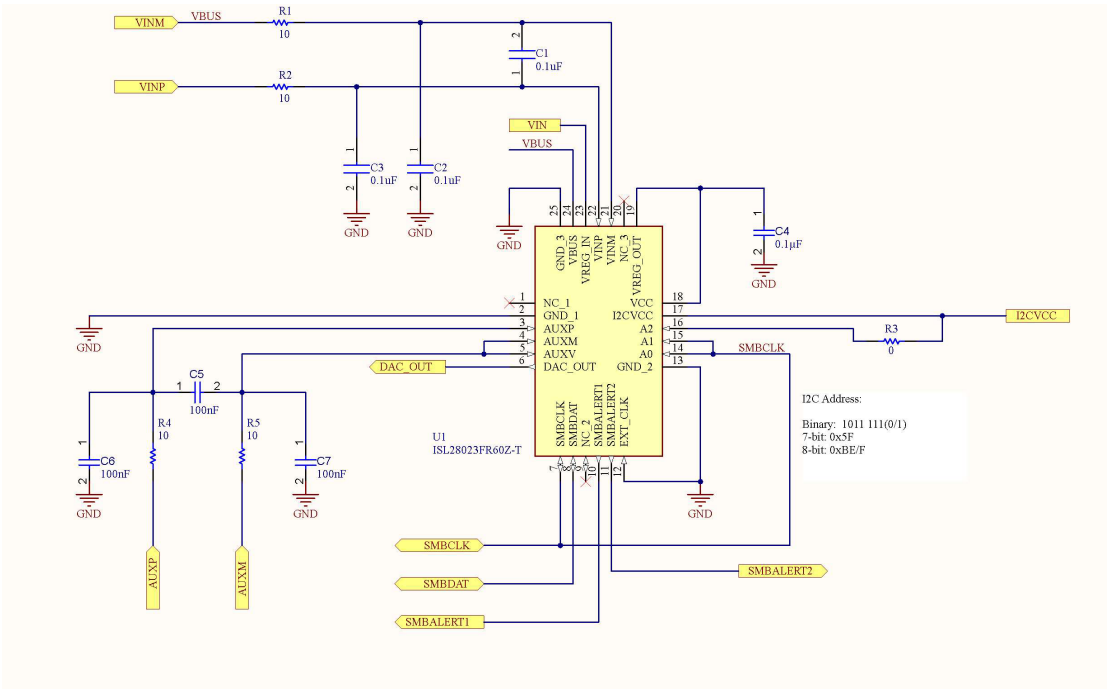


Figure 7. ISL28023 Digital Power Monitor Schematic

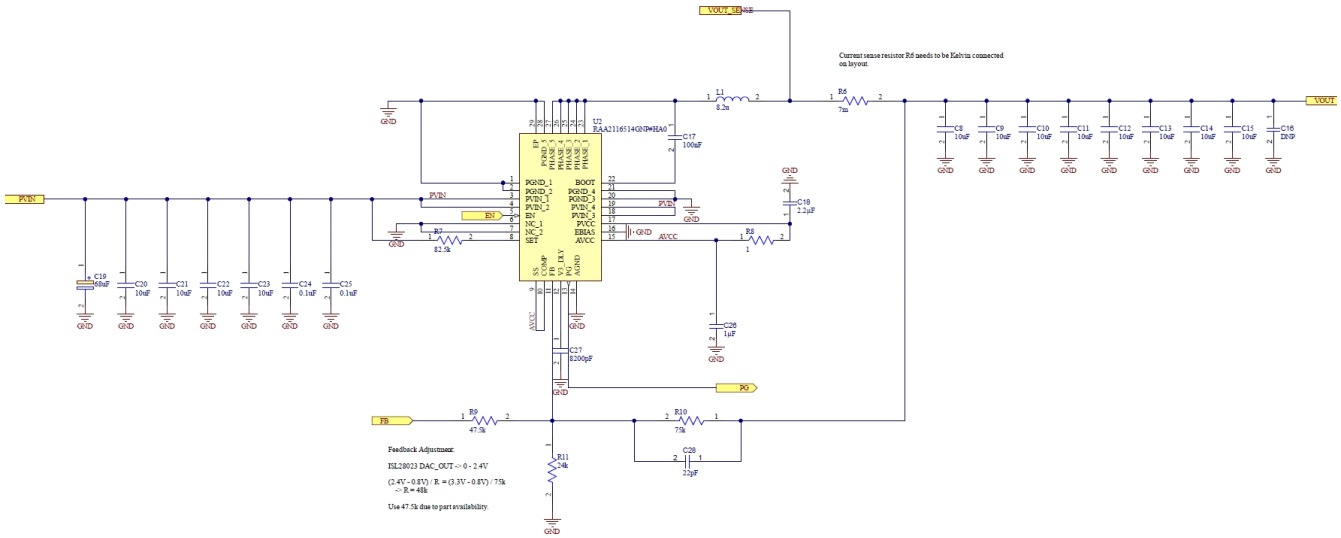


Figure 8. RAA211651 Buck Regulator Schematic

2.2 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
3	C1, C2, C3	CAP CER 0805 0.1UF 63V X7R 10%	KEMET	C0805C104KMREC7800
4	C4, C29, C30, C31	CAP CER 0.1UF 10V X7R 0603	KEMET	C0603C104M8RAC7867
4	C5, C6, C7, C17	CAP CER 0.1UF 16V X7R 0402	Murata Electronics	GRM155R71C104JA88D
12	C8, C9, C10, C11, C12, C13, C14, C15, C20, C21, C22, C23	CAP CER MLCC	Murata Electronics	GRM32EC72A106KE05K
1	C18	CAP CER 2.2UF 10V X5R 0402	Yageo	CC0402MRX5R6BB225
1	C19	CAP ALUM 68UF 20% 80V SMD	Vishay	MAL214699705E3
2	C24, C25	CAP CER 0.1UF 100V X7R 0603	Murata Electronics	GRM188R72A104KA35J
1	C26	CAP CER 1UF 16V X5R 0402	TDK	CGB2A1X5R1C105K033BC
1	C27	CAP CER 8200PF 25V X7R 0402	KEMET	C0402C822J3RACTU
1	C28	CAP CER 22PF 25V NP0 0402	KYOCERA	04023A220KAT2A
1	J1	CONN HEADER R/A 12POS 2.54MM	Samtec	TSW-106-08-F-D-RA
1	J2	CONN RCPT 12POS 0.1 GOLD PCB R/A	Samtec	SSW-106-02-F-D-RA-006
4	J3, J4, J5, J6	CONN HEADER VERT 2POS 1.27MM	Samtec	FTS-102-01-L-S
2	J7, J8	TERM BLK 2P SIDE ENT 5.08MM PCB	Phoenix Contact	1729128
1	L1	IND,7.3X6.6X4.8MM,8.2UH20%,7.5A,	Bourns	SRP7050AA-8R2M
2	LED1, LED2	LED RED CLEAR 0402 SMD	QT Brightek (QTB)	QTB-QBLP595_V
4	R1, R2, R4, R5	RES SMD 10 Ω 1% 1/10W 0402	Panasonic	ERJ-2RKF10R0X
1	R3	RES 0 Ω JUMPER 1/16W 0402	Yageo	RC0402JR-070RL
1	R6	RES 0.007 Ω 1% 1W 1206	TE	TLR2B10DR007FTDG
1	R7	RES 82.5K Ω 1% 1/10W 0402	KOA	RK73H1ETTP8252F
1	R8	RES SMD 1 Ω 1% 1/10W 0603	Vishay	CRCW06031R00FKEA
1	R9	RES 47.5K Ω 1% 1/10W 0603	Yageo	RC0603FR-0747K5L
1	R10	RES SMD 75K Ω 1% 1/10W 0402	Panasonic	ERJ-S02F7502X
1	R11	RES SMD 24K Ω 1% 1/10W 0402	Panasonic	ERJ-2RKF2402X
4	R12, R13, R16, R17	RES SMD 4.7K Ω 1% 1/16W 0402	Bourns	CR0402-FX-4701GLF
2	R14, R15	RES SMD 1.5K Ω 0.1% 1/20W 0201	Panasonic	ERA-1AEB152C
1	R18	RES 0.005 Ω 1% 1W 1206	Bourns	CRK0612-FZ-R005E

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
1	U1	Power Supply Controller Digital Power Monitor 24-QFN (4x4)	Renesas Electronics America Inc	ISL28023FR60Z-T
1	U2	Buck Switching Regulator IC Positive Adjustable 0.8V 1 Output 5A 28-VFQFN Exposed Pad	Renesas Electronics America Inc	RAA2116514GNP#HA0

2.3 Board Layout

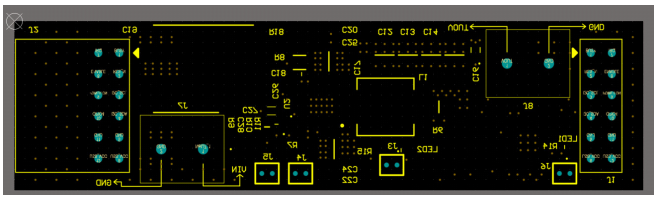


Figure 9. Top Overlay

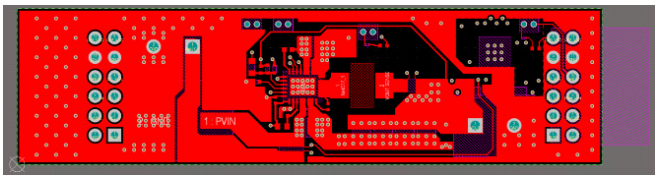


Figure 10. Top Layer

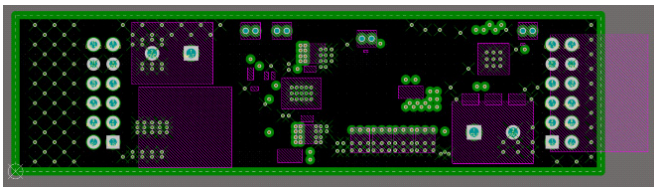


Figure 11. Layer 2 (GND)

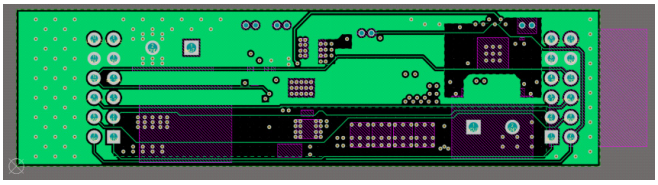


Figure 12. Layer 3 (Signal)

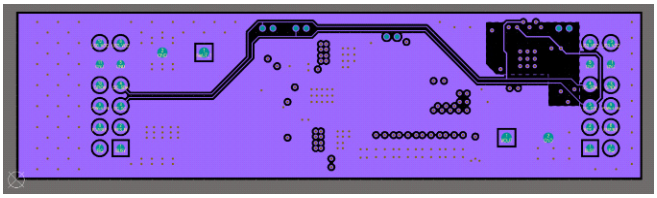


Figure 13. Layer 4 (Signal)

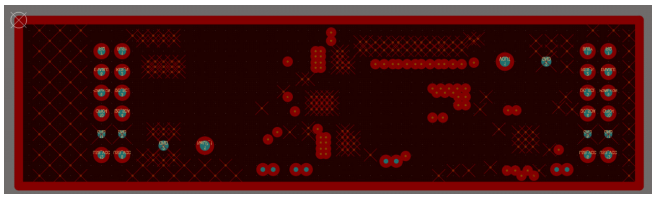


Figure 14. Layer 5 (GND)

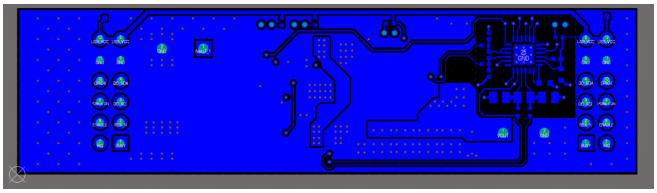


Figure 15. Bottom Layer

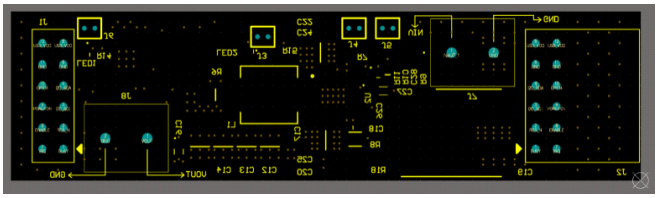


Figure 16. Bottom Overlay

3. Typical Performance Graphs

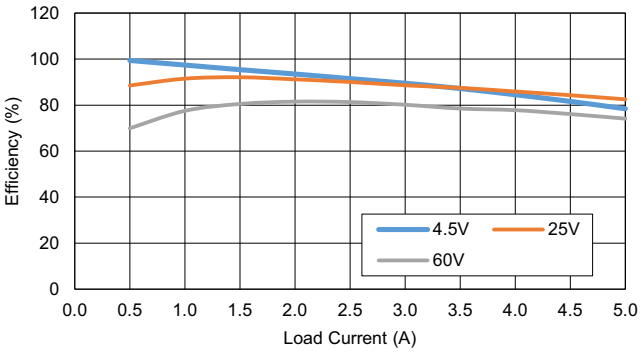


Figure 17. Efficiency

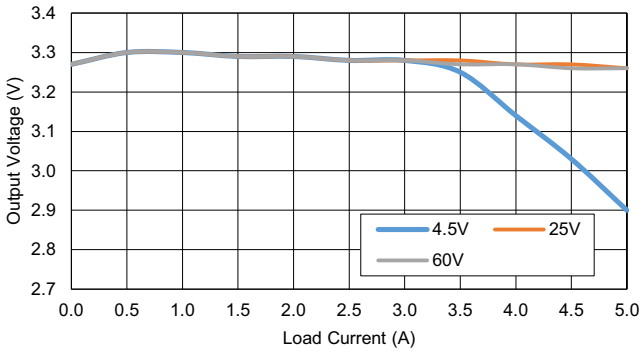


Figure 18. Load Regulation

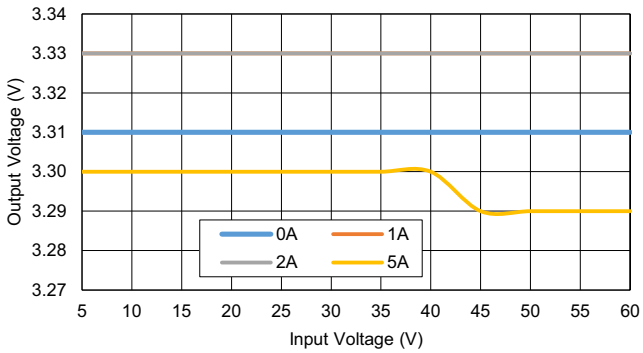


Figure 19. Line Regulation

4. Software Design

The following sections give an overview of the software implementation for the QCIOT-5APWRPOCZ, which is based on the Renesas RA Family's Flexible Software Package (FSP). These sections detail the project's code structure, the system's software modules, and the main system flow. Information such as the software API, pin functions, and fault handling is also provided.

4.1 Project Code Structure

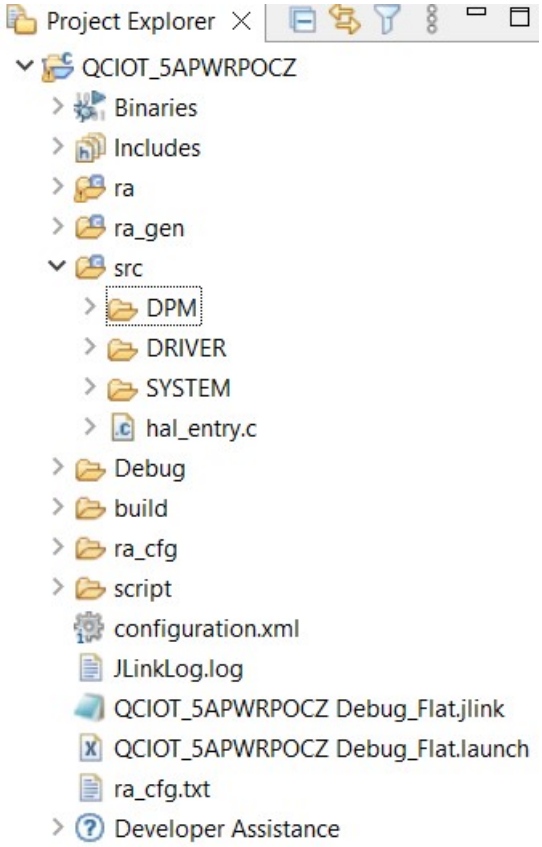
The Quick Connect DPM project is designed to be a highly modular solution, where each device has an associated module folder that can be easily configured independently of other modules (if required) or ported to other end applications.

The project is split into 3 main modules:

- DPM – ISL28023 device driver code for power monitoring
- DRIVER – Include the Communication Layer driver that talks to I2C
- SYSTEM – Main system code that enables the driver code and implements system flow

Each module folder contains the C source files and header files for that module. The DPM module also has an additional profile header file (dpmProfile.h) for specific user configurations. Refer to the User Settings section for details regarding user configurations.

Figure 20 shows the structure of the project in e^2 studio.



ra - includes automatically generated files for FSP drivers

ra_gen - includes main file and generated files for FSP driver settings

src - contains the module code that uses FSP drivers

- DPM - digital power monitor code
  - dpm.c - dpm source code
  - dpm.h - dpm header file
  - dpmProfile - User settings
- DRIVER - I^{2}C communication layer driver code
- SYSTEM - main system code
  - system.c - system code and system flow
  - system.h - system code header file
- hal_entry.c - start of code execution, which calls system main

Figure 20. Quick Connect DPM Code Structure

Figure 21 shows the general code structure in terms of its dependencies. Execution begins in hal_entry.c that calls the main function in system.c beginning the main system flow that in turn uses the DPM module to execute the project. All associated header files reference the lower-level Flexible Software Package (FSP) drivers.

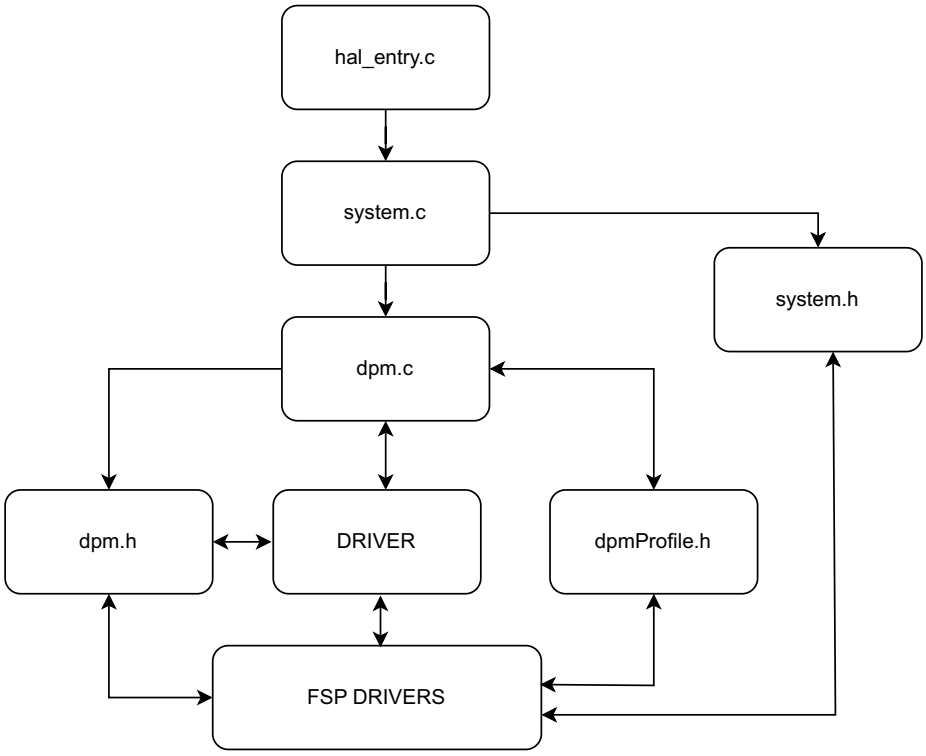


Figure 21. Code Dependency Graph

4.2 Software Module Overview

The system module contains the main system algorithm that is described in the main system flow; this module is responsible for initializing and setting up the driver that is used in the main algorithm. Also, this module makes calls to the other modules to initialize and setup. After initialization, this module is responsible for monitoring the system, displaying faults (if any), and shutting down the system in the event of faults. This module also keeps a continuous check of the I^2C connection. The algorithm is responsible for initializing and setting up DPM module and adjusting the DAC to the required output.

4.2.1 DPM - ISL28023 (Digital Power Monitor)

The DPM module is a device driver that can monitor the current and voltage in the system for added protection. This module is responsible for initializing the FSP I^2C driver and setting up the DPM device with the user-configured settings.

After setup, the module provides the following features:

- Performing various device commands (clear faults, reset, and others)
- Reading the 60V system voltage
- Reading the system for the current and primary and auxiliary side voltage
- Reading device faults (overvoltage, undervoltage, overcurrent, and others)
- Reading from and writing to all device registers
- Adjusting the DAC according to the voltage set by the user

4.2.2 Algorithm Flowchart

Figure 22 describes the algorithm at a high level.

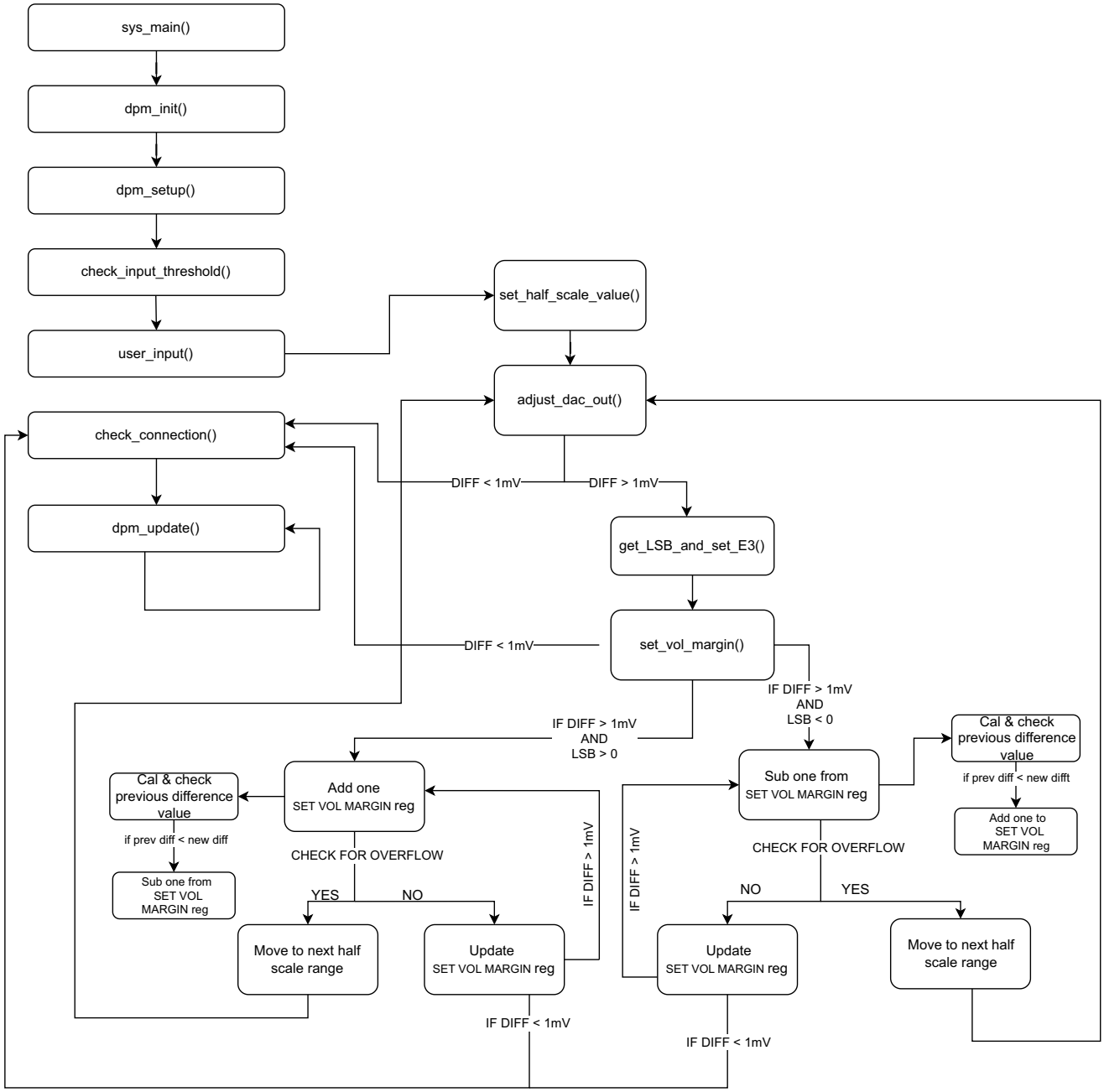


Figure 22. Code Dependency Graph

The functions outlined in Figure 22 are described as follows:

- sys_main()
  - Calls dpm_init() function
  - Calls dpm_setup() function
  - Calls check_input_threshold() function()
  - Calls user_input() function
  - Calls check_connection() function
  - Calls dpm_update() function
  - Calls check_output_threshold() function

- dpm_init()
  - Opens the IIC master module which initializes the IIC pins as SDA and SCL
  - Set the slave address

- dpm_setup()
  - Do a soft reset.
  - Configure the DPM registers

- check_input_threshold()
  - Clear the DPM faults
  - Check for system fault on the input side

- user_input()
  - Calls set_reg_vol_to() function

- Check_connection()
  - Continuously check for IIC connection

- dpm_update()
  - Update the DPM
  - Take updated DPM readings

- Check_output_threshold()
  - Check for system fault on the input side

- set_reg_vol_to()
  - Calls dpm_set_dac_out() function

- dpm_set_dac_out()
  - Calls the dpm_set_half_scale_value() function
    - Calls the dpm_cal_Vdac() function to calculate Vdac
    - Depending on the Vdac value the half scale range is set
    - Voltage margin is set and configure accordingly
  - Calls the adjust_dac_out() function.
    - Calculates the diff = VOL_REG_USER - g_dpm.vout_aux
    - If diff is greater than 1mV, get_LSB_and_set_SET_VOL_MARGIN_E3_reg () function is called

- get _LSB_and_SET_VOL_MARGIN_E3_reg ()
  - Calculates the Delta value
  - Calculates the no of LSB required
  - Reconfigure voltage margin registers
  - If diff > 0 and no of LSB > 0, add 1 to the SET_VOL_MARGIN register else subtract 1 from SET_VOL_MARGIN register

- add_one_to_SET_VOL_MARGIN_E3_reg ()
  - Check for overflow
  - If no overflow, add one to the SET_VOL_MARGIN register
  - Reconfigure voltage margin registers
  - If overflow detected, move to next half scale range

- set_vol_margin()
  - Clear the load bit
  - Set the voltage margin register with the updated value
  - Set the load bit

- sub_one_from_SET_VOL_MARGIN_E3_reg
  - Check for overflow.
  - If no overflow, subtract one from SET_VOL_MARGIN register.
  - Reconfigure voltage margin registers.
  - If overflow detected, move to next half scale range.

4.2.3 Hierarchy Chart

Figure 23 outlines the hierarchy of function calls.

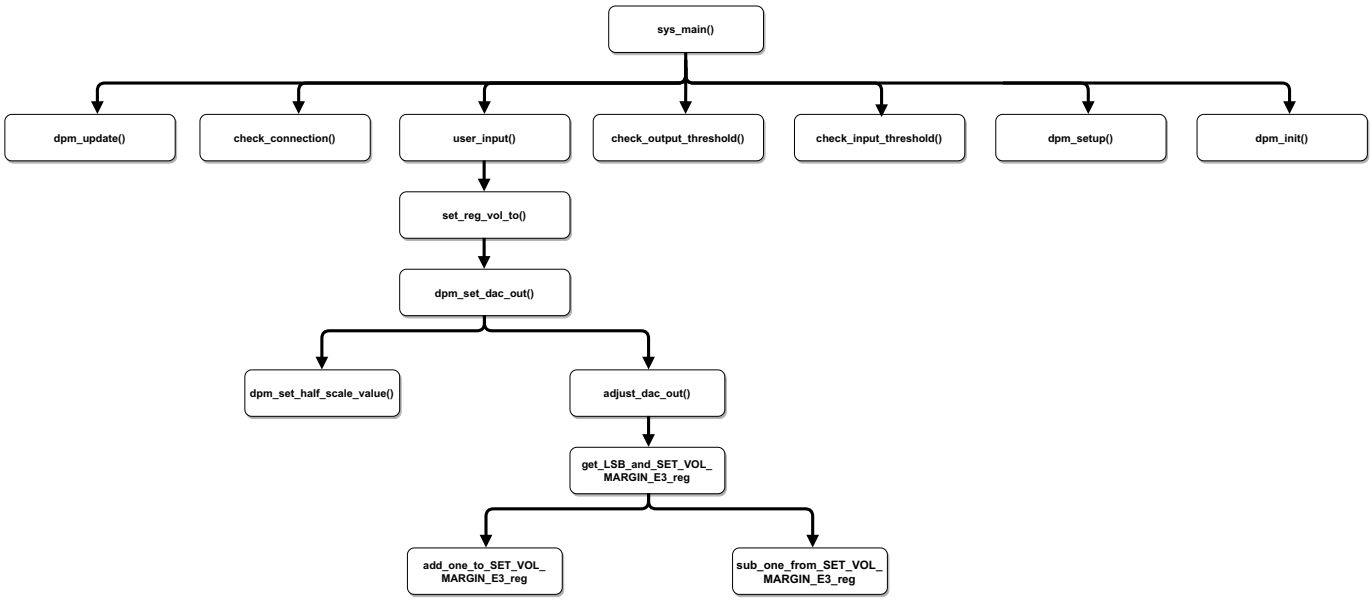


Figure 23. Function Call Hierarchy

After DPM is initialized and configured, the main system loops continuously to get the DPM readings using the dpm_init() and dpm_setup() function calls. After DPM is configured, the main system checks for input threshold and takes user input to set the DAC voltage; this process is achieved using check_input_threshold() and user_input() function calls, respectively. If any faults occur at the input side, the faults are displayed on the Renesas Debug Virtual Console; if the faults are on the output side, the system shuts down.

4.3 User Settings

4.3.1 Configure DPM

This section outlines all the configurable user settings in the demo project. Configurable settings are mainly included in the Profile header files for the DPM. These configurations are defined macros with the _USER suffix. The list of user configurable settings for the DPM device is not exhaustive; the most used settings are included in the Profile headers, but all register settings in the DPM setup functions can also be adjusted directly. Refer to the datasheet for guidance on register settings and values. *Note:* The user will require an E2 emulator to make changes to the project.

dpm_USER.c | dpmProfile.h | dpm.c

```
/* DISCLAIMER
 * File Name    : dpmProfile.h
 * History : DD.MM.YYYY Version  Description

 Includes   <System Includes> , "Project Includes"

 Macro definitions
#ifndef DPM_DPMPROFILE_H_
#define DPM_DPMPROFILE_H_

#define RSHUNT_USER                (0.005)     // resistance of the shunt resistor
#define DPM_MODE_USER              (0x000F)    // set to measure All, default is 0x0A
#define IOUT_CAL_USER              (0x0831)    // gain calculation is based on 80mV max diff voltage and 1mOhm shunt resistor
#define OC_THRESHOLD_USER          (2.125)     // IOUT_DIR = 1 (Setup for discharge). Vshunt range = 80mV. Vshunt OC = 21.25A
#define IOUT_DIR_USER              (0)         // 1 = VINM to VINP (negative to positive)
#define VSHUNT_RNG_USER            (0)
#define OV_THRESHOLD_USER          (12.5)      // OV selected. Threshold range = 12V. OV threshold = ~12.5V. // 0x00B3 for 12.5V
#define UV_THRESHOLD_USER          (11.4)      // UV Threshold range = 12V. UV threshold = ~11.4V
#define OC_BLANKING_USER           (50)        // 50 milliseconds

#define OV_THRESHOLD_USER_OUTPUT   (3)
#define UV_THRESHOLD_USER_OUTPUT   (0.1)
#define OC_THRESHOLD_USER_OUTPUT   (10)

#define AUX_RSHUNT_USER            (0.007)     // 7m Ohm register

#endif /* DPM_DPMPROFILE_H_ */
```

Figure 24. Profile Header Files

The user settings and their usage are outlined in the Table 1. The user can adjust these values to fit the end application. *Note:* Some register settings adhere to multiple settings, and those settings are not fully listed. Refer to the datasheet for more information.

Table 1. Register Settings

Name	Usage	Default Value
RSHUNT_USER	Primary shunt resistance value in ohms	0.005
DPM_MODE_USER	Selects options for which elements to scan (voltage, current, temperature)	0x000F(All)
IOUT_CAL_USER	Current gain calibration value	0x0831
OC_THRESHOLD_USER	The OC threshold value in amperes	21.25
IOUT_DIR_USER	Direction of current flow (1 is negative to positive)	0
VSHUNT_RNG_USER	Primary shunt full-scale range (0 is 80mV)	0
OV_THRESHOLD_USER	OV threshold for the 12V supply to the system	*user value*
UV_THRESHOLD_USER	UV threshold for the 12V supply to the system	*user value*
OC_BLANKING_USER	Blanking time to catch inrush current OC in milliseconds	50
OV_THRESHOLD_USER_OUTPUT	OV threshold on the output side	*user value*
UV_THRESHOLD_USER_OUTPUT	UV threshold on the output side	*user value*
OC_THRESHOLD_USER_OUTPUT	OC threshold on the output side	*user value*
AUX_REG_USER	Auxiliary shunt resistance value in ohms	0.007

4.3.2 Set Output DAC Voltage

User can use the set_reg_vol_to(USER_VOLTAGE) API to set the output voltage.

For example, if the user wants to set the voltage to 2.8V. The API for this is set_reg_vol_to(2.8f).

Figure 25 shows this user setting.

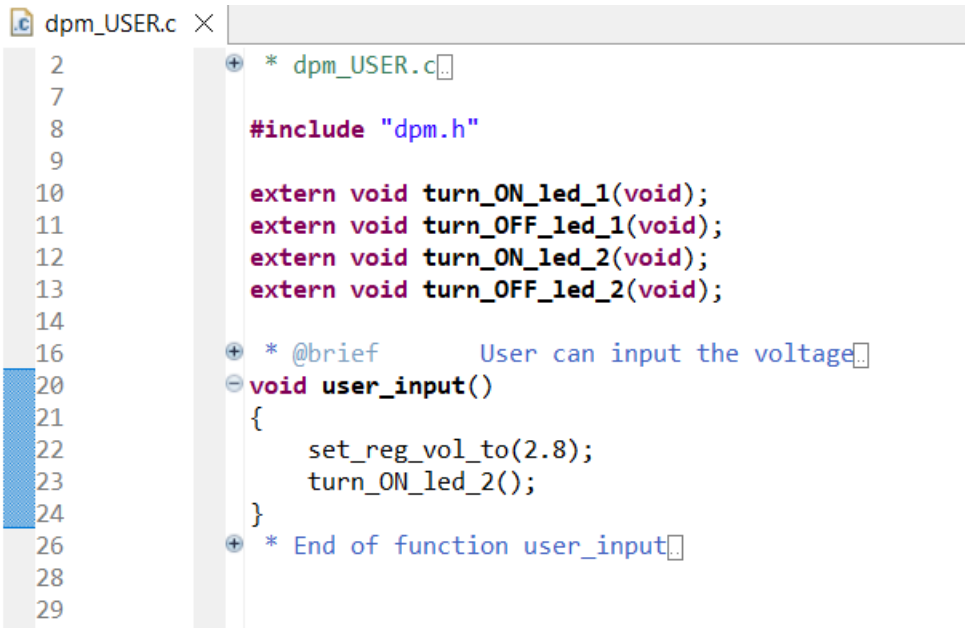


Figure 25. User Settings

5. Ordering Information

Part Number	Description
QCIOT-5APWRPOCZ	QCIOT-5APWRPOCZ Evaluation Board

6. Revision History

Revision	Date	Description
1.06	May 29, 2024	Updated Figure 3.
1.05	Apr 5, 2024	▪ Updated equation 2 in section 1.1.1. ▪ Changed SMBALERT1 signals to “pin 7” from “pin 1” in section 1.1.2.1.
1.04	Mar 29, 2024	▪ Updated software version text in section 1.2.1 Software Installation and Usage. ▪ Updated item 3 in section 1.2.2 Kit Hardware Connections. ▪ Updated section 4.1 Project Code Structure with DRIVER module information. ▪ Updated Figure 20, Figure 21, and Figure 25.
1.03	Feb 12, 2024	▪ Removed references to QCIOT-006 from title and on page 1. ▪ Changed orderable part number to QCIOT-5APWRPOCZ from QCIOT-006.
1.02	Jan 4, 2024	▪ Updated Figure 1, Figure 4 and Figure 5. ▪ Replaced “QCIOT-006 Power Board” with “QCIOT-5APWRPOCZ” throughout the document.
1.01	Jun 21, 2023	Product changed from QCIOT-5APWRPOCZ to QCIOT-5APWRPOCZ.
1.00	Dec 20, 2022	Initial release

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