# RA9530-R

Evaluation Kit

The RA9530-R-EVK Wireless Power Evaluation Board can demonstrate the features and performance of the RA9530 Wireless Power Receiver with WattShare™ mode. The board comes with pre-programmed reference firmware in which GPIOs are configured for specific functions that meet broader customer requirements.

The RA9530 features Multiple-Time Programmable (MTP) non-volatile memory that enables customers to customize the design parameters such as default output voltage and FOD thresholds. The RA9530 includes over-temperature and voltage protection. Fault conditions associated with power transfer are managed by an industry-leading 32-bit ARM® Cortex®-M0 processor offering a high level of programmability while consuming low standby power. The RA9530 Windows Graphical User Interface (GUI) can be used to configure the design parameters, monitor operating parameters such as Rectifier voltage, and program the new configuration into the RA9530.

The RA9530-R-EVK is designed for evaluation purposes only. It must not be used for module or mass production purposes.

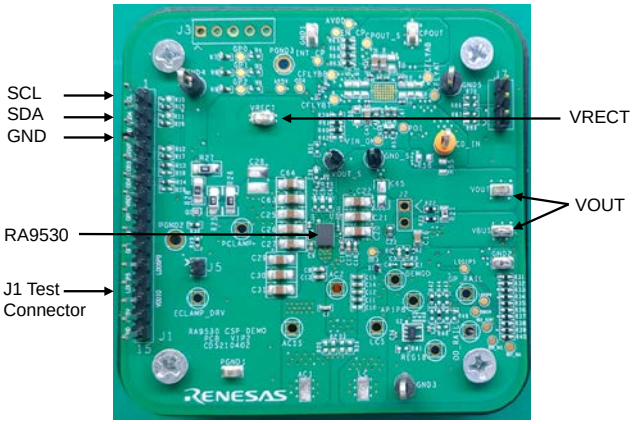
## Evaluation Kit Contents

- RA9530-R Demo Board assembled with coil

## Features

- Delivers up to 30W of power in Renesas high power mode when paired with P9247-GB-EVK
- ±1.5% accurate output current sensing for robust FOD detection
- WattShare™ TRx mode with up to 10W Tx capability
- Supports latest WPC 1.3 specification
- Supports bi-directional data communications
- 90% peak efficiency (system end-to-end)
- Switch mode PCLAMP/ECLAMP for robust overvoltage clamping
- Embedded 32-bit ARM™ Cortex®-M0 processor
- 32kB EEPROM memory to support OTA updates
- Easy to use GUI for customizing the design parameters
- 1.2V and multiple other IO voltage rail support to interface with processors of advanced technology nodes
- RA9530 Device Package: 6 × 8 ball array, 2.53 × 3.31 × 0.60 mm, 48-DSBGA with 0.40mm ball pitch

## Evaluation Board



# Contents

# Figures

# Tables

# 1. Board Setup

## 1.1 Required or Recommended User Equipment

The following additional equipment is required for using the kit:

- P9247-GB-EVK (REA High power mode enabled Tx) or P9243-GB-EVK (EPP transmitter with fast charge modes) or any WPC-certified transmitter for Rx mode test
- DC power source or adapter that power transmitter
- P9222-R EVK or any WPC-certified receiver for Wattshare (TRx) mode test
- Electronic load that can be connected to the RA9530-R-EVK
- WPD-USB-DONGLE for connecting with RA9530-R Windows GUI on computer and doing I2C transactions. WPD-USB- DONGLE is not shipped along with evaluation board and needs to be ordered separately

## 1.2 Required Software on Computer

Visit the RA9530-R-EVK web page and download latest version of the RA9530 Windows GUI and USB drivers. The Window GUI software provides an intuitive GUI for reading and writing to RA9530 registers, and programming custom user configurations to internal MTP memory.

### 1.2.1. Software Installation

Complete the following procedures to install the software:

1. Do not connect the WPD-USB-DONGLE dongle before installing the software.
2. Run the RA9530-R Windows GUI exe file. If you encounter a USB driver issue, please complete the following steps.
   a. Run the downloaded *USB Drivers Setup* executable file and follow the user prompts to install the USB drivers.
   b. After finishing the setup of the USB drivers, connect one of the WPD-USB-DONGLE dongles to the USB port. Wait for a few moments to let Windows® map the drivers for the dongle.
   c. Open the Device Manager from the Windows control panel and check the devices listed under “Universal Serial Bus controllers” section. “FT4222H Interface A” and “FT4222H Interface B” should appear in this section as shown in the following figure.

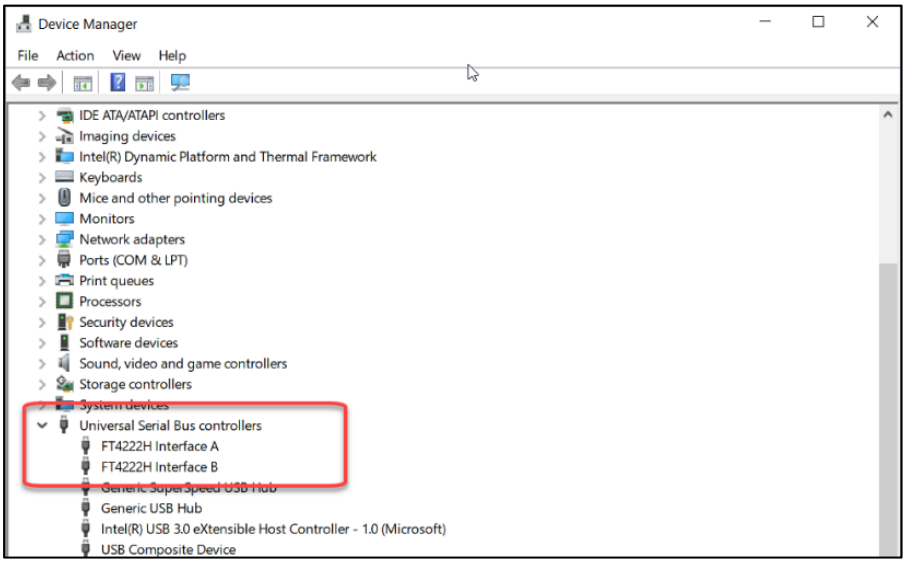



**Figure 1. Windows Device Manager Display for the USB Connection**

## 1.3 Usage Guide

The RA9530-R-EVK board can demonstrate the performance and functionality of the RA9530 wireless power receiver with TRX mode in a lab bench test environment.

## 1.4 Kit Hardware Connections for Rx Mode

Complete the following procedures to set up the kit as shown in Figure 2:

1. Set up the P9247-GB-EVK (REA high-power mode enabled Tx) or P9243-GB-EVK (EPP transmitter with fast charge modes) or other WPC certified transmitter according to the board's user manual and apply power.
2. Place the RA9530-R-EVK board on the transmitter coil surface with the coil back facing upwards.
3. Verify that the red LED on the P9247-GB EVK board is illuminated, which indicates that power transfer has been established.

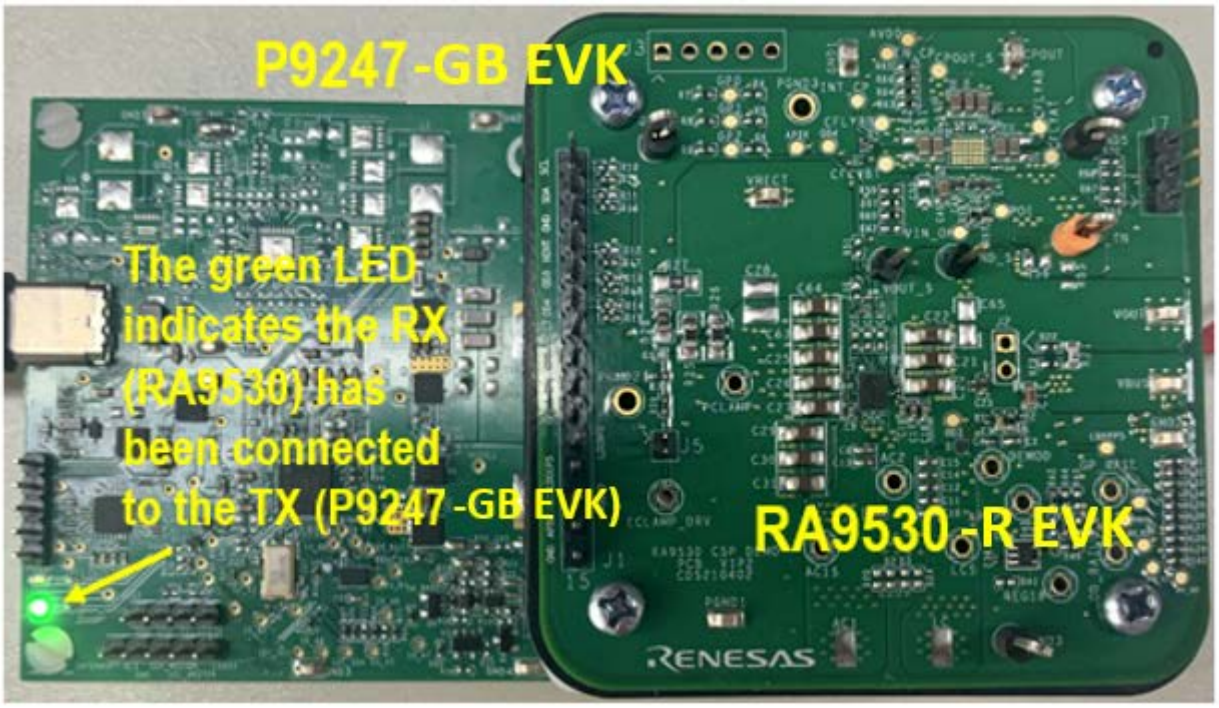



**Figure 2. Evaluation Kit Connections for Rx Mode Test**

### 1.4.1. Start Guide for Rx Operation

Place the bottom side of RA9530-R EVK onto an P9247-GB-EVK (REA High power mode enabled Tx) or P9243-GB-EVK (EPP transmitter with fast charge modes) or other WPC certified Tx unit. The RA9530-R-EVK includes a 55 × 55 × 0.4 mm TRx coil assembly. The charging pad can be a pre-powered and can be powered after placing the Rx coil on Tx charging pad.

Measure Rx output voltage at the VOUT test point to ground (GND). For convenience and measurement accuracy, two test points have been placed which allow for kelvin voltage sensing of the output voltage to omit conduction losses during evaluation (VOUT and GND). These should be used when performing efficiency measurements. The I2C dongle connector J3 can be used to interface with WPD-USB-DONGLE for programming the user configurable design parameters and it can be used to monitor the system status, mode, operating frequency, voltage, and current.

### 1.4.2. Rx Start Up

These procedures demonstrate Rx start-up operation:

1. Set up the Tx as described in section 1.4 and provide 18V DC to P9243-GB Vin.
2. Place Rx on Tx interface surface.
3. Trigger oscilloscope sweep on VRECT, VOUT and AC1 test point when Rx starts up.

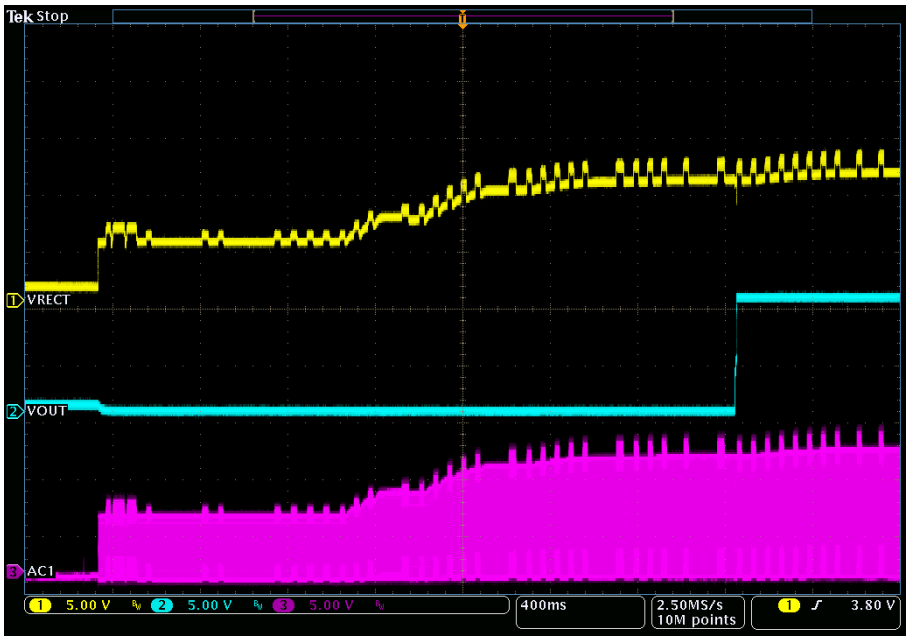



**Figure 3. Rx Start Up**

### 1.4.3. Modulation Waveform

RA9530-R modulates Rx AC signal with communication capacitor to send ASK packet to Tx.

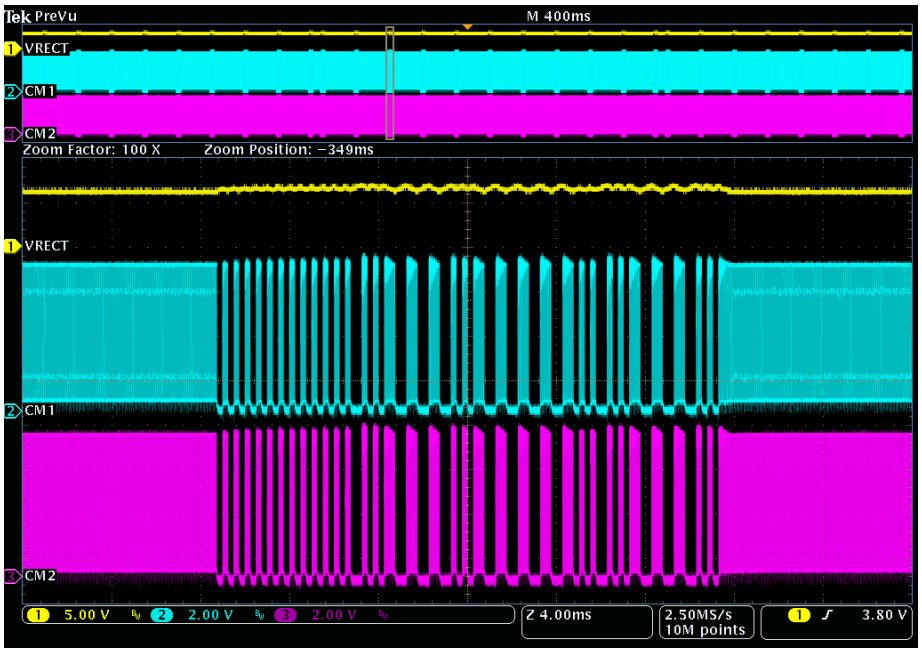



**Figure 4. ASK Modulation Signal on CM1 and CM2**

### 1.4.4. Load Step

The procedure for load step is as follows

1. Set up the Tx as described in section 1.4.
2. Provide a Rx Vout load from no load (high impedance) to 7ohm
3. Monitor load current, VRECT and VOUT voltage as shown in the following figure.

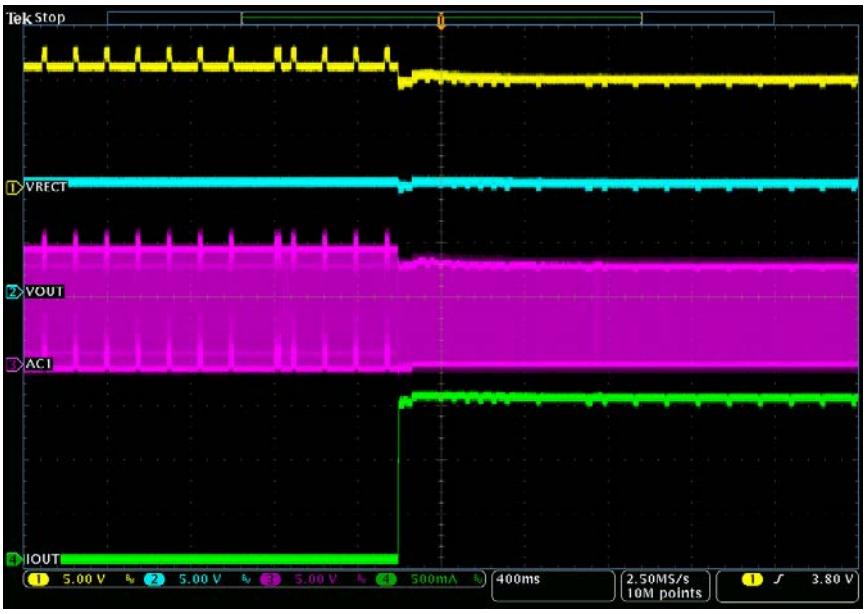



**Figure 5. Load Step**

### 1.4.5. Load Dump

The procedure for load dump is as follows

1. Set up the Tx as described in section 1.4.
2. Provide a Rx Vout load from 7ohm to no load (high impedance).
3. Monitor load current, VRECT and VOUT voltage as shown in the following figure.

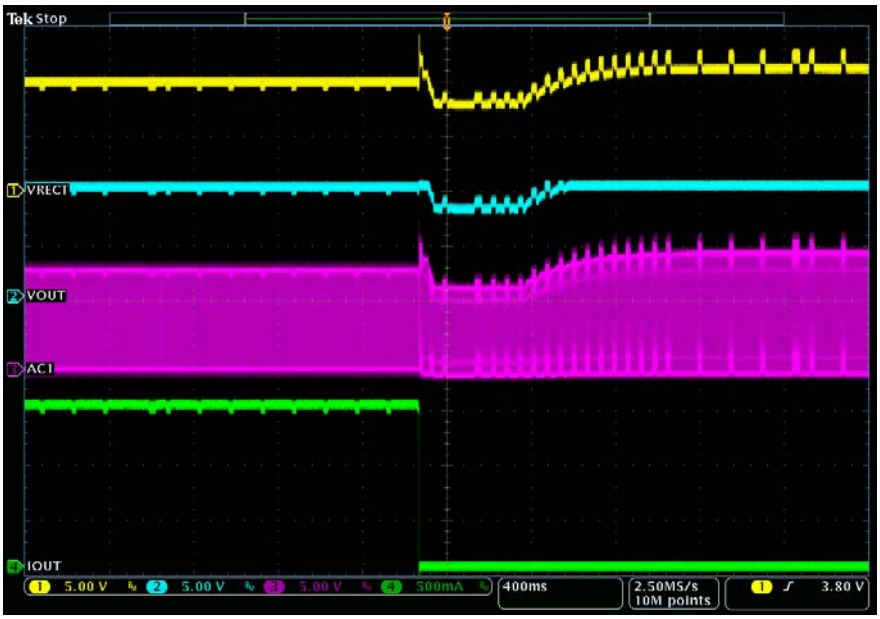



**Figure 6. Load Dump**

## 1.4.6. Rx System Efficiency

Figure 7 and Figure 8 show the Rx system efficiency using Tx P9235A-RB (BPP) and P9243-GB (EPP, HPP). Rx power is measured across RA9530-R VOUT and GND. Tx power is measured across Tx VIN and GND.

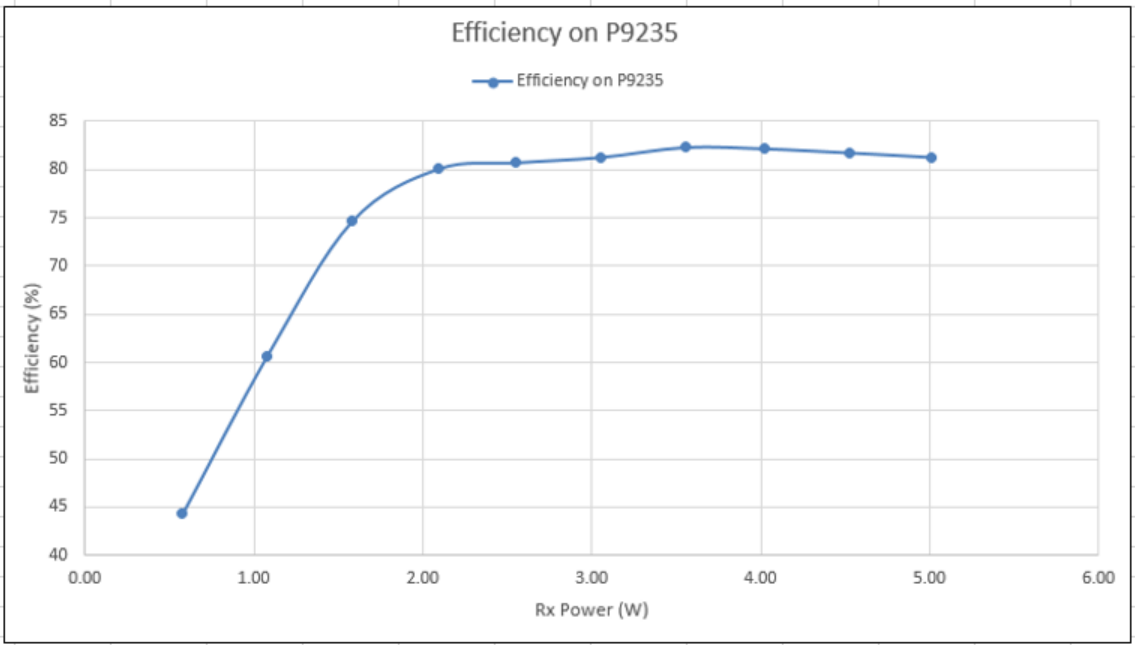



**Figure 7. Efficiency on P9235A-RB Tx (BPP, Vout = 5V)**

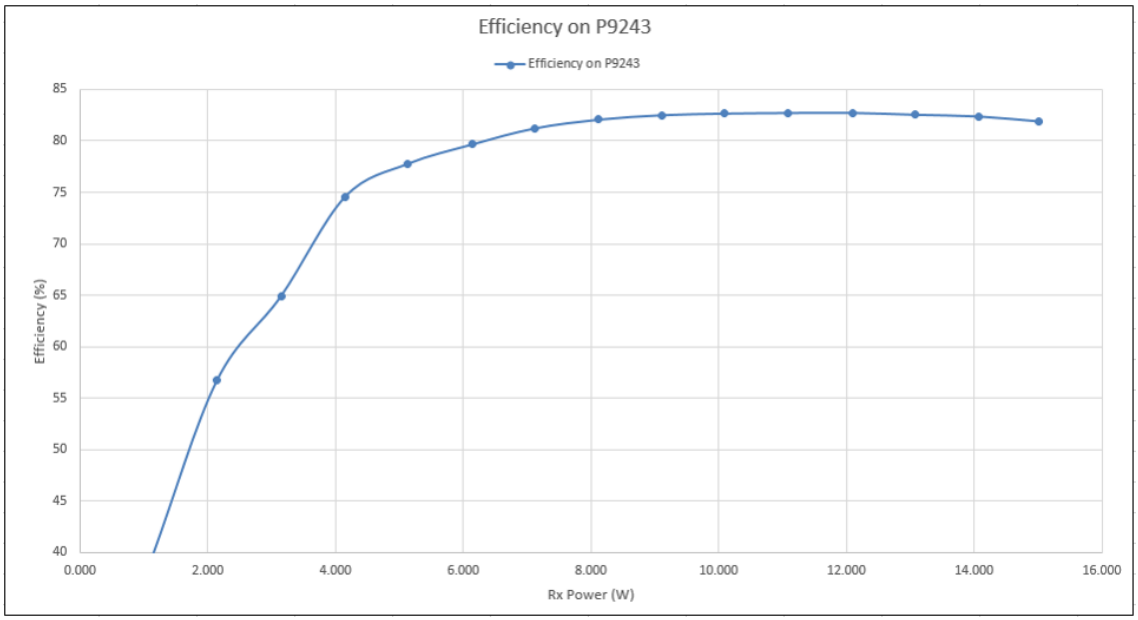



**Figure 8. Efficiency on P9243-GB Tx (EPP, Vout = 10V)**

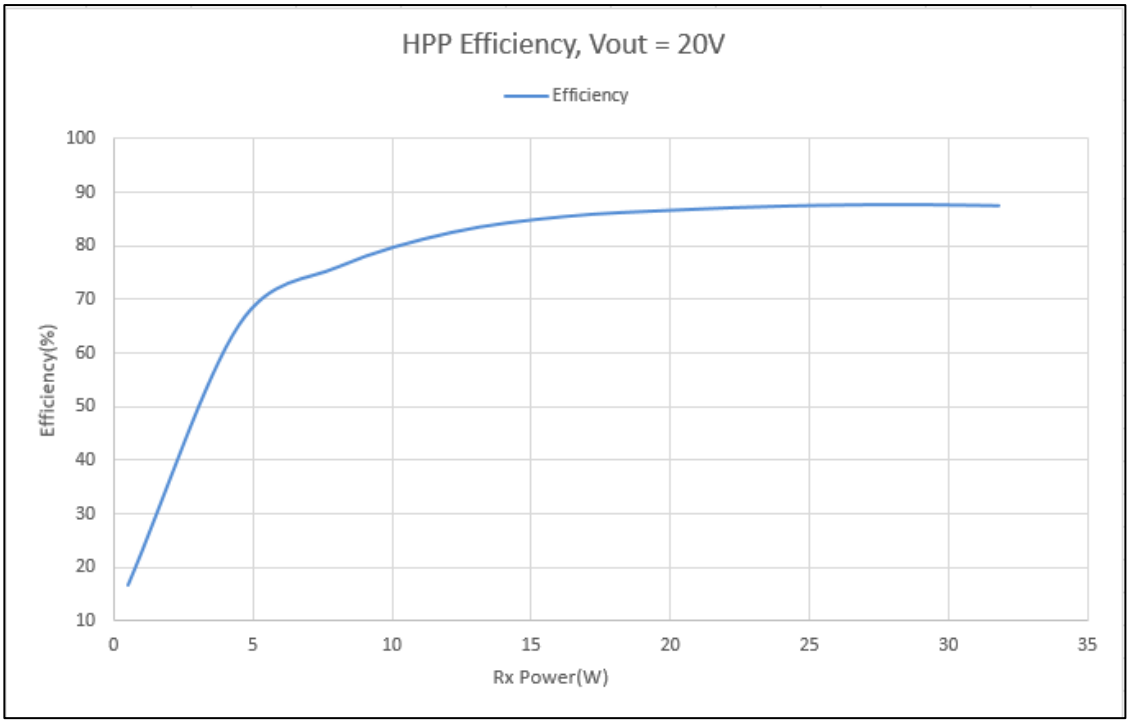



**Figure 9. Efficiency on P9243-GB Tx (High Power, Vout = 20V)**

### 1.4.7. Rx Rectifier Voltage Level

Rx Vrect target voltage level is changed by Rx Iout current for system stability and optimal efficiency performance. The test procedure is as follows:

1. Set up the Tx as described in section 1.4.
2. Provide 18V DC to P9242-GB Vin (EPP Tx) and 5V DC to P9235A-RG Vin (BPP Tx).
3. Change Rx Iout load current from low to maximum gradually and monitor Rx Vrect voltage level.

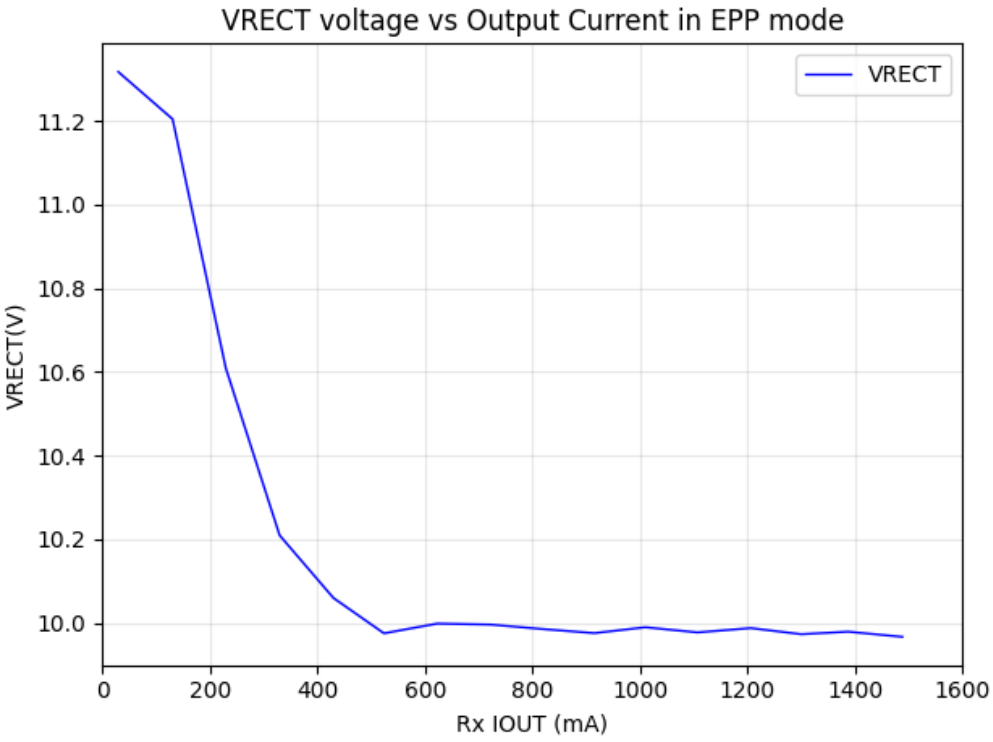



**Figure 10. Rx VRECT Target Voltage on P9243-GB Tx (EPP Mode)**

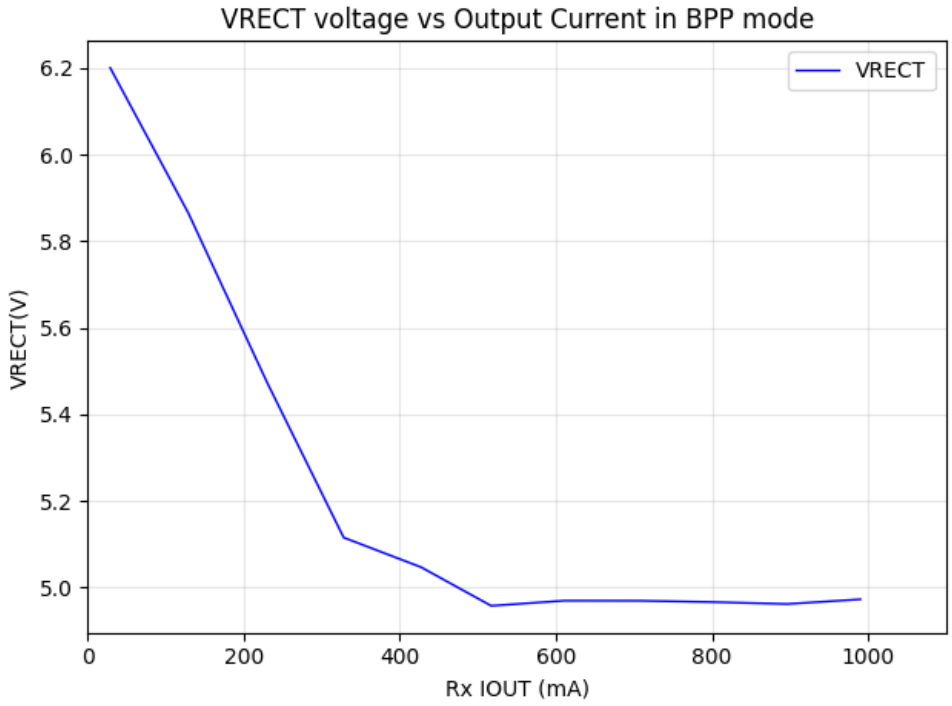



**Figure 11. Rx Vrect Target Voltage on P9235A-RB Tx (BPP Mode)**

### 1.4.8. Power Good operation – GP0

GP0 functions as power good indication. Figure 10 and Figure 11 show EPP and BPP mode power good waveform.

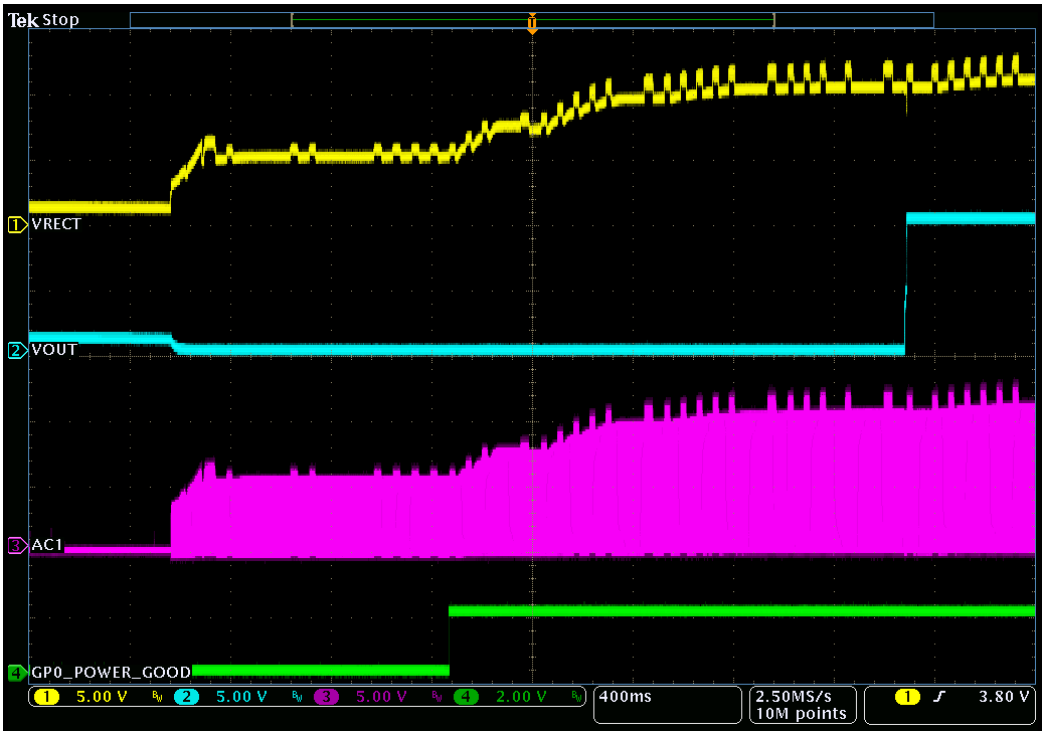



**Figure 12. GP0 Output High when EPP Negotiation is Complete by Default (EPP Mode)**

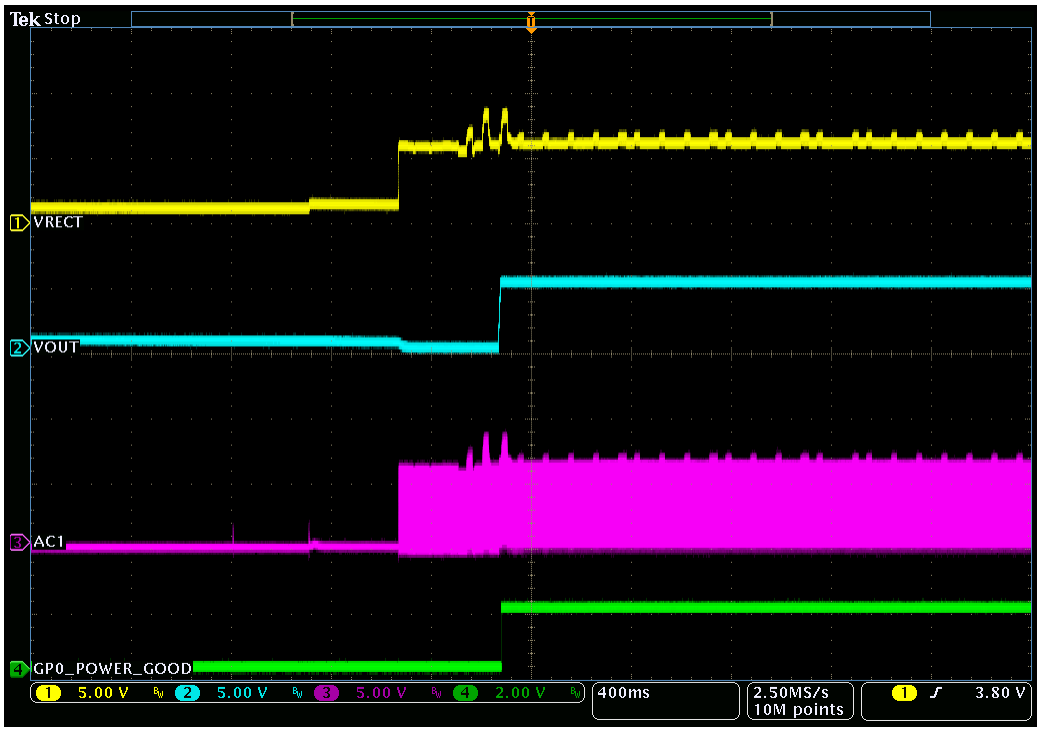



**Figure 13. GP0 Output High when VOUT Turns on (BPP Mode)**

### 1.4.9. INHIBIT – OD4

OD4 functions as INHIBIT(Sleep) operation. If OD4 is high, Rx does not send ASK packet at start up and sends End Power Transfer packet at power transfer phase.

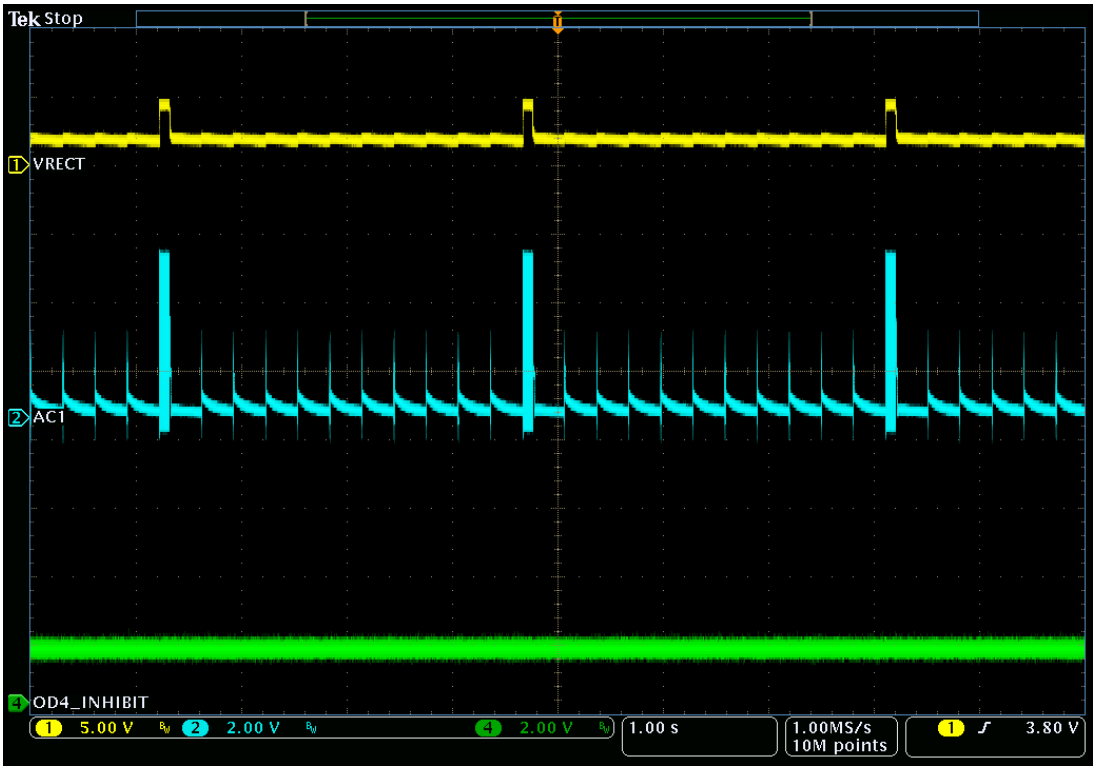



**Figure 14. No ASK Packet when INHIBIT High at Start Up**

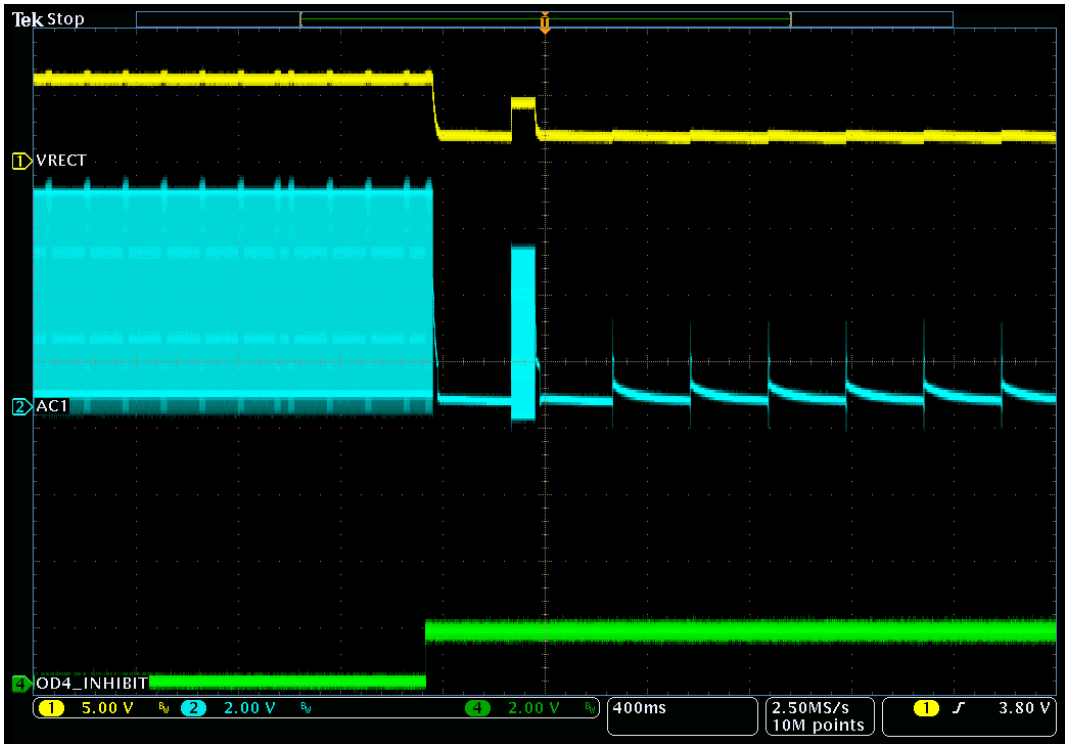



**Figure 15. Send EPT Packet when INHIBIT High at Power Transfer Phase**

## 1.5 Kit Hardware Connections for Wattshare (TRx) Mode

To set up the kit as shown in Figure 16, complete the following procedure:

1. Supply power on RA9530-R-EVK VOUT with DC power supply (7.5V).
2. Connect a WPD-USB-DONGLE on the RA9530-R-EVK J3 connector. USB dongle black line (GND) should be on J3 Pin3.
3. Send TRx mode command with RA9530-R Windows GUI (write 0x01 on 0x007C register).
4. Place the P9222-R-EVK Board or WPC-certified receiver on the reverse side of the RA9530-R-EVK. RA9530-R-EVK PCB boards acts as a spacer between Tx surface and Rx coil.
5. Verify that the green LEDs on P9222-R is illuminated, which indicates that power transfer has been established.

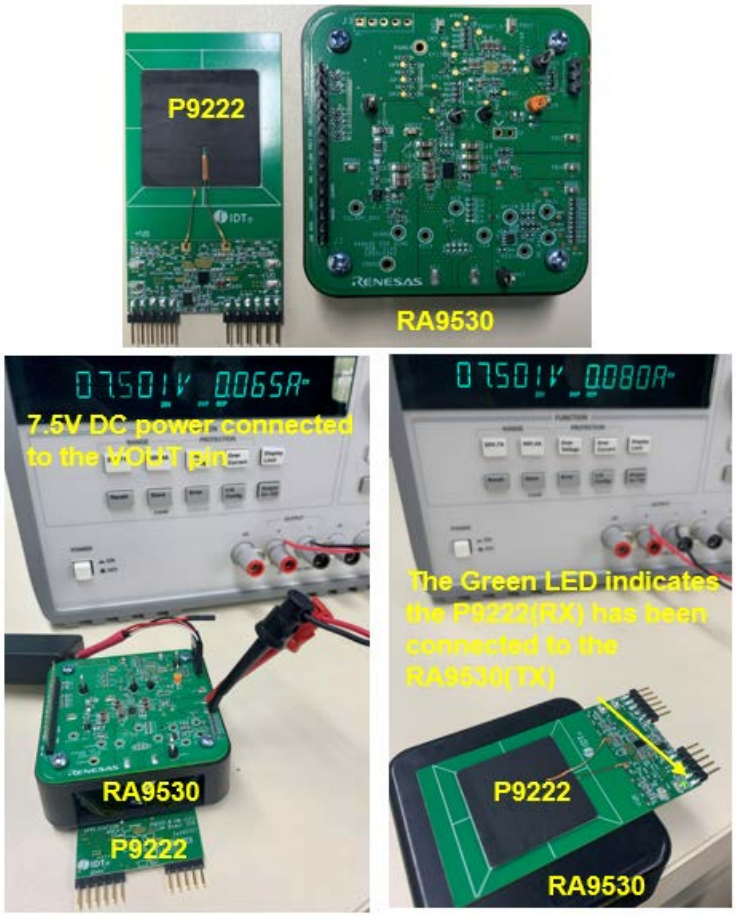



**Figure 16. Evaluation Kit Connections for TRx Mode Test**

### 1.5.1. Start Guide for Wattshare TRx Mode Operation

The RA9530 can be configured as a wireless power transmitter. The device uses an on-chip full/half-bridge inverter, a PWM generator, a modulator/demodulator for communication, and a microcontroller to produce an AC power signal to drive external L-C tank to operate as a wireless power transmitter (TRx). The RA9530 uses the same L-C tank in both Rx mode and TRx mode. In TRx mode, the power needs to be applied on the VOUT pin first which is the same node as the power receiver output when the device operates in Rx Mode. To avoid Tx conflict, ensure that the RA9530-R-EVK is not on the Tx pad.

1. Supply power (5V to 9V) on RA9530-R-EVK VOUT.
2. Write 0x0001 data to 0x007C register to enable TRx mode with RA9530-R Windows GUI or another I2C tool.
3. RA9530 starts sending digital pings after enabling TRx mode. Probe AC1 and check digital ping waveform.

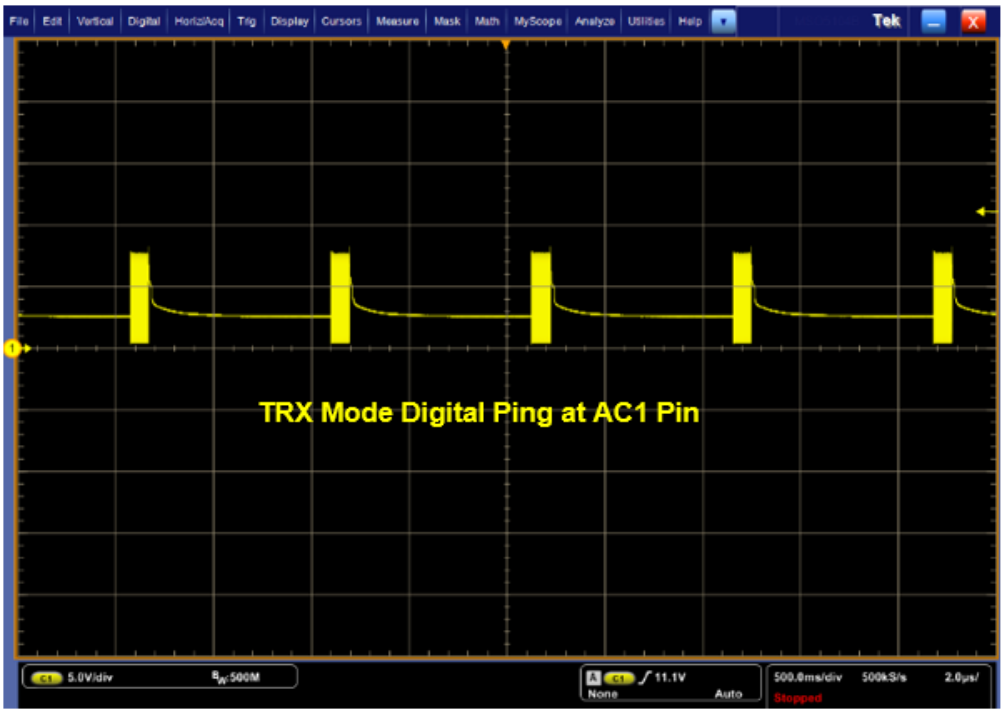



**Figure 17. TRx Mode Digital Ping Waveform**

4. Place the WPC compliant receiver on the RA9530-R-EVK TRx coil. The RA9530 will detect the Rx device and start power transfer right after WPC ID and Configuration packet.
5. Probe Rx VRECT and Rx VOUT, and confirm that charging is functional.

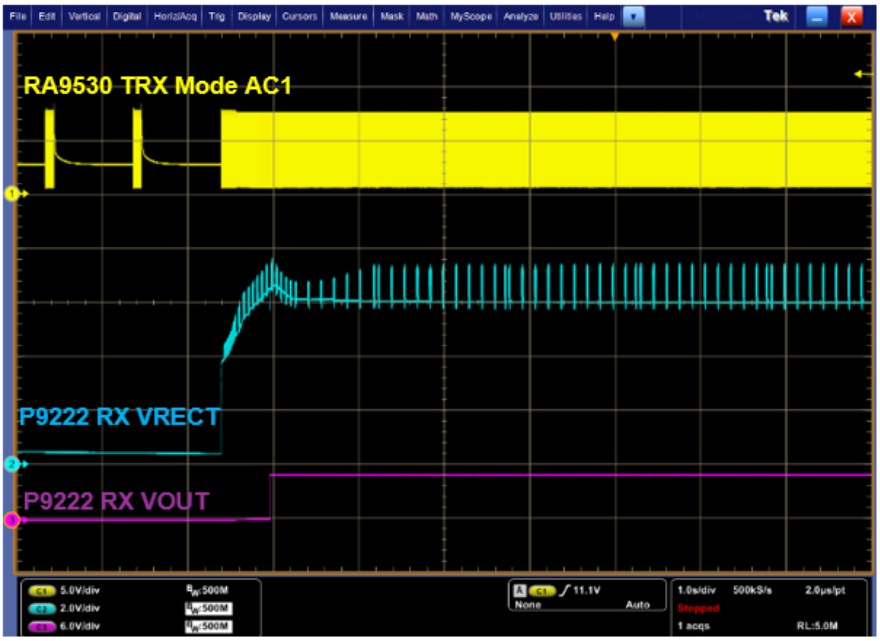



**Figure 18. TRx Mode Charging Waveform**

6. TRx default digital ping frequency is 171kHz and the normal operating frequency range is from 115kHz to 145kHz in the default configuration. They can be changed using the RA9530-R GUI.

### 1.5.2. Wattshare TRx Mode Input Voltage

The RA9530 can transfer up to 5W of power in TRx mode. It follows the WPC 1.2.4 BPP protocol to transfer the power to other Qi-certified receivers such as mobile devices and earbud charging cases. The maximum power delivered in TRx mode depends on the input voltage on the VOUT pin, coil characteristics (such as AC resistance), and the friendly metal around the coil. Because the coil used for power transfer in TRx mode has high AC resistance compared to transmitter coil used in a charging pad, the input voltage on the VOUT pin in TRx mode must be around 7 to 9V to deliver 5W of power to the receiver.

### 1.5.3. TRx Mode Auto-Enable

The RA9530-R enters into TRx mode automatically if GP2 level is high when Vout is powered by external power or AP. The RA9530-R starts sending digital ping on TRx AC lines.

1. Pull up the GP2 test pin with external power 1.8V.
2. Provide 5V DC on RA9530-R VOUT.
3. Monitor AC line if digital ping signal comes out periodically.

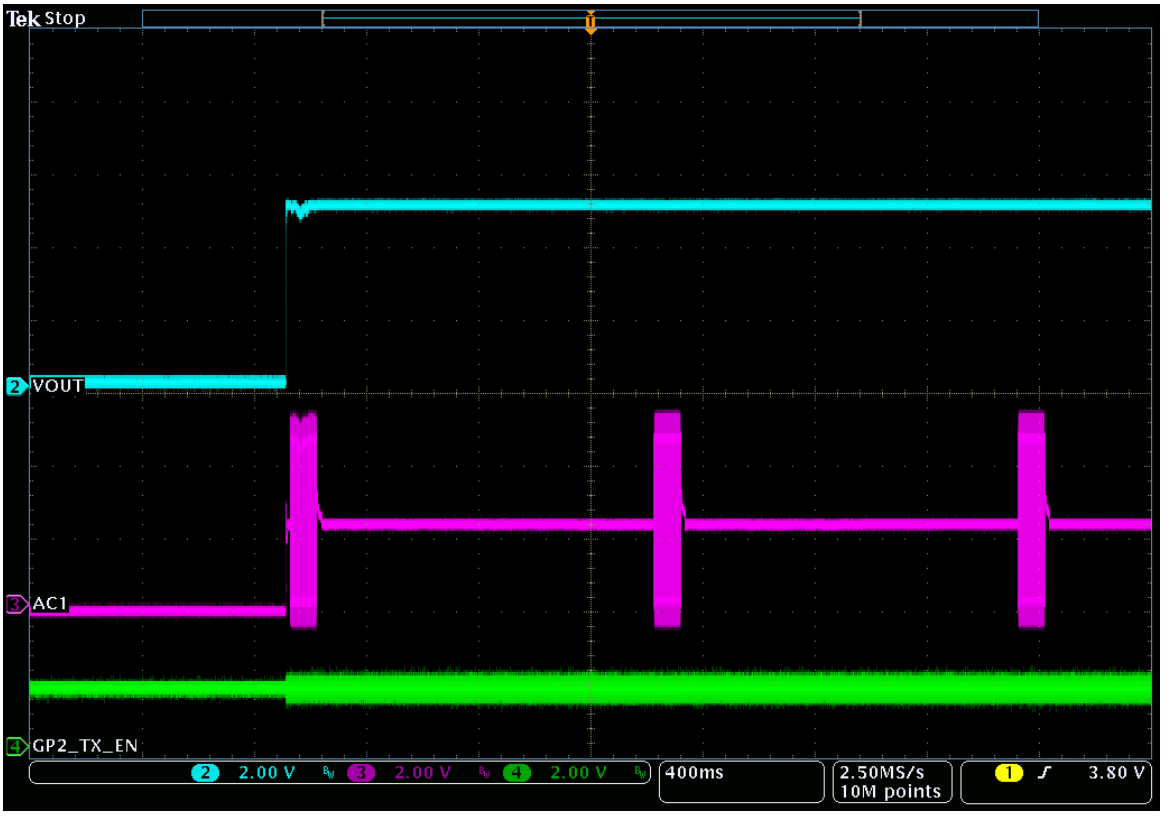



**Figure 19. TRx Mode Charging Waveform**

### 1.5.4. TRx System Efficiency

Figure 20Figure 19 shows TRx system efficiency using P9415-R Rx at 7.5V and 9V TRx input voltage conditions. TRx power is measured across RA9530-R VOUT and GND. Rx power is measured across R9415-R VOUt and GND.

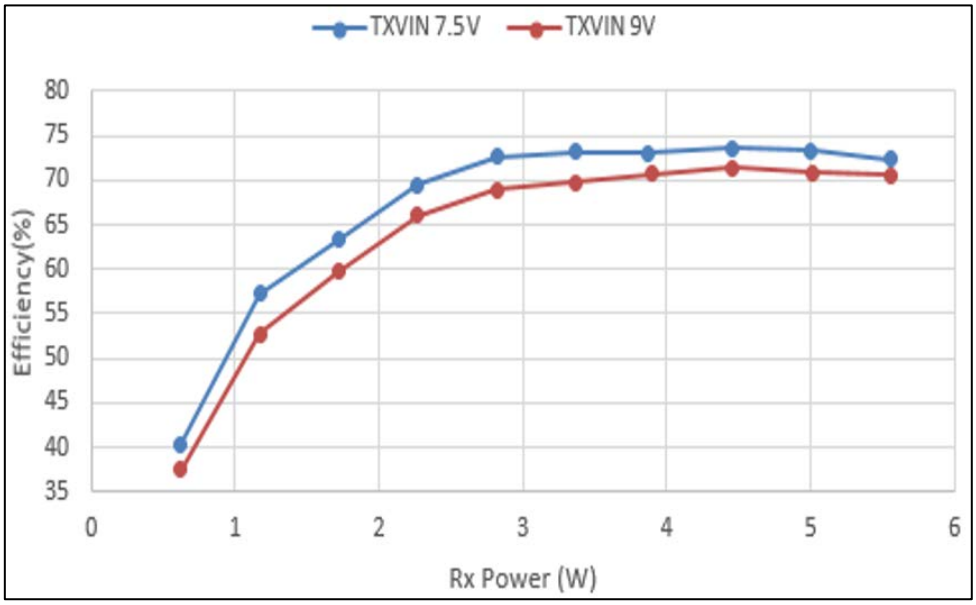



**Figure 20. TRx System Efficiency**

# 2. RA9530-R-EVK Evaluation Board Test Point and Connector

There are many test points placed around the RA9530-R_EVK board that can be used for quick and easy evaluation of RA9530 performance. VOUT, VRECT, and GND have large size test points for easy test cable connection for supplying power and loading. J3 and J1 are the pin type connector for USB-I2C bridge dongle interface connection and system configuration and monitoring.

## 2.1 RA9530-R-EVK Evaluation Board Test Point Placement

To locate the test points, see “Board Layout” section.

### 2.1.1. J3 Dongle Connector Pin Descriptions

| Pin Number | Name | Type | Description |
|---|---|---|---|
| 1 | SCL | Input | I2C Interface Clock signal |
| 2 | SDA | Input /Output | I2C Interface Data signal |
| 3 | GND | Power | Ground Reference |
| 4 | VRECT | Power | Dongle Power supply from USB Dongle Cable (Optional) |
| 5 | OD2_NINT | Output | Interrupt Signal from RA9530. Connect OD2_NINT to AP GPIO with PU |

### 2.1.2. J1 Test Connector Pin Descriptions

| Pin Number | Name | Type | Description |
|---|---|---|---|
| 1 | SCL | Input | I2C Interface Clock signal |
| 2 | SDA | Input /Output | I2C Interface Data signal |
| 3 | GND | Power | Ground Reference |
| 4 | OD2_NINT | Output | Interrupt Signal from RA9530. Connect OD2_NINT to AP GPIO with PU |
| 5 | OD3 | Input/Output | Reserved |
| 6 | OD4 | Input/Output | INHIBIT(SLEEP) |
| 7 | VRECT | Power | VRECT power supply from USB dongle |
| 8 | GP0 | Output | POWER GOOD Signal from LDO1p5 (Optional) |
| 9 | GP1 | Input/Output | Available for GPIO Use. Connect to ground if not used |
| 10 | GP2 | Input | TX EN |
| 11 | LDO5P0 | Power | Internal Power Regulator 5.0V |
| 12 | LDO1P5 | Power | Internal Power Regulator 1.5V |
| 13 | VDDIO | Input/Output | Internal capless LDO is connected and programmable as 1.2V/1.5V/1.8V. (Can be powered externally) |
| 14 | AP5V | Input | 5V powered externally from AP (Optional) |
| 15 | GND | Power | Ground Reference |

# 3. Hardware Connections Renesas USB-I2C Dongle to Windows GUI

The RA9530 firmware provides great flexibility to customize operating parameters for custom applications. Default values of the RA9530 operating parameters such as output voltage, FOD parameters, and current limit, are set in the firmware programmed into the internal electrically erasable programmable (EEPROM) memory. Based on the end application, the RA9530 operating parameters can be configured by either writing to internal SRAM registers or program parameter permanently to internal EEPROM memory via the I2C interface.

WPD-USB-DONGLE and USB-FTDI-V2-1 are recommended USB-I2C dongles. Both have same internal circuitry bit with a different dongle headers. Connect the WPD-USB-DONGLE/ USB-FTDI-V2-1 (USB-Bridge dongle) to a PC via the USB connector. Attach the Bridge to the I2C terminal J1 dongle on the RA9530-R-EVK board as shown on Figure 23. The dongle should only be plugged-in in one direction extending away from the RA9530-R-EVK PCB, and dongle cable black line (ground) should be connected to J1 Pin3 GND.

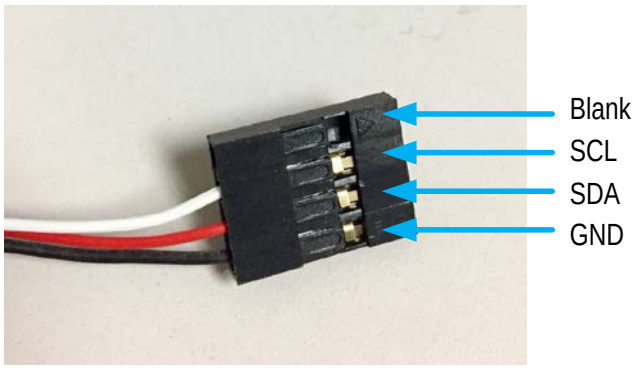



**Figure 21. USB to I2C Dongle Header of "USB-FTDI-V2-1"(FTDI) Dongle.**

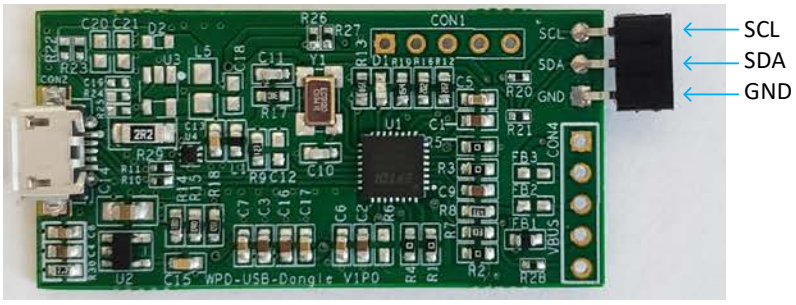



**Figure 22. USB to I2C Dongle Header of "WPD-USB- DONGLE".**

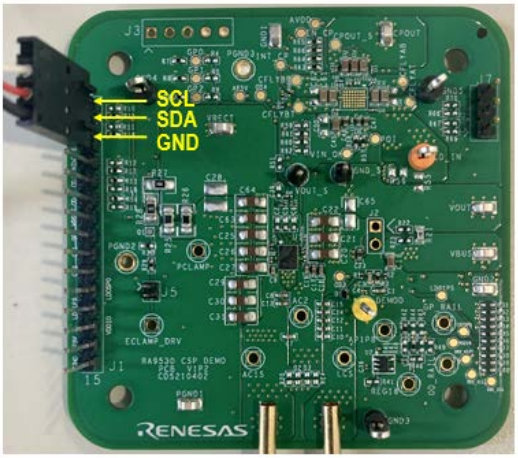



**Figure 23. USB-I2C Bridge Connected to I2C Terminal J1 of RA9530-R EVK Board**

## 3.1 Using the GUI to Program the RA9530

To program the device, remove the RA9530-R-EVK demo board coil from the Tx, connect GND, SDA, and SCL to the WPD-USB-DONGLE or other USB-I2C bridge as shown on Figure 23 and power Vrect or Vout from an external 5V power supply.

1. Open the GUI program – RenesasStandardGUI3.exe or newer version. The initial screen of the RA9530-R Windows GUI is shown below.

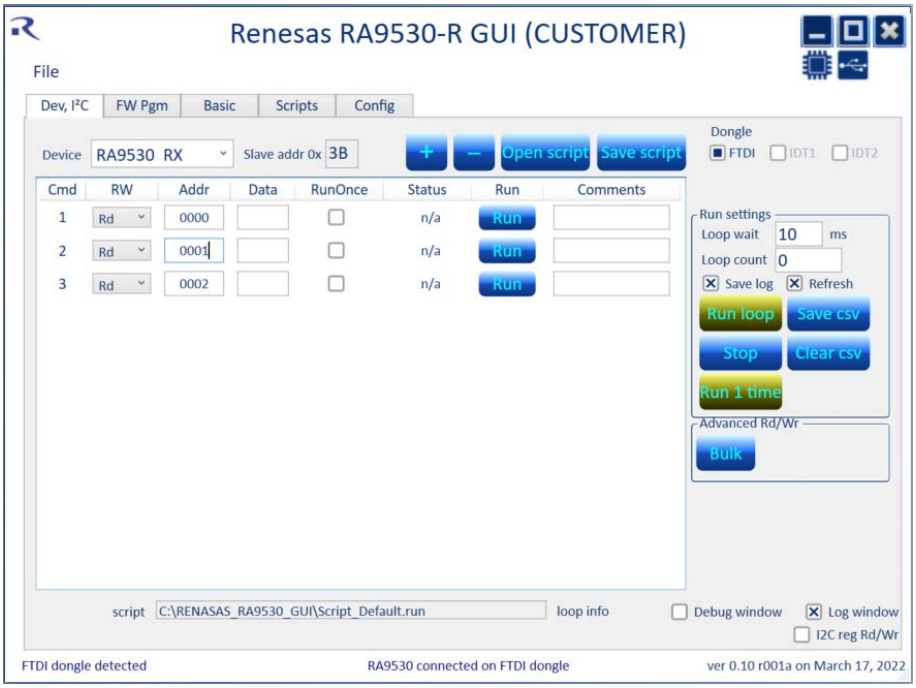



**Figure 24. Initial Screen of RA9530-R GUI**

*Note*: Make sure the external 5V power supply is turned on and the USB-I2C Bridge is connected to the PC. Verify that the Device selected is the RA9530, and that the slave address is set to 0x3B at the top of screen. Check the “FTDI dongle detected” and “RA9530 connected on FTDI dongle” messages are shown at the bottom of the screen. If you do not see these messages, unplug the USB cable at the PC side, plug it in again and check all connections.

If the message indicates that the “FTDI dongle detected” but the RA9530 is not connected, it may be necessary to click on “FTDI” to redetect the device (see Figure 37).

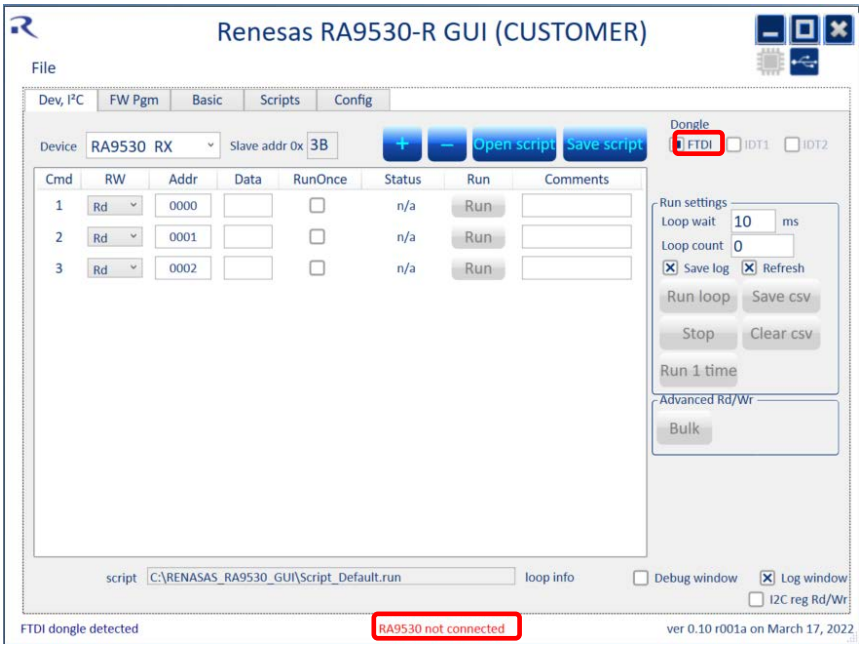



**Figure 25. USB-bridge is Detected; RA9530 is Not Connected**

2. To update the EEPROM program, select the “FW Pgm” tab. Select BIN or HEX box depending on the file format you intend to use and press the “Load file” button. A popup window will appear. Navigate to the current RA9530 FW file and open the file (see the following figure, which indicates the FW file was read successfully).

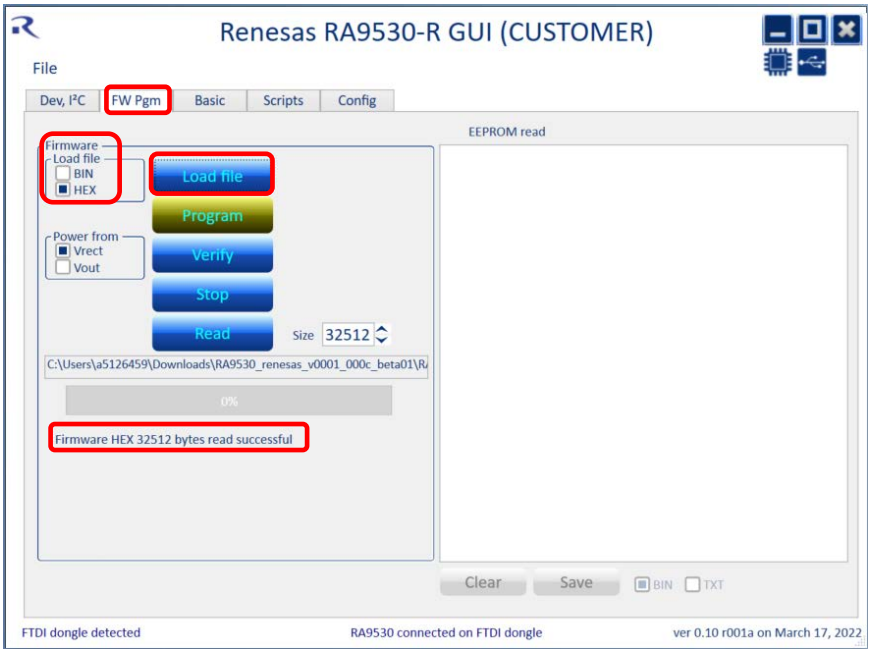



**Figure 26. RA9530 EEPROM Programming Using I2C Slave Device Address 0x3B**

3. After loading the file, select Vrect or Vout depending on where your power supply is connected to and press the “Program” button. The EEPROM will be programmed and the GUI will indicate if successful or if there were errors. See Figure 10, which indicates that the programming was successful. If there are any errors, attempt to program again.

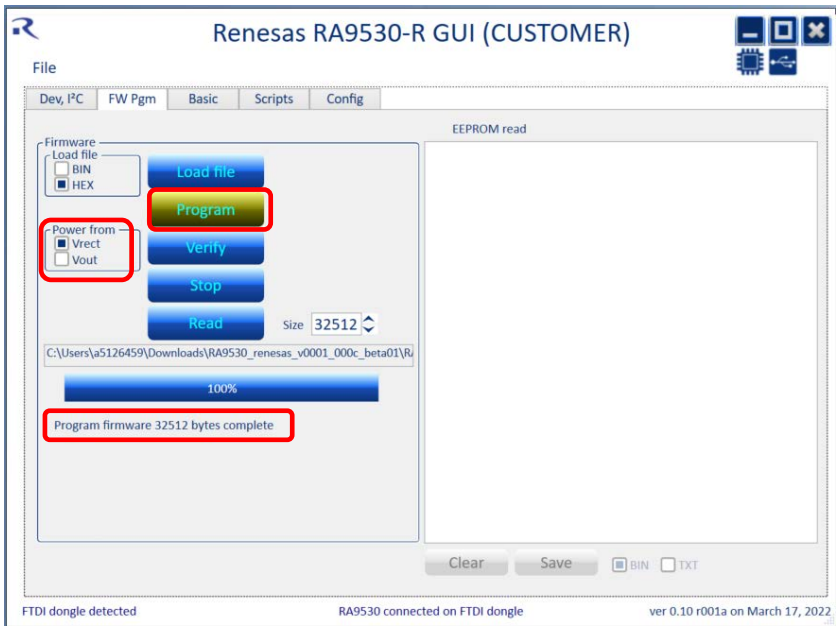



**Figure 27. EEPROM Programming Successful**

4. If the firmware was programmed successfully, power cycle the external 5V power supply (turn the power supply off, then on), then press the “Verify” button. A total match should be indicated for successful programming (see Figure 39. If there are any errors, attempt to program again.

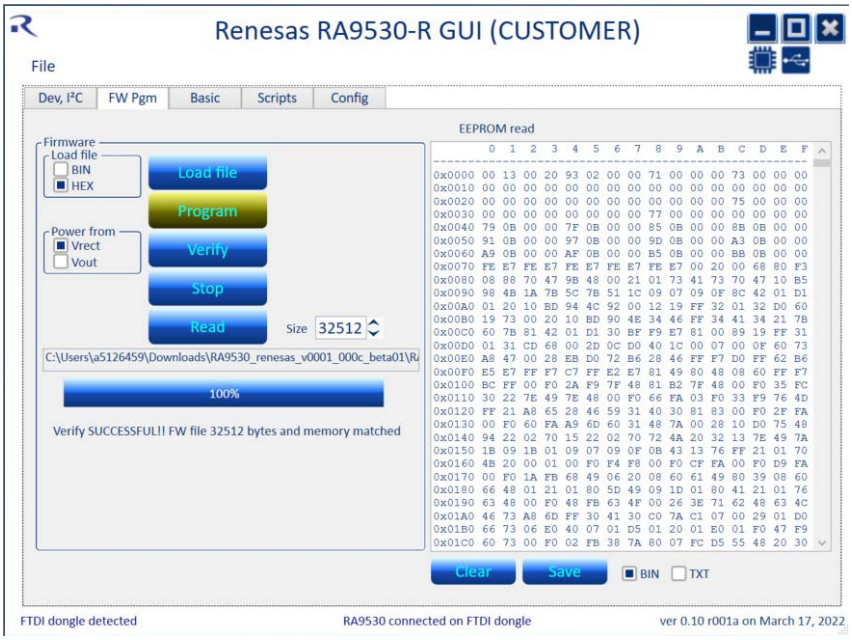



**Figure 28. FW Program Verification Success**

5. After programming and verification success:
   a. Verify programming. It is recommended to select the “Basic 1” tab and press the “Read 1 time” button to check the FW revision, date code is correct.
   b. Turn off and remove the external 5V power supply on Vrect and Vout and place the RA9530-R-EVK on a compatible Tx.

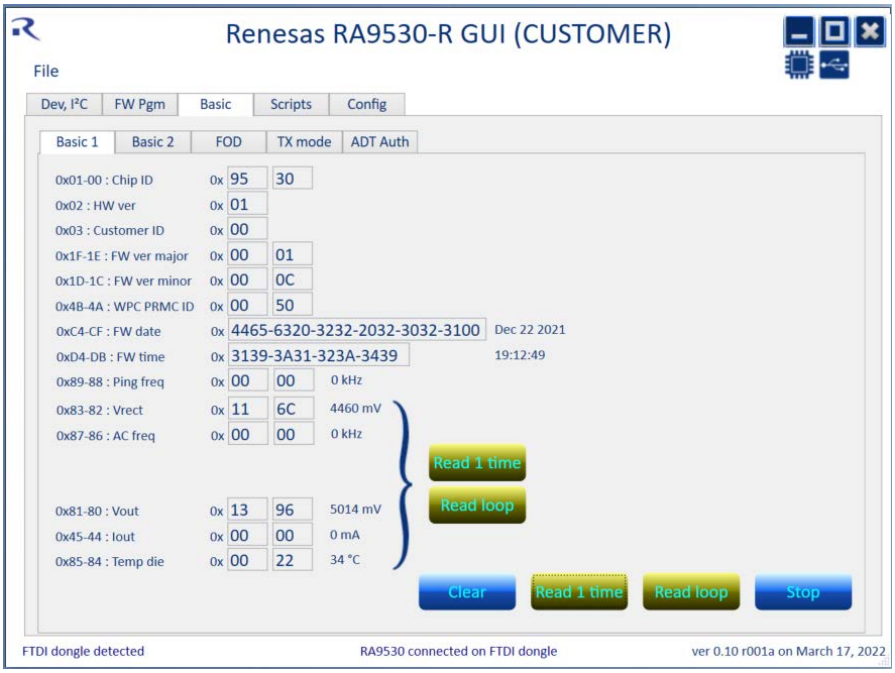



**Figure 29. Verify FW Revision and Date Code**

## 3.2 Using the GUI to Read / Write to Registers

Access to the RA9530 status and control settings are done by reading and writing the I2C registers. The registers are described in “Device Registers”. To read and write to the registers, complete one of the following procedures:

1. To read and write specific registers, select the “Dev, I2C” tab.
   a. To read from a register, select “Rd” and click “Run” to read the hex register address that specified in the “Addr” box. Hex data will be displayed in “Data” box.
   b. To write to a register, select “Wr” and click “Run” to write the hex data provided in “Data” to the hex register address in “Addr”.
   c. To read/write all the registers in the boxes, click “Run 1 time”. The sequence of the read/write operation will be the same as how the registers are listed.
   d. To read/write all the registers in the boxes repeatedly, click “Run loop”. “Loop wait” and “Loop count” can be set to configure the operation interval time and total counts. If “Loop count” is 0, the loop will go infinitely.
2. To read and write specific registers, click the “I2C reg Rd/Wr” box in “Dev, I2C” tab. The I2C Rd/Wr block will stay accessible.

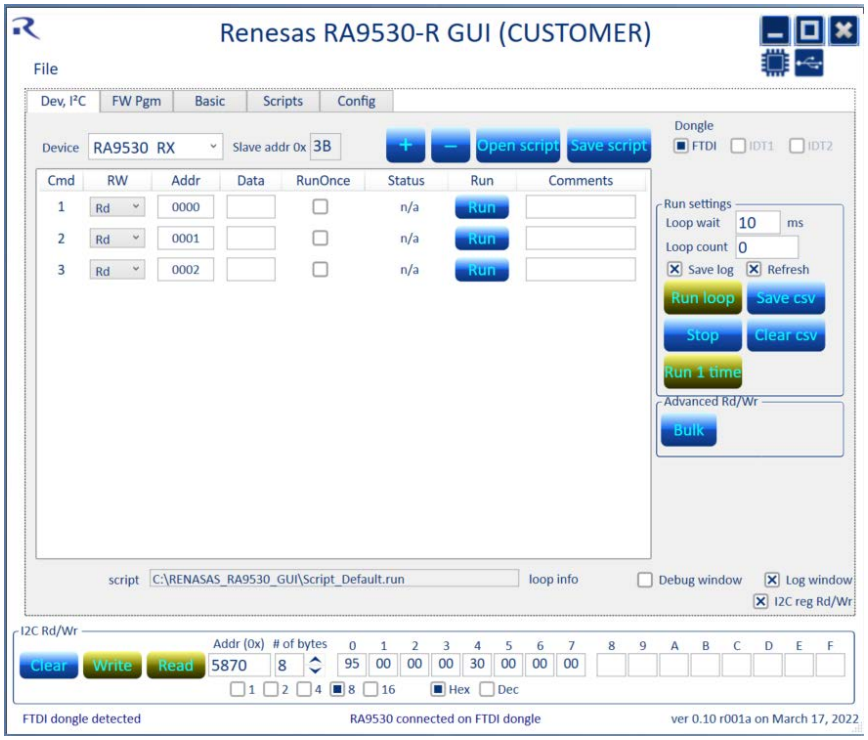



**Figure 30. Read / Write to Registers**

3. For bulk reading of common operating registers, select the “Basic” tab and click the ‘Read 1 time” or the “Run loop”. “Run loop” can be stopped by selecting ‘Stop’. Click “Write” to write data to the according register.

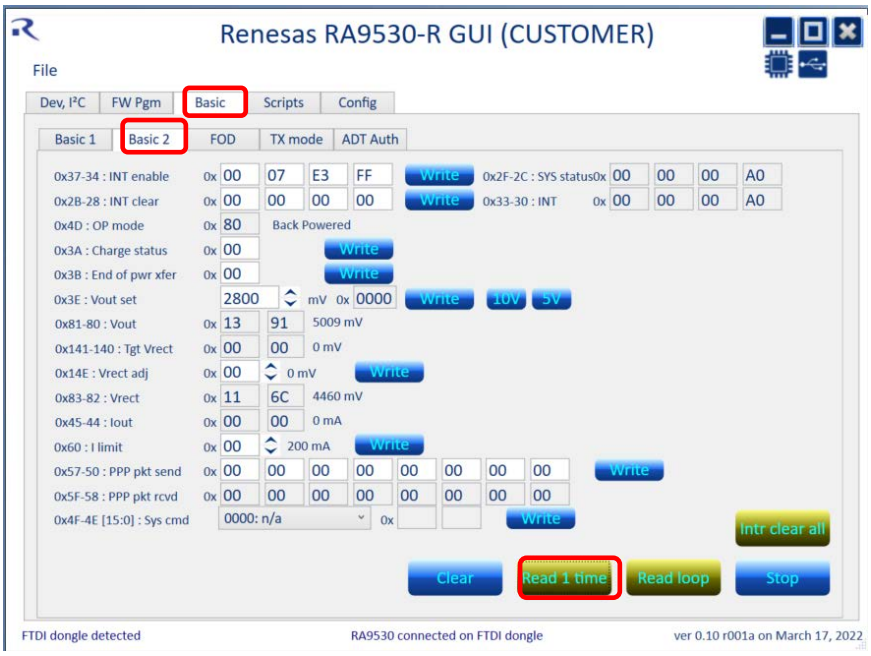



**Figure 31. Basic Tab, after Clicking “Read 1 time”**

4. Read and write data to the RA9530 registers through scripting. To write 1byte data value 0x01 to register address 0x3200, select the “Scripts” tab and type in “.i2c_cmd_wr(3200, 1, 01)” as shown in Figure 42 and click “Cmd 01”. To read 2bytes data from register address 0x3200, type in “.i2c_cmd_rd(3200, 2)” and click “Cmd 02”. The reading result will be shown in the log window. To perform all operations listed in the “Script commands”, click “Run”. The sequence of the read/write operation will be the same as how the commands are listed.

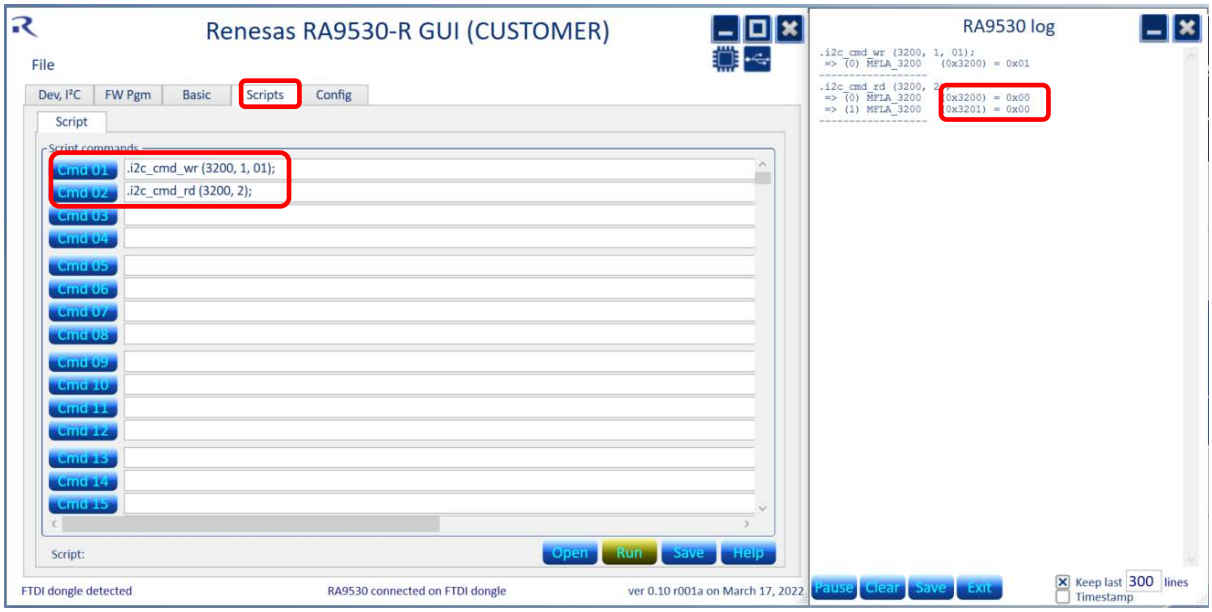



**Figure 32. Scripts Tab, after Clicking “Run”**

## 3.3 Using the GUI to Read / Write Configuration Parameters to EEPROM

Configuration parameters in RX mode and TRx mode operation can be read from and written to EEPROM flash memory after modification. The configuration parameters written in EEPROM are non-volatile.

1. Select the “Config” tab and click “Read chip”. The configuration hex parameters will be read from EEPROM and displayed in the tables of both the TRx and RX setting. In the TRx setting page, proprietary FOD setting can be configured in a new window by clicking “Proprietary FOD”. If “Reset cfg” is clicked, the tables in both TRx setting and RX setting are updated with the default configuration parameters.
2. After modifying the hex parameters in tables, click “Write chip” and all the data displayed in the tables of both TRx setting and RX setting will be written to EEPROM. Power off and on chip after “Write chip”. New parameters will be applied from the next time wireless charging operation. You can also save the modified configuration parameters in your local drive by clicking “Save cfg file”. “Open cfg file” will read the cfg file in your local drive and display the configuration parameters in the tables.


**Figure 33. Config Tab, after click “Read chip”**

# 4. Rx Mode Functions

## 4.1 Synchronous Rectifier

The efficiency of the full-bridge rectifier in the RA9530 is increased by implementing it as a synchronous rectifier. The rectifier comprises four internally-driven switches that work in a full synchronous mode of operation when the load applied to VOUT is higher than the programmed threshold value. Below that threshold, the rectifier works in half-synchronous rectification mode. In half-synchronous rectification mode, only the low-side N-MOSFETs are driven and the high-side N-MOSFETs are forced into diode mode. At power-up, when the voltage is below the UVLO threshold, the rectifier works by using the body diodes associated with the NMOS transistors. The BST capacitors are used to provide power to drive the gates of high-side NMOS switches.

## 4.2 Rectifier and VRECT Level

When VRECT powers up to be greater than UVLO, the full-bridge rectifier switches to half synchronous or full synchronous mode (depending on the loading conditions) to efficiently transfer energy from the transmitter to the load applied to VOUT. The control loop of the RA9530 maintains the rectifier voltage between 5V and 23.5V, depending on the output current ($I_{OUT}$) and the programmed output voltage. VRECT must not be directly loaded.

## 4.3 Over-Voltage Protection

When VRECT reaches 90% of the over-voltage threshold voltage, the OVP interrupt is triggered and the PCLMAP function is turned on. On an over-voltage condition, the RA9530 turns on the internal PCLAMP to bring the rectifier voltage back to a safe operating level and sends an interrupt to the AP to notify of the over-voltage condition. The over-voltage threshold value is different by Rx operation mode and there is hysteresis to make a stable operation. In BPP mode, the default OVP threshold voltage is 13V for rising and 12V for falling direction. In EPP mode default OVP voltage is 21V for rising and 19V for falling. In HPP mode, OVP voltage is 24.6V for rising and 22.9V for falling. These thresholds can be configured in EEPROM . When PCLAMP is turned on, excessive power is consumed by the external PCLAMP resistor. Select the appropriate resistor value based on the power rating.

PCLAMP current is OVP threshold voltage/ PCLAMP resistor. The PCLAMP maximum current should be less than 300mA.

## 4.4 Over-Current Protection, Over-Temperature Protection, and Thermal Shutdown

The RA9530 uses over-current (OC) protection and over-temperature (OT) protection by sending an interrupt to the AP if the output current or die temperature exceeds the operating limits.

If output current exceeds the over-current threshold value, an over-current fault interrupt is sent to the AP with the expectation that the AP will respond by reducing the output consumption being drawn from the RA9530. If the output current reaches the over-current threshold plus the over-current threshold hysteresis value, an over-current fault interrupt is sent to AP and an End Power Transfer packet (OCP) is sent to the transmitter.

If the die temperature exceeds the over-temperature threshold1 (default 105°C), the RA9530 first sends an interrupt (OTP) to the AP to alarm the over-temperature condition and starts the OTP timer (180sec default). If the temperature falls below over-temperature threshold1 – hysteresis (5°C), OTP timer resets. If the die temperature keeps increasing and exceeds the over-temperature threshold2 (default 135°C) or the OTP timer expires, the RA9530 sends an End Power Transfer Packet to the transmitter to terminate a power transfer. If the temperature keeps increasing and exceeds the thermal shutdown threshold (typical 140°C), the RA9530 turns off output LDO.

## 4.5 LDO Regulators

The RA9530 has 4 LDOs. The Main LDO (VOUT pin) is programmable from 5V to 20V and LDO5P0 is powered by VRECT. LDO1P5 and VDDIO are powered by LDO5P0. Both LDO5P0 and LDO1P5 are used for supplying power to internal low voltage blocks. The LDOs must have local ceramic bypass capacitors placed near the RA9530. VDDIO is internal capless LDO that can be used for general purpose IO power. VDDIO is programmable as 1.2V/1.5V/1.8V based on application IO power. 1.8V is default level.

## 4.6 MLDO Output Enable Conditions

In BPP mode, after entering the power transfer phase, the RA9530 starts sending control error packets with high value to raise the VRECT voltage close to its target value and starts a two-second timer. The RA9530 enables the MLDO when the VRECT voltage reaches the target voltage or the two-second timer expires.

In the EPP mode, the RX9530 enables the MLDO when it receives ACK from Tx in calibration phase1 and Vrect is within target voltage range. If the RA9530 does not reach target Vrect level in calibration phase 1 until it sends

mode1 RPP 8 times(default), the MLDO target voltage is reduced from 10V to 9V (default configurable) and move to calibration mode2 after enabling MLDO.

## 4.7 Renesas High-Power Mode

The application processor on the receiver can authenticate the Transmitter using the in-band communication. After successful authentication of the transmitter, the high-power mode can be enabled. Thereafter, the application processor should use the Fast Charging Voltage Register to control the desired output levels. The RA9530 will automatically change VOUT value if the Fast Charge Sequence is successful.

1. Place the Rx on Renesas HPP supporting Tx (P9247-GB EVK).
2. The Rx will authenticate Tx ID using proprietary packet during power transfer phase.
3. The Rx reports AP of authentication result using interrupt signal.
4. If interrupt register (0x30) bit 13 is set, authentication is a success.
5. The AP can set the fast charging voltage in register (0x78) if authentication is success.
6. The Rx will increase Vout voltage to the target level along with automatic Tx Vin voltage control.

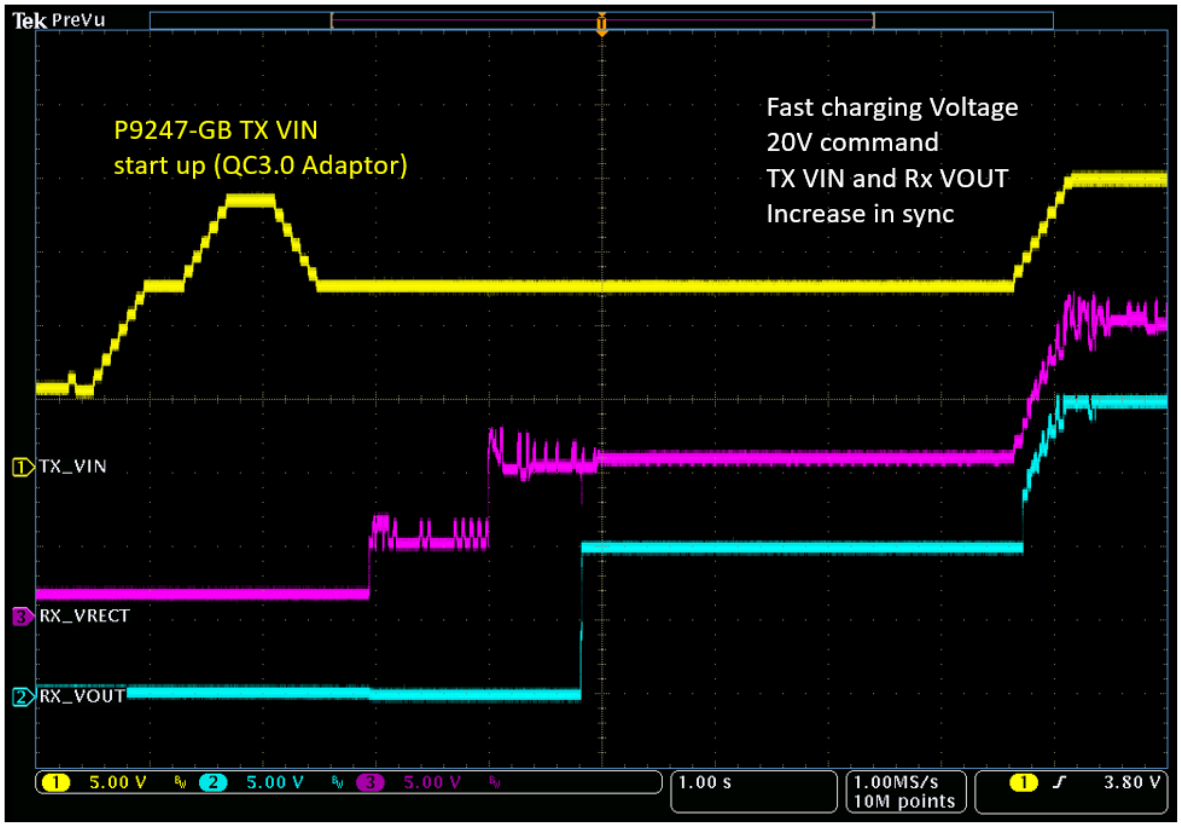



**Figure 34. HPP Start-Up Waveform**

# 5. Wattshare Mode TRx Functions

## 5.1 Demodulator

In TRx Mode, the Rx sends WPC protocol packets to the RA9530. Using the demodulation (DEMOD) filter shown in Figure35 and the internal demodulator circuitry, the RA9530 decodes the ASK modulation packets Rx sent. Based on the packet information, the RA9530 modulates the transmitted power by adjusting the operating frequency or duty cycle and detects a foreign object between Tx and Rx.

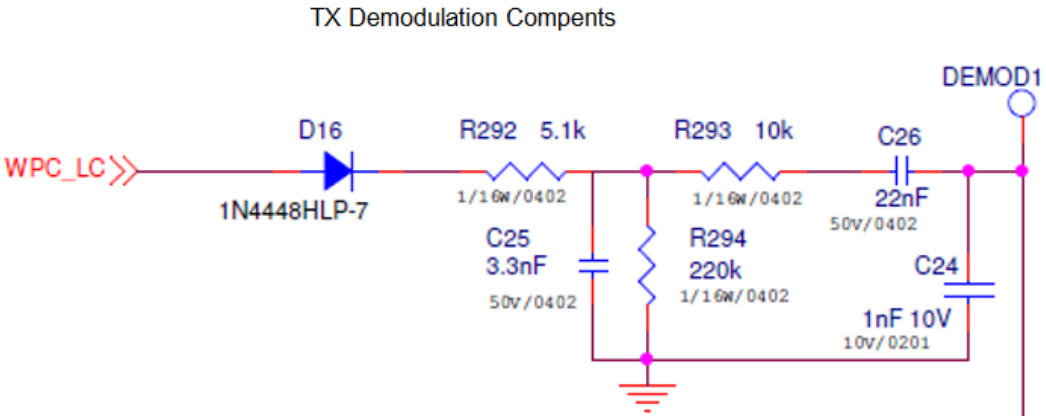



**Figure 35. WattShare Mode Demodulation Filter**

## 5.2 WattShare Mode Input Under Voltage, Over Voltage, and Current Limit

In the default firmware there are several over-current protection thresholds in the WattShare mode that are applied differently depending on the operation phase.

In the ping phase, if the input current exceeds the Ping OCP threshold (default 1.5A), the RA9530 sets flag EPT_POCP in TRx End Power Transfer Reason Register and sends an interrupt EPT_TYPE_INT to the AP and disables the TRX function. TRx will not resume until the AP recycles the power on the VOUT pin and enables the TRx mode again.

In the power transfer phase, if the input current exceeds the IgnoreCepThd (default 2.5A), the RA9530 enters in CEP Ignore mode. If the average input current exceeds the OCP threshold (default 2.5A), the RA9530 sets flag EPT_OCP in TRx End Power Transfer Reason Register and sends an interrupt EPT_TYPE_INT to the AP and disables the TRx function. TRx will not resume until the AP recycles the power on the VOUT pin and enables the TRx mode again.

If the voltage on the VRECT pin is higher than the over-voltage protection OVP threshold (default 11V), the RA9530 sends interrupt EPT_TYPE_INT to AP, sets the EPT_OVP bit of TRx End Power Transfer Reason Register, and disables the TRx function.

If the voltage on the VOUT pin is lower than the low voltage protection (LVP) threshold (Default 4.5V), the RA9530 sends interrupt (EPT_TYPE_INT) to AP.

## 5.3 Transmitter Conflict in WattShare Mode

When the RA9530 is in WattShare mode, the user may accidentally place the RA9530 on another WPC transmitter. The pings from the WPC transmitter will generate an AC voltage in the resonant tank connected to the RA9530. The RA9530 detects this voltage, sends an interrupt (TX_Conflict) to the AP, and exits TRx mode. The AP must disable the external power supply connected to the VOUT pin of the RA9530.

# 6. TRx Wireless Power Coil

The TRx coil is dependent on customer requirements and most are custom designs. Renesas recommends the following TRx coil and it was installed in RA9530-R demo board.

- Ls = 8 to 10μH
- DCR = < 0.3Ω
- ACR = < 0.4Ω

**Table 1. Coil Manufacturer**

| Output Power | Vendor | Part Number | Inductance at 100kHz | Resonant Caps (Cs) | DC Resistance at 20℃ |
|---|---|---|---|---|---|
| 15W | Luxshare | ICTR-QS5858031L-MW034 | 9.0 ±0.2μH | 400nF | 195mΩ ±10% |

# 7. Resonance Capacitors

The series resonance capacitors (C10, C11, C12, C14, and C15) are critical components and must be chosen carefully. All current that flows to the load flows through these components plus any current loss in the rectifier AC to DC conversion. The recommended capacitor is the 100nF Murata (GRM155C71H104KE19, X7S, 50V, or GRM155R61H104KE19, X5R, 50V), which have an ESR < 0.1ohms at 100kHz. The GRM155C71H104KE19 capacitor is the best choice based on ESR value and DC bias effects. If another capacitor is chosen, inspecting the ESR vs. Frequency curve of the manufacturer's capacitor datasheet is necessary to compare ESR characteristics as well as the DC bias effects on the capacitor value. Adding non-populated (NP) component placement (C10) is advised if the additional capacitance is needed for a particular Rx coil.

# 8. Input Capacitor (VRECT Capacitors)

The LDO input capacitors (VRECT capacitors) should be located as close as possible to the VRECT pins and ground (PGND). Ceramic capacitors are recommended for their low ESR and small profile.

# 9. Output Capacitor (VOUT Capacitors)

The output capacitor connection to the ground pins (PGND) should be made as short as practical for maximum device performance. Because the LDO is designed to function with very low ESR capacitors, a ceramic capacitor is recommended for the best performance. For better transient response, the total amount of output capacitance should be increased to meet the output voltage variation target of the application (VRECT capacitance may need to be increased as well).

# 10. LDO1P5 Capacitor

The RA9530 has an internal LDO regulator that must have at least a 1μF to 2.2μF capacitor connected from the LDO1P5 pin to PGND. This capacitor should be as close as possible to the LDO1P5 pin with a close GND connection. A 0.1μF capacitor in a 0201 or 0402 size package can be added for improved high-frequency decoupling of the LDO1P5 power rail because this voltage powers the internal ARM Cortex-M0 processor.

# 11. LDO5P0 Capacitor

The RA9530 has an internal LDO regulator that must have at least a 1μF to 2.2μF capacitor connected from the LDO5P0 pin to PGND. This capacitor should be as close as possible to the LDO5P0 pin with a close PGND connection. A 0.1μF capacitor in a 0201 or 0402 size package can be added for improved high-frequency decoupling of the LDO5P0 power rail because this voltage powers the internal ADC and UVLO circuits.

For additional power savings at higher input voltages, an external 5V supply should be connected to supply power to the RA9530 via the LDO5P0 pin. The applied voltage to this pin must be > LDO5P0 regular output voltage to power the low-voltage circuitry from the external 5V supply, while the external 5V supply should be between 5.2V and 5.5V.

# 12. PCLAMP Connection

The RA9530 has an internal automatic DC clamping feature to protect the device from events that cause high voltages to occur on the AC or DC side of the rectifier. The clamping engages by the VRECT connection to the PCLAMP pin. The VRECT node must be connected to the PCLAMP pin at all times during Rx mode operation. For space-constrained designs, the PCLAMP pin can be directly connected to the VRECT node for 5W or lower power operation.

Also, there is an option for external FET and resistor clamping by the use of the ECLAMP_DRV pin which can output 5V to drive the gate of external MOSFET. This output is synchronized with the internal PCLAMP signal. ECLAMP_DRV can provide additional clamping capability as needed and there is no thermal increase in the IC side because clamping energy is consumed in external components.

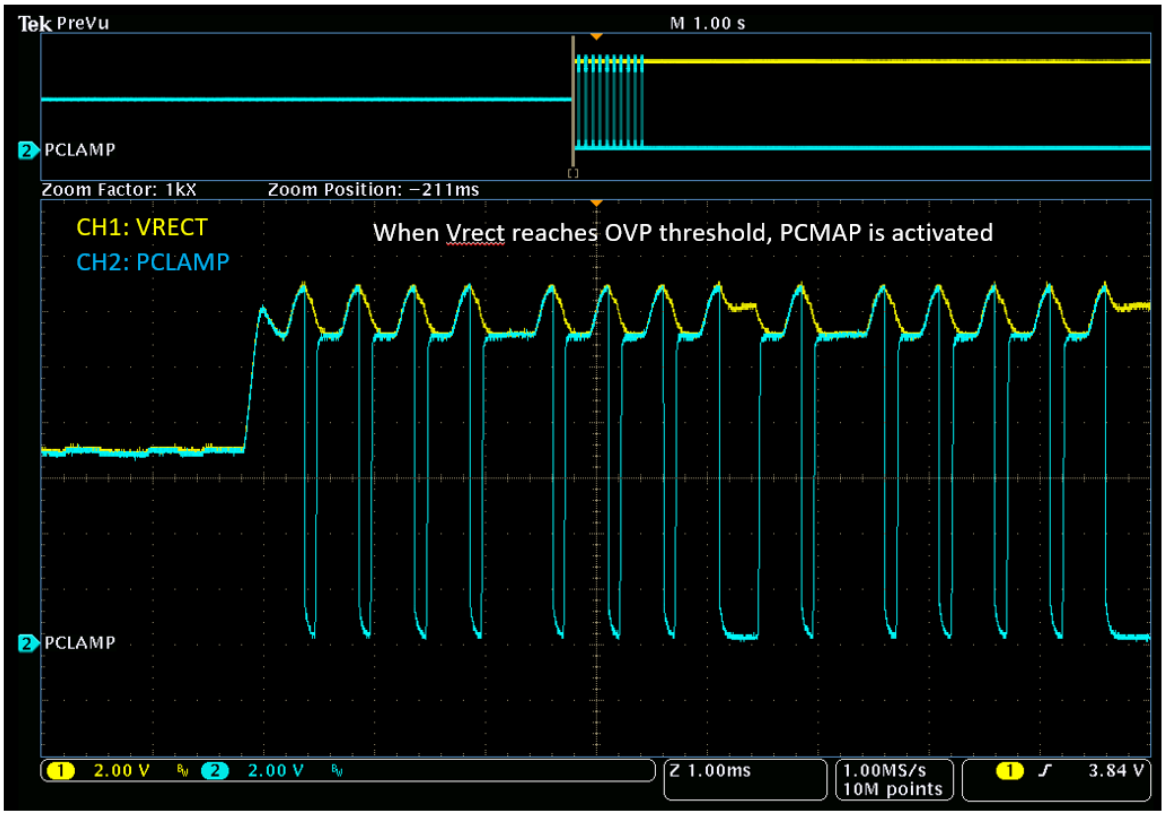



**Figure 36. PCLAMP Operation at OVP Condition in BPP Mode**

# 13. GPIO Pins

The RA9530 has general-purpose input-output (GPIO) pins. The OD0-OD4 and GP0-GP6 pins are all multi-functional.OD0-OD4 pins have an open-drained structure and GP0-GP6 pins have a push-pull structure. In the default firmware used in the evaluation board the GPIO pins are given specific functions to meet broad customer requirements. Below pin descriptions explains the specific functions allocated to GPIO pins

## 13.1 OD0/SCL Pin

The OD0 pin has a digital function open-drain structure. It is assigned to SCL of the I2C function for the serial interface between the AP and the RA9530. An external pull-up register on the SCL line is required for I2C communication and 1.8V power is pulled up in RA9530-R demo board. OD0 can operate up to 5V.

## 13.2 OD1/SDA Pin

The OD1 pin is set as a digital function open-drain structure. It is assigned to the SDA function of the I2C serial interface bus between the AP and the RA9530. An external pull-up resistor on the SDA line is required for I2C communication and 1.8V power is pulled up in RA9530-R demo board. OD1 can operate up to 5V.

## 13.3 OD2/nINT Pin

The OD2 pin is set as a digital function open-drain structure. It is assigned as the nINT signal for interrupt notification to the AP. nINT pin indicates a major change of states or error modes such as over-current, over-voltage, or over-temperature event. Connect this pin to the AP I/O voltage rail using an external pull-up resistor. The RA9530 drives this pin LOW to notify the AP of status changes.

## 13.4 OD4/INHIBIT(SLEEP)

The OD4/SLEEP pin is a digital input referenced to VDDIO. When the SLEEP pin is low, the Rx mode is enabled. Pulling the SLEEP pin high will prevent the RA9530 from connecting to the transmitter. The AP can use this pin to safely enable and disable the wireless power transfer function with proper VRECT node protections. If this pin is driven high in the power transfer phase, the RA9530 will send an End Power Transfer packet to the transmitter and wireless power transfer will be disabled while Vrect protection is alive.

## 13.5 GP0/PWRGD Pin

The GP0 pin is a digital output referenced to VDDIO. The AP can use the power good signal to turn on the charging connection indicator or other system functions. Power good (PWRGD) pin is low by default. In BPP mode, the power good pin is output high when MLDO is enabled. In EPP mode, the power good pin is high at the end of the negotiation phase by default. It can be configured to be high when MLDO Vout is enabled. If the PWRGD function is not required, pull down the GP0 pin to the ground with 100k~300kOhm.

## 13.6 GP2/TX_EN

The GP2 pin is a digital input referenced to VDDIO. If GP2 is pulled up by VDDIO, TRx mode starts working automatically when external power is connected to the VOUT pin. If GP2 (TX_EN) is not used, directly connect the GP2 pin to ground.

## 13.7 Unused GP/OD Pin

An unused GP pin is required to be connected to ground and OD pin is connected to VDDIO. Floating is not recommended.

# 14. Foreign Object Detection

When metallic objects are exposed to an alternating magnetic field, eddy currents cause such objects to heat up. Examples of such parasitic metal objects are coins, keys, paper clips, etc. The amount of heating depends on the strength of the coupled magnetic field, as well as the characteristics of the object, such as its resistivity, size, and shape. In a wireless power transfer system, the heating manifests itself as a power loss, and therefore a reduction in power-transfer efficiency. Moreover, if no appropriate measures are taken, the heating could be sufficient that the foreign object could become heated to an unsafe temperature.

In the Extended Power Profile, there are two methods of foreign object detection (FOD). One is by measuring the system quality factor before entering the power transfer phase, and the other is to measure the power loss

difference between the received power and the transmitted power during the power transfer phase. Before entering the power transfer phase, the RA9530 sends a reference Q-factor (default 30) in the negotiation phase. The transmitter measures the Q-factor on its coil and compares it with the reference Q-factor provided by the RA9530. If the difference is large, the transmitter presumes that there is a foreign object (FO) between the Tx and Rx and shuts down. The power loss foreign object detection method is used in both the Extended Power Profile (EPP) and the Basic Power Profile (BPP) modes power transfer phase. During the power transfer phase, the RA9530 continuously sends to the transmitter the amount of power received using the Received Power Packet (RPP). The transmitter will compare the RPP packet information received from the receiver with its measured transmitted power. If there is a significant difference the transmitter presumes that there is a foreign object (FO) between Tx and Rx that is absorbing the transmitted power and will stop the power transfer to avoid heating of FO.

## 14.1 FOD Parameters in Receiver Mode

For a WPC power loss foreign object detection to function effectively, the receiver must account and compensate for all of their known losses. Such losses, for example, could be due to resistive losses or nearby metals that are part of the receiver. Because the system accurately measures its power and accounts for all known losses, it can thereby detect foreign objects because they cause an unknown loss. The WPC specification requires that a power receiver must report to the power transmitter its received power (PPR) in an RPP. The maximum value of the received power accuracy $P\Delta$ depends on the maximum power of the power receiver as defined in the following table.

The power receiver must determine its PPR with an accuracy of $\pm P\Delta$, and report its received power as PRECEIVED = PPR + $P\Delta$. This means that the reported received power is always greater than or equal to the transmitted power (PPT) if there is no foreign object (FO) present on the interface surface.

**Table 2. Recommended Maximum Estimated Power Loss**

| Maximum Power (W) | Maximum $P\Delta$ (mW) |
|---|---|
| 5 | 350 |
| 10 | 500 |
| 15 | 750 |

The compensation algorithm includes parameter values that are programmable either by an internal register or customer configuration table in MTP. Programmability is necessary so that the calibration settings can be optimized to match the power transfer characteristics of each particular WPC system to include the power losses of the transmit and receive coils, battery, shielding, and case materials under no-load to full-load conditions. The values are based on the comparison of the received power against a reference power curve so that any foreign object can be sensed when the received power is different than the expected system power.

FOD parameters consist of eight sections. Each section is divided by output current and consists of gain and offset to compensate for Rx internal power loss; each section is also adjusted for Reported Rx power. The following comprises the Rx load current ranges for the FOD sections:

- FOD section [0] is from 100mA to section 0 current in EPP. From 0mA to section0 current in BPP.
- FOD section [1] is not used in EPP. In BPP it is from section 0 current to 380mA.
- FOD section [2] is from section 0 current to 510mA in EPP. In BPP it is from 380mA to 510mA.
- FOD section [3] is from 510mA to 670mA.
- FOD section [4] is from 670mA to 870mA.
- FOD section [5] is more than 870mA.
- FOD section [6] is used for diode mode, current 0mA to 100mA in EPP. BPP does not have diode mode.

Section 0 current is the point where the internal rectifier changes the bridge configuration from half-bridge to full-bridge. In the default configuration, if VOUT is set to less than 7V, the section0 current is 280mA. If Voutset is higher than 7V, the section0 current is 380mA. There is around ±30mA load current hysteresis for changing the FOD sections. These settings can be changed using the *RA9530-R Wireless Power Pro GUI.*

The formula of Rx Reported Power is:

$$Rx\ Reported\ Power[0..5] = Power(Rx\ delivered\ power) * FOD\ Gain[0 \dots 5] + Offset[0..5]$$

Place the receiver with the RA9530 on the Nok9 FOD transmitter. Ramp the current on the output of the RA9530 in steps of 50mA to 100mA and monitor power difference between the Nok9 transmitted power and the receiver reported power value. The difference should be within maximum Power loss delta in above Power lossTable. If the difference exceeds the maximum power loss delta, adjust the FOD gain or FOD offset of that particular output current section to bring the difference back to within range. The AP can modify the FOD gain and FOD offset by writing to the Foreign Object Detection Customer Registers (0x68-0x77). In the final product, the AP can use the VRECTON as a trigger to update the FOD registers.

## 14.2 FOD Parameters in Transmitter Mode

For a WPC power loss foreign object detection to function effectively, the transmitter must set the FOD threshold at a reasonable value by accounting for all its known losses such as Coil resistance loss and losses because of metal around the coil integrated into the product. In the power transfer phase, the RA9530 will continuously calculate the difference between its measured transmitted power and RPP packet information received from the receiver. If the difference is higher than the FOD threshold, the RA9530 presumes that there is a foreign object (FO) between Tx and Rx that is absorbing the transmitted power and will stop the power transfer to avoid heating the FO.

The FOD threshold value changes based on the Received Power Packet value (RPP) from the receiver:

- The FodSegThd, FodThdH, and FodThdL are configurable by config table in MTP using the *RA9530-R Wireless Power Pro GUI*
- FOD criteria: FOD threshold > Transmitted Power (PPT) – Received Power (RPP)

# 15. I²C Function

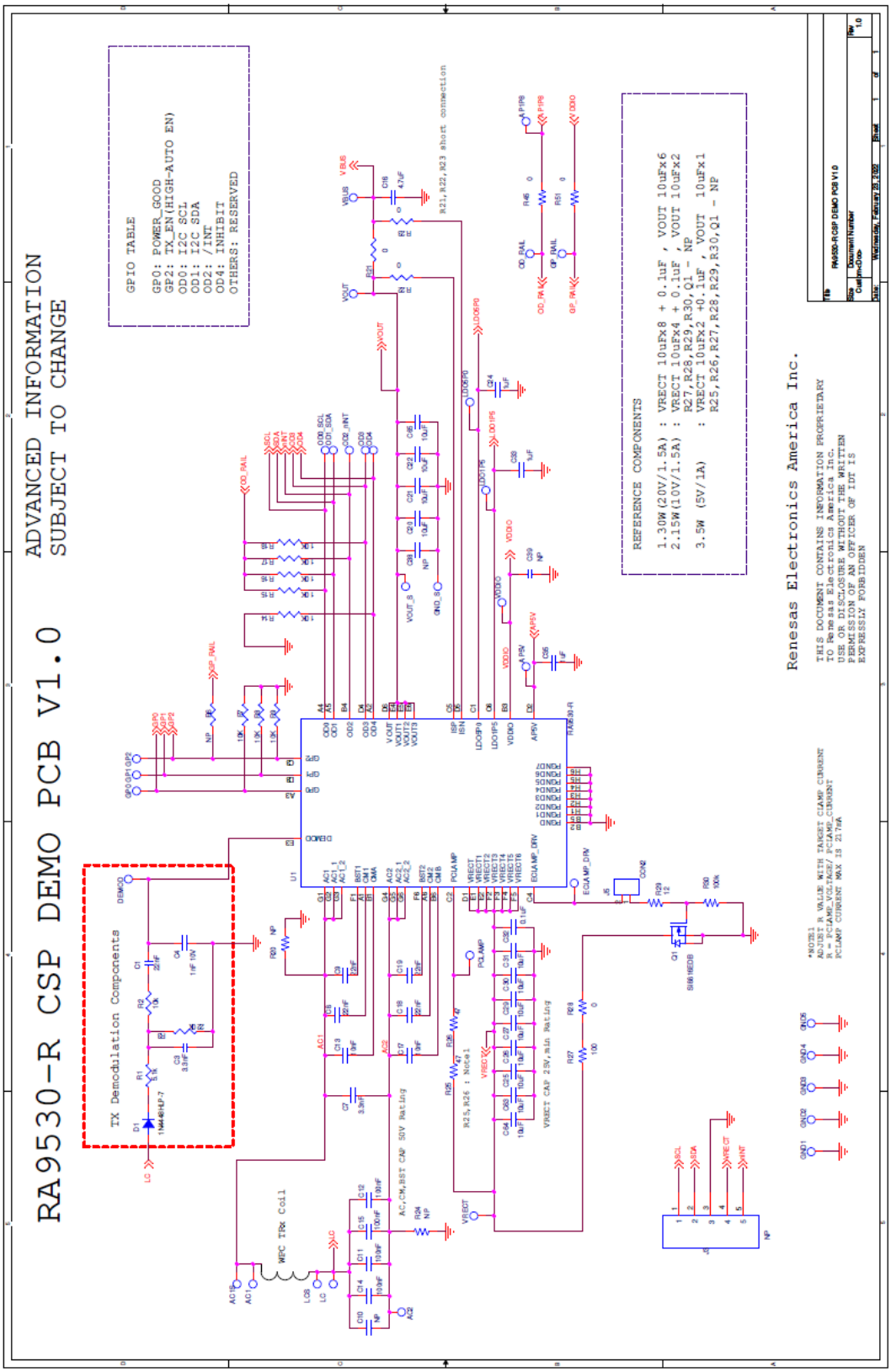
The RA9530 uses the standard I²C slave implementation protocol to communicate with a host Application Processor (AP) or other I2C peripherals. The I2C address is 0x3B.

The AP can write to only the registers that are marked as Read/Write (RW). Registers marked as Read Only (R) should never be sent a Write command. Likewise, register locations marked Reserved should not receive a Write command. When writing to a RW register that contains a combination of RW fields and reserved fields, a read-modify-write should be performed to the intended bit/field only. All other bits, including reserved bits should “not” be modified.

# 16. Board Design

This section contains board design information about the RA9530-R EVK demo board (Rev1.0).

## 16.1 Schematic Diagram



## 16.2 Bill of Materials

| Item | Qty | Reference | Part | PCB Footprint | Part Number |
|---|---|---|---|---|---|
| 1 | 2 | AC1,LC | NP | test_pt_sm_135x70 | NP |
| 2 | 3 | AC1S,AC2,LCS | NP | test_pt70_52d | 5010 |
| 3 | 10 | AP5V,LDO1P5,LDO5P0,VIN_OK,VDDIO,POI,INT_CP,EN_CP,CPOUT_S,AVDD | NP | tp_sm_45cir | NP |
| 4 | 5 | Reg18,AP1P8,OD_RAIL,GP_RAIL,PCLAMP | NP | test_pt70_52d | 5013 |
| 5 | 1 | CD_IN | 5013 | TEST_PT70_52D | 5013 |
| 6 | 4 | CFLYBT,CFLYBB,CFLYAT,CFLYAB | NP | tp_sm_45cir | SMD_Pad_Only |
| 7 | 7 | PGND1,GND1,GND2,VRECT,VOUT,VBUS,CPOUT | 5015 | test_pt_sm_135x70 | 5015 |
| 8 | 3 | C1,C8,C18 | 22nF | 402 | GRM155R71H223KA12D |
| 9 | 3 | C2,C5,C6 | NP | 402 | CL05B102JB5NNNC |
| 10 | 2 | C3,C7 | 3.3nF | 402 | CL05B332KB5NNNC |
| 11 | 1 | C4 | 1nF 10V | 201 | 100R05W102KV4T |
| 12 | 2 | C9,C19 | 22nF | 0402_typ | GRM155R71H223KA12D |
| 13 | 1 | C10 | NP | 402 | GRM155R61H104KE19D |
| 14 | 4 | C11,C12,C14,C15 | 100nF | 402 | GRM155R61H104KE19D |
| 15 | 2 | C13,C17 | 10nF | 402 | CGA2B3X5R1H103M050BB |
| 16 | 1 | C16 | 4.7uF | 603 | GRM188R6YA475KE15 |
| 17 | 12 | C20,C21,C22,C25,C26,C27,C29,C30,C31,C63,C64,C65 | 10uF | 0402_0603_0805 | GRM21BR6YA106KE43L |
| 18 | 1 | C23 | NP | 402 | GRM155C71A225KE11D |
| 19 | 3 | C24,C33,C35 | 1uF | 201 | GRM033C81A105ME05D |
| 20 | 3 | C34,C36,C37 | NP | 201 | GRM033C81A105ME05D |
| 21 | 1 | C28 | NP | cap_pol_3p5x2p8mm | T521T685M035APE090 |
| 22 | 2 | C52,C54 | 10uF | 603 | GRM188R6YA106MA73D |
| 23 | 2 | C32,C53 | 0.1uF | 201 | GRM033R6YA104KE14D |
| 24 | 1 | C38 | NP | 201 | GRM033R6YA104KE14D |

| Item | Qty | Reference | Part | PCB Footprint | Part Number |
|---|---|---|---|---|---|
| 25 | 1 | C39 | NP | 402 | GRM155R71H223KA12D |
| 26 | 2 | C40,C62 | NP | 603 | CL10A226MO7JZNC |
| 27 | 5 | C41,C42,C55,C58,C61 | 22uF 16V | 603 | CL10A226MO7JZNC |
| 28 | 6 | C43,C44,C51,C56,C59,C60 | 100nF 10V | 201 | CL03A104MP3NNNC |
| 29 | 1 | C45 | 4.7uF 35V | 603 | CL10A475KL8NRNC |
| 30 | 3 | C46,C47,C48 | 2.2uF 35V | 0402_typ | GRM155R6YA225ME1D |
| 31 | 1 | C49 | 100pF | 201 | GRM0335C1H101JA01D |
| 32 | 1 | C50 | NP | Cap_pol_2p0x1p25mm | T58W9105M035C0500 |
| 33 | 1 | C57 | 2.2uF | 201 | CL03A225MP3CRNC |
| 34 | 2 | ECLAMP_DRV,DEMOD | NP | test_pt70_52d | 5013 |
| 35 | 1 | D1 | DIODE | dfn1006_2ld_diode | 1N4448HLP-7 |
| 36 | 2 | D2,D3 | NP | 402 | ACPDQC24VE-HF |
| 37 | 2 | VOUT_S,GND_S | TP | test_pt70_52d | 61300111121 |
| 38 | 3 | GND3,GND4,GND5 | PTH_TP | test_pt70_52d | 5011 |
| 39 | 8 | OD1_SDA,GP1,OD2_nINT,GP2,OD3,OD4,OD0_SCL,GP0 | PTH_TP | tp_sm_45cir | NP |
| 40 | 1 | J1 | Header15 | Header15 | TSW-115-14-T-S |
| 41 | 1 | J2 | NP | jumper2pin01in | 68000-102HLF |
| 42 | 1 | J3 | NP | header_1x5_0p1Pitch60p42d | 901200765 |
| 43 | 1 | J4 | NP | molex_12pin_FPC_conn | 52207-1233 |
| 44 | 1 | J5 | CON2 | header_1x2_pitch50_28d | GRPB021VWVN-RC |
| 45 | 1 | J7 | HEADER 3 | header_1x3_0p1Pitch60p42d | 68000-203HLF |
| 46 | 2 | PGND2,PGND3 | NP | test_pt90_65d | 5011 |
| 47 | 1 | Q1 | Si8816EDB | BGA-4 | SI8816EDB-T2-E1 |
| 48 | 1 | R1 | 5.1k | 201 | ERJ-1GEJ512C |
| 49 | 1 | R2 | 10k | 201 | RC0201JR-0710KL |
| 50 | 1 | R3 | 220k | 402 | CRCW0402220KFKED |
| 51 | 8 | R4,R5,R6,R10,R11,R12,R13,R19 | NP | 402 | RC1005F103CS |
| 52 | 8 | R7,R8,R9,R14,R15,R16,R17,R18 | 10K | 402 | RC1005F103CS |

| Item | Qty | Reference | Part | PCB Footprint | Part Number |
|---|---|---|---|---|---|
| 53 | 2 | R20,R24 | NP | 402 | RC0402JR-07100KL |
| 54 | 1 | R21 | 0 | 603 | RC0603JR-070RL |
| 55 | 2 | R22,R23 | 0 | 402 | RC0402FR-070RL |
| 56 | 2 | R25,R26 | 47 | 805 | ERJ-P6WJ470V |
| 57 | 1 | R27 | 100 | 0402_0603_0805 | ERJ-P06J101V |
| 58 | 1 | R28 | 0 | 805 | RMCF0805ZT0R00 |
| 59 | 1 | R29 | 12 | 402 | RC0402JR-0712RL |
| 60 | 1 | R30 | 100K | 402 | RC0402JR-07100KL |
| 61 | 18 | R31,R32,R33,R34,R35,R36,R37,R38,R39,R40,R45,R51,R57,R58,R63,R64,R65,R66 | 0 | 402 | RMCF0402ZT0R00 |
| 62 | 6 | R42,R47,R67,R68,R69,R70 | NP | 402 | RMCF0402ZT0R00 |
| 63 | 6 | R41,R43,R44,R46,R48,R49 | NP | 402 | RC0402JR-130RL |
| 64 | 1 | R50 | NP | 201 | ERJ-1GEF10R0C |
| 65 | 3 | R52,R53,R54 | 220k | 201 | AC0201FR-07220KL |
| 66 | 2 | R55,R56 | NP | 603 | RMCF0603ZT0R00 |
| 67 | 2 | R59,R62 | NP | 402 | RMCF0402ZT0R00 |
| 68 | 2 | R60,R61 | 2.2k | 402 | CR0402-JW-222GLF |
| 69 | 1 | U1 | RA9530 | RA9530CSP | RA9530 |
| 70 | 1 | U2 | NP | SC70-5 | ISL9008AIECZ-T |
| 71 | 1 | U3 | NP | csp48_2p645x3p445_0p4mm | LN8282 |

## 16.3 Board Layout

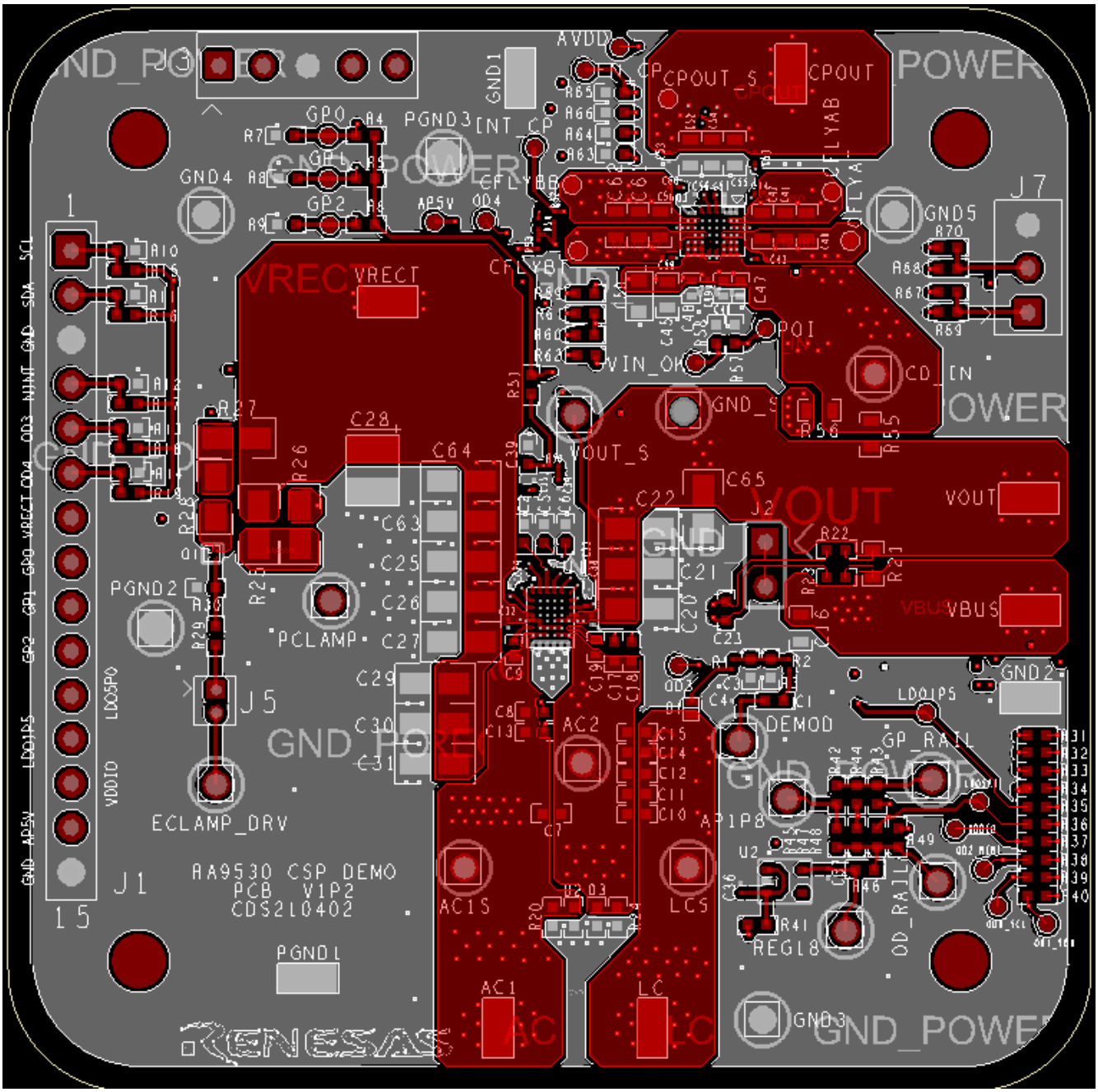



**Figure 37. Top and Top Silkscreen Layer**

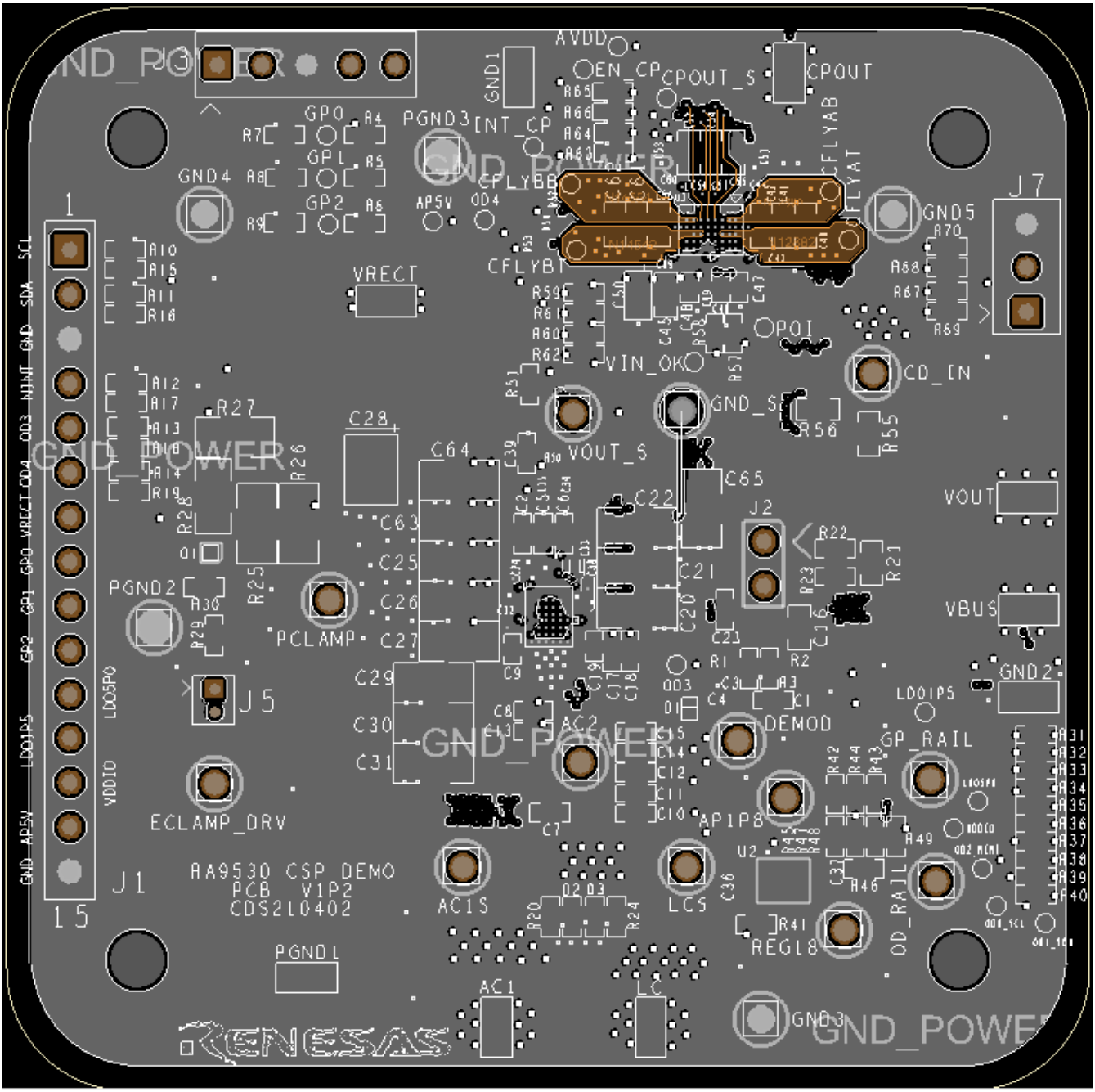



**Figure 38. Inner1 Layer (GND Layer)**

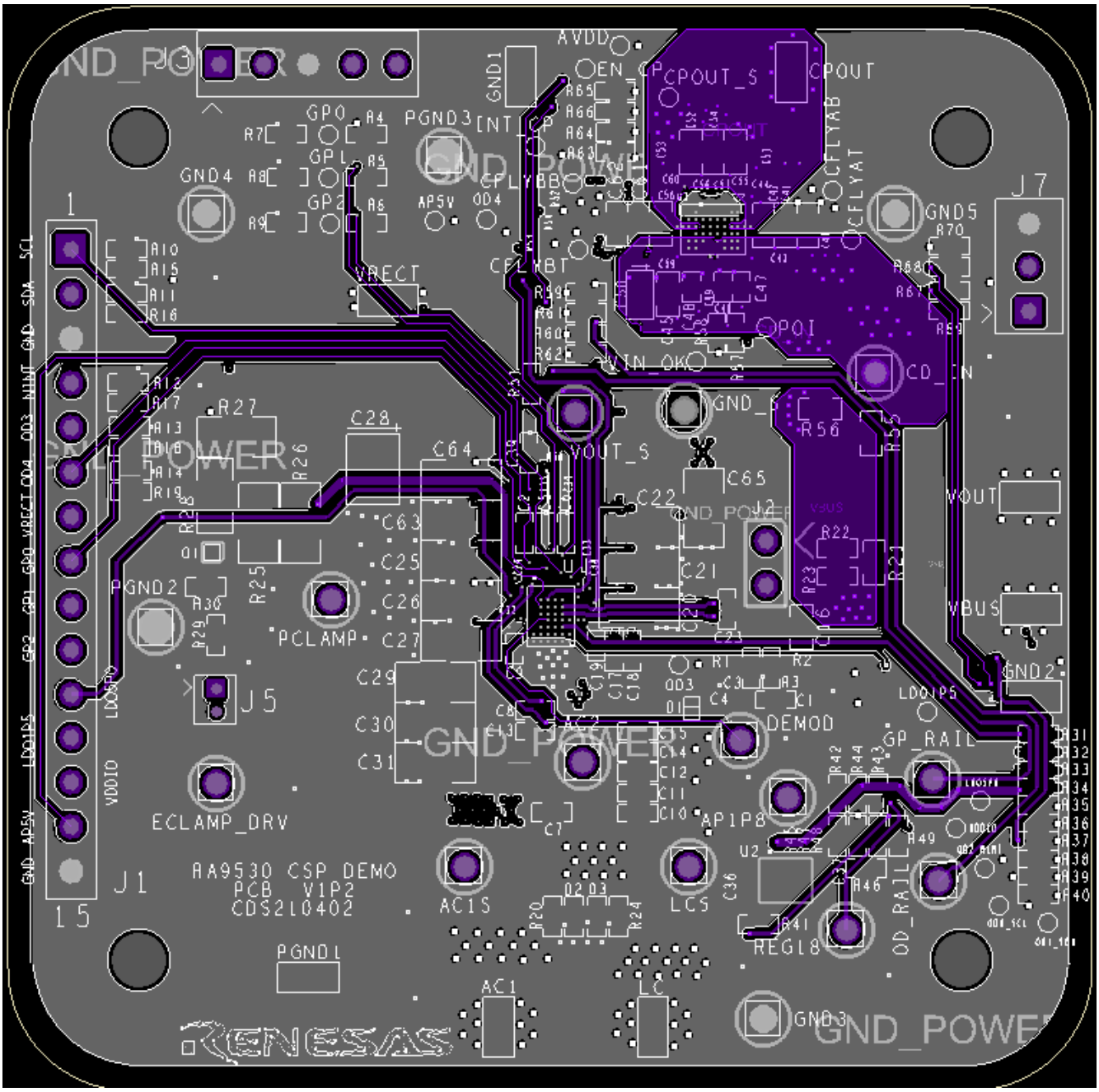



**Figure 39. Inner2 Layer (POWER/Signal/GND Layer)**

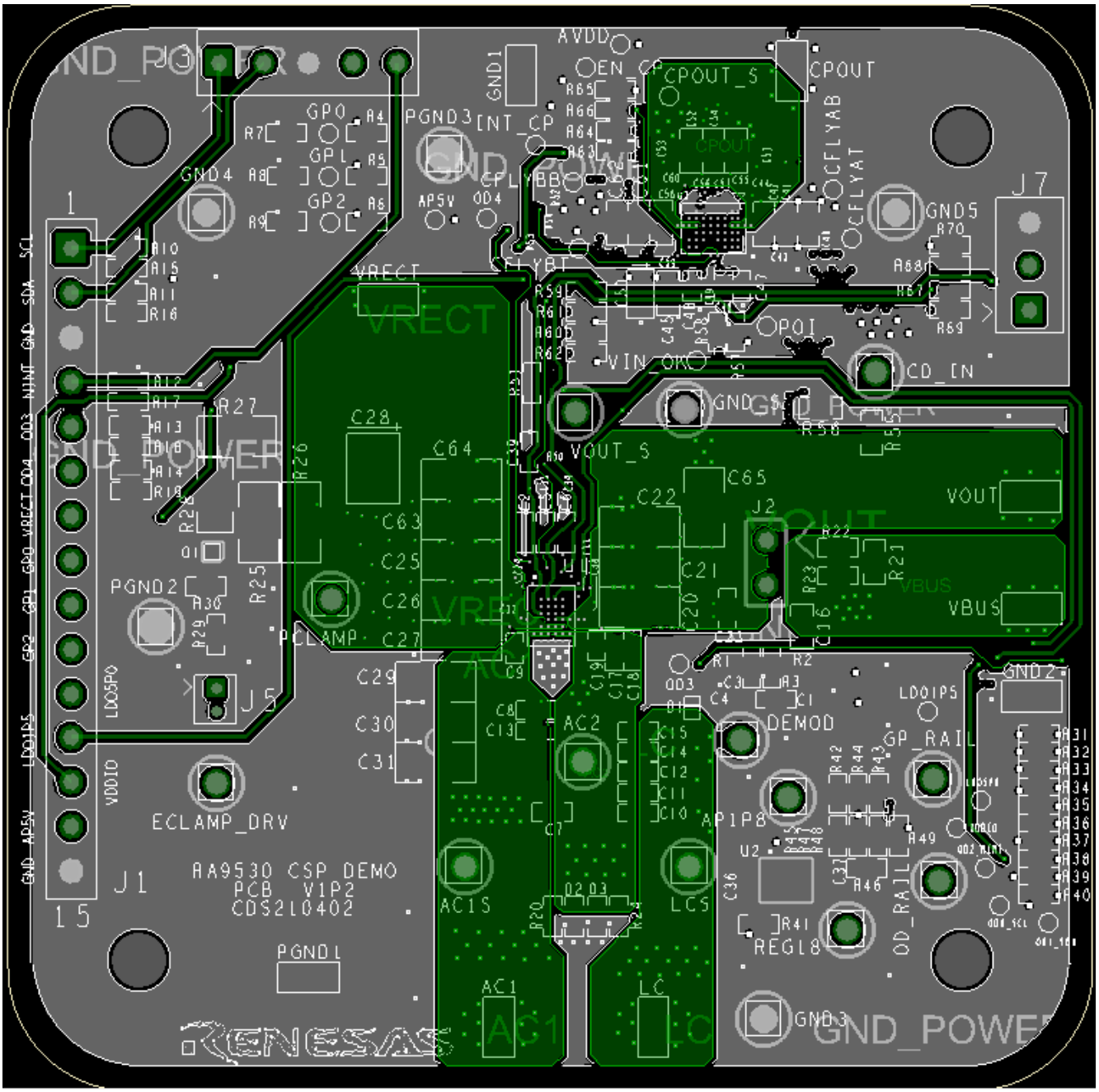



**Figure 40. Inner3 Layer (POWER/Signal/GND Layer)**

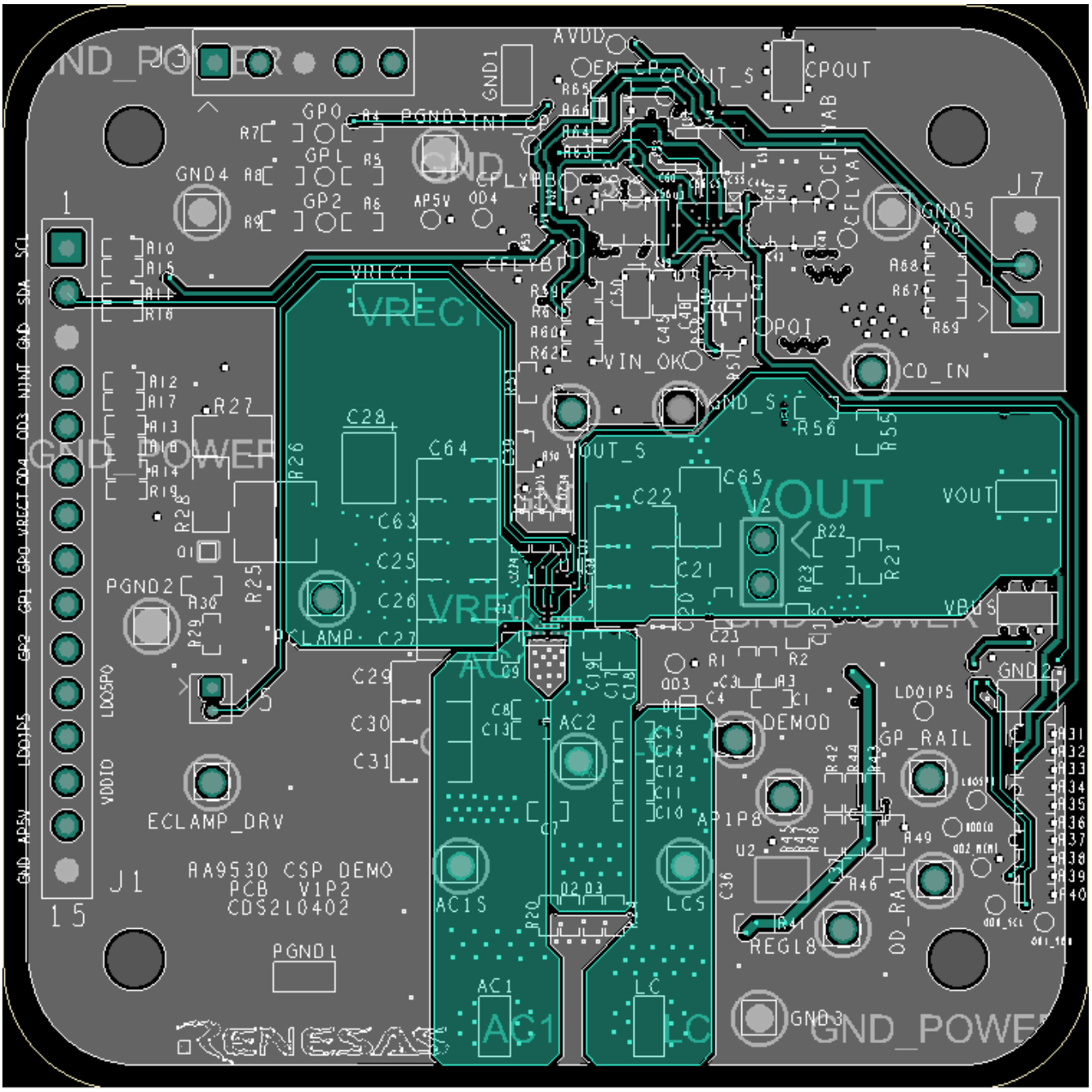



**Figure 41. Inner4 Layer (POWER/Signal/GND Layer)**

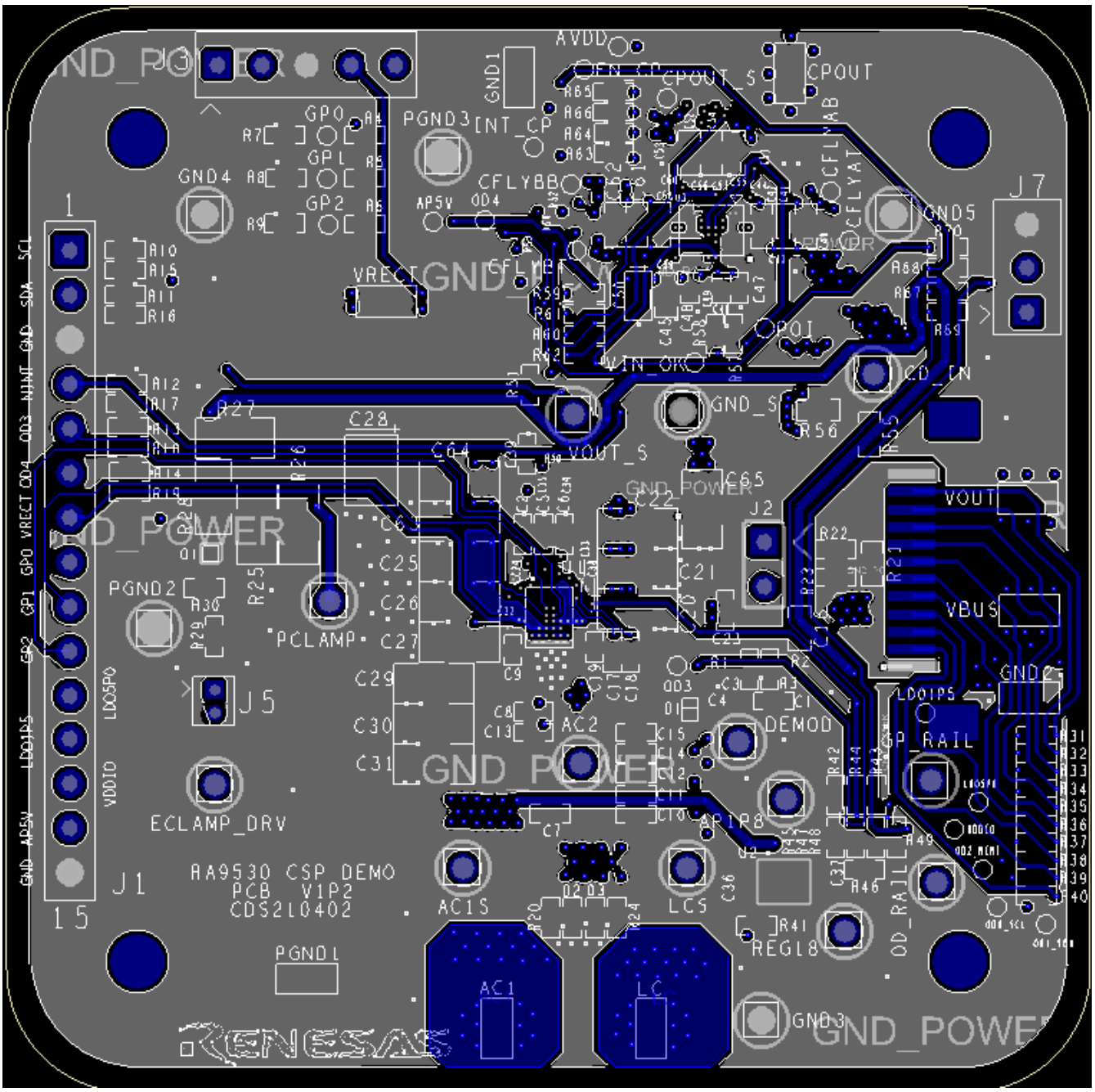



**Figure 42. Bottom Layer**

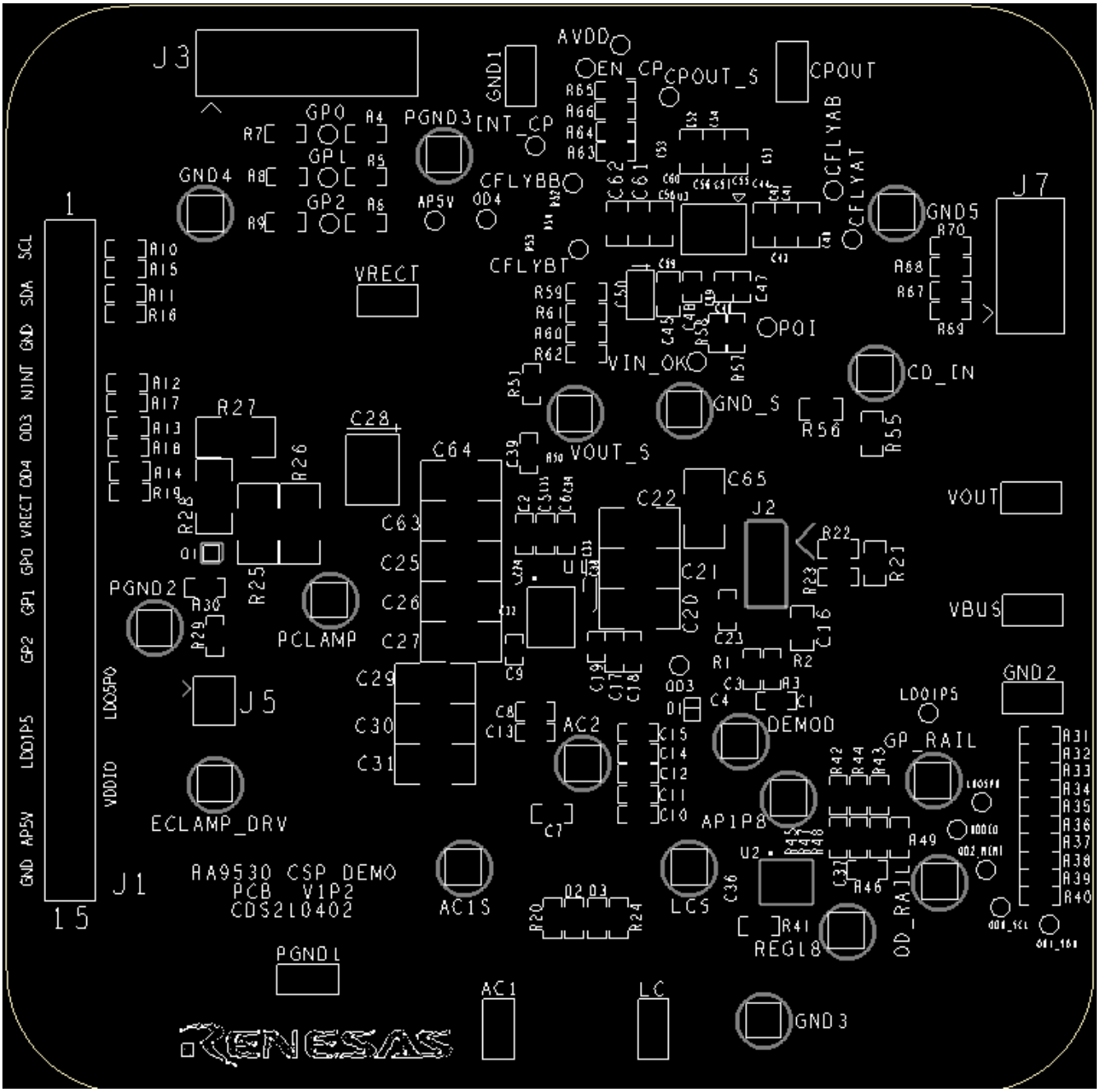



**Figure 43. Assembly Drawing**

# 17. Device Registers

The RA9530 uses the standard I2C slave implementation protocol to communicate with a host AP or other I2C peripherals. The communication protocol is implemented by using 8 bits for data and 16 bits for addresses. The default slave address of the RA9530 is 0x3B (high 7 bits).

When writing to the device, care should be taken to only write to registers marked exclusively as Read/Write (RW). Registers marked as Read Only (R) should never be sent a Write command or unexpected behavior may occur. In addition, register locations marked Reserved should not receive a Write command. When writing to a RW register that contains a combination of RW fields and reserved fields, a read-modify-write should be performed to the intended bit/field only. All other bits/field, including reserved bits/fields, should “not” be modified.

The following section contains a comprehensive list of address locations, field names, available operations (R or RW), default values, and functional descriptions of all internally accessible registers contained within the device.

## 17.1 Common Registers

### 17.1.1. Chip Type (0x0000, 16-Bit)

| Bit | Field Name | RW | Default Value | Description |
|---|---|---|---|---|
| 15:0 | Chip Type | R | 0x9530 | Chip ID byte |

### 17.1.2. Hardware Revision (0x0002, 8-Bit)

| Bit | Field Name | RW | Default Value | Description |
|---|---|---|---|---|
| 7:0 | HW Rev | R | 0x02 | Hardware revision |

### 17.1.3. Customer Code (0x0003, 8-Bit)

| Bit | Field Name | RW | Default Value | Description |
|---|---|---|---|---|
| 7:0 | Customer Code | R | 0x00 | Customer Code |

### 17.1.4. Firmware Beta Revision (0x0017, 8-Bit)

| Bit | Field Name | RW | Default Value | Description |
|---|---|---|---|---|
| 7:0 | FW Beta Rev | RW | - | FW Beta Revision for Debug releases |

### 17.1.5. Firmware Minor Revision (0x001C, 16-Bit)

| Bit | Field Name | RW | Default Value | Description |
|---|---|---|---|---|
| 15:0 | FW Minor Rev | RW | - | Minor revision of firmware |

### 17.1.6. Firmware Major Revision (0x001E, 16-Bit)

| Bit | Field Name | RW | Default Value | Description |
|---|---|---|---|---|
| 15:0 | FW Major Rev | RW | - | Major revision of firmware |

### 17.1.7. WPC Manufacturer ID (0x004A, 16-Bit)

| Bit | Field Name | RW | Default Value | Description |
|---|---|---|---|---|
| 15:0 | WPC Manufacturer ID | R | - | WPC Manufacturer ID |

The following table shows the WPC specified table for the packet that is being sent by Rx during ID and Configuration phase.

<table>
<tr><th></th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr>
<tr><td>B0</td><td colspan="4">Major Version</td><td colspan="4">Minor Version</td></tr>
<tr><td>B1</td><td colspan="8">(msb)</td></tr>
<tr><td>B2</td><td colspan="7">Manufacturer Code</td><td>(lsb)</td></tr>
<tr><td>B3</td><td>Ext</td><td colspan="7" rowspan="3">(msb)<br>Basic Device Identifier<br>(lsb)</td></tr>
<tr><td>…</td><td rowspan="2"></td></tr>
<tr><td>B6</td></tr>
</table>

## 17.1.8. Firmware Date Code (0x00C4 - 0x00CF, 12 Bytes)

| Address | Field Name | RW | Default Value | Description |
|---|---|---|---|---|
| 0xCF | FW Date Code [96:88] | RW | - | Date Code of firmware in NVM Data Encoding Format: ASCII code E.g.,) Dec 10 2015(11:53:41) |
| 0xCE | FW Date Code [87:80] | RW | - | |
| 0xCD | FW Date Code [79:72] | RW | - | |
| 0xCC | FW Date Code [71:64] | RW | - | |
| 0xCB | FW Date Code [63:56] | RW | - | |
| 0xCA | FW Date Code [55:48] | RW | - | |
| 0xC9 | FW Date Code [47:40] | RW | - | |
| 0xC8 | FW Date Code [39:32] | RW | - | |
| 0xC7 | FW Date Code [31:24] | RW | - | |
| 0xC6 | FW Date Code [23:16] | RW | - | |
| 0xC5 | FW Date Code [15:8] | RW | - | |
| 0xC4 | FW Date Code [7:0] | RW | - | |

| Register | Value | ASCII |
|---|---|---|
| 0xCF | 00 | Null |
| 0xCE | 35 | 5 |
| 0xCD | 31 | 1 |
| 0xCC | 30 | 0 |
| 0xCB | 32 | 2 |
| 0xCA | 20 | Space |
| 0xC9 | 30 | 0 |
| 0xC8 | 31 | 1 |
| 0xC7 | 20 | Space |
| 0xC6 | 63 | c |
| 0xC5 | 65 | e |
| 0xC4 | 44 | D |

### 17.1.9. Firmware Time Code (0x00D4 - 0x00DB, 8 Bytes)

| Address | Field Name | RW | Default Value | Description |
|---|---|---|---|---|
| 0xDB | FW Time Code [55:48] | RW | - | Time Code of firmware in NVM Data Encoding Format: ASCII code Ex: Dec 10 2015(11:53:41) |
| 0xDA | FW Time Code [47:40] | RW | - | |
| 0xD9 | FW Time Code [39:32] | RW | - | |
| 0xD8 | FW Time Code [31:24] | RW | - | |
| 0xD7 | FW Time Code [15:8] | RW | - | |
| 0xD6 | FW Time Code [23:16] | RW | - | |
| 0xD5 | FW Time Code [13:8] | RW | - | |
| 0XD4 | FW Time Code [7:0] | RW | - | |

| Register | Value | ASCII |
|---|---|---|
| 0xDB | 31 | 1 |
| 0xDA | 34 | 4 |
| 0xD9 | 3A | : |
| 0xD8 | 33 | 3 |
| 0xD7 | 35 | 5 |
| 0xD6 | 3A | : |
| 0xD5 | 31 | 1 |
| 0xD4 | 31 | 1 |

### 17.1.10. System Operating Mode Register (0x004D, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | System Mode | RX | R | - | 0x80 – Back Powered, Indication that the chip is powered by VRECT or VOUT, but TX function is not enabled<br>0x09 – Extended WPC<br>Mode 0x04 – TRx Mode<br>0x01 – Basic WPC Mode<br>0x00 – AC Missing Mode<br>Rest all values are Reserved |

## 17.2 RX Mode Registers

### 17.2.1. System Interrupt Clear Register in RX Mode (0x0028 - 0x002B, 32-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 31 | ADT Error | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 30 | ADT Received | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 29 | ADT Sent | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 28 | RX EPP | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 27 | Reserved | - | - | - | Reserved |
| 26 | VRECT ON | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 25 | No I2C data Timeout | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 24:23 | Reserved | - | - | - | Reserved |
| 22 | BPP/EPP Check | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 21 | Power Loss OTP | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 20 | Over Current Fault | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 19 | Re-negotiation Fail | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 18 | Re-negotiation Success | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 17 | RPP Read | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 16 | AP 5V Disable | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 15 | Fast Charging Failure | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 14 | Sleep Mode | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 13 | ID Authentication Success | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 12 | ID Authentication Failure | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 11 | Back Channel Success | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 10 | Back Channel Timeout | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 9 | TX Authentication Success | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 8 | TX Authentication Failure | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 7 | LDO Disable | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 6 | LDO Enable | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 5 | Operation Mode Change | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 4 | TX Data Receive | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 3 | Fast Charging Success | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 2 | Over Temperature | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 1 | Over Voltage | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 0 | Over Current | RX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |

### 17.2.2. System Status Register in RX Mode (0x002C - 0x002F, 32-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 31 | ADT Error | RX | R | - | 1 = ADT error occurs |
| 30 | ADT Received | RX | R | - | 1 = ADT received |
| 29 | ADT Sent | RX | R | - | 1 = ADT sends |
| 28 | RX EPP | RX | R | - | 1 = Send RPP in EPP mode |
| 27 | Reserved | - | - | - | Reserved |
| 26 | VRECT ON | RX | R | - | 1 = AC power is applied. The flag is set before the Configuration Packet. It is cleared on system reset or when power is removed. Interrupt event is generated on SET event |
| 25 | No I2C data Timeout | RX | RW | - | 1 = No I2C data function timeout |

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 24:23 | Reserved | - | - | - | Reserved |
| 22 | BPP/EPP Check | RX | R | - | 1 = BPP/EPP check |
| 21 | Power Loss OTP | RX | R | - | 1 = Power Loss condition |
| 20 | Over Current Fault | RX | R | - | 1 = Iout is close to Ilim value |
| 19 | Re-negotiation Fail | RX | R | - | 1 = Renegotiation is failed. |
| 18 | Re-negotiation Success | RX | R | - | 1 = Renegotiation is successful |
| 17 | RPP Read | RX | R | - | 1 = Out of band communication is successful |
| 16 | AP 5V Disable | RX | R | - | 1 = AP5V is disabled |
| 15 | Fast Charging Failure | RX | R | - | 1 = Fast Charging condition is failed |
| 14 | Sleep Mode | RX | R | - | 1 = Rx is in sleep mode |
| 13 | ID Authentication Success | RX | R | - | 1 = ID authentication is passed |
| 12 | ID Authentication Failure | RX | R | - | 1 = ID authentication is failed |
| 11 | Back Channel Success | RX | R | - | 1 = Backchannel packet is received by Tx |
| 10 | Back Channel Timeout | RX | R | - | 1 = Backchannel packet is sending failed |
| 9 | TX Authentication Success | RX | R | - | 1 = Device authentication is passed |
| 8 | TX Authentication Failure | RX | R | - | 1 = Device authentication is failed |
| 7 | LDO Disable | RX | R | - | 1 = LDO is disabled |
| 6 | LDO Enable | RX | R | - | 1 = LDO is enabled |
| 5 | Operation Mode Change | RX | R | - | 1 = Operating mode is changed |
| 4 | TX Data Receive | RX | R | - | 1 = Proprietary packet from Tx is received |
| 3 | Fast Charging Success | RX | R | - | 1 = Fast Charging is successful |
| 2 | Over Temperature | RX | R | - | 1 = Over Temperature condition |

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 1 | Over Voltage | RX | R | - | 1 = Over Voltage condition |
| 0 | Over Current | RX | R | - | 1 = Over Current Error condition |

### 17.2.3. System Interrupt Register in RX Mode (0x0030 - 0x0033, 32-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 31 | ADT Error | RX | R | 0 | 1 = ADT error happens.<br>0 = No such condition exists |
| 30 | ADT Received | RX | R | 0 | 1 = ADT is received.<br>0 = No such condition exists |
| 29 | ADT Sent | RX | R | 0 | 1 = ADT is sent<br>0 = No such condition exists |
| 28 | RX EPP | RX | R | 0 | 1 = Send RPP in EPP mode<br>0 = No such condition exists |
| 27 | Reserved | - | - | 0 | Reserved |
| 26 | VRECT ON | RX | R | 0 | 1 = AC power is applied. The flag is set before the Configuration Packet. It is cleared on system reset or when power is removed. Interrupt event is generated on SET event<br>0 = No such condition exists |
| 25 | No I2C data Timeout | RX | RW | 0 | 1 = No I2C data function timeout 0 = No such condition exists |
| 24:23 | Reserved | - | - | 0 | Reserved |
| 22 | BPP/EPP Check | RX | R | 0 | 1 = BPP/EPP Check<br>0 = No such condition exists |
| 21 | Power Loss OTP | RX | R | 0 | 1 = Power Loss condition<br>0 = No such condition exists |
| 20 | Over Current Fault | RX | R | 0 | 1 = Iout is close to Ilim value<br>0 = No such condition exists |
| 19 | Re-negotiation Fail | RX | R | 0 | 1 = Re-negotiation is failed<br>0 = No such condition exists |
| 18 | Re-negotiation Success | RX | R | 0 | 1 = Re-negotiation is successful<br>0 = No such condition exists |
| 17 | RPP Read | RX | R | 0 | 1 = Out of band communication is successful<br>0 = No such condition exists |
| 16 | AP 5V Disable | RX | R | 0 | 1 = AP5V is disabled<br>0 = No such condition exists |
| 15 | Fast Charging Failure | RX | R | 0 | 1 = Fast Charging command is failed 0 = No such condition exists |

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 14 | Sleep Mode | RX | R | 0 | 1 = Rx is in sleep mode<br>0 = No such condition exists |
| 13 | ID Authentication Success | RX | R | 0 | 1 = ID authentication is passed<br>0 = No such condition exists |
| 12 | ID Authentication Failure | RX | R | 0 | 1 = ID authentication is failed<br>0 = No such condition exists |
| 11 | Back Channel Success | RX | R | 0 | 1 = Backchannel packet is received by Tx<br>0 = No such condition exists |
| 10 | Back Channel Timeout | RX | R | 0 | 1 = Backchannel packet is sending failed<br>0 = No such condition exists |
| 9 | TX Authentication Success | RX | R | 0 | 1 = Device authentication is passed<br>0 = No such condition exists |
| 8 | TX Authentication Failure | RX | R | 0 | 1 = Device authentication is failed<br>0 = No such condition exists |
| 7 | LDO Disable | RX | R | 0 | 1 = LDO is disabled<br>0 = No such condition exists |
| 6 | LDO Enable | RX | R | 0 | 1 = LDO is enabled<br>0 = No such condition exists |
| 5 | Operation Mode Change | RX | R | 0 | 1 = Operating mode is changed<br>0 = No such condition exists |
| 4 | TX Data Receive | RX | R | 0 | 1 = Proprietary packet from Tx is received<br>0 = No such condition exists |
| 3 | Fast Charging Success | RX | R | 0 | 1 = Fast Charging is successful<br>0 = No such condition exists |
| 2 | Over Temperature | RX | R | 0 | 1 = Over Temperature condition<br>0 = No such condition exists |
| 1 | Over Voltage | RX | R | 0 | 1 = Over Voltage condition<br>0 = No such condition exists |
| 0 | Over Current | RX | R | 0 | 1 = Over Current Error condition<br>0 = No such condition exists |

### 17.2.4. System Interrupt Enable Register in RX Mode (0x0034 - 0x0037, 32-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 31 | ADT Error | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 30 | ADT Received | RX | RW | 1 | 1 = Corresponding interrupt is enabled |
| | | | | | 0 = Corresponding interrupt is disabled |
| 29 | ADT Sent | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 28 | RX EPP | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 27 | Reserved | - | - | - | Reserved |
| 26 | VRECT ON | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 25 | No I2C data Timeout | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 24:23 | Reserved | - | - | - | Reserved |
| 22 | BPP/EPP Check | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 21 | Power Loss OTP | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 20 | Over Current Fault | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 19 | Re-negotiation Fail | RX | R | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 18 | Re-negotiation Success | RX | R | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 17 | RPP Read | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 16 | AP 5V Disable | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 15 | Voltage Switch Failure | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 14 | Sleep Mode | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 13 | ID Authentication Success | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 12 | ID Authentication Failure | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 11 | Back Channel Success | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 10 | Back Channel Timeout | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 9 | TX Authentication Success | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 8 | TX Authentication Failure | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 7 | LDO Disable | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 6 | LDO Enable | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 5 | Operation Mode Change | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 4 | TX Data Receive | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 3 | Fast Charging Success | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 2 | Over Temperature | RX | RW | 1 | 1 = Corresponding interrupt is enabled 0 = Corresponding interrupt is disabled |
| 1 | Over Voltage | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 0 | Over Current | RX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |

### 17.2.5. Battery Charge Status Register (0x003A, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | Charge Status | RX | RW | 0x00 | In RX mode the AP writes this register with the value intended to be sent as payload to the Charge Status Packet. The FW does not verify or modify the value in any way.<br>The value should be filled based on the following: 0x0 = Reserved<br>0x1 = Charge status packet sent with parameter = 1 (1%) 0x2 - Charge status packet send with parameter = 2 (2%)<br>…<br>0x64 - Charge status packet send with parameter = 100 (100%)<br>0x65 ~ 0xFE : Reserved<br>0xFF - No Battery Charge Device or Not Providing Charge Status Packet |

*Note*: After writing to this register, Send Charge Status bit of Command Register (0x4E) needs to be set for transmission to begin.

### 17.2.6. End of Power Transfer Register in RX Mode (0x003B, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | EPT/EOC/EOP Reason | RX | RW | 0x00 | In RX mode the AP writes this register with the value intended to be sent as payload to the Charge Status Packet. The FW does not verify or modify the value in any way.<br>A WPC End of Power Transfer packet/message will be sent with the following definition:<br>0 = WPC mode, unknown<br>1 = WPC mode, Charge Complete<br>2 = WPC mode, Internal Fault<br>3 = WPC mode, Over Temperature<br>4 = WPC mode, Over Voltage<br>5 = WPC mode, Over Current<br>6 = WPC mode, Battery Failure<br>7 = WPC mode, Re-Configuration<br>8 = WPC mode, No Response<br>10 = WPC mode, Negotiation Failure<br>11 = WPC mode, Restart Power<br>All other values are reserved. |

*Note*: After writing to this register, Send EPT bit of Command Register (0x4E) needs to be set for transmission to begin.

### 17.2.7. Vout ADC Reading (0x003C, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | VoutAdc | RX | R | 0x00 | Vout uncompensated raw ADC reading. Scaled as 12-bit number for 21V full scale. |

### 17.2.8. Vout Set Register (0x003E, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | VOutSet | RX | RW | 0x00DE (BPP)<br>0x02D7 (EPP) | Main LDO Vout set value.<br>When default Vout is changed by AP through this register, target Vrect will be automatically adjusted (by Internal MCU).<br>VoutSet = ((Vout (mV) -2800)*10/99) |

### 17.2.9. Vrect ADC Reading (0x0040, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | VrectAdc | RX | R | – | Vrect uncompensated raw ADC reading. Scaled as 12-bit number for 25.2V full scale. |

### 17.2.10. Iout Value Register (0x0044, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | IOut | RX | R | - | RX mode IOut value. |

### 17.2.11. System Command Register (0x004E, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15 | Renegotiation | RX | W | 0 | AP sets 1 to generate renegotiation |
| 14:10 | Reserved | - | - | 0 | Reserved |
| 9 | Send WPC1P3 Data Packet | RX | W | 0 | AP sets 1 to generate WPC 1.3 data packet transfer |
| 8 | Soft Restart | RX | W | 0 | AP sets 1 to turn off and restart LDO<br>Chip clears the bit after processing the command |
| 7 | Fast Charging | RX | W | 0 | AP sets 1 to switch the Voltage to fast charging<br>Chip clears the bit after processing the command |
| 6 | Reserved | - | - | 0 | Reserved |
| 5 | Clear Interrupt | RX | W | 0 | AP sets 1 to send Clear Interrupt command<br>Chip clears the bit after processing the command |
| 4 | Send Charge Status | RX | W | 0 | AP sets 1 to send Charge Status packet in RX mode<br>Chip clears the bit after processing the command |
| 3 | Send End of Power | RX | W | 0 | AP sets 1 to send End of Power Transfer Packet in RX mode<br>Chip clears the bit after processing the command |
| 2 | Send Device Authentication | RX | W | 0 | AP sets 1 to send Device Authentication<br>Chip clears the bit after processing the command |
| 1 | Reserved | - | - | 0 | Reserved |
| 0 | Send PROP | RX | W | 0 | AP sets 1 to send proprietary packet<br>Chip clears the bit after processing the command |

*Note*: It costs time to implement the command. AP could write new command to System Command Register 3~5ms after the previous command.

### 17.2.12. Proprietary Data-Out Registers (0x0050 - 0x0057, 8 Bytes)

| Address | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 0x0057 | Prop Data 7 | RX | RW | 0x00 | Byte 6 of Proprietary packet data |
| 0x0056 | Prop Data 6 | RX | RW | 0x00 | Byte 5 of Proprietary packet data |
| 0x0055 | Prop Data 5 | RX | RW | 0x00 | Byte 4 of Proprietary packet data |
| 0x0054 | Prop Data 4 | RX | RW | 0x00 | Byte 3 of Proprietary packet data |
| 0x0053 | Prop Data 3 | RX | RW | 0x00 | Byte 2 of Proprietary packet data |
| 0x0052 | Prop Data 2 | RX | RW | 0x00 | Byte 1 of Proprietary packet data |
| 0x0051 | Prop Data 1 | RX | RW | 0x00 | Byte 0 of Proprietary packet data |
| 0x0050 | Proprietary Header | RX | RW | 0x00 | Proprietary Packet Header. Allows up to 7 bytes to be included in the proprietary packet |

### 17.2.13. Proprietary Data-In Registers (0x0058 - 0x005F, 8 Bytes)

| Address | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 0x005F | Prop Data 7 | RX | RW | 0x00 | Byte 6 of Proprietary packet data |
| 0x005E | Prop Data 6 | RX | RW | 0x00 | Byte 5 of Proprietary packet data |
| 0x005D | Prop Data 5 | RX | RW | 0x00 | Byte 4 of Proprietary packet data |
| 0x005C | Prop Data 4 | RX | RW | 0x00 | Byte 3 of Proprietary packet data |
| 0x005B | Prop Data 3 | RX | RW | 0x00 | Byte 2 of Proprietary packet data |
| 0x005A | Prop Data 2 | RX | RW | 0x00 | Byte 1 of Proprietary packet data |
| 0x0059 | Prop Data 1 | RX | RW | 0x00 | Byte 0 of Proprietary packet data |
| 0x0058 | Proprietary Header | RX | RW | 0x00 | Proprietary Packet Header. Allows up to 7 bytes to be included in the Proprietary packet |

### 17.2.14. ILIM Register (0x0060, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | ILim Set | RX | RW | 0x09 | Main LDO output current limit (by which LDO will behave as a constant current source) set value. 200 mA step ILim Set = (ILim Value (mA) / 200) – 1<br>Example: if ILIM value is 2A, then the ILIM Set would be 0x09 |

*Note*: This register is not recommended to do change. Alternatively, the

### 17.2.15. Over Voltage Register (0x0061, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | OV Clamp Voltage | RX | RW | 0x04 (BPP) 0x01 (EPP) | 0x00 = 18V<br>0x01 = 21V<br>0x02 = 16.7V<br>0x03 = 14.7V<br>0x04 = 13V<br>0x05 = 23.4V<br>0x06 = 24.7V<br>0x07 = 26V<br>0x08 = 27V<br>0x09 = 28V<br>0x0A = 29V<br>0x0B = 30V<br>0x0C = 31V<br>0x0D = 32V<br>0x0E = 33V<br>0x0F = 34.3V |

*Note*: This register could be set only when chip works in non-autoOV mode. And this register should be used with extreme caution.

### 17.2.16. Reference Resonance Frequency Register (0x0065, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | Reference Resonance Frequency | RX | RW | 0x76 | Reference Resonance Frequency which is included in FOD/rf packet.<br>A value of zero corresponds to a Reference Resonance Frequency in the range of 35.75kHz up to (but not including) 36.25kHz; and a value of 255 corresponds to a Reference Resonance Frequency in the range of 163.25 up to (but not including) 163.75kHz. |

### 17.2.17. RX Mode Communication Modulation FET Register (0x0067, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | Com Mod Cap Settings | RX | RW | 0x00 | Modulation Channel Settings: (0b – Disable, 1b – Enable)<br>BIT4: CMA BIT5: CMB BIT6: COM1 BIT7: COM2<br>Value – 0x00: Auto set Modulation Capacitors according to VOutset Value |

### 17.2.18. FOD Registers (0x0068 - 0x0077, 16 Bytes)

The FOD registers are divided into eight pairs. Each pair has one byte for gain setting and one byte for offset setting. The first six pairs control the Received Power calculation for six power sectors during the Power Transfer phase. The seventh pair calibrates the internal DC Load. The set values of the FOD registers are found with the help of a Renesas developed calibration procedure using the nok9 tester.

The firmware initializes the FOD registers according to work mode (BPP/EPP). The correct set is loaded at completion of the ID and Configuration Phase. The AP can modify the registers at any time if needed to update the values.

| Address and Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 0x0077 | Offset_7 | RX | RW | 0x48 | FOD coefficients for Power Region 7: Offset Settings |
| 0x0076 | Gain_7 | RX | RW | 0x80 | FOD coefficients for Power Region 7: Gain (slope settings) |
| 0x0075 | Offset_6 | RX | RW | 0x41 | FOD coefficients for Power Region 6: Offset Settings |
| 0x0074 | Gain_6 | RX | RW | 0xA5 | FOD coefficients for Power Region 6: Gain (slope settings) |
| 0x0073 | Offset_5 | RX | RW | 0x20 | FOD coefficients for Power Region 5: Offset Settings |
| 0x0072 | Gain_5 | RX | RW | 0x93 | FOD coefficients for Power Region 5: Gain (slope settings) |
| 0x0071 | Offset_4 | RX | RW | 0x45 | FOD coefficients for Power Region 4: Offset Settings |
| 0x0070 | Gain_4 | RX | RW | 0x8F | FOD coefficients for Power Region 4: Gain (slope settings) |
| 0x006F | Offset_3 | RX | RW | 0x54 | FOD coefficients for Power Region 3: Offset Settings |
| 0x006E | Gain_3 | RX | RW | 0x8F | FOD coefficients for Power Region 3: Gain (slope settings) |
| 0x006D | Offset_2 | RX | RW | 0x48 | FOD coefficients for Power Region 2: Offset Settings |
| 0x006C | Gain_2 | RX | RW | 0x91 | FOD coefficients for Power Region 2: Gain (slope settings) |
| 0x006B | Offset_1 | RX | RW | 0x59 | FOD coefficients for Power Region 1 = Offset Settings |
| 0x006A | Gain_1 | RX | RW | 0x96 | FOD coefficients for Power Region 1 = Gain (slope settings) |
| 0x0069 | Offset_0 | RX | RW | 0x59 | FOD coefficients for Power Region 0 = Offset Settings |
| 0x0068 | Gain_0 | RX | RW | 0x96 | FOD coefficients for Power Region 0 = Gain (slope settings) |

### 17.2.19. Fast Charging Voltage Register (0x0078, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Fast Charging Voltage | RX | RW | 0x0000 | Fast Charging Voltage in mV |

### 17.2.20. Vout Value Register (0x0080, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | VOut | RX | R | - | Current VOut voltage value in mV in RX mode |

### 17.2.21. Vrect Value Register (0x0082, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Vrect | RX | R | - | Current Vrect Voltage value in mV |

### 17.2.22. Die Temperature Value Register (0x0084, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | DIE Temperature in degrees Celsius | RX | R | - | Current Die Temperature value in degrees Celsius. |

### 17.2.23. Operating Frequency Register (0x0086, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Operating Frequency | RX | R | - | Current operating frequency of the AC signal frequency in kHz. |

### 17.2.24. Digital Ping Frequency Register (0x0088, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Ping Frequency | RX | R | - | Digital Ping Frequency of the AC signal (kHz) in RX mode |

### 17.2.25. CEP Value Register (0x00A5, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | CEPValue | RX | R | - | 8-bit signed number representing the last CEP value sent in Rx mode. |

### 17.2.26. Tx Manufacturer Code Register (0x00B0, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | mpTxManufCode | RX | R | - | Tx Manufacturer code which is loaded from GETIDREQ packet in negotiation phase. |

### 17.2.27. TX Guaranteed Power Register (0x00B3, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Tx Guaranteed Power | RX | R | - | TX Guaranteed Power |

### 17.2.28. TX WPC Revision ID Register (0x00B6, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | Tx Revision | RX | R | - | Tx WPC Revision ID |

### 17.2.29. Re-Negotiation Status Register (0x00B7, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:3 | Reserved | RX | R | 0x00 | Reserved |
| 2 | Renegotiation Error | RX | RW | 0 | Re-Negotiation phase is completed but error or NAK is met. |
| 1 | Renegotiation Done | RX | RW | 0 | Re-Negotiation phase is completed without error. |
| 0 | TX Capability Require | RX | RW | 0 | Request to send General Request Capabilities Packet during Re-Negotiation phase. This bit is self-cleared upon exit from the phase. |

### 17.2.30. Current Guaranteed Power (0x00B9, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | MpCur.GP | RX | R | 0x1E | Guaranteed Power Value in current power contract. |

### 17.2.31. Request Guaranteed Power (0x00BD, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | mpReq.GP | RX | RW | 0x1E | Requested Guaranteed Power Value. Units is 0.5W. |

### 17.2.32. Q-FACTOR Register (0x00D2, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | Q Factor | RX | RW | 0x53 | Q-FACTOR value which is reported to TX in negotiation phase. |

### 17.2.33. Signal Strength Packet Register (0x00D3, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | Signal Strength | RX | R | - | Signal Strength value. |

### 17.2.34. Hvod Sink Current Register (0x00F9, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | HvodSinkCurrent | RX | RW | 0x1f | PCLAMP Sink Current Value, only valid when PCLAMP OV mode is constant current mode and OV status is met. It is 7mA/step. The max value is 0x1f, which means 217mA. |

### 17.2.35. Software Over Current Threshold Register (0x010C, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Software OCP Threshold | RX | RW | 0x0DAC | Software OCP threshold. When current exceeds this threshold, interrupt [Over Current Fault] is sent to AP. |

### 17.2.36. Software Over Current Threshold Hysteresis Register (0x010E, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | Software OCP Threshold Hysteresis | RX | RW | 0xC8 | Software OCP threshold hysteresis. When current exceeds (Software OCP Threshold + Software OCP Threshold Hysteresis), interrupt [Over Current Fault] is sent to AP, and EPT[OCP] is sent to Tx. |

### 17.2.37. Vrect Knee Register (0x0142, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | PwrKnee | RX | RW | 25 (BPP) 50 (EPP) | Threshold in units of 0.1W output power at which minimal window is applied. |

### 17.2.38. Vrect Correction Factor Register (0x0143, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | VrCorrFactor | RX | RW | 12 (BPP) 4 (EPP) | Coefficient value which is used in the Vrect Target calculation algorithm. |

### 17.2.39. Vrect Maximum Correction Register (0x0144, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | VrMaxCorr | RX | RW | 195 (BPP)<br>195 (EPP) | Maximum value of the header room in ADC codes. |

### 17.2.40. Vrect Minimum Correction Register (0x0146, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | VrMinCorr | RX | RW | 0 (BPP)<br>0 (EPP) | Minimum value of the header room in ADC codes. |

### 17.2.41. FOD Section Register (0x0149, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Fod Section | RX | R | 0x00 | Contains the index of the FOD section used during the last RPP value calculation. Used for debug only. |

### 17.2.42. Vrect Adjust Register (0x014E, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | VRect Adjust | RX | R | 0x00 | 8-bit signed integer representing Vrect final adjustment in ADC codes. The adjustment is applied during the final step of the VrectTarget calculation, thus overwriting Minimum and Maximum boundaries |

# 18. TX Mode Register

## 18.1 System Interrupt Clear Register in TX Mode (0x0028 - 0x002B, 32-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 31:19 | Reserved | - | - | - | Reserved |
| 18 | Adaptor Detection Done | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 17 | ID Authentication Pass | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 16 | ID Authentication packet Received | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 15 | CSP Packet Received | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 14 | EPT Restart Received | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 13 | Proprietary Packet Received | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 12:9 | Reserved | - | - | - | Reserved |
| 8 | BLE Address Received | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 7 | TX Initialization Done | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 6 | TX Conflict | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 5 | Operation Mode Change | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 4 | Configuration Packet Received | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 3 | Identification Packet Received | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 2 | Signal Strength Packet Received | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 1 | Start Digital Ping | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |
| 0 | EPT Type | TX | RW | 0 | AP writes 1 to clear the corresponding Interrupt Registers' bit and this bit is self-cleared to 0 (by M0) afterwards. |

## 18.2 System Status Register in TX Mode (0x002C - 0x002F, 32-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 31:19 | Reserved | - | - | - | Reserved |
| 18 | Adaptor Detection Done | TX | R | - | 1 = Adaptor detection is done. Extra circuit is necessary for this function. |
| 17 | ID Authentication Pass | TX | R | - | 1 = ID authentication is passed. |
| 16 | ID Authentication packet Received | TX | R | - | 1 = ID authentication packet is received. |
| 15 | CSP Packet Received | TX | R | - | 1 = CSP packet is received. Cleared together with the corresponding interrupt flag |
| 14 | EPT Restart Received | TX | R | - | 1 = EPT is received, Restart communication |
| 13 | Proprietary Packet Received | TX | R | - | 1 = Proprietary packet is received |
| 12:9 | Reserved | - | - | - | Reserved |
| 8 | BLE Address Received | TX | R | - | 1 = BLE address is received. |
| 7 | TX Initialization Done | TX | R | - | 1 = TX Initialization is successful |
| 6 | TX Conflict | TX | R | - | 1 = Chip works in Tx mode but is put on another Tx device. |
| 5 | Operation Mode Change | TX | R | - | 1 = Operating mode is changed |
| 4 | Configuration Packet Received | TX | R | - | 1 = Configuration packet is received |
| 3 | Identification Packet Received | TX | R | - | 1 = Identification packet is received |
| 2 | Signal Strength Packet Received | TX | R | - | 1 = Signal Strength packet is received |
| 1 | Start Digital Ping | TX | R | - | 1 = Digital Ping started |
| 0 | EPT Type | TX | R | - | 1 = Error is met and recommend AP to remove power in this case.<br>AP could read the error type from TRx End Power Transfer Reason Register |

## 18.3 System Interrupt Register in TX Mode (0x0030 - 0x0033, 32-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 31:19 | Reserved | - | - | - | Reserved |
| 18 | Adaptor Detection Done | TX | R | 0 | 1 = Adaptor detection is done. Extra circuit is necessary for this function.<br>0 = No such condition exists |
| 17 | ID Authentication Pass | TX | R | 0 | 1 = ID authentication is passed.<br>0 = No such condition exists |
| 16 | ID Authentication packet Received | TX | R | 0 | 1 = ID authentication packet is received.<br>0 = No such condition exists |
| 15 | CSP Packet Received | TX | R | 0 | 1 = CSP packet is received. Cleared together with the corresponding interrupt flag<br>0 = No such condition exists |
| 14 | EPT Restart Received | TX | R | 0 | 1 = EPT is received, Restart communication<br>0 = No such condition exists |
| 13 | Proprietary Packet Received | TX | R | 0 | 1 = Proprietary packet is received<br>0 = No such condition exists |
| 12:9 | Reserved | - | - | - | Reserved |
| 8 | BLE Address Received | TX | R | 0 | 1 = BLE address is received.<br>0 = No such condition exists |
| 7 | TX Initialization Done | TX | R | 0 | 1 = TX Initialization is successful<br>0 = No such condition exists |
| 6 | TX Conflict | TX | R | 0 | 1 = Chip works in Tx mode, but is put on another Tx device<br>0 = No such condition exists |
| 5 | Operation Mode Change | TX | R | 0 | 1 = Operating mode is changed<br>0 = No such condition exists |
| 4 | Configuration Packet Received | TX | R | 0 | 1 = Configuration packet is received<br>0 = No such condition exists |
| 3 | Identification Packet Received | TX | R | 0 | 1 = Identification packet is received<br>0 = No such condition exists |
| 2 | Signal Strength Packet Received | TX | R | 0 | 1 = Signal Strength packet is received<br>0 = No such condition exists |
| 1 | Start Digital Ping | TX | R | 0 | 1 = Digital Ping started<br>0 = No such condition exists |
| 0 | EPT Type | TX | R | 0 | 1 = Error is met and recommend AP to remove power in this case.<br>AP could read the error type from TRx End Power Transfer Reason Register<br>0 = No such condition exists |

## 18.4 System Interrupt Enable Register in TX Mode (0x0034 - 0x0037, 32-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 31:19 | Reserved | - | - | - | Reserved |
| 18 | Adaptor Detection Done | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 17 | ID Authentication Pass | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 16 | ID Authentication packet Received | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 15 | CSP Packet Received | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 14 | EPT Restart Received | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 13 | Proprietary Packet Received | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 12:9 | Reserved | - | - | - | Reserved |
| 8 | BLE Address Received | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 7 | TX Initialization Done | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 6 | TX Conflict | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 5 | Operation Mode Change | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 4 | Configuration Packet Received | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 3 | Identification Packet Received | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 2 | Signal Strength Packet Received | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 1 | Start Digital Ping | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |
| 0 | EPT Type | TX | RW | 1 | 1 = Corresponding interrupt is enabled<br>0 = Corresponding interrupt is disabled |

## 18.5 Battery Charge Status Register (0x003A, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | Charge Status | TX | R | 0x00 | In TX mode, it is the value in Charge Status Packet which is sent by Rx. |

## 18.6 End of Power Transfer Register in TX Mode (0x003B, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | EPT/EOC/EOP Reason | TX | R | 0x00 | The EPT reason which is read from previous EPT packet from Rx.<br>A WPC End of Power Transfer packet/message will be sent with the following definition:<br>0 = WPC mode, unknown<br>1 = WPC mode, Charge Complete<br>2 = WPC mode, Internal Fault<br>3 = WPC mode, Over Temperature<br>4 = WPC mode, Over Voltage<br>5 = WPC mode, Over Current<br>6 = WPC mode, Battery Failure<br>7 = WPC mode, Re-Configuration<br>8 = WPC mode, No Response<br>10 = WPC mode, Negotiation Failure<br>11 = WPC mode, Restart Power<br>All other values are reserved. |

## 18.7 Iin Value Register (0x0044, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Iin | TX | R | - | Iin in TX Mode, value in mA. |

## 18.8 Proprietary Data-Out Registers (0x0050 - 0x0057, 8 Bytes)

| Address | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 0x0057 | Prop Data 7 | TX | RW | 0x00 | Byte 6 of Proprietary packet data |
| 0x0056 | Prop Data 6 | TX | RW | 0x00 | Byte 5 of Proprietary packet data |
| 0x0055 | Prop Data 5 | TX | RW | 0x00 | Byte 4 of Proprietary packet data |
| 0x0054 | Prop Data 4 | TX | RW | 0x00 | Byte 3 of Proprietary packet data |
| 0x0053 | Prop Data 3 | TX | RW | 0x00 | Byte 2 of Proprietary packet data |
| 0x0052 | Prop Data 2 | TX | RW | 0x00 | Byte 1 of Proprietary packet data |
| 0x0051 | Prop Data 1 | TX | RW | 0x00 | Byte 0 of Proprietary packet data |

| Address | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 0x0050 | Proprietary Header | TX | RW | 0x00 | Proprietary Packet Header. Allows up to 7 bytes to be included in the proprietary packet |

## 18.9 Proprietary Data-In Registers (0x0058 - 0x005F, 8 Bytes)

| Address | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 0x005F | Prop Data 7 | TX | RW | 0x00 | Byte 6 of Proprietary packet data |
| 0x005E | Prop Data 6 | TX | RW | 0x00 | Byte 5 of Proprietary packet data |
| 0x005D | Prop Data 5 | TX | RW | 0x00 | Byte 4 of Proprietary packet data |
| 0x005C | Prop Data 4 | TX | RW | 0x00 | Byte 3 of Proprietary packet data |
| 0x005B | Prop Data 3 | TX | RW | 0x00 | Byte 2 of Proprietary packet data |
| 0x005A | Prop Data 2 | TX | RW | 0x00 | Byte 1 of Proprietary packet data |
| 0x0059 | Prop Data 1 | TX | RW | 0x00 | Byte 0 of Proprietary packet data |
| 0x0058 | Proprietary Header | TX | RW | 0x00 | Proprietary Packet Header. Allows up to 7 bytes to be included in the Proprietary packet |

## 18.10 Tx EPT Type Register (0x007A, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15 | EPT POCP | TX | R | 0 | 1 = indicates current protect during digital ping<br>0 = No such Error |
| 14 | EPT OTP | TX | R | 0 | 1 = indicates Over Temperature Error<br>0 = No such Error |
| 13 | EPT FOD | TX | R | 0 | 1 = indicates FOD<br>0 = No such Error |
| 12 | EPT LVP | TX | R | 0 | 1 = indicates Low Voltage Error<br>0 = No such Error |
| 11 | EPT OVP | TX | R | 0 | 1 = indicates Over Voltage Error<br>0 = No such Error |
| 10 | EPT OCP | TX | R | 0 | 1 = indicates Over Current Error<br>0 = No such Error |
| 9 | EPT RPP TIMEOUT | TX | R | 0 | 1 = indicates RPP Timeout Error<br>0 = No such Error |
| 8 | EPT CEP TIMEOUT | TX | R | 0 | 1 = indicates CEP Timeout Error<br>0 = No such Error |

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7 | EPT TIMEOUT | TX | R | 0 | 1 = indicates Watch-Dog Timeout Error<br>0 = No such Error |
| 6 | EPT NOI2CDATA TIMEOUT | TX | R | 0 | 1 = indicates NoI2C data Timeout Error<br>0 = No such Error |
| 5 | EPT TX CONFLICT | TX | R | 0 | 1 = indicates Tx Conflict Error<br>0 = No such Error |
| 4 | EPT PING VOLTAGE | TX | R | 0 | 1 = indicates the ping voltage exceeds the correct range. Only valid in VPWM mode<br>0 = No such Error |
| 3 | EPT AUTHENTICATION FAIL | TX | R | 0 | 1 = indicates the authentication is failed and power is removed. Only valid when authentication is required. 0 = No such Error |
| 2 :1 | Reserved | - | - | - | Reserved |
| 0 | EPT CMD | TX | R | 0 | 1 = indicates EPT Command from WPC RX<br>0 = No such Error |

## 18.11 TX System Command Register (0x007C, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15 | TX TGL OPEN LOOP | TX | RW | 0 | AP sets 1 to toggle open loop mode.<br>Chip clears the bit after processing |
| 14 | TX OPEN LOOP SYNC | TX | RW | 0 | AP sets 1 to synchronize open loop parameters one time.<br>Chip clears the bit after processing |
| 13:5 | Reserved | - | - | - | Reserved |
| 4 | TX WD | TX | RW | 0 | AP sets 1 to enable Watch Dog in TX mode.<br>Chip clears the bit after processing |
| 3 | TX BC | TX | RW | 0 | AP sets 1 to send proprietary packet to RX.<br>Chip clears the bit after processing |
| 2 | TX DIS | TX | RW | 0 | AP sets 1 to disable Tx function.<br>Chip clears the bit after processing |
| 1 | CLR Interrupt | TX | RW | 0 | AP sets 1 to clear interrupts.<br>Chip clears the bit after processing |
| 0 | TX EN | TX | RW | 0 | AP sets 1 to start digital ping.<br>Chip clears the bit after processing |

## 18.12 TX Status Register (0x007E, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:4 | Reserved | - | - | - | Reserved |
| 3 | TX transfer | TX | RW | 0 | Chip works in power transfer phase |
| 2 | Reserved | - | - | - | Reserved |
| 1 | TX ready | TX | RW | 0 | Chip is ready and wait for TX_EN command |
| 0 | TX Digital Ping | TX | RW | 0 | Chip works in digital ping phase |

## 18.13 Vin Value Register (0x0080, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Vin | TX | R | - | Current Vin voltage in TX mode, value in mV |

## 18.14 Vrect Value Register (0x0082, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Vrect | TX | R | - | Current Vrect voltage value in Tx mode, value in mV |

## 18.15 Die Temperature Value Register (0x0084, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Die Temperature in degrees Celsius | TX | R | - | Current Die Temperature value in degrees Celsius. |

## 18.16 CEP Value Register (0x00A5, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | CEP Value | TX | R | 0x00 | 8-bit signed number in last received CEP. |

## 18.17 Rx Manufacturer Code Register (0x00B0, 16- Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | RxManufCode | TX | R | - | The WPC Manufacturer code of the pairing device. |

## 18.18 Signal Strength Packet Register (0x00D3, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | Signal Strength | TX | R | - | Signal Strength value which is received at the beginning of power transfer |

## 18.19 Ping Interval Register (0x00E0, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Ping Interval | TX | RW | 0x04B0 | The interval between each digital ping, value in ms. |

## 18.20 Ping Frequency Register (0x00E2, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Ping Frequency | TX | RW | 0x015F | Frequency = 60 MHz / N. |

## 18.21 Ping Duty Setting Register (0x00E4, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | Ping Duty Setting | TX | RW | 0x4C | Duty cycle at the beginning of digital ping. |

## 18.22 Low Voltage Threshold Register (0x00EC, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | LVP | TX | RW | 0x1194 | Threshold for Low Voltage Protection in mV |

## 18.23 Over Voltage Threshold Register (0x00E8, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | OVpThd | TX | RW | 0x2AF8 | Over Voltage Threshold in TX mode, value in mV |

## 18.24 FOD Low Segment Threshold Register (0x00F8, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | FodThdL | TX | RW | 0x005A | FOD threshold for low level segment in Tx mode, value in mW, signed number. |

## 18.25 FOD High Segment Threshold Register (0x00FA, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | FodThdH | TX | RW | 0x005A | FOD threshold for high level segment in Tx mode, value in mW, signed number, The value of 0xff9c means – 100mW. |

## 18.26 FOD Segment Threshold Register (0x00FC, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | FodSegThd | TX | RW | 0x0802 | Threshold for two segment FOD threshold. Value in mW. If Rx Power is higher than FOD Segment Threshold, the High Level FOD Threshold is used, otherwise, the Low Level FOD Threshold is used as FOD threshold. |

## 18.27 Over Current Threshold Register (0x0108, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | OCpThd | TX | RW | 0x09C4 | Over Current Threshold in TX mode, value in mA |

## 18.28 Minimum Operating Frequency in FB Register (0x0114, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Minimum Operating Frequency in Full Bridge mode | TX | RW | 0x0208 | Minimum operating frequency (AC signal frequency on the coil) in Full Bridge.<br>Frequency = 60 MHz / N, Default is 0x209 (115KHz) |

## 18.29 Minimum Operating Frequency in HB Register (0x0116, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Minimum Operating Frequency in Half Bridge mode | TX | RW | 0x01F3 | Minimum operating frequency (AC signal frequency on the coil) in Half Bridge.<br>Frequency = 60 MHz / N Default is 0x1F3 (120 KHz) |

## 18.30 Maximum Operating Frequency Register (0x0118 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Maximum Operating Frequency | TX | RW | 0x019C | Maximum operating frequency (AC signal frequency on the coil) in TX mode.<br>Frequency = 60 MHz / N Default is 0x19C (145 KHz). |

## 18.31 Minimum Duty Register (0x011A, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | Minimum Duty | TX | RW | 0x28 | Minimum duty cycle when the operating frequency has reached the maximum value.<br>Duty = N / (256 *2) Default is 0x29(8%). |

## 18.32 TX DC Power Register (0x0156, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | TX DC Power | TX | R | - | Input power which is used in power loss FOD detection. |

## 18.33 Operating Frequency Register (0x0182, 16-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 15:0 | Operation Frequency | TX | R | - | Operating Frequency (AC signal frequency on the coil). Operation Frequency = 60MHz / N. |

## 18.34 Operating Duty-Cycle Register (0x018C, 8-Bit)

| Bit | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 7:0 | TX Operating Duty Cycle | TX | R | - | TX duty cycle when the operating frequency has reached the maximum value.<br>Duty = N / (256 *2)<br>For example: 0x19(5%) ~ 0xFF(50%) |

## 18.35 BLE MAC Address Registers (0x01B4 - 0x01B9, 6 Bytes)

| Address | Field Name | Mode | RW | Default Value | Description |
|---|---|---|---|---|---|
| 0x01B9 | BLE MAC Address [5] | TX | RW | 0x00 | Byte 5 of BLE MAC address |
| 0x01B8 | BLE MAC Address [4] | TX | RW | 0x00 | Byte 4 of BLE MAC address |
| 0x01B7 | BLE MAC Address [3] | TX | RW | 0x00 | Byte 3 of BLE MAC address |
| 0x01B6 | BLE MAC Address [2] | TX | RW | 0x00 | Byte 2 of BLE MAC address |
| 0x01B5 | BLE MAC Address [1] | TX | RW | 0x00 | Byte 1 of BLE MAC address |
| 0x01B4 | BLE MAC Address [0] | TX | RW | 0x00 | Byte 0 of BLE MAC address |

# 19. Ordering Information

| Part Number | Description |
|---|---|
| RTKA9530A0D00000BU | RA9530-R Evaluation Kit |

# 20. Revision History

| Revision | Date | Description |
|---|---|---|
| 2.00 | Jul 22, 2022 | Updated sample signal waveforms<br>Completed minor changes throughout |
| 1.00 | Jun 2, 2022 | Initial release. |

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