RA9530/RA9520

Stylus Application AP

This document is intended to provide a high-level understanding of AP operations and communication between the Applications Processor (AP) and a Wireless Power Charging IC, and is applicable for both a wireless power transmitter and receiver ICs interaction with AP.

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1. Introduction

Wireless power technology has been adopted in many portable electronics and various applications include but not limited to mobile phones, accessories, tablets, and active stylus.

Renesas Electronics Inc. has developed a turnkey solution reference design for tablet/stylus wireless charging application. A complete set of design collateral and evaluation demo boards are available, please contact your local Renesas sales representatives for more information.

This guide is applicable for both wireless power transmitter and receiver ICs interaction with AP. In this stylus application guide, the RA9530 IC is featured as wireless Tx and RA9520 IC is featured as the Rx device.

Refer to the stylus application system overview in Figure 1.

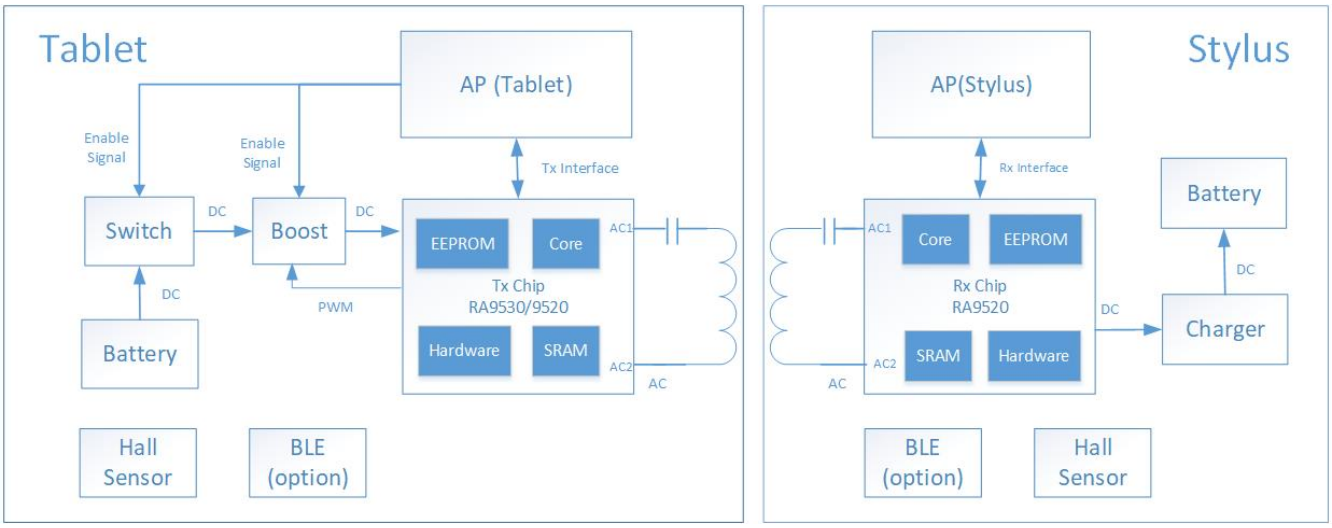

Figure 1. Stylus Application System Overview

2. Hardware IO Connection

The ICs have a good number of GPIOs that would be interconnected with AP. Some of the GPIOs have been assigned a default function in wireless charging application and some of them can be configured as per the needs of application.

For the tablet/stylus application, some of the GPIOs of the RA9530/RA9520 that have default functions that are controlled by firmware are described in sections 2.1, 2.2, and 2.3:

2.1 GPOI Function

The default GPIO functions of the RA9520 Rx IC (Stylus Side) is in Table 1.

Table 1. Rx IC (Stylus Side) GPIO Function

Function Name	GPIO	Pin Number	Description
Power Good (PG)	GP0	E2	Output pin from IC to AP. It is low by default. When the wireless charging is initiated, the output voltage is present on Vout, the IC pulls this pin to high.
Sleep	OD4	A3	Input pin to IC from AP. By default, AP should pull this pin low. During wireless charging, when AP pulls this pin to high, the RX IC will send EPT (Restart) command to TX IC, and the wireless power transfer will stop gracefully.
I2C-SCL	OD0	B3	The IC communicates with AP via I2C communication interface and is configured as an I2C slave. AP would be able to access SRAM registers through I2C interface. This pin corresponds to serial clock line of I2C interface and should always be pulled up by an external resistor.
I2C-SDA	OD1	B4	The IC communicates with AP via I2C communication interface and is configured as an I2C slave. AP would be able to access SRAM registers through I2C interface. This pin corresponds to serial data line of I2C interface and should always be pulled up by an external resistor.

Function Name	GPIO	Pin Number	Description
Interrupt	OD2	D3	Output pin from IC to AP. This pin serves as an interrupt to AP when the IC needs to send data/notification to AP. This pin is set to high by default and IC pulls this pin low to notify AP of the interrupt event. This pin should always be pulled up by an external resistor.

The default GPIO functions of RA9530 Tx IC (Tablet Side) is in Table 2.

Table 2. Tx IC (Tablet Side) GPIO Function

Function Name	GPIO	Pin Number	Description
PWM	GP1	(RA9530) D3 (RA9520) A2	Output pin from IC to AP. This pin is used to control the external Boost IC and adjust its output voltage. Connect this pin to the enable input of the external Boost IC.
I2C-SCL	OD0	(RA9530) A4 (RA9520) B3	The IC communicates with AP via I2C communication interface and is configured as an I2C slave. AP would be able to access SRAM registers through I2C interface. This pin corresponds to serial clock line of I2C interface and should always be pulled up by an external resistor.
I2C-SDA	OD1	(RA9530) A5 (RA9520) B4	The IC communicates with AP via I2C communication interface and is configured as an I2C slave. AP would be able to access SRAM registers through I2C interface. This pin corresponds to serial data line of I2C interface and should always be pulled up by an external resistor.
Interrupt	OD2	(RA9530) B4 (RA9520) D3	Output pin from IC to AP. This pin serves as an interrupt to AP when the IC needs to send data/notification to AP. This pin is set to high by default and the IC pulls this pin low to notify AP of the interrupt event. This pin should always be pulled up by an external resistor.

2.2 The Hardware Connection between Rx IC and AP (Stylus) – Rx Side

The hardware connection between the Rx IC and AP(Stylus) is shown in Figure 2.

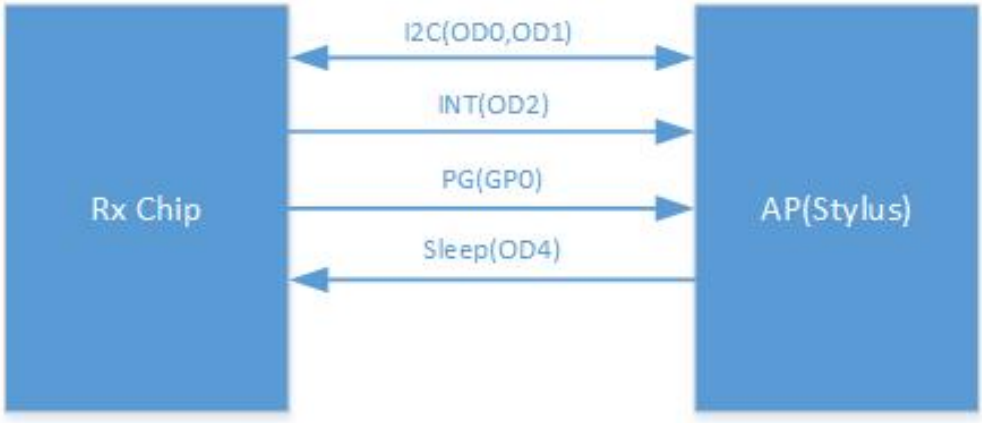

Figure 2. Hardware GPIO Connection between Rx IC and AP (Stylus) – Rx Side

2.3 The Hardware Connection between AP (Tablet) and Tx IC – Tx Side

The hardware connection between Tablet and Tx IC is shown in Figure 3.

Note: When using the IC in Tx mode, note that AP should have the ability to remove input power to the IC, therefore, an external switch needs to be connected between input power and V_{IN}. **The voltage slew rate on V_{IN} pin should be less than 5V/ms**.

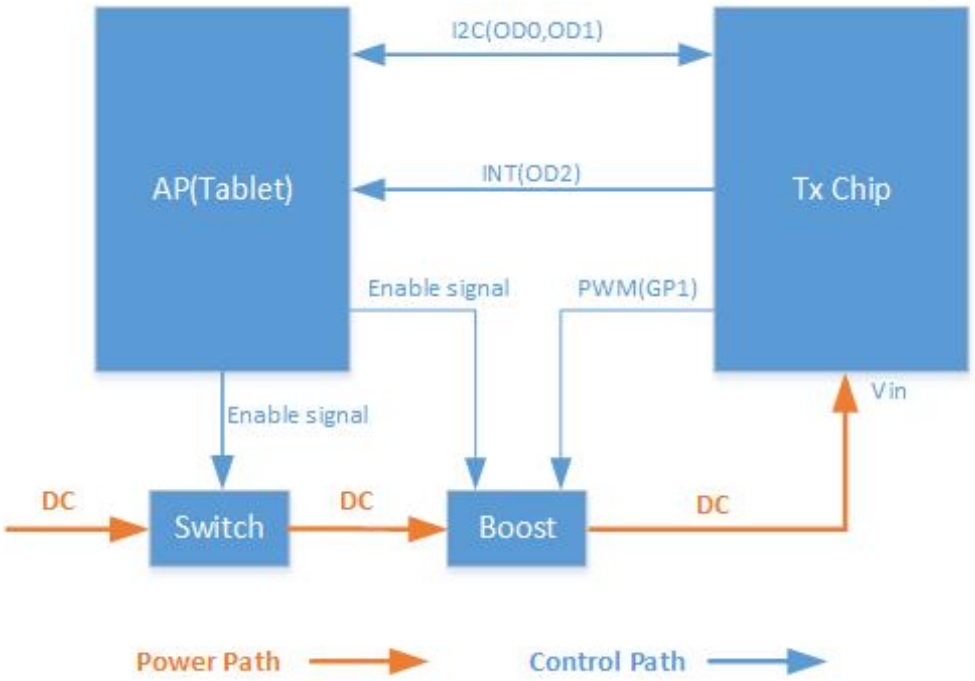

Figure 3. Hardware GPIO Connection between AP (Tablet) and Tx IC – Tx Side

3. Overall System Level Communication Flow Chart

The communication flow chart of stylus application is shown in Figure 4.

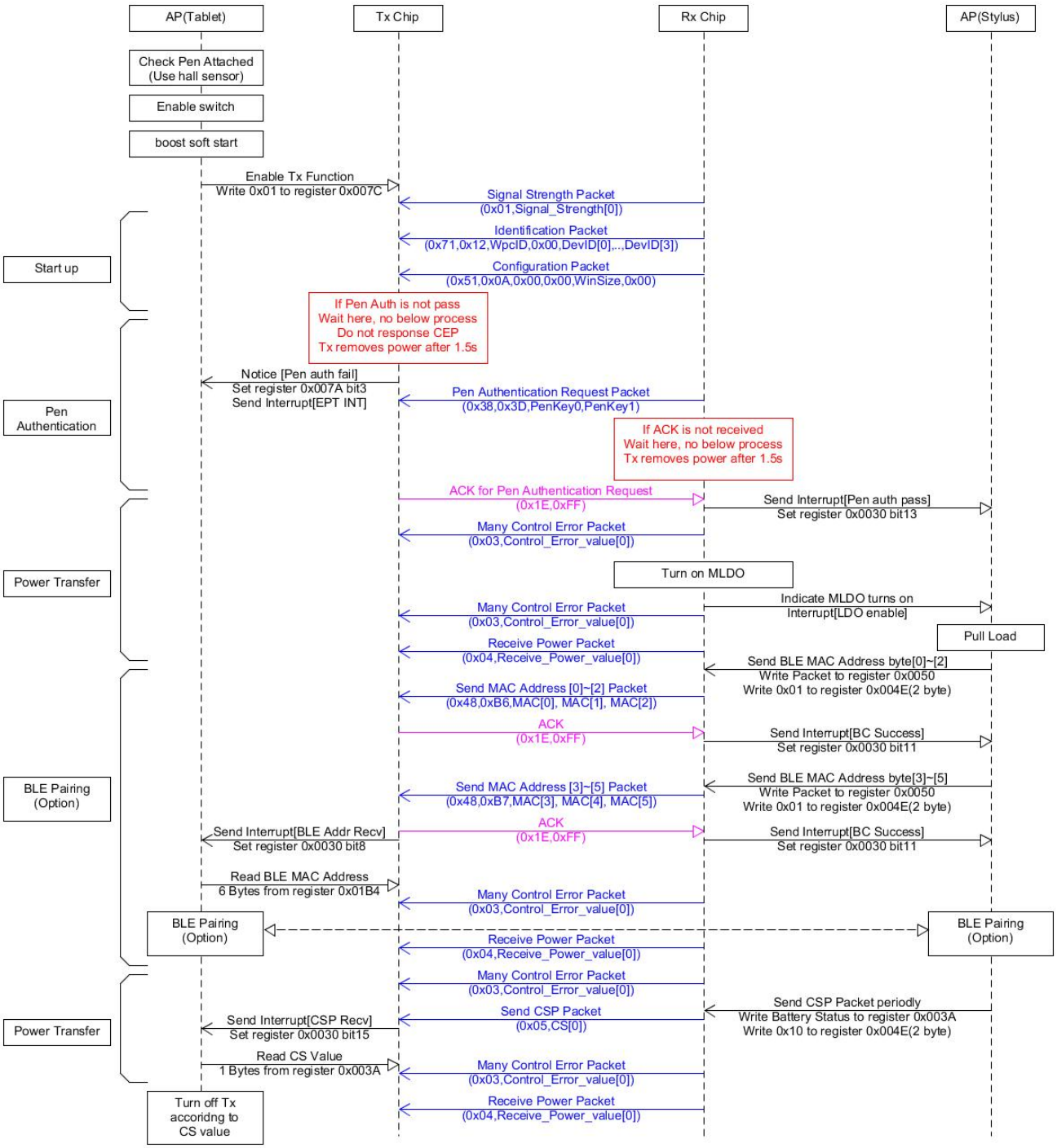

Figure 4. Stylus Application Communication Flow Chart

4. Detailed AP Interaction with Tx and Rx ICs

4.1 AP (Stylus) Flow Chart – Rx Side

The high-level task items of AP (Stylus) are:

1. Configure user registers for RX operation, if required.
2. Handle interrupts and perform appropriate actions.
3. BLE pairing operations (optional).
4. Send charge status to Tx.

The main flow chart of AP (Stylus) side is shown in Figure 5.

1. Consider dead battery case. AP reads interrupt and clears interrupts when it wakes up.
2. AP checks V_{OUT} turns on indication (see section 5.3.3). Do BLE pairing operation, (see section 5.3.7) if needed.
   a. If V_{OUT} does not turn on, AP waits for V_{OUT} turn on indication. Handle interrupt if there is one (see section 5.1 for details of interrupt operation).
   b. If V_{OUT} turns on already, AP sends Charge Status Packet to Tx with a certain interval (for example, 6–10s).

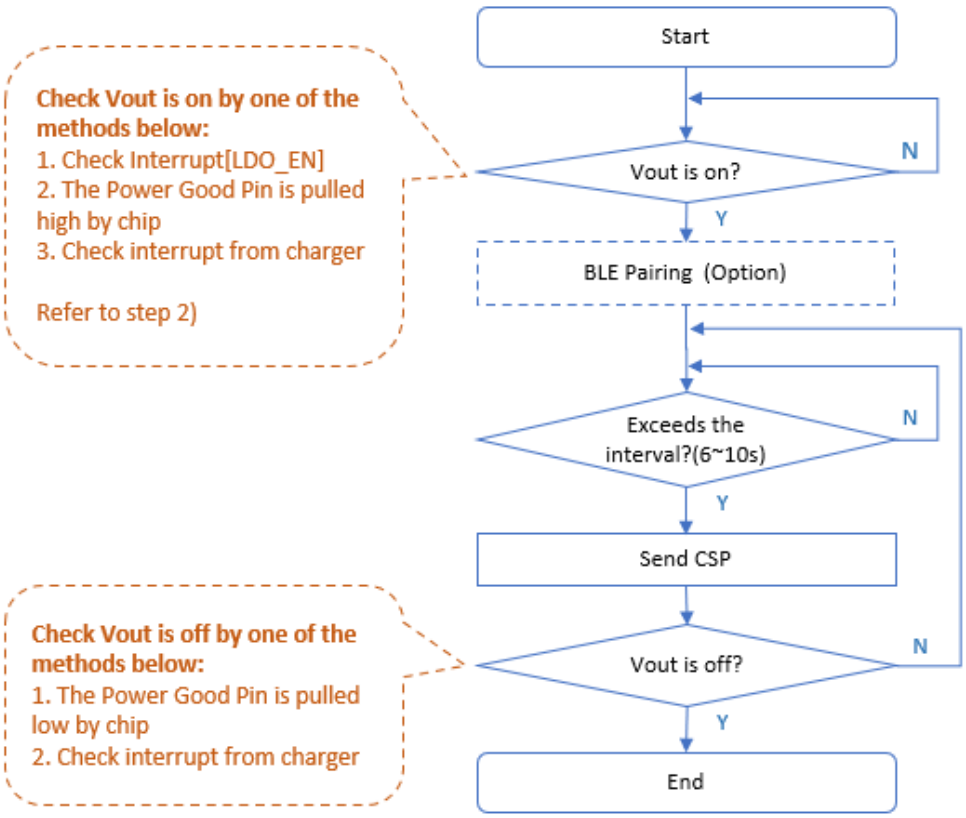

Figure 5. AP (Stylus) Main Flow Chart – Rx Side

Note: This flow chart is for reference only. Customers could develop their own flow chart according to their project needs.

4.2 AP (Tablet) Flow Chart – Tx Side

The high-level task items of AP (Tablet) are:

1. Configure user registers for Tx operation, if required.
2. Handle interrupts and perform appropriate actions.
3. Enable/Disable the power path.
4. BLE pairing operations (optional).
5. Receive stylus charge status.

The main flow chart of AP (Tablet) side is shown in Figure 6.

1. Wait for the stylus to be attached to the tablet.
2. After stylus is attached, turn on Switch IC.
3. Wait for 5ms.
4. Enable Boost IC with soft start.
5. Wait until interrupt TX Initialization Done is received, and perform below steps.
    a. If interrupt EPT Type is received, AP reads and records the value from Tx EPT Type Register, turns off Switch IC to remove power and skips the process below.
6. Turn on Tx function (see section 5.4.1 for details).
7. Wait for interrupts from IC and perform corresponding operations accordingly (see section 5.1 for details of interrupt operation).
8. When the Charge Status packet (CSP) packet is received, AP reads and records the battery status from Rx side (refer to section 5.4.3). Depending on the application, AP may decide to remove power to the wireless charging system when battery is fully charged to save power. AP may also decide to remove power based on Tablet's and Stylus's battery status.

Some examples of power saving control schemes are detailed below.

    a. If tablet battery status is greater than threshold, say 90%, when the stylus sends CSP value (of around 80–90%), AP (Tablet) may turn off Tx function m minutes later.
    b. If tablet battery status is less than threshold, say 90%, when the stylus sends a 50%–60% CSP value, AP (Tablet) turns off Tx function to save power.

The Tablet and Stylus battery charge threshold values can be set based on the application.

9. If in case of any communication timeout, AP starts a timer with a certain timeout value a second. Keep digital ping during a second, resume the power transfer and stops the timer if the Rx response. If timeout is met without Rx response, record read value from Tx EPT Type Register, record and then turns off switch IC to remove power

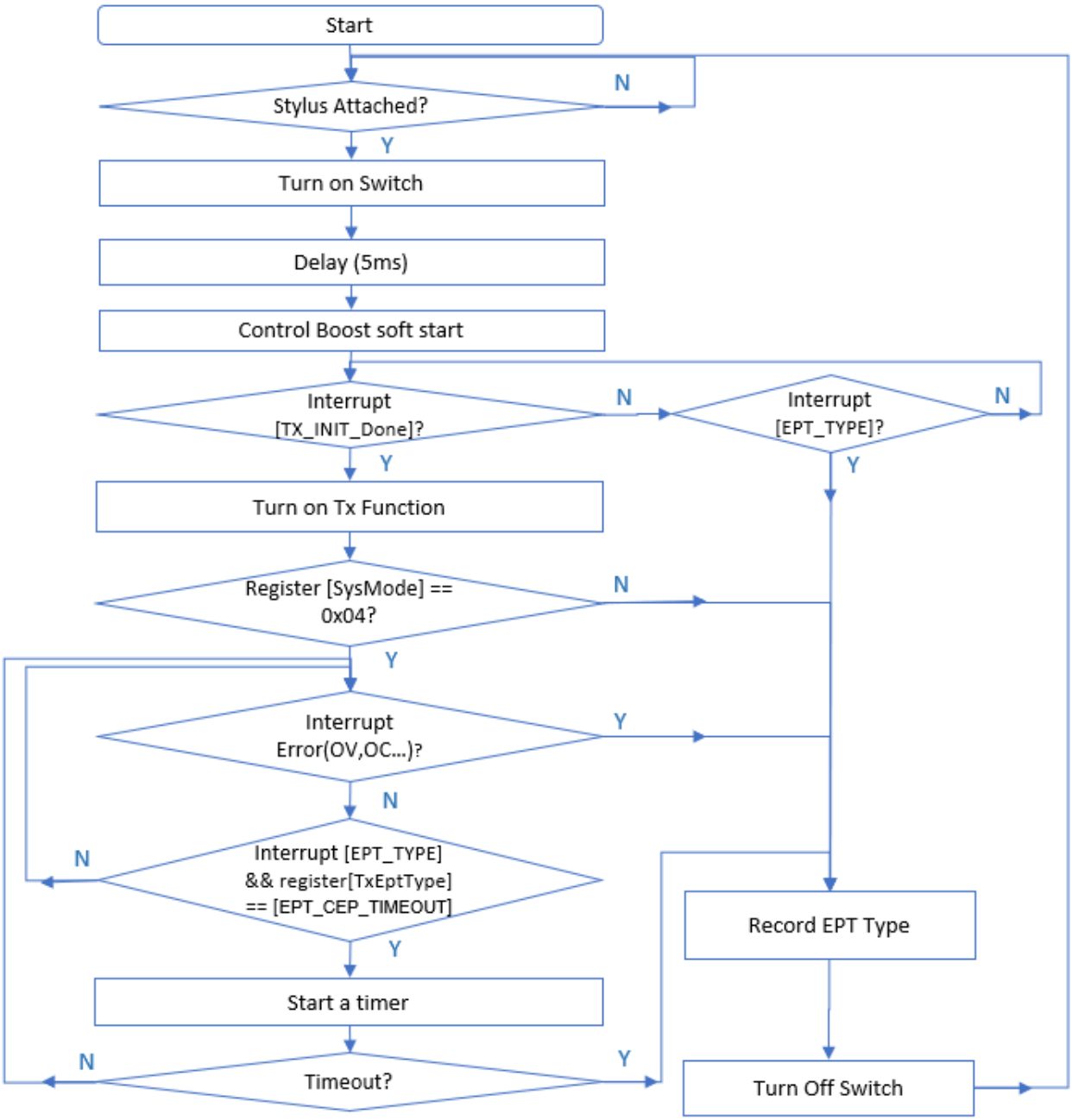

Figure 6. AP (Tablet) Main Flow Chart – Tx Side

Note: This flow chart is for reference only. Customers could develop their own flow chart according to their project needs.

5. Reference Procedure

5.1 Interrupt

5.1.1. Interrupt Detection and Clear

The INT pin (input to AP) is set to default high by an external pull up resistor. When there are interrupt events, the IC pulls the INT pin low to notice AP of the events. The INT pin on AP side needs to be configured as an interrupt pin with active falling edge.

It is recommended to clear the interrupt and take appropriate action as soon as it happens to achieve optimal system performance.

The interrupt logic is same for both Tx and Rx ICs.

The recommended procedure to handle an interrupt is described below.

1. Over the course of operation, the IC generates an event and pulls the INT pin low.
2. AP detects the falling edge on INT pin.
3. AP reads Rx System Interrupt Register / Tx System Interrupt Register through I2C bus and stores the reading value ‘m’.
4. AP writes the value ‘m’ that is read from previous step to Rx System Interrupt Clear Register / Tx System Interrupt Clear Register.
5. AP writes Rx Clear Interrupt / Tx Clear Interrupt command to system command register to clear interrupt.

   Rx mode: AP writes 0x20 to System Command Register.

   Tx mode: AP writes 0x02 to Tx System Command Register.
6. AP can check whether the interrupt is cleared successfully by either of the following methods.
   a. Reads status of INT pin. The INT pin has to be set to default state – high. If it is low, then the interrupt is not cleared.
   b. Reads Rx System Interrupt Register / Tx System Interrupt Register. A non-zero value of this register means that the interrupt is not cleared.
7. Based on the result from step 6, AP follows the procedure below:
   a. If interrupt is cleared, AP processes interrupt according to value ‘m’ and takes corresponding action.
   b. If interrupt is not cleared, it means that there are new interrupts that have been generated during steps 3–6, so repeat steps 3–6.

Note:

1. Only when the related set bits in Rx System Interrupt Register / Tx System Interrupt Register are set in Rx Clear Interrupt Register / Tx Clear Interrupt Register, the Rx Clear Interrupt / Tx Clear Interrupt command is effective.
2. After clearing the interrupt successfully, the INT pin is pulled up by the IC to wait for new interrupt events.
3. After clearing the interrupt successfully, the Rx System Interrupt Register / Tx System Interrupt Register is ‘0’.
4. AP should clear the interrupt register first, then perform the interrupt event operation.

5.1.2. Interrupt Event Operation

The interrupt information 'm' which is read from Rx System Interrupt Register / Tx System Interrupt Register is a 4-bytes value. Each bit corresponds to an interrupt event. AP should check all the bits set to '1' and perform the related operation. For the non-used interrupts, AP can disable the interrupts by clearing the corresponding bits in Rx System Interrupt Enable Register / Tx System Interrupt Enable Register.

The interrupt event operation for stylus application is displayed in Table 3 as a reference. This table is for reference and can be customized based on the application by referring to the RA9530_RA9520_User_Register_Map document.

5.1.3. Reference Interrupt Event Operation for Rx (Stylus) Side

Table 3. Reference Interrupt Event Operation for Rx IC – Stylus Side

Bit	Register Field Name	Function and Description
31:27	Other bits	AP does nothing besides clear interrupt.
26	VRECT ON	It indicates AC power is applied. AP configures the user registers (if needs) after this event.
25	AP Watch Dog	AP does nothing besides clear interrupt.
24:23	Reserved	AP does nothing besides clear interrupt.
22	BPP/EPP Check	AP does nothing besides clear interrupt.
21	Power Loss OTP	AP does nothing besides clear interrupt.
20	Over Current Fault	AP does nothing besides clear interrupt.
19:15	Other bits	AP does nothing besides clear interrupt.
14	Sleep Mode	It indicates IC works in sleep mode, and there is digital ping from Tx set. AP decides whether pulls low the sleep pin to exit sleep mode.
13	Pen Authentication Success	It indicates the pen authentication is success. AP could do nothing for this event. It is recommended to record it in AP log.
12	Pen Authentication Failure	It indicates the pen authentication is failed. AP could do nothing for this event. It is recommended to record it in AP log.
11	Back Channel Success	It indicates the proprietary packet is received by Tx. AP stops the timer to check proprietary packet and mark the packet is sent successful.
10	Back Channel Timeout	It indicates no Tx feedback for the proprietary packet which is sent earlier. AP decides whether re-send the packet.
9:8	Other bits	AP does nothing besides clear interrupt
7	LDO Disable	It indicates the MLDO turns off. It should not be taken as the indication for wireless power remove, because when the Rx is removed from Tx set, the Rx is powered off and AP may not fast enough to read the interrupt information.
6	LDO Enable	It indicates the MLDO turns on. AP could start to pull load.
5	Operation Mode Change	AP does nothing besides clear interrupt.
4	TX Data Receive	It indicates the proprietary packet from Tx is received. AP could read the received packet from Proprietary Data-In Registers.

Bit	Register Field Name	Function and Description
3	Other bits	AP does nothing beside clear interrupt.
2	Over Temperature	It indicates over temperature event happen. AP sends EPT(OTP) to Tx.
1	Over Voltage	It indicates over voltage event happen. AP sends EPT(OVP) to Tx.
0	Over Current	It indicates over current event happen. AP sends EPT(OCP) to Tx.

5.1.4. Reference Interrupt Event Operation for Tx (Tablet) Side

Table 4. Reference Interrupt Event Operation for Tx IC – Tablet Side

Bit	Register Field Name	Function and Description
31:18	Other bits	AP does nothing besides clear interrupt.
17	Pen Authentication Pass	It indicates the pen authentication is success. AP could do nothing for this event. It is recommended to record it in AP log.
16	Pen Authentication packet Received	AP does nothing besides clear interrupt.
15	CSP Packet Received	It indicates the CSP packet is received. AP reads battery charge status information from Battery Charge Status Register.
14	EPT Restart Received	AP does nothing besides clear interrupt.
13	Proprietary Packet Received	It indicates there is proprietary packet received from Rx. AP reads proprietary packet from Proprietary Data-In Registers.
12:9	Reserved	AP does nothing be besides side clear interrupt.
8	BLE Address Received	It indicates the BLE address is received. AP reads BLE MAC address (if needs) from BLE MAC Address Registers.
7	TX Initialization Done	It indicates TX Initialization is done. AP configures the user registers (if needs) and enable Tx function after this event.
6	TX Conflict	AP does nothing besides clear interrupt.
5	Operation Mode Change	AP does nothing besides clear interrupt.
4	Configuration Packet Received	AP does nothing besides clear interrupt.
3	Identification Packet Received	AP does nothing besides clear interrupt.
2	Signal Strength Packet	AP does nothing besides clear interrupt.
1	Start Digital Ping	AP does nothing besides clear interrupt.
0	EPT Type	It indicates error happens during wireless charge. AP reads EPT type information from Tx EPT Type Register and record. Remove the input voltage to IC at first, remove the error and then restart Tx function.

5.2 Common

5.2.1. Operation for the Full Battery

The reference process for removing wireless power according to battery status is described below.

1. AP Rx (Stylus) sends Charge Status packet (CSP) to tablet with a predefined interval (6–10s) during the power transfer.
2. AP Tx (Tablet) waits for interrupt type CSP Packet Received, then reads and records the battery status from Battery Charge Status Register.
3. AP Tx (Tablet) decides when to turn off Tx function in accordance to both tablet battery status and stylus battery status.

The application could set thresholds on Rx and Tx battery charge status to turn off Tx function. This would save power on the Tx battery. Some examples of power conversation include:

a. If tablet battery status is greater than threshold (say 90%) when the stylus battery CSP value (of 90% – 100%) is received, AP Tx (Tablet) turns off Tx function ‘m’ minutes later.

b. If tablet battery status is less than threshold (say 90%) when the stylus battery CSP value (of 50% – 60%) is received, AP Tx (Tablet) turns off Tx function.

5.3 Rx (Stylus) Side

5.3.1. EPT Packet Sending

The reference process for sending End of Power packet (EPT) is described below.

1. AP writes EPT reason to End of Power Transfer Register. For more details about EPT reason, see the RA9530_RA9520_User_Register_Map document.
2. AP writes Send End of Power command to System Command Register.

5.3.2. CSP Packet Sending

The reference process for sending Charge Status packet (CSP) is described below.

1. AP writes CSP value to Battery Charge Status Register. The CSP value is 1–100, which indicates percent value of battery.
2. AP writes Send Charge Status command to System Command Register.

5.3.3. The Indication of Wireless Power Ready

One of the items below could be considered as the indication of wireless power Ready:

1. The interrupt LDO Enable from the IC.
2. The Power Good pin is pulled high by the IC.
3. The related interrupt from external charger IC.

5.3.4. The Indication of Wireless Power Removal

One of the items below indicate the removal of wireless charging:

1. The Power Good pin is pulled low by the IC
2. The related interrupt from external charger IC.

Note: For wireless power removal indication, AP may not solely rely on the interrupt from the WPC IC as it is possible that the WPC IC loses power as soon as wireless power is removed and before AP reads the interrupt.

5.3.5. Proprietary Packet Sending

AP(Stylus) could send the proprietary packet to Tx (Tablet) by the following process:

1. AP writes the proprietary packet to Proprietary Data-Out Registers. The packet includes header and payload specified in WPC protocol, but does not include the checksum.
2. AP writes command Send PROP to System Command Register.
3. AP starts a timer with timeout value 600–800ms.
4. AP waits for interrupts from the IC.
   a. If interrupt Back Channel Success is received, it means Tx has received the proprietary packet. AP stops the timer and follows the procedure below. In this case:
      i. If interrupt Tx Data Receive is received, it indicates Tx has feedback data. AP reads the Input proprietary packet from Proprietary Data-In Registers.
      ii. If interrupt Tx Data Receive is not received, it indicates Tx sent notice for packet receiving. No action is expected from AP.
   b. If interrupt Back Channel Timeout is received, or both Back Channel Success and Back Channel Timeout are not received when timer meets timeout, it means the packet sending has failed. AP could re-send the proprietary packet by following steps 1–4. The recommended retry times is 3.

5.3.6. Proprietary Packet Receiving

AP(Stylus) could receive proprietary packet from Tx (Tablet) by the following process:

1. In case of interrupt Tx Data Receive.
2. AP reads the Input proprietary packet from Proprietary Data-In Registers.

5.3.7. BLE MAC Address Sending (Optional)

If there is BLE requirement, AP(Stylus) sends BLE MAC address to Tx (Tablet) by the following process:

1. AP sends BLE MAC address [0] – [2] by following the process in section 5.3.5. The proprietary packet for BLE MAC address [0] – [2] is [0x48, 0xB6, MAC [0], MAC [1], MAC [2]]. Tx responds for this packet.

If step 1 is successful, AP sends BLE MAC address [3] ~ [5] by following the process in section 5.3.5. The proprietary packet for BLE MAC address [3] – [5] is [0x48, 0xB7, MAC [3], MAC [4], MAC [5]].

2. Finished. No more action is needed from AP. Wait for BLE pairing request from AP(Tablet).

5.4 Tx (Tablet) Side

5.4.1. Turn On Tx Function

1. AP turns on input power to the IC. **The voltage slew rate must be less than 5V/1ms**.
   - Enable Switch IC
   - Some delay
   - Enable Boost IC with soft start
2. AP detects interrupt Tx Initialization Done.
3. AP configures user registers if required (optional).
4. AP writes Tx EN command to Tx System Command Register.
5. Wait for 100ms.
6. AP reads System Operating Mode Register.
   a. If the value is 0x04, it means the Tx function enable is successful.
   b. If the value is not 0x04, it means the Tx function enable is failed. AP should read System Interrupt Register, records the events and removes input power to the IC.

5.4.2. Turn Off Tx Function

If AP intends to turn off Tx function, the best way is removing the input power to the IC.

1. Turn off Boost IC.
2. Some delay.
3. Turn off Switch IC.

If there are errors during the power transfer, it is also necessary to remove the input power to the IC.

It is not recommended to just disable Tx function, but in the case where AP desires to just disable Tx function by retaining input power to the IC, the below process could be used:

1. AP writes command Tx DIS to Tx System Command Register.
2. Wait for 100ms.
3. AP reads System Operating Mode Register and:
   a. If the value is 0x04, it means the Tx function disable is successful.
   b. If the value is not 0x04, it means the Tx function disable failed. AP should read System Interrupt Register, record the events and remove input power to the IC.

5.4.3. Charge Status Packet (CSP) Reception

The reference process for receiving CSP packet is described below.

1. AP detects interrupt from the IC.
2. AP reads interrupt type from System Interrupt Register.
3. If the interrupt CSP Packet Received is received, AP reads CSP value from the Battery Charge Status Register.

5.4.4. BLE MAC Address Receiving (Option)

The reference process for BLE MAC Address reception is described below.

1. AP detects interrupt from the IC.
2. AP reads interrupt type from System Interrupt Register.
3. If the interrupt BLE Address Received is received, AP reads 6 bytes of BLE MAC Address from BLE MAC Address Registers.

5.4.5. Proprietary Packet Transmission

AP(Tablet) could send proprietary packet to Rx (Stylus) by the following process:

1. AP writes the proprietary packet to Proprietary Data-Out Registers. The packet includes header and payload as specified in WPC Qi protocol, but does not include the checksum.
2. AP writes Tx BC command to Tx System Command Register.

5.4.6. Proprietary Packet Reception

AP(Tablet) could receive proprietary packet to Rx (Stylus) by the following process:

When AP receives interrupt Proprietary Packet Received:

1. AP reads the Input proprietary packet from Proprietary Data-In Registers.

5.4.7. Firmware Update

The firmware update procedure for the IC is described in a separate document. For more details, see the *EEPROM Programming Guide*.

6. Basic User Registers List

The RA9530/RA9520 uses the standard I2C slave implementation protocol to communicate with a host AP or other I2C peripherals. The communication protocol is implemented by using 8 bits for data and 16 bits for addresses. The default slave address of the RA9530/RA9520 is 0x3B (high 7 bits).

When writing to the IC, care should be taken to write to registers marked exclusively as Read/Write (RW) ONLY. Registers marked as Read Only (R)/Reserved should never be written and any such write operation would result in unexpected behavior. When writing to a RW register that contains a combination of RW fields and reserved fields, care should be taken to retain reserved or Read-Only bits/fields. All other bits/field, including reserved bits/fields, should NOT be modified.

A brief list of registers related to this reference design are in below table. For a detailed list of registers, refer to the RA9530_RA9520_User_Register_Map document. The register names in these two documents are identical.

6.1 Rx IC – Basic User Registers (Stylus Side)

Table 5. Basic User Registers for Rx IC – Stylus Side

Register Field Name	Address	RW	Length (bytes)	Function and Description
System Interrupt Clear Register in RX Mode	0x0028	RW	4	AP writes “1” to clear the corresponding Interrupt Registers’ bit and writes Clear Interrupt command to System Command Register to clear interrupt.
System Interrupt Register in RX Mode	0x0030	R	4	AP reads interrupt events information from this register.
System Interrupt Enable Register in RX Mode	0x0034	RW	4	AP writes “1” to corresponding bit to enable the interrupt, and writes “0” to corresponding bit to disable the interrupt.
Battery Charge Status Register	0x003A	RW	1	AP writes battery charge status to this register, then writes Send Charge Status command to System Command Register to send the battery charge status to Tx.
End of Power Transfer Register	0x003B	RW	1	AP writes EPT type to this register, then writes Send End of Power command to System Command Register to send the EPT packet to Tx.
System Operating Mode Register	0x004D	R	1	AP reads work mode of IC from this register.
System Command Register	0x004E	RW	2	AP writes “1” to corresponding bit to trigger a command one time. It is self-clean register. After the command is handled by IC, IC clear the related bit. The interval to write this register should be at least 3~5ms.
Proprietary Data-Out Registers	0x0050	RW	8	AP writes the output proprietary packet in these registers, then writes Send PROP command to System Command Register to send the packet to Tx.
Proprietary Data-In Registers	0x0058	RW	8	AP reads the input proprietary packet, which is from Tx, after receiving interrupt TX Data Receive.

6.1.1. System Command Register Bit Map

Table 6. Bit Map of System Command Register

Bit	Register Field Name	Mode	RW	Default Value	Function and Description
15	Renegotiation	RX	W	0	AP sets '1' to generate renegotiation.
14:10	Reserved	-	-	0	Reserved.
9	Send WPC1P3 Data Packet	RX	W	0	AP sets '1' to generate WPC 1.3 data packet transfer.
8	Soft Restart	RX	W	0	AP sets '1' to turn off and restart LDO. IC clears the bit after processing the command.
7	Fast Charging	RX	W	0	AP sets '1' to switch the Voltage to fast charging. IC clears the bit after processing the command.
6	Reserved	-	-	0	Reserved.
5	Clear Interrupt	RX	W	0	AP sets '1' to send Clear Interrupt command. IC clears the bit after processing the command.
4	Send Charge Status	RX	W	0	AP sets '1' to send Charge Status packet in RX mode. IC clears the bit after processing the command.
3	Send End of Power	RX	W	0	AP sets '1' to send End of Power Transfer Packet in RX mode. IC clears the bit after processing the command.
2	Send Device Authentication	RX	W	0	AP sets '1' to send Device Authentication. IC clears the bit after processing the command.
1	Reserved	-	-	0	Reserved.
0	Send PROP	RX	W	0	AP sets '1' to send proprietary packet. IC clears the bit after processing the command.

Note: It costs time to implement the command. AP could write new command to System Command Register 3–5ms after the previous command.

6.2 Tx IC – Basic User Registers (Tablet Side)

Table 7. Required User Registers for Tx IC – Tablet Side

Register Field Name	Address	RW	Length (bytes)	Function and Description
System Interrupt Clear Register in TX Mode	0x0028	RW	4	AP writes '1' to clear the corresponding Interrupt Registers' bit and writes Clear Interrupt command to Tx System Command Register to clear interrupt.
System Interrupt Register in TX Mode	0x0030	R	4	AP reads interrupt events information from this register.
System Interrupt Enable Register in TX Mode	0x0034	RW	4	AP writes '1' to corresponding bit to enable the interrupt, and writes "0" to corresponding bit to disable the interrupt.
Battery Charge Status Register	0x003A	R	1	AP reads Rx battery charge status from this register, after receiving interrupt CSP Packet Received.

Register Field Name	Address	RW	Length (bytes)	Function and Description
System Operating Mode Register	0x004D	R	1	AP reads work mode of IC from this register.
Proprietary Data-Out Registers	0x0050	RW	8	AP writes the output proprietary packet in these registers, then writes TX BC command to Tx System Command Register to send the packet to Rx.
Proprietary Data-In Registers	0x0058	RW	8	AP reads the input proprietary packet, which is from Rx, after receiving interrupt Proprietary Packet Received.
Tx EPT Type Register	0x007A	R	2	AP reads the EPT type from this register, after receiving interrupt EPT Type.
TX System Command Register	0x007C	RW	2	AP writes '1' to corresponding bit to trigger a command one time. It is self-clean register. After the command is handled by IC, IC clear the related bit. The interval to write this register should be at least 3–5ms.
BLE MAC Address Registers	0x01B4	R	6	AP reads the BLE MAC Address from this register, after receiving interrupt BLE Address Received.

6.2.1. Tx System Command Register Bit Map

Table 8. Bit Map of TX System Command Register

Bit	Register Field Name	Mode	RW	Default Value	Function and Description
15	TX TGL OPEN LOOP	TX	RW	0	AP sets 1 to toggle open loop mode. IC clears the bit after processing.
14	TX OPEN LOOP SYNC	TX	RW	0	AP sets 1 to synchronize open loop parameters one time. IC clears the bit after processing.
13:5	Reserved	-	-	-	Reserved.
4	TX WD	TX	RW	0	AP sets 1 to enable Watch Dog in TX mode. IC clears the bit after processing.
3	TX BC	TX	RW	0	AP sets 1 to send proprietary packet to RX. IC clears the bit after processing.
2	TX DIS	TX	RW	0	AP sets 1 to disable Tx function. IC clears the bit after processing.
1	CLR Interrupt	TX	RW	0	AP sets 1 to clear interrupts. IC clears the bit after processing.
0	TX EN	TX	RW	0	AP sets 1 to start digital ping. IC clears the bit after processing.

Note: It costs time to implement the command. AP could write new command to System Command Register 3–5ms after the previous command.

6.2.2. Tx EPT Type Register Bit Map

Table 9. Bit Map of TX EPT Type Register

Bit	Register Field Name	Mode	RW	Default Value	Function and Description
15	EPT POCP	TX	R	0	1: indicates current protect during digital ping. 0: No such Error.
14	EPT OTP	TX	R	0	1: indicates Over Temperature Error. 0: No such Error.
13	EPT FOD	TX	R	0	1: indicates FOD. 0: No such Error.
12	EPT LVP	TX	R	0	1: indicates Low Voltage Error. 0: No such Error.
11	EPT OVP	TX	R	0	1: indicates Over Voltage Error. 0: No such Error.
10	EPT OCP	TX	R	0	1: indicates Over Current Error. 0: No such Error.
9	EPT RPP TIMEOUT	TX	R	0	1: indicates RPP Timeout Error. 0: No such Error.
8	EPT CEP TIMEOUT	TX	R	0	1: indicates CEP Timeout Error. 0: No such Error.
7	EPT TIMEOUT	TX	R	0	1: indicates Watch-Dog Timeout Error. 0: No such Error.
6	EPT APWD TIMEOUT	TX	R	0	1: indicates AP Watch-Dog Timeout Error. 0: No such Error.
5	EPT TX CONFLICT	TX	R	0	1: indicates Tx Conflict Error. 0: No such Error.
4	EPT PING VOLTAGE	TX	R	0	1: indicates the ping voltage exceeds the correct range. Only valid in VPWM mode. 0: No such Error.
3	EPT AUTHENTICATION FAIL	TX	R	0	1: indicates the authentication is failed and power is removed. Only valid when authentication is required. 0: No such Error.
2 :1	Reserved	-	-	-	Reserved.
0	EPT CMD	TX	R	0	1: indicates EPT Command from WPC RX. 0: No such Error.

7. I2C Interface Introduction

The AP communicates with the WPC IC via an I2C interface. AP needs to access the SRAM registers to configure the WPC IC in RX or TX mode. AP can configure/program the WPC IC's SRAM/Programmable memory using I2C protocol.

Refer to the following sections for an understanding of I2C Read and Write operations.

7.1 General Description

For all operations, standard I2C sequential read or write protocols are followed. In most cases, the details of I2C transactions on the host side are implemented by the host driver software. If the I2C communication protocol is implemented by host driver software then the Application Programmer can just specify only the RA9530/RA9520 I2C address, the memory address, and the data bytes.

The I2C read and write operations are defined in sections 7.2 and 7.3 respectively.

7.2 I2C Read Operation

The I2C read process is detailed below.

1. I2C Start Condition.
2. Send I2C Slave Address (0x3B) with R/W bit = W = 0.
3. Send two-byte memory address.
4. I2C Repeated Start Condition (no intervening I2C stop condition).
5. Send I2C Slave Address (0x3B) with R/W = R = 1.
6. Read as many sequential data bytes as required. (After each data byte is read, the memory address is auto incremented by one).
7. I2C Stop Condition.

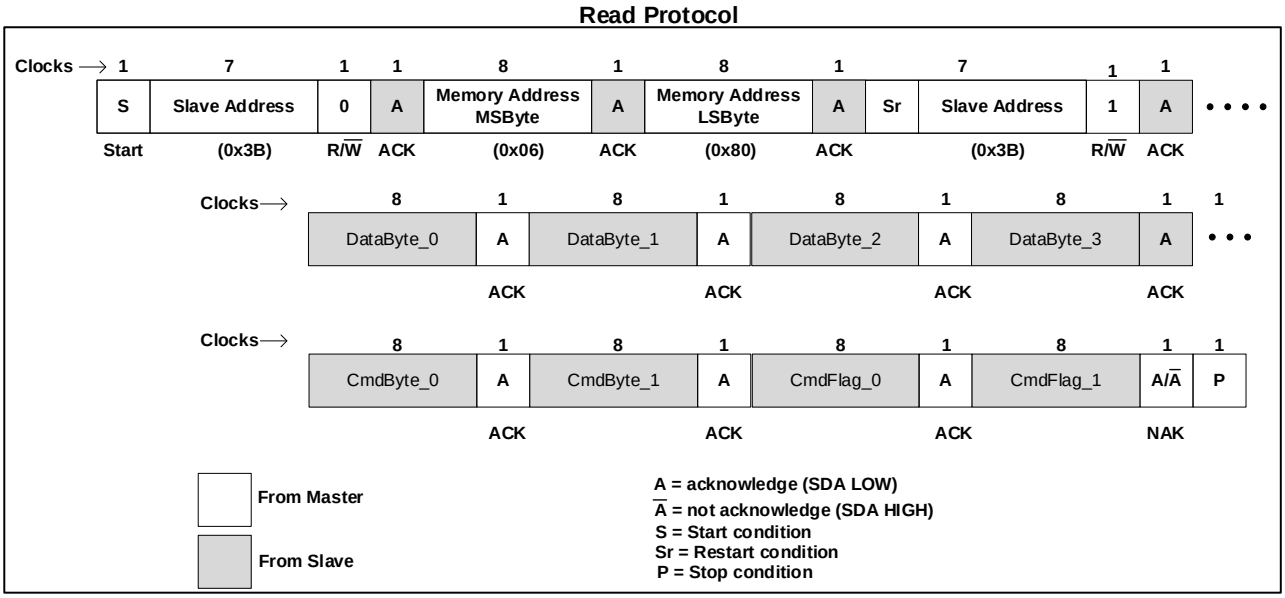

Figure 7. I2C Read Operation

7.3 I2C Write Operation

1. I2C Start Condition.
2. Send I2C Slave Address (0x3B) with R/W bit = W = 0.
3. Send two-byte memory address.
4. Send as many sequential data bytes as required. After each data byte is written, the memory address is auto incremented by one.
5. I2C Stop Condition.

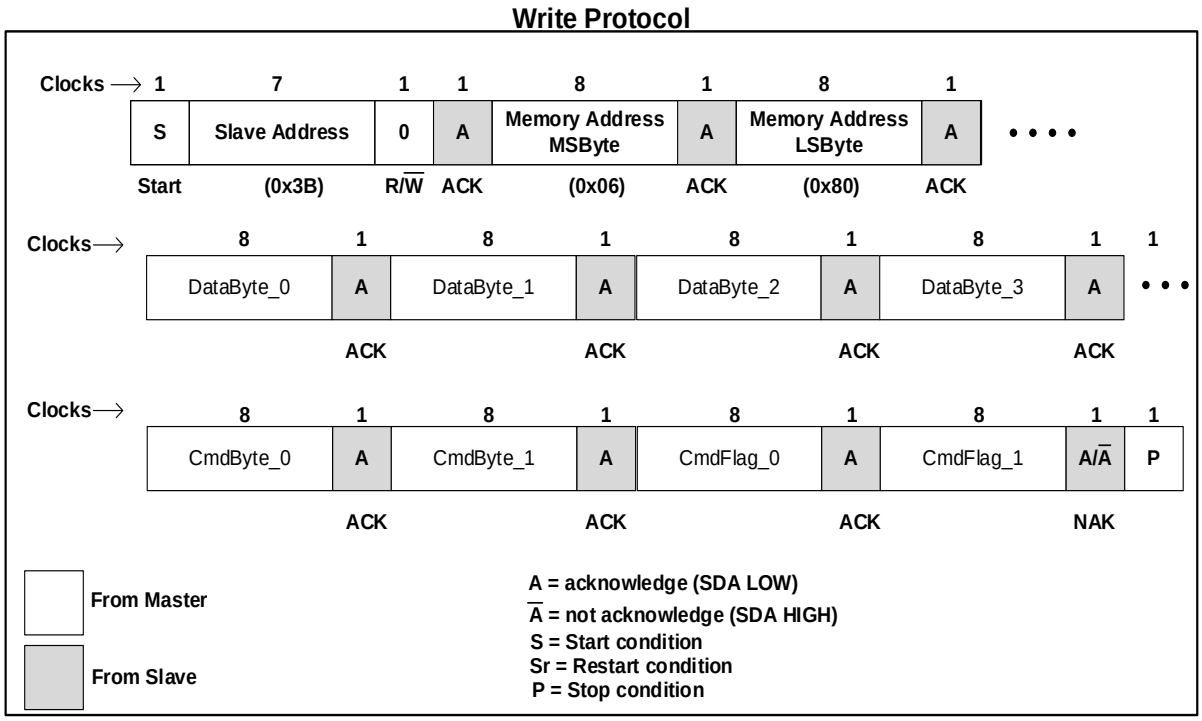

Figure 8. I2C Write Operation

8. Revision History

Revision	Date	Description
1.00	Jun 28, 2022	Initial release.

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