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PTX Tunneling Library v1.4.1 for STM32CubeIDE

The PTX Tunneling library can be used to evaluate and optimize the performance (antenna matching, system/RF configuration, etc.) of any custom-made device using a PTX100x device via SPI serial interface.

Embedding this library into the device firmware enables the translation of communication from **UART to SPI**, so that the full functionality of the **PTX100x** * **Config Tool** can be used in a custom environment. This document also provides instructions on how to create a sample application using an <u>ST32L562E-DK</u> development board.

Contents

1.	Requ	uirements	2				
2.	Sam	ple Firmware	2				
	2.1	Creating the Project	2				
		2.1.1. Configuration File	2				
		2.1.2. Creating the Project	7				
	2.2	Importing the Library	8				
		2.2.1. Adding the Include Path	10				
		2.2.2. Adding the Library File	11				
	2.3 Implementing the HAL						
	2.4 Calling the Library Functions						
	2.5 Building the Firmware						
3.	Prep	paring the Hardware	18				
	3.1	Debug Configuration	19				
4.	Usin	ng the Tunneling Feature	19				
5.	Revi	ision History	20				

1. Requirements

The footprint of the library is ~13kB Flash and 10kB RAM. Moreover, a hardware abstraction layer must be implemented by the user for the particular uC/Board, which executes the low-level commands requested by the library. From the resource point of view, only the SysTick timer, UART, SPI, and the IRQ pin will be used.

The library can be seamlessly integrated into a CMAKE project as well, but the STM32Cubelde is used in this document (for more information, see <u>STM32Cubelde</u> is used in this document).

2. Sample Firmware

The sample application is used for creating and serving the tunnel between the host PC UART interface and the PTX100x chip connected by SPI. The library can be used either as a precompiled static library or as a source-library – most steps are the same for both cases.

2.1 Creating the Project

The used HAL source code will be picked from the SDK and copied to the project folder by the *STM32CubeIde* based on the configuration file (.ioc). This is the most convenient way to start a new project.

2.1.1. Configuration File

The configuration file ptxTunneling.ioc must be created in an arbitrary place with the following content:

File.Version=6 GPIO.groupedBy=Group By Peripherals KeepUserPlacement=false LPTIM1.ClockPrescaler=LPTIM PRESCALER DIV16 LPTIM1.IPParameters=ClockPrescaler LPTIM2.ClockPrescaler=LPTIM_PRESCALER_DIV16 LPTIM2.IPParameters=ClockPrescaler Mcu.ContextProject=TrustZoneDisabled Mcu.Family=STM32L5 Mcu.IPO=LPTIM1 Mcu.IP1=LPTIM2 Mcu.IP2=NVIC Mcu.IP3=PWR Mcu.IP4=RCC Mcu.IP5=SPI3 Mcu.IP6=SYS Mcu.IP7=USART1 Mcu.IPNb=8 Mcu.Name=STM32L5620EIxO Mcu.Package=UFBGA132 Mcu.Pin0=PB4 (NJTRST) Mcu.Pin1=PG9 Mcu.Pin10=VP LPTIM2 VS LPTIM counterModeInternalClock Mcu.Pin11=VP PWR VS DBSignals Mcu.Pin12=VP SYS VS Systick Mcu.Pin2=PB5 Mcu.Pin3=PA9 Mcu.Pin4=PA10 Mcu.Pin5=PF5 Mcu.Pin7=PB13 Mcu. Pin8=PF12 Mcu.Pin9=VP LPTIM1 VS LPTIM counterModeInternalClock Mcu.PinsNb=13 Mcu.ThirdPartyNb=0 Mcu.UserConstants= Mcu.UserName=STM32L562QEIxQ MxCube.Version=6.0.0 MxDb.Version=DB.6.0.0 NVIC.BusFault IRQn=true\:0\:0\:false\:false\:true\:false\:false NVIC.DebugMonitor IRQn=true\:0\:0\:false\:false\:true\:false\:false NVIC.ForceEnableDMAVector=true NVIC.HardFault_IRQn=true\:0\:0\:false\:false\:true\:false NVIC.LPTIM1_IRQn=true\:0\:0\:false\:false\:true\:true\:true NVIC.LPTIM2 IRQn=true\:0\:0\:false\:false\:true\:true NVIC.MemoryManagement IRQn=true\:0\:0\:false\:false\:true\:false\:false NVIC.NonMaskableInt IRQn=true\:0\:0\:false\:false\:true\:false\:false NVIC.PendSV IRQn=true\:0\:0\:false\:false\:true\:false\:false NVIC.PriorityGroup=NVIC PRIORITYGROUP 3 NVIC.SPI3 IRQn=true\:3\:0\:true\:false\:true\:true\:true NVIC.SVCall IRQn=true\:0\:0\:false\:false\:true\:false NVIC.SysTick_IRQn=true\:0\:0\:false\:false\:true\:false\:true NVIC.USART1 IRQn=true\:0\:0\:false\:false\:true\:true NVIC.UsageFault IRQn=true\:0\:0\:false\:false\:true\:false\:false PA10.Locked=true PA10.Mode=Asynchronous PA10.Signal=USART1 RX PA9.Locked=true PA9.Mode=Asynchronous PA9.Signal=USART1 TX

PB13.GPIOParameters=PinState,GPIO Label PB13.GPIO Label=SPI3 NSS PB13.Locked=true PB13.PinState=GPIO PIN SET PB13.Signal=GPIO_Output PB4\ (NJTRST).GPIOParameters=GPIO Speed,GPIO PuPd,GPIO Label,GPIO Mode PB4\ (NJTRST).GPIO_Label=SPI3_MISO PB4\ (NJTRST).GPIO_Mode=GPIO_MODE_AF_PP PB4\ (NJTRST).GPIO_PuPd=GPIO_NOPULL PB4\ (NJTRST).GPIO Speed=GPIO SPEED FREQ MEDIUM PB4\ (NJTRST).Locked=true PB4\ (NJTRST).Mode=Full Duplex Master PB4\ (NJTRST).Signal=SPI3 MISO PB5.GPIOParameters=GPIO Speed, GPIO Label PB5.GPIO Label=SPI3 MOSI PB5.GPIO Speed=GPIO SPEED FREQ MEDIUM PB5.Mode=Full Duplex_Master PB5.Signal=SPI3 MOSI PF11.Locked=true PF11.Signal=GPIO Output PF12.Locked=true PF12.Signal=GPIO Output PF5.GPIOParameters=GPIO Label PF5.GPIO Label=PTX IRQ PF5.Locked=true PF5.Signal=GPIO Input PG9.GPIOParameters=GPIO Speed, GPIO Label PG9.GPIO Label=SPI3 SCK PG9.GPIO Speed=GPIO SPEED FREQ MEDIUM PG9.Locked=true PG9.Mode=Full_Duplex_Master PG9.Signal=SPI3 SCK PinOutPanel.CurrentBGAView=Top PinOutPanel.RotationAngle=0 ProjectManager.AskForMigrate=true ProjectManager.BackupPrevious=false ProjectManager.CompilerOptimize=6 ProjectManager.ComputerToolchain=false ProjectManager.CoupleFile=false ProjectManager.CustomerFirmwarePackage= ProjectManager.DefaultFWLocation=true ProjectManager.DeletePrevious=true ProjectManager.DeviceId=STM32L562QEIxQ ProjectManager.FirmwarePackage=STM32Cube FW L5 V1.3.0 ProjectManager.FreePins=false ProjectManager.HalAssertFull=false ProjectManager.HeapSize=0x200 ProjectManager.KeepUserCode=true ProjectManager.LastFirmware=false ProjectManager.LibraryCopy=1 ProjectManager.MainLocation=Core/Src ProjectManager.NoMain=false ProjectManager.PreviousToolchain=STM32CubeIDE ProjectManager.ProjectBuild=false ProjectManager.ProjectFileName=demo2.ioc ProjectManager.ProjectName=demo2 ProjectManager.RegisterCallBack= ProjectManager.StackSize=0x400 ProjectManager.TargetToolchain=STM32CubeIDE ProjectManager.ToolChainLocation=

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ProjectManager.UnderRoot=true ProjectManager.functionlistsort=1-MX GPIO Init-GPIO-false-HAL-true,2-SystemClock Config-RCC-false-HAL-false, 3-MX LPTIM1 Init-LPTIM1-false-HAL-true, 4-MX LPTIM2 Init-LPTIM2false-HAL-true, 5-MX SPI3 Init-SPI3-false-HAL-true, 6-MX USART1 UART Init-USART1-false-HAL-true, 0-MX PWR Init-PWR-false-HAL-true RCC.ADCFreq_Value=96000000 RCC.AHBFreq_Value=110000000 RCC.APB1Freq_Value=11000000 RCC.APB1TimFreq Value=110000000 RCC.APB2Freq Value=110000000 RCC.APB2TimFreq Value=110000000 RCC.CK48CLockSelection=RCC USBCLKSOURCE MSI RCC.CRSFreq Value=48000000 RCC.CortexFreq Value=110000000 RCC.DFSDMAudioFreq Value=48000000 RCC.DFSDMFreq Value=110000000 RCC.FCLKCortexFreq Value=110000000 RCC.FDCANFreq Value=110000000 RCC.FamilyName=M RCC.HCLKFreg Value=110000000 RCC.HSE VALUE=8000000 RCC.HSI48 VALUE=48000000 RCC.HSI VALUE=16000000 RCC.I2C1Freq Value=110000000 RCC.I2C2Freq Value=110000000 RCC.I2C3Freq Value=110000000 RCC.I2C4Freq Value=110000000 RCC.IPParameters=ADCFreq Value,AHBFreq Value,APB1Freq Value,APB1TimFreq Value,APB2Freq V alue, APB2TimFreq Value, CK48CLockSelection, CRSFreq Value, CortexFreq Value, DFSDMAudioFreq Value, DFSDMFreq_Value, FCLKCortexFreq_Value, FDCANFreq_Value, FamilyName, HCLKFreq_Value, HSE _VALUE,HSI48_VALUE,HSI_VALUE,I2C1Freq_Value,I2C2Freq_Value,I2C3Freq_Value,I2C4Freq_Value ,LPTIM1CLockSelectionVirtual,LPTIM1Freq_Value,LPTIM2CLockSelectionVirtual,LPTIM2Freq_Val ue,LPTIM3Freq_Value,LPUART1Freq_Value,LSCOPinFreq_Value,LSE_VALUE,LSI_VALUE,MCO1PinFreq_ Value, MSIClockRange, MSI_VALUE, OCTOSPIMFreq_Value, PLLM, PLLN, PLLPoutputFreq_Value, PLLQoutp utFreq_Value,PLLRCLKFreq_Value,PLLSAI1M,PLLSAI1N,PLLSAI1P,PLLSAI1PoutputFreq_Value,PLLSA IlQoutputFreq_Value, PLLSAI1RoutputFreq_Value, PLLSAI1Source, PLLSAI2PoutputFreq_Value, PWRF req_Value, RNGFreq_Value, SAI1Freq_Value, SAI2Freq_Value, SDMMCClockSelection, SDMMCFreq_Valu e,SYSCLKFreq VALUE,SYSCLKSource,UART4Freq Value,UART5Freq Value,USART1Freq Value,USART2F req Value, USART3Freq Value, USBFreq Value, VCOInput2Freq Value, VCOInput3Freq Value, VCOInpu tFreq Value,VCOOutputFreq Value,VCOSAI1OutputFreq Value,VCOSAI2OutputFreq Value RCC.LPTIM1CLockSelectionVirtual=RCC LPTIM1CLKSOURCE HSI RCC.LPTIM1Freq Value=16000000 RCC.LPTIM2CLockSelectionVirtual=RCC LPTIM2CLKSOURCE HSI RCC.LPTIM2Freq_Value=16000000 RCC.LPTIM3Freq_Value=110000000 RCC.LPUART1Freq Value=110000000 RCC.LSCOPinFreq Value=32000 RCC.LSE VALUE=32768 RCC.LSI VALUE=32000 RCC.MCO1PinFreq Value=110000000 RCC.MSIClockRange=RCC MSIRANGE 11 RCC.MSI VALUE=48000000 RCC.OCTOSPIMFreq_Value=11000000 RCC.PLLM=12 RCC.PLLN=55 RCC.PLLPoutputFreq_Value=31428571.42857143 RCC.PLLQoutputFreq_Value=110000000 RCC.PLLRCLKFreq Value=110000000 RCC.PLLSAI1M=4 RCC.PLLSAI1N=48 RCC.PLLSAI1P=RCC PLLP DIV17

RCC.PLLSAI1PoutputFreq Value=11294117.647058824 RCC.PLLSAI1QoutputFreq Value=96000000 RCC.PLLSAI1RoutputFreq Value=96000000 RCC.PLLSAI1Source=RCC PLLSAI1SOURCE HSI RCC.PLLSAI2PoutputFreq Value=54857142.85714286 RCC.PWRFreq Value=110000000 RCC.RNGFreq_Value=48000000 RCC.SAI1Freq_Value=11294117.647058824 RCC.SAI2Freq_Value=11294117.647058824 RCC.SDMMCClockSelection=RCC SDIOCLKSOURCE CLK48 RCC.SDMMCFreq Value=4800000 RCC.SYSCLKFreq VALUE=110000000 RCC.SYSCLKSource=RCC SYSCLKSOURCE PLLCLK RCC.UART4Freq Value=110000000 RCC.UART5Freq Value=110000000 RCC.USART1Freq Value=110000000 RCC.USART2Freq Value=110000000 RCC.USART3Freq Value=110000000 RCC.USBFreq_Value=48000000 RCC.VCOInput2Freq Value=4000000 RCC.VCOInput3Freq Value=48000000 RCC.VCOInputFreq_Value=4000000 RCC.VCOOutputFreg Value=22000000 RCC.VCOSAI1OutputFreg Value=192000000 RCC.VCOSAI2OutputFreq Value=384000000 SPI3.BaudRatePrescaler=SPI BAUDRATEPRESCALER 16 SPI3.CalculateBaudRate=6.875 MBits/s SPI3.Direction=SPI DIRECTION 2LINES SPI3.IPParameters=VirtualType, Mode, Direction, BaudRatePrescaler, CalculateBaudRate, DataSiz SPI3.Mode=SPI MODE MASTER SPI3.VirtualType=VM MASTER USART1.FIFOMode=FIFOMODE DISABLE USART1.IPParameters=VirtualMode-Asynchronous,FIFOMode,RXFIFOThreshold USART1.RXFIFOThreshold=RXFIFO THRESHOLD HALFFULL USART1.VirtualMode-Asynchronous=VM ASYNC VP_LPTIM1_VS_LPTIM_counterModeInternalClock.Mode=Counts__internal_clock_event_00 LPTIM1 VS LPTIM counterModeInternalClock.Signal=LPTIM1 VS LPTIM counterModeInternalCl VP VP LPTIM2 VS LPTIM counterModeInternalClock.Mode=Counts internal clock event 00 LPTIM2 VS LPTIM counterModeInternalClock.Signal=LPTIM2 VS LPTIM counterModeInternalCl VP VP PWR VS DBSignals.Mode=DisableDeadBatterySignals VP PWR VS DBSignals.Signal=PWR VS DBSignals VP SYS VS Systick.Mode=SysTick VP SYS VS Systick.Signal=SYS VS Systick board=STM32L562E-DK boardIOC=true isbadioc=false

This file will be used as a template when creating the project.

2.1.2. Creating the Project

Create a new project in *stm32cubeide* from Menu File > New > STM32Project from an Existing

STM32CubeMX Configuration file (*.ioc) with selecting the ptxTunneling.ioc file in the dialog window. After specifying a name to the project, it can be generated by clicking on the **Finish** button. If the requested SDK version has not been downloaded yet, this process may take a few minutes to complete.

DE STM32 Project Fro	m Existing STM32CubeMX Configurati	. –					
			IDE				
Setup STM32 projec	:						
STM32CubeMX .ioc	ile						
File: C:\Work\ptxTur	neling.ioc		Browse				
Project							
Project Name: demo							
Use default locati	on						
Location: C:/W	ork/wsE_eclipse/STM32CubeIDE/mole		Browse				
Options							
Targeted Language	Targeted Language						
● C ○ C++							
Targeted Device Usage							
Enable TrustZo	ne						
Targeted Binary Ty	96						
Executable	Static Library						
Targeted Project Ty	pe						
• STM32Cube	Empty						
? < <u>B</u> ack	<u>N</u> ext > <u>F</u> inish		Cancel				

2.2 Importing the Library

There is no difference whether the source or the precompiled package is being used: the library archive must be imported to the project using **File > Import > Archive File**.

To keep the folder structure clean, the library will be imported to the PtxTunneling subfolder by appending it to the default location displayed in following figure.

Inport		-			×
Archive file Import the contents of an archive file in zip o	r <mark>t</mark> ar format fr	om the local file system.			D,
From archive file: C:\Work\ptxTunnelingLib-v	1.0.0.src.tar.gz	· · · · · · · · · · · · · · · · · · ·	•	Browse.	
✓ ✓ ✓ > ✓ ▷ > ✓ ▷ > ✓ ▷ > ✓ ▷ > ✓ ▷ > ✓ ▷ Filter Types Select All D	eselect All	 Image: Image: Claring format Image: CMakeLists.txt Image: DISCLAIMER Image: Image: Image: Optimized and the second and			~
Into folder: demo/PtxTunneling				Bro <u>w</u> se.	
Qverwrite existing resources without warning	ng				
?	< <u>B</u> ack	Next > Einish		Cancel	

In the case where the library will be used in source form, the subfolder PtxTunneling and PtxTunneling/src folders must be included in the build. This can be done by opening the context menu with a right-mouse click on the folder name in the **Project Explorer** and selecting **Properties**. The checkbox **Exclude resource from build** found in **C/C++ Build > Settings** must be unchecked as displayed in the following figure.

DE Properties for src	$ \Box$ \times
type filter text	Settings $\diamond \star \star$
> Resource	
✓ C/C++ Build	Configuration: [All configurations]
Settings	
Run/Debug Settir	Exclude resource from build
	 Toolchain Version
	Select what toolchain to use
	Default
	○ Fixed
	Type GNU Tools for STM32
	Version 7-2018-q2-update ~
	Toolchain location: \${gnu_tools_for_stm32_compiler_path}
< >	Restore <u>D</u> efaults <u>Apply</u>
?	Apply and Close Cancel

2.2.1. Adding the Include Path

In order for the compiler to find the header (.h) files containing the API functions, the library folder inc must be added to the list of user-defined include directories. This can be done by navigating to **Project > Properties >** C/C++ Build > Settings > Tool Settings > MCU GCC Compiler > Include paths. Next, click on the Add button on the right side of the small toolbar and use the **Workspace** button in the popup window to locate the folder.



2.2.2. Adding the Library File

This step is required only if you are working with the precompiled binary package. Since there is no source code to be compiled, the linker must be able to find the functions in the library. In the same dialog window, changing to **MCU GCC Linker > Libraries** section, the PtxTunneling/lib folder can be added to the list of folders (lower pane) where the compiler is looking for external libraries. Additionally, the exact library needs also to be specified (upper pane) by its name PtxTunneling. From this the compiler will automatically find the static library file libPtxTunneling.a.

DE Properties for den	no				×	65 (2)
type filter text	Settings			⇔ ▼ 0	⇒ ▼	•
Resource Builders	 Toolchain Version ✤ Tool Setti 	ngs 🎤 Build Steps 😤 Build Artifact	Binary Parsers	♀ Error ◀	•	^
✓ C/C++ Build	🖉 MCU Settings	Libraries (-I)	4	🔊 🔊 🖗 🖗	21	
Build Variables	MCU Post build outputs	PtxTunneling		13		
Environment	➤ ⑧ MCU GCC Assembler			Add		
Logging	🖉 General					
Settings	🖉 Debugging					
> C/C++ General	Preprocessor					
CMSIS-SVD Settir	Include paths					
Project Reference:	Miscellaneous					
Run/Debug Settir	✓ [™] MCU GCC Compiler					
	🖉 General					
	🖉 Debugging					
	Preprocessor					
	Include paths					
	Øptimization				-	
	🖉 Warnings	Library search path (-L)	4	1 🔊 🕲 🖗 🕯	21	
	Miscellaneous	"\${workspace_loc:/\${ProjName}/Ptx	Funneling/lib}"			
	✓ [™] MCU GCC Linker					
	🖉 General					
	🐸 Libraries					
< >	Miscellaneous					~
1		Ар	ply and Close	Cancel		

2.3 Implementing the HAL

The library functions cannot access the underlying hardware or software resources; they require to access the Hardware Abstraction Layer (HAL) which then performs the requested action. Since this layer depends on the specific hardware configuration, it must be implemented for the exact setup.

The PtxTunneling library includes the header file <u>ptx_tunneling_hal.h</u>. It contains all the functions that must be provided by the host platform.

For the current case there should be the file ptx_tunneling_hal.c created in the source code folder Core/Src with the following content.

PTX Tunneling Library v1.4.1 for STM32CubeIDE QuickStart Manual

/*
SPDX-License-Identifier: BSD-3-Clause
Copyright (c) 2024, Renesas Electronics Corporation and/or its affiliates
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1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer.
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Project : PtxTunneling Module : HAL
File : ptx_tunneling_hal.c
Description : Implementation of HAL for tunneling */ /*
* ####################################

<pre>#include <assert.h> #include <cmsis_compiler.h> #include <string.h></string.h></cmsis_compiler.h></assert.h></pre>
#include "main.h" // for GPIO/SPI/Timer names #include "stm32l5xx.h"
<pre>#include "ptx_tunneling_hal.h"</pre>
/*

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```
struct ptxHal
UART HandleTypeDef *hUart.
extern SPI_HandleTypeDef hspi3;
static uint8 t uartRxBuf[2048];
static uint16 t writePos = 0;
static uint8 t rx[COMMS MAX MESSAGE LENGTH];
void startUartReceiving(UART HandleTypeDef *huart)
   hUart = huart;
   HAL StatusTypeDef st = HAL UART Receive IT(huart, rx, 1);
void HAL_UART_RxCpltCallback(UART_HandleTypeDef *huart)
    if (rxi != 0 || rx[rxi] == CMD_CODE_TUNNELING_MSG)
       rxi++;
```

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```
if (rxi >= COMMS HEADER SIZE)
        uint16_t packLen = COMMS HEADER SIZE +
                           (rx[OFFSET CMD LENGTH BYTE] == 0 ? 256 :
rx[OFFSET CMD LENGTH BYTE]);
       if (rxi >= packLen)
            memcpy(uartRxBuf + writePos, rx, rxi);
            writePos += rxi;
   HAL UART Receive IT(huart, &rx[rxi], 1);
bool ptxTunneling GPIO IsIrqPinAsserted(ptxHal t *context)
   return HAL GPIO ReadPin(PTX IRQ GPIO Port, PTX IRQ Pin) == GPIO PIN SET;
int ptxTunneling UART rxLength(ptxHal t *context)
   UNUSED (context);
   const count = writePos - readPos;
int ptxTunneling_UART_read(ptxHal_t *context, uint8_t *buf, unsigned int len)
   UNUSED (context);
     disable irq();
   int readCount = writePos - readPos;
   if (readCount > len)
       readCount = len;
   memcpy(buf, uartRxBuf + readPos, readCount);
    readPos += readCount;
   if (readPos == writePos)
       readPos = 0;
       writePos = 0;
    __enable_irq();
```

PTX Tunneling Library v1.4.1 for STM32CubeIDE QuickStart Manual

```
int ptxTunneling UART write(ptxHal t *context, const uint8 t *buf, unsigned int len)
   UNUSED (context);
   HAL StatusTypeDef res = HAL OK;
            res = HAL UART Transmit(hUart, buf, len, 1000);
        } while (res == HAL TIMEOUT);
        assert(!res);
void ptxTunneling Timer stopwatchStart(ptxHal t *context, ptxTimeDiff t *startVal)
    *startVal = HAL GetTick() * 1000;
void ptxTunneling Timer stopwatchStop(ptxHal t *context, ptxTimeDiff t *startStopVal)
    *startStopVal = HAL GetTick() * 1000 - *startStopVal;
void ptxTunneling Timer ThreadSleep(ptxHal t *context, uint32 t msSleep)
   HAL Delay(msSleep);
void ptxTunneling NVIC disableInterrupts()
    ___disable_irq();
void ptxTunneling NVIC enableInterrupts()
   __enable_irq();
int ptxTunneling SPI trx(ptxHal t *context, uint8 t *const txBuf[], const size t
txLen[],
   const uint32 t spiTimeout = 100000;
   HAL_StatusTypeDef st = HAL ERROR;
   HAL GPIO WritePin(SPI3 NSS GPIO Port, SPI3 NSS Pin, GPIO PIN RESET);
   if ((NULL != txBuf) && (NULL != txLen))
        while (index < numBuffers)</pre>
```



Note: This implementation is specific to the ST32L562E-DK board and is not guaranteed to work on any other hardware.

2.4 Calling the Library Functions

The main loop will provide the tunneling functionality by calling the library's superloop function, the ptxTunneling_poll(). This function performs the data processing and translation, and also the SPI communication. The **main()** function can be found in the Core/Src/main.c file. Update this file with the following code:



2.5 Building the Firmware

After the source files have been created, the project can be built with the **Project > Build Project**. When the build process has finished successfully, a table similar to the following will show with the footprint sizes.

arm-none-eabi-size --format=berkeley "demo.elf" text data bss dec hex filename 23460 124 7620 31204 79e4 demo.elf

3. Preparing the Hardware

To demonstrate the usage of the tunneling functionality, a PTX evaluation board must be connected to the ST32L562E Evaluation Kit through the PMOD connector.



Before powering up the PTX evaluation board from the USB-C port, it is important to remove the jumper named **pmod 3v3** and set the **Serial Interface switches** to **"0"** state to select the SPI communication protocol.

The ST32L562E-DK board must be connected to the host PC via the **CN17 STLNK** USB connector. This connection provides both a UART interface named **STMicroelectronics STLink Virtual COM Port** (used in PTX100x * Config Tool) and access to the on-board ST-Link debugger.



3.1 Debug Configuration

In order to upload the firmware onto the device, the Debug configuration must be created from the **Run > Debug Configurations**. Please create a new configuration (if not yet present) for the **STM32 Cortex-m C/C++ Application**. The most important settings are:

- Select the Debug/demo.elf application from the project
- Select ST-LINK (ST_LINK GDB server) among the debug probes

When the settings are updated, pressing the **Debug** button initiates the debug session with flashing the firmware onto the chip.



The firmware execution will halt at the main function by default; F8 must then be pressed to continue the execution.

4. Using the Tunneling Feature

To use of the tunneling functionality, the **PTX100x** * **Config Tool** must be started and configured to use the USB serial communication port (identified in Device manager previously) by selecting the correct entry in the dropdown list in toolbar.

🛟 РТХ	(100x	POS C	onfig Tool	0.0						
File	Edit	He	lp							
	8	7	Generate DAT files	Generate C files	۵	ŝ	a	Evalboard	COM9	~
Module	es					ð	VE)PA Calibrati	<none> COM9 COM10</none>	63

The configuration is now ready. Any test started will communicate with the PTX100x via the tunneling firmware.

5. Revision History

Revision	Date	Description
1.01	Jun 18, 2024	Updated license text in ptx_tunneling_hal.c file.
1.00	Jan 15, 2024	Initial release.

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