RICBox GUI Software for FemtoClock3

This document explains how to use the Renesas IC Toolbox (RICBox) software to configure and control FemtoClock3 devices. For general instructions about RICBox, see RICBox Software Manual.

Contents

1. Installation and Setup

Ensure that the latest version of the RICBox software is installed on your computer. New versions are released frequently and can provide a better experience with the latest functionality. The RICBox software can be installed directly from the RICBox product page on the Renesas website.

For instructions on how to install the latest version of RICBox, device plugins, and maintain updates, please see the RICBox Software Manual sections 1 and 11.

2. Loading and Creating Configurations

2.1 Creating a new Configuration

1. Start > RICBox.
2. Click Create New Project.

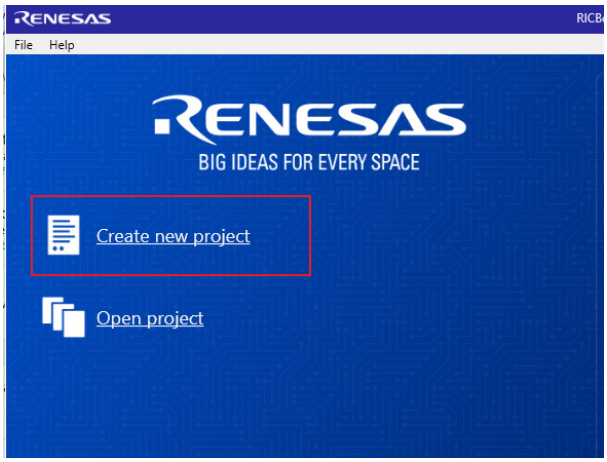

Figure 1. Open New Project in RICBox

3. Use the **Select a Product Family** box to choose the “FemtoClock3” devices.
4. Select the variant being evaluated and click **OK**. In this example the RC32312A is used.

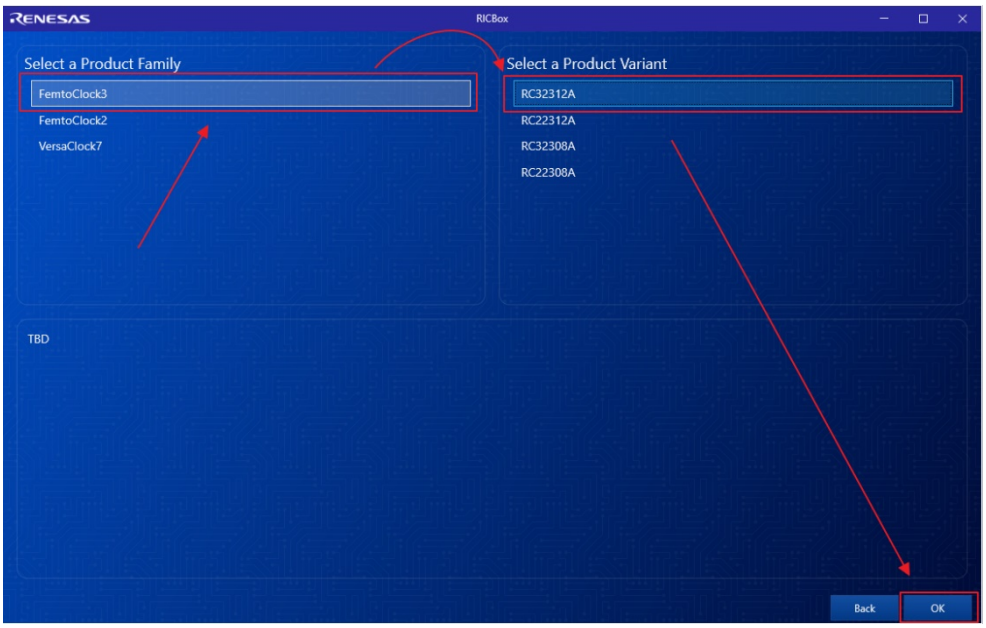

Figure 2. Selecting RC32312A Device GUI in RICBox

2.2 Loading a Settings File

Loading a settings file is like creating a new one.

1. To load an existing settings file, click on the **Browse** button just after opening the RICBox software. This will take you to a file browser.

   Note: Recently used settings files are located under the “Recent Files” section.

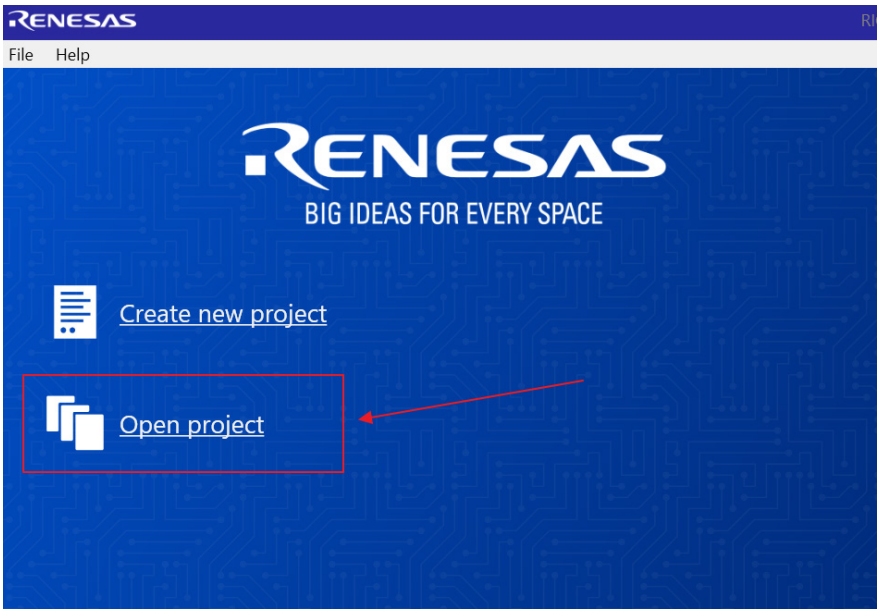

Figure 3. Open Existing Project

2. Navigate to the directory that stores the settings file and select it. RICBox settings files have the file type “.rbs”.

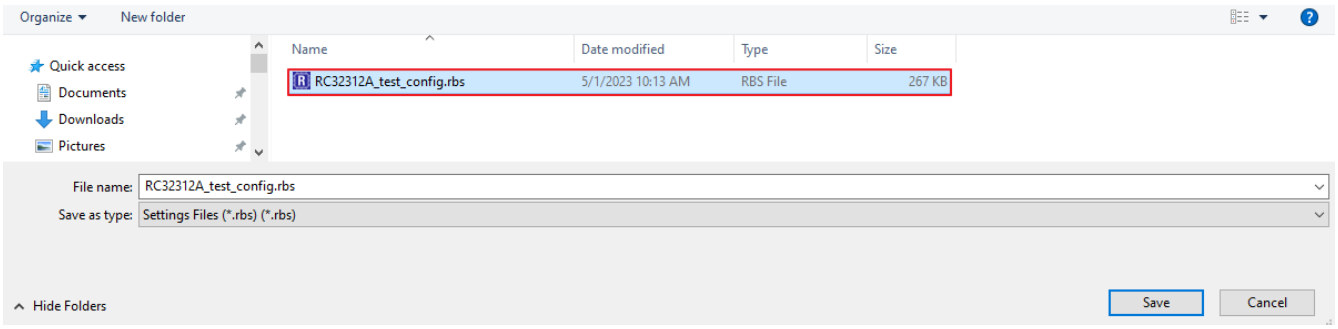

Figure 4. Select rbs File

2.3 Adding Configurations to a Settings File

More than one device configuration can be created at a time. Different configurations can hold differing device settings but still be saved to the same RICBox settings file (.rbs).

1. In the lower-right corner of a plugin GUI, click on the part number box to view the configuration selection drop-down menu.

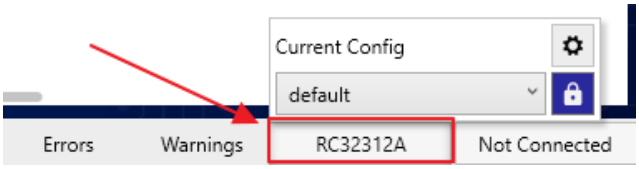

Figure 5. Configuration Menu

Use this menu to change the currently active configuration. The initial configuration is always labeled *default*.

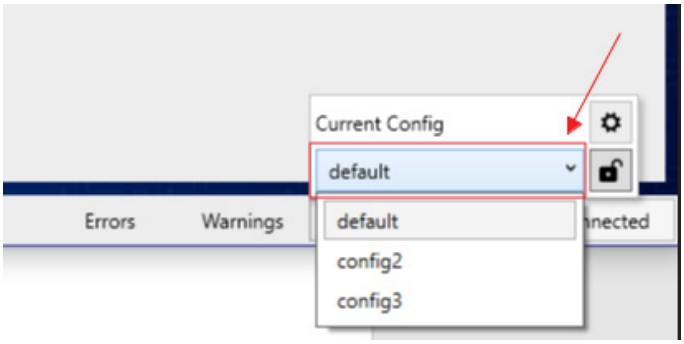

Figure 6. Configuration Selection

2. Click on the settings button to view the configurations pop-up menu.

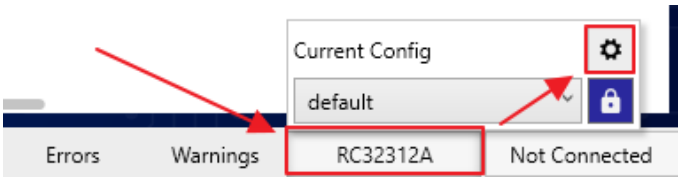

Figure 7. Configuration Settings

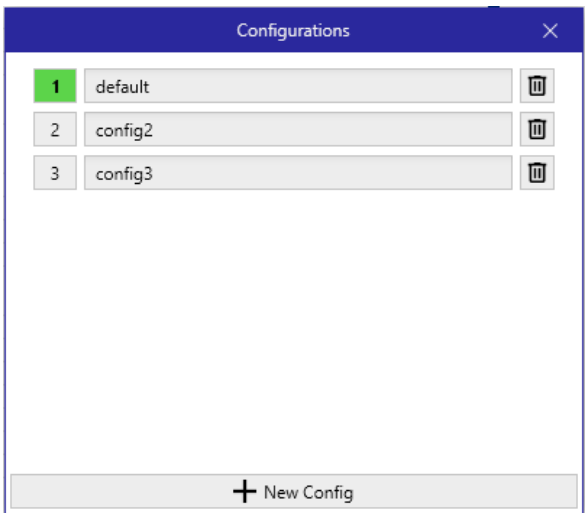

Figure 8. Configurations Pop-up Menu

3. Click the numbers to change the currently active configuration. Green is the active configuration.

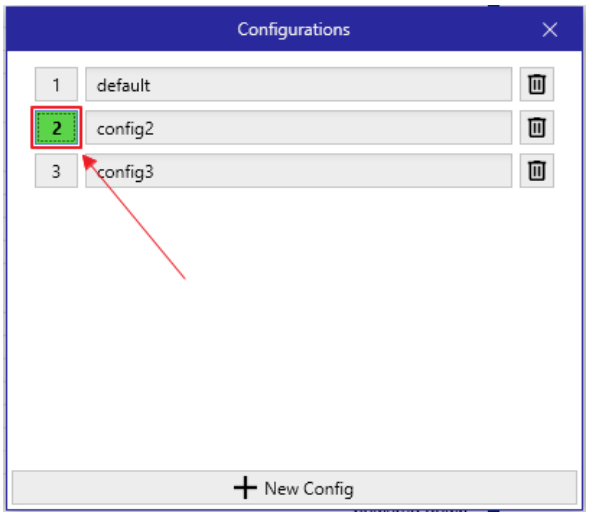

Figure 9. Currently Active Configuration

3. Wizard Setup

3.1 Inputs

The first page in the wizard setup is for configuring input clocks. This section is divided between the crystal input and the clock inputs. The DPLL operation mode can be set to Jitter Attenuation, Synthesizer, or DCO modes. The input clocks are only available in Jitter Attenuation mode.

Note: Some devices may not have both Jitter Attenuator and DCO modes together.

The crystal frequency corresponds to the input frequency to the XIN pin, which can be configured from 25MHz to 80MHz. Crystal load capacitance can be configured internally. This can range from 8.24pF to 10.1451pF, where 8.24pF is the measured stray capacitance of the device package and evaluation board.

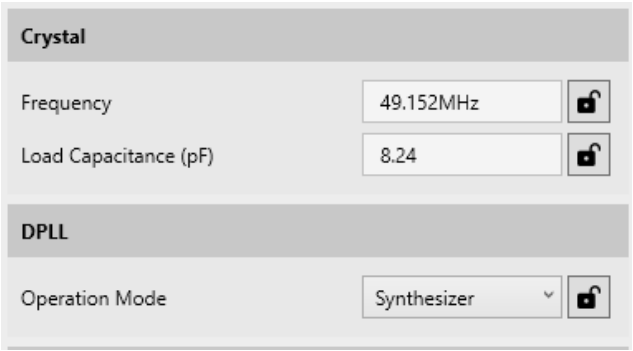

Figure 10. Wizard Crystal Configuration

Note: Leaving the value at 8.24pF will turn the internal tuning capacitors off.

Input clocks are only functional when the DPLL is in Jitter Attenuation mode. Use the input clocks section to set up the input clock frequency, assign a corresponding reference, and set input clock signal type (input mode).

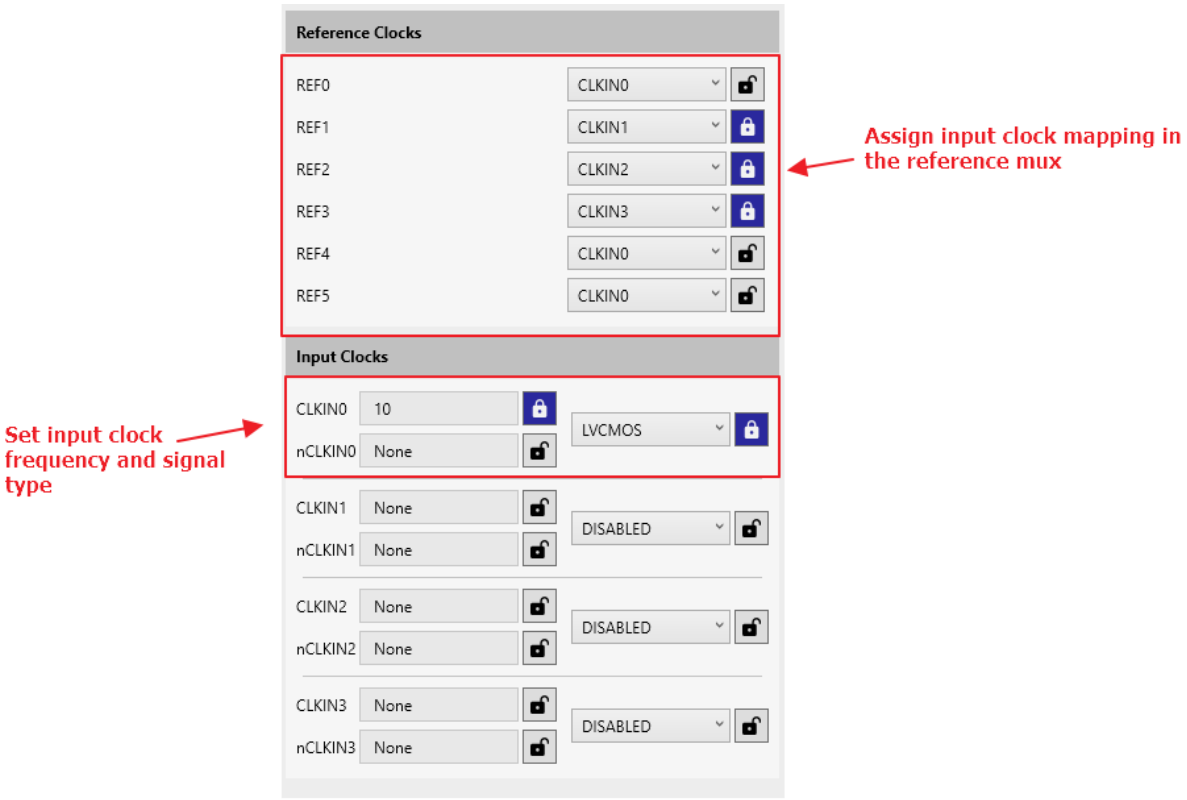

Figure 11. Wizard Input Configuration

3.2 DPLL

The DPLL section is only available when the device is configured for Jitter Attenuation mode. The DPLL section enables manual adjustment of the bandwidth, decimator, gain peaking, and phase slope limit values. Alternatively, there is the option to select a predefined SyncE profile that will automatically populate the adjustable settings.

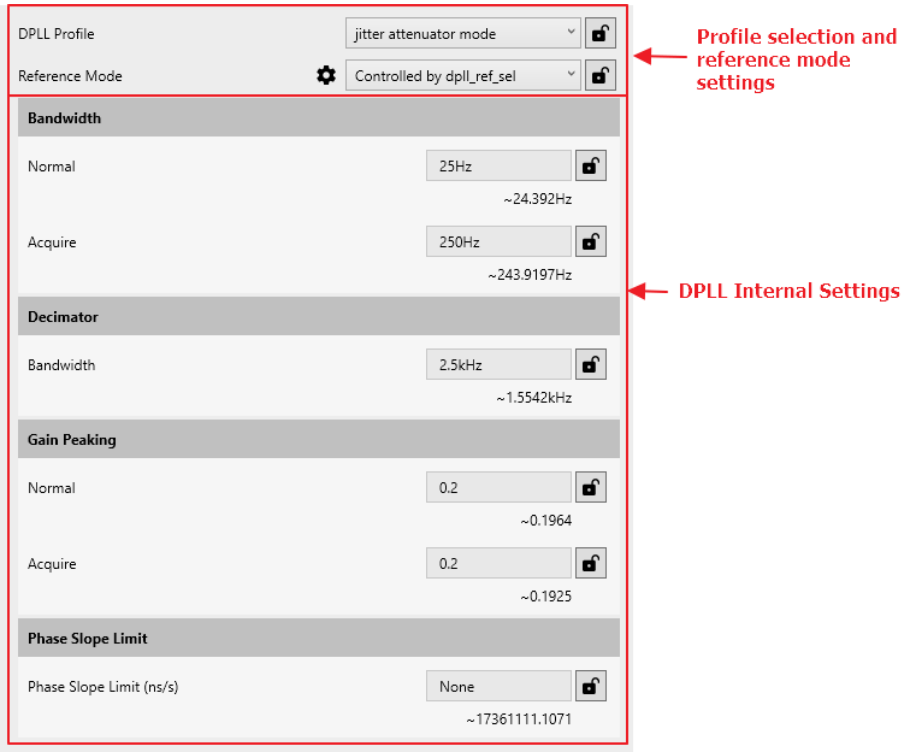

Figure 11. Wizard DPLL Configuration

The DPLL reference mode can be changed between manual and automatic selection. The manual reference can also be selected by clicking the settings button next to the Reference Mode dropdown menu.

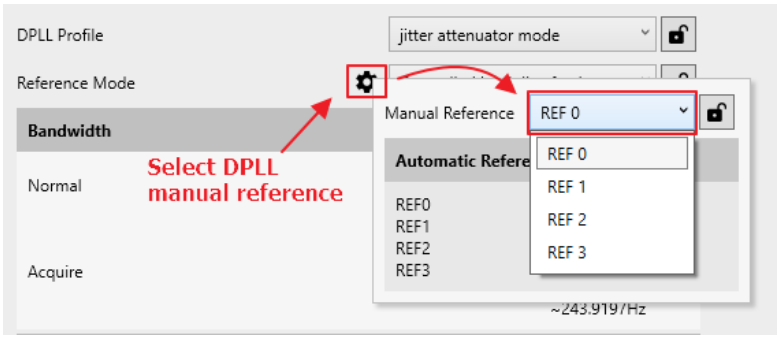

Figure 12. Wizard Manual Reference Configuration

3.3 Outputs

The output section of the Wizard can be used to configure the VCO frequency, output frequency, output type settings, and output voltage/amplitude settings.

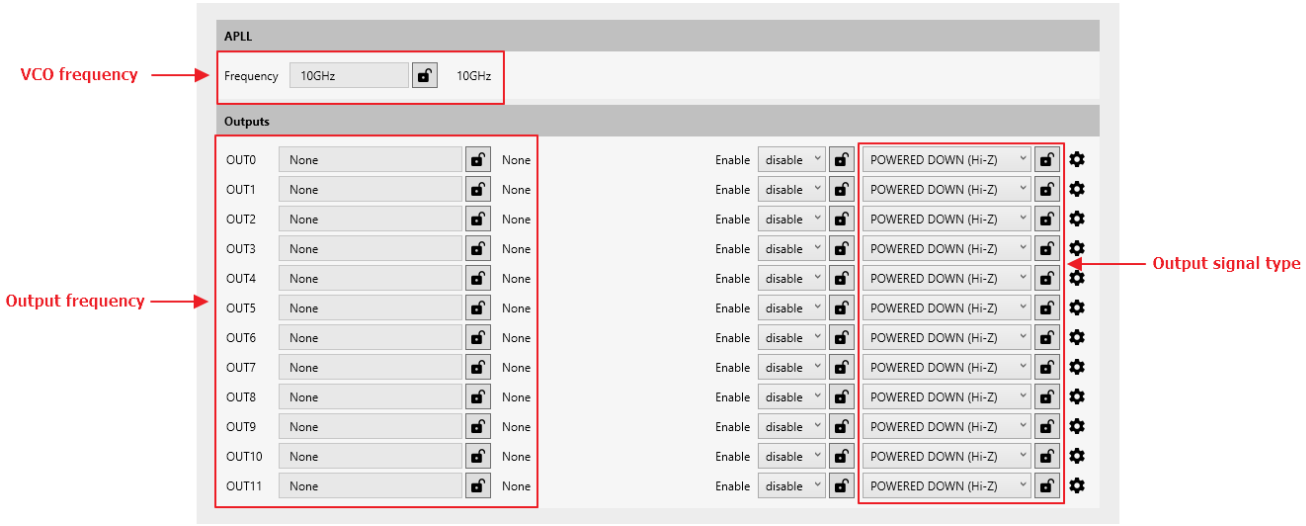

Figure 13. Wizard Outputs Configuration

To adjust the output voltage/amplitude settings, click on the settings button next to each of the output type selection menus.

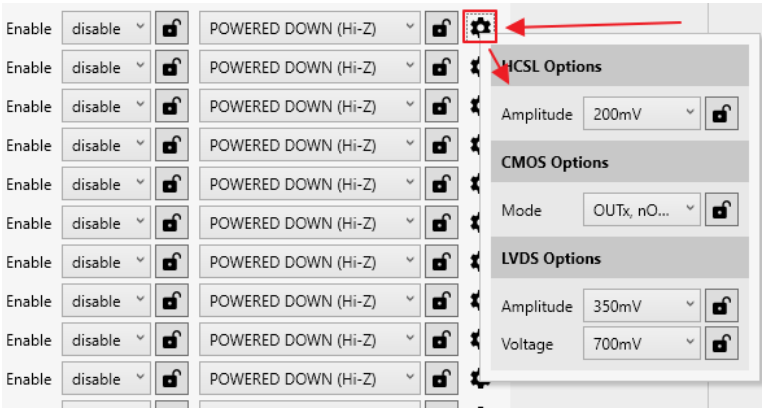

Figure 14. Wizard Output Voltage/Amplitude Configuration

Click the **Finish** button at any time to exit Wizard View.

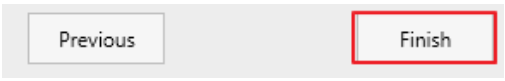

Figure 15. Wizard Finish Button

4. Side Panel Buttons

The side panel consists of five separate buttons. Each button opens a separate page. Each page has a unique view, allowing the configuration of the device from different perspectives.

- **Control Panel** button opens the device overview page.
- **Wizard** button opens the initial wizard page.
- **Configuration** button displays the register settings in a readable text format with a search engine.
- **Registers** button shows a graphic of the registers in the device.
- **Block Diagram** button opens a configurable block diagram view

Figure 16. Side Panel Buttons

5. Control Panel View

The control panel view displays an overview page depicting a device's major settings. This page can be used as an important reference for the overall device configuration.

RC32312A	3.1.0
Settings	
Dash Code	
Mode	
Current Mode	JA
Inputs	
XIN	49.152MHz
CLKIN0	10MHz
CLKIN1	None
CLKIN2	None
CLKIN3	None
nCLKIN0	None
nCLKIN1	None
nCLKIN2	None
nCLKIN3	None
SysClock	
Quad sys clock	~227.2727MHz
Outputs	
OUT0	disabled (Hi-Z/Hi-Z)
OUT1	disabled (Hi-Z/Hi-Z)
OUT2	disabled (Hi-Z/Hi-Z)
OUT3	disabled (Hi-Z/Hi-Z)
OUT4	disabled (Hi-Z/Hi-Z)
OUT5	disabled (Hi-Z/Hi-Z)
OUT6	disabled (Hi-Z/Hi-Z)
OUT7	disabled (Hi-Z/Hi-Z)
OUT8	disabled (Hi-Z/Hi-Z)
OUT9	disabled (Hi-Z/Hi-Z)
OUT10	disabled (Hi-Z/Hi-Z)
OUT11	disabled (Hi-Z/Hi-Z)
APLL	
APLL Frequency	10GHz (-0.006ppt from goal of 10GHz)
Divider	~203.4505
Loop Bandwidth	~691.3361kHz
Phase Margin	~78.7392 degrees
DPLL	
Enabled	yes
DPLL Profile	JAMODE (jitter attenuator mode)
DPLL Frequency	10GHz
Divider	500
Normal Bandwidth	~24.392Hz
Acquire Bandwidth	~243.9197Hz
Decimator Bandwidth	~1.5542kHz
Normal Gain Peaking	~0.1964 (-1.776% from goal of 0.2)dB
Acquire Gain Peaking	~0.1925 (-3.7496% from goal of 0.2)dB

Figure 17. Control Panel View

6. Configuration View

Configuration View enables easy movement through register settings via the tabs at the top of the page. Each section has all the critical registers and data fields listed to configure the device block.

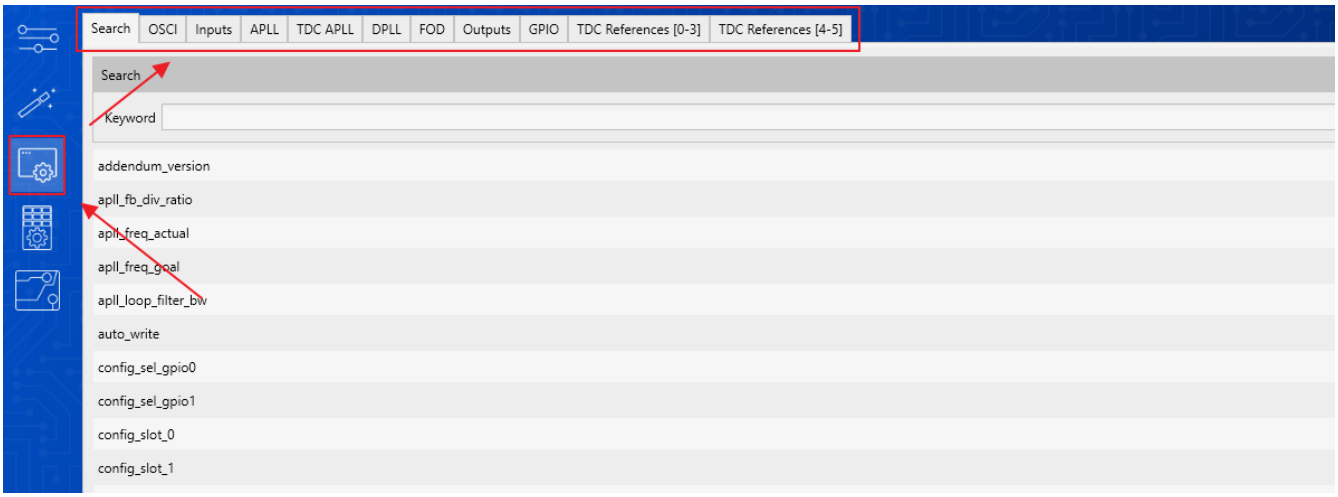

Figure 18. Configuration View

The Search tab provides access to the configurable fields through a search bar. The search function can be used to find any specific configurable field.

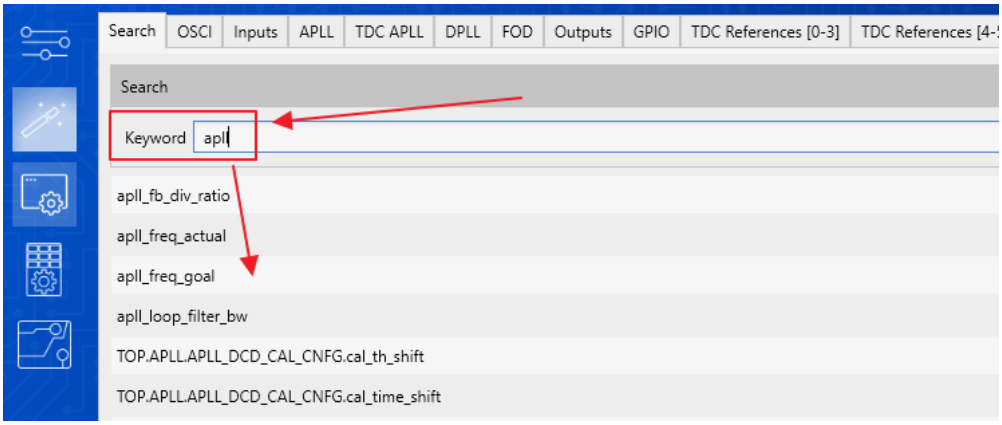

Figure 19. Search for Registers

7. Register View

The Register View shows a graphical diagram of the registers and enables reading or writing any of any register. By clicking on the individual register block, the given registers for that block will appear to the right. They can be adjusted by writing directly to the diagram, or entering values into the data fields on the right.

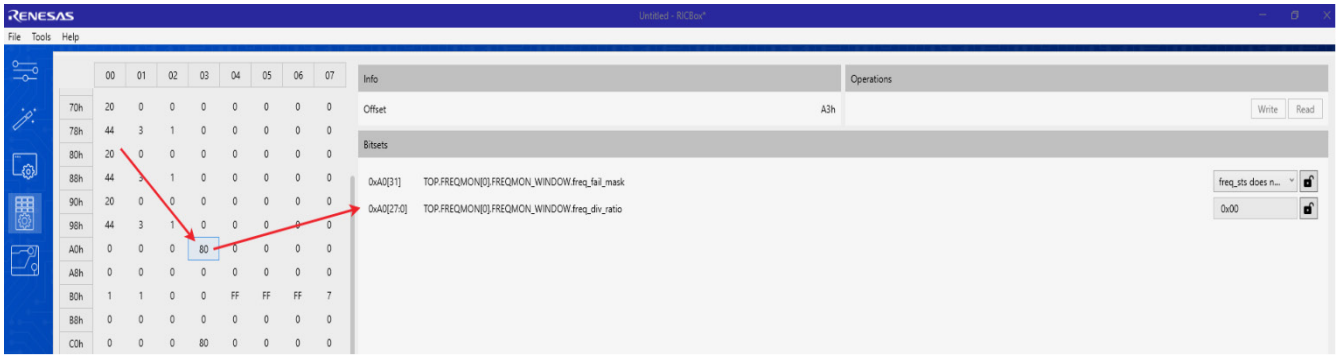

Figure 20. Register View

8. Block Diagram View

The Block Diagram view shows the datasheet representation of the FemtoClock3 devices. The main diagram enables adjustment of the operation mode, setting the output frequency, setting the XIN frequency, setting the input frequencies, and viewing the output frequency estimate. Each block has its own pop-out page. This can be accessed by clicking on the block.

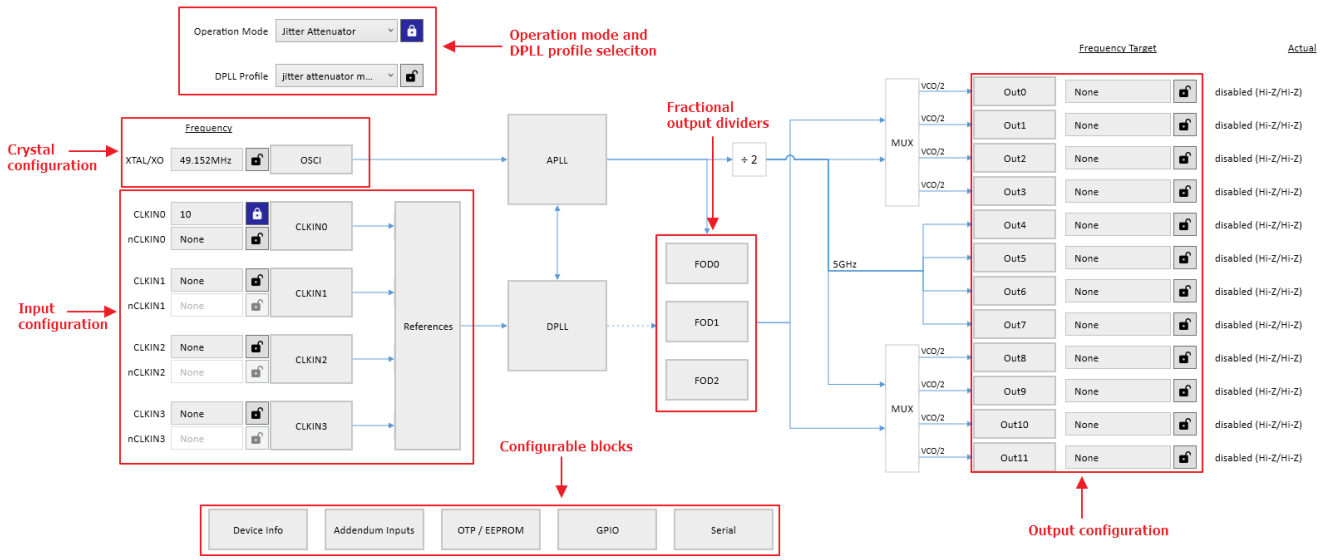

Figure 21. Main Block Diagram

8.1 OSCI Block

Similar to the Inputs section of the wizard view, the OSCI Block can be used to control the crystal frequency and the input lock capacitance.

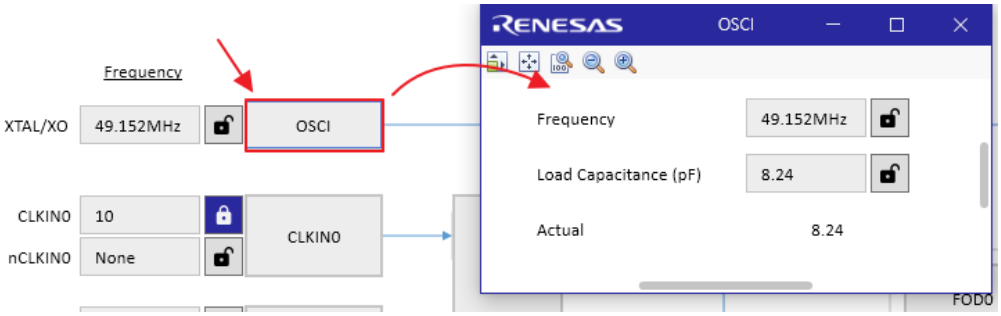

Figure 22. OSCI Block

8.2 APLL Block

The APLL Block gives access to the crystal frequency, VCO frequency, low pass filter (LPF) resistor, and feedback divider. The feedback divider is automatically calculated by the software when the VCO frequency and crystal frequency are set.

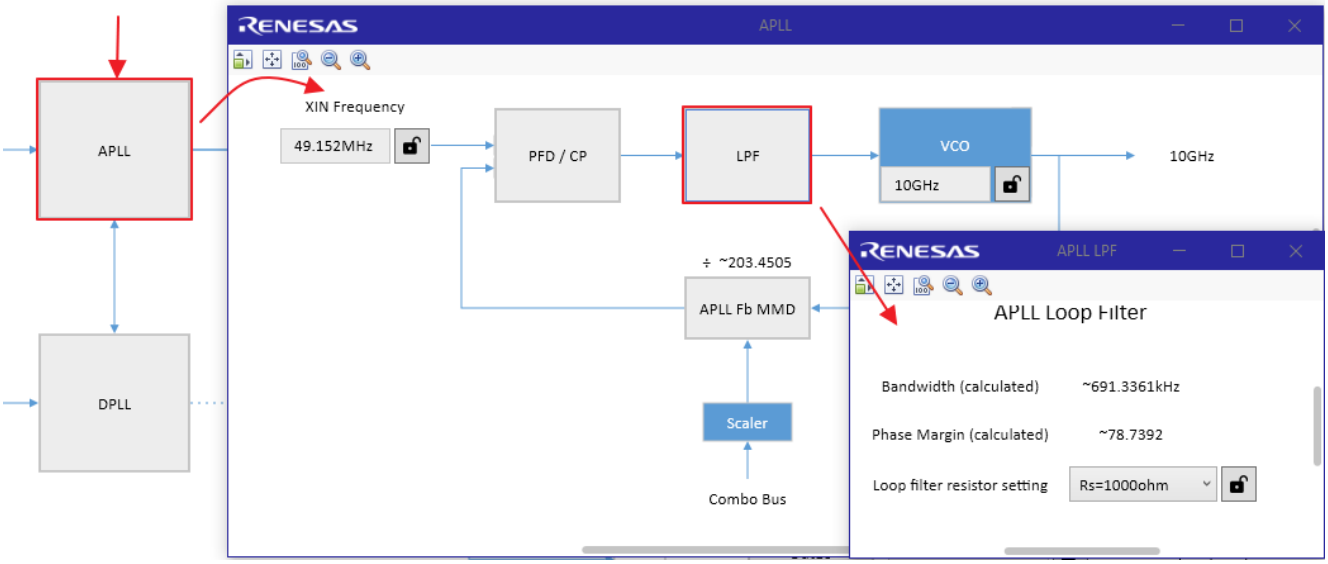

Figure 23. APLL Block

8.3 Outputs Block

The Output Block consists of the output reference selection, integer output divider (IOD), and output signal type selection.

Output references can be selected between FODs and VCO/2. This indicates the input frequency that is divided down by the IOD. The input reference is displayed on the main diagram.

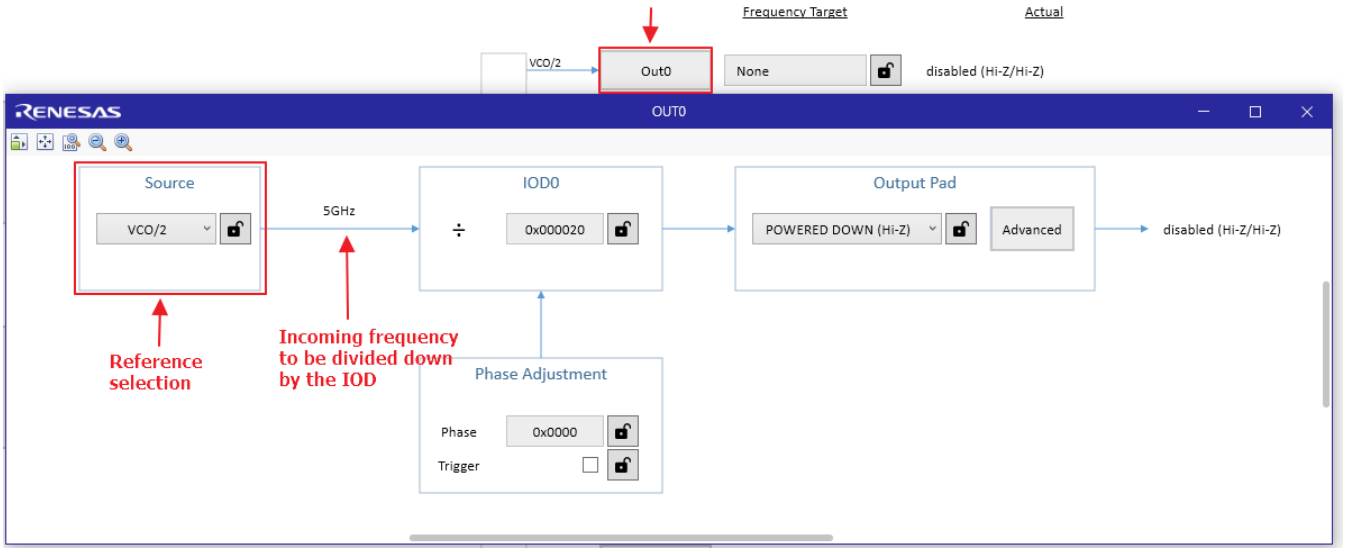

Figure 24. Output Block

Note: Out 4 to Out 7 can only reference VCO/2.

Output frequency can range from 1MHz to 1GHz for differential signals and 1MHz to 250MHz for single-ended signals. Output type can be selected between LVDS, HSCL, and CMOS.

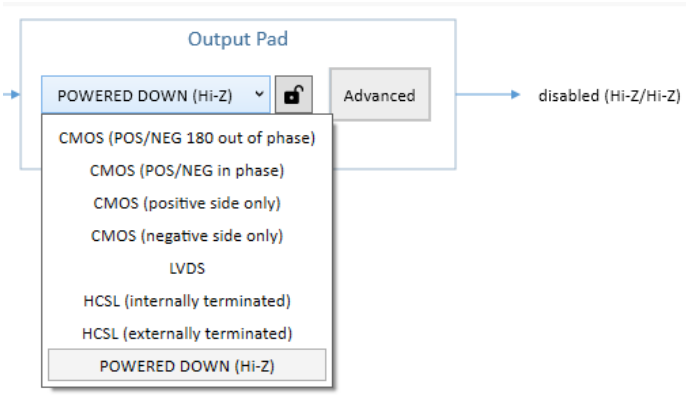

Figure 25. Output Signal Type Selection

The Advanced Block allows for configuring the output frequency, disabled states, terminations, and voltage/amplitude settings. The Enable Source section dropdown menu selects how the output enable is controlled, either through GPIO or register setting.

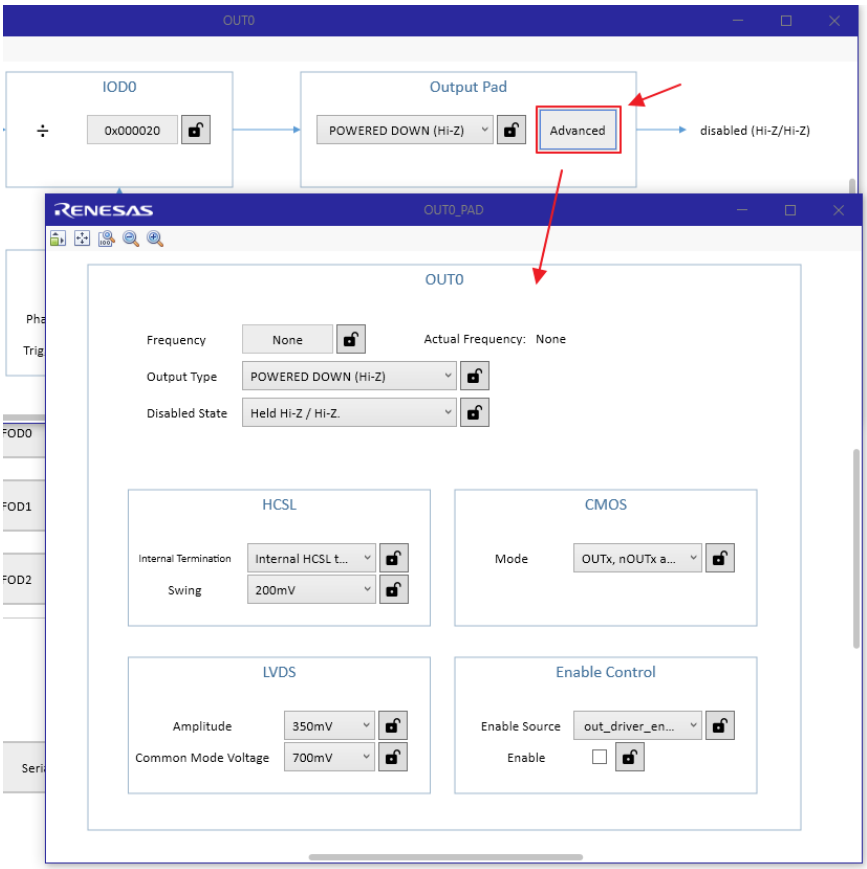

Figure 26. Output Signal Advanced Settings

8.4 FOD Block

The FOD Block is used to control the fraction output dividers. The page shows settings for FOD output frequency, FOD mode, and the fractional output divider.

The FOD input reference is the VCO frequency. FOD output frequency ranges from 120MHz to 700MHz. The divider is automatically calculated by the software when the FOD frequency is set.

FOD mode can be chosen between Synchronous, Synthesizer, and DCO. A FOD in Synchronous mode tracks the input phase and frequency accuracy from the DPLL. Synthesizer mode allows the FOD to track the phase and frequency accuracy from the APLL only (free run). DCO mode allows for frequency control words to be written to the FOD to offset the outputs by a specified frequency.

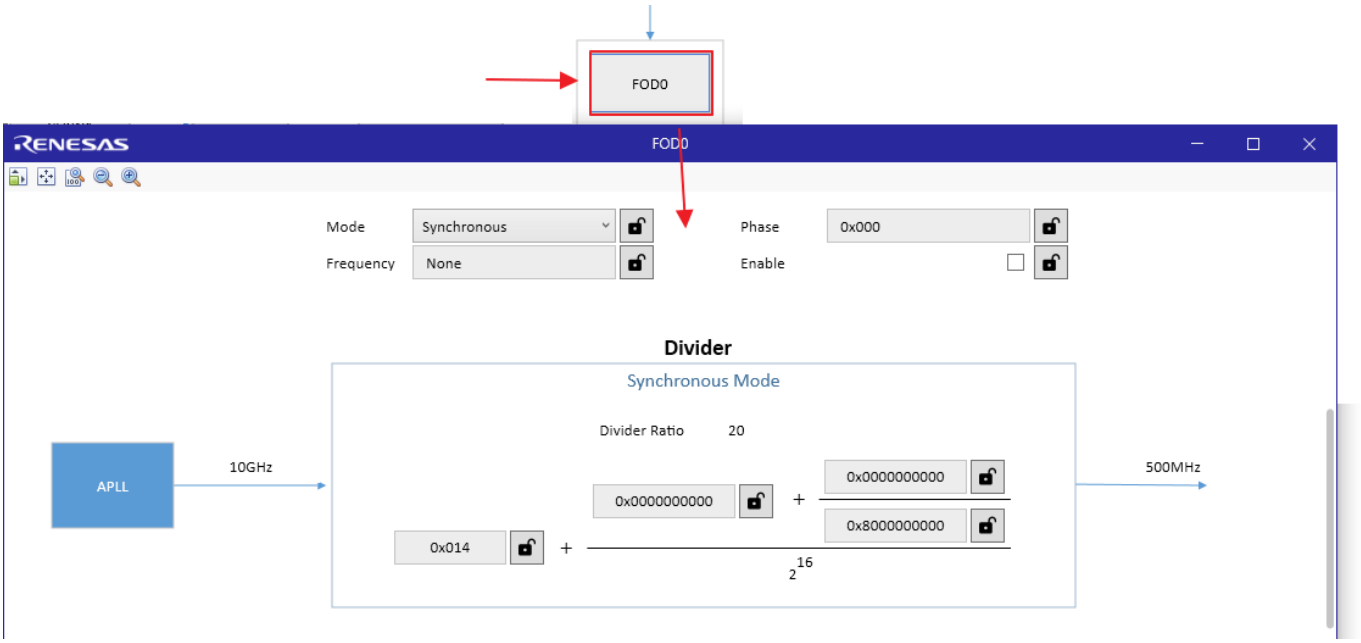

Figure 27. FOD Block

Note: The FOD feedback divider registers change between synthesizer and synchronous modes.

8.5 CLKIN Inputs Block

Clicking on the CLKINx Block allows the control of the input signal type selection, input frequency, and AC-coupling.

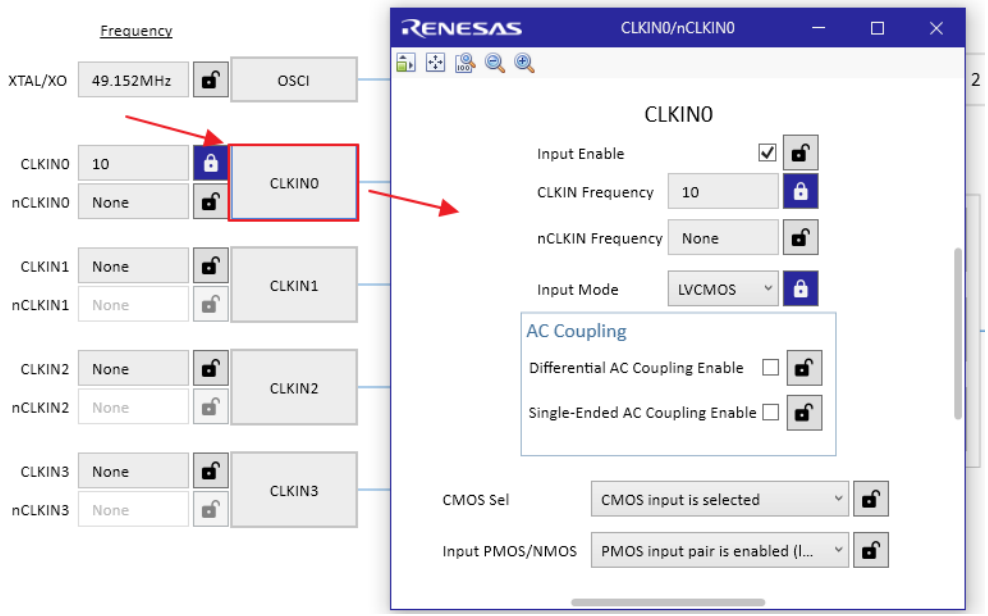

Figure 28. CLKIN Block

8.6 References Block

Clock inputs are connected to a mux to determine which reference each clock corresponds to. The user can choose between references 0-3 as its input.

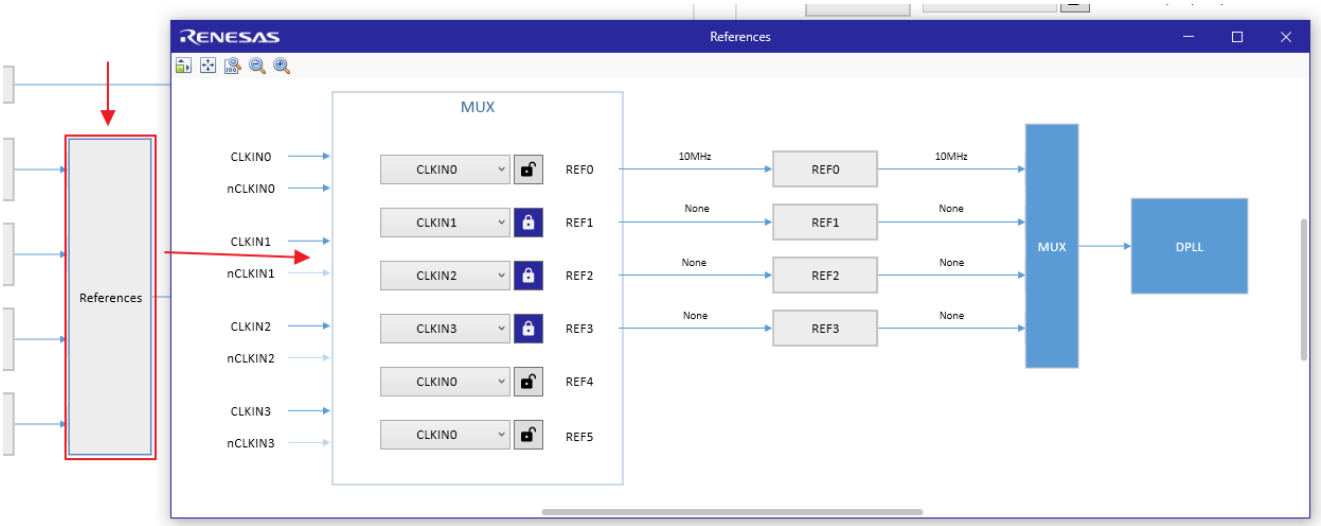

Figure 29. References Block

References must be divided down below 33MHz for the DPLL to lock to them. The input reference divider is accessible through the REF buttons. Clock loss of signal and frequency monitors are available through the Clock Monitor Button.

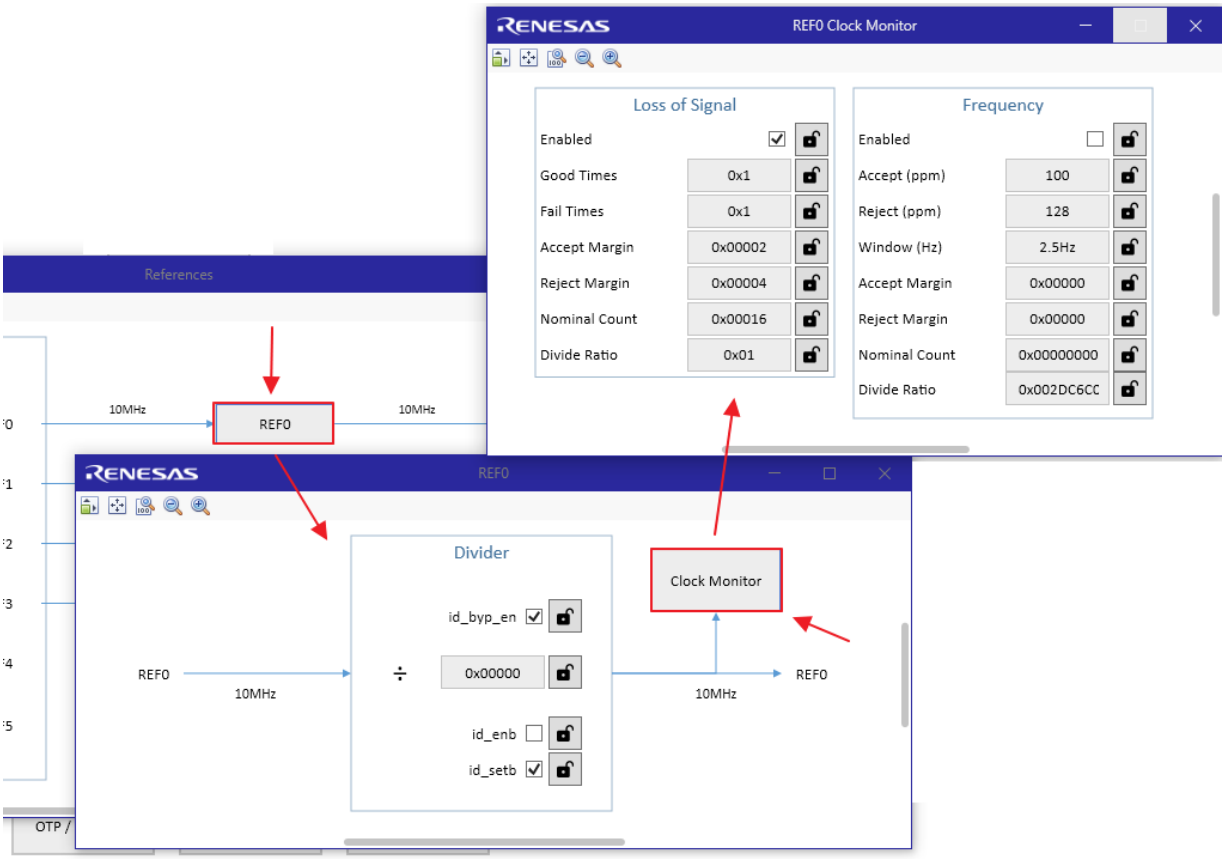

Figure 30. Advanced Reference Settings

8.7 DPLL Block

The DPLL Block is accessible only when the device operation mode is set to Jitter Attenuator. This block contains all features pertaining to the DPLL. Clicking on the DPLL block enables revertive or hitless switching, reference selection, and the ability to change the digital loop filter settings.

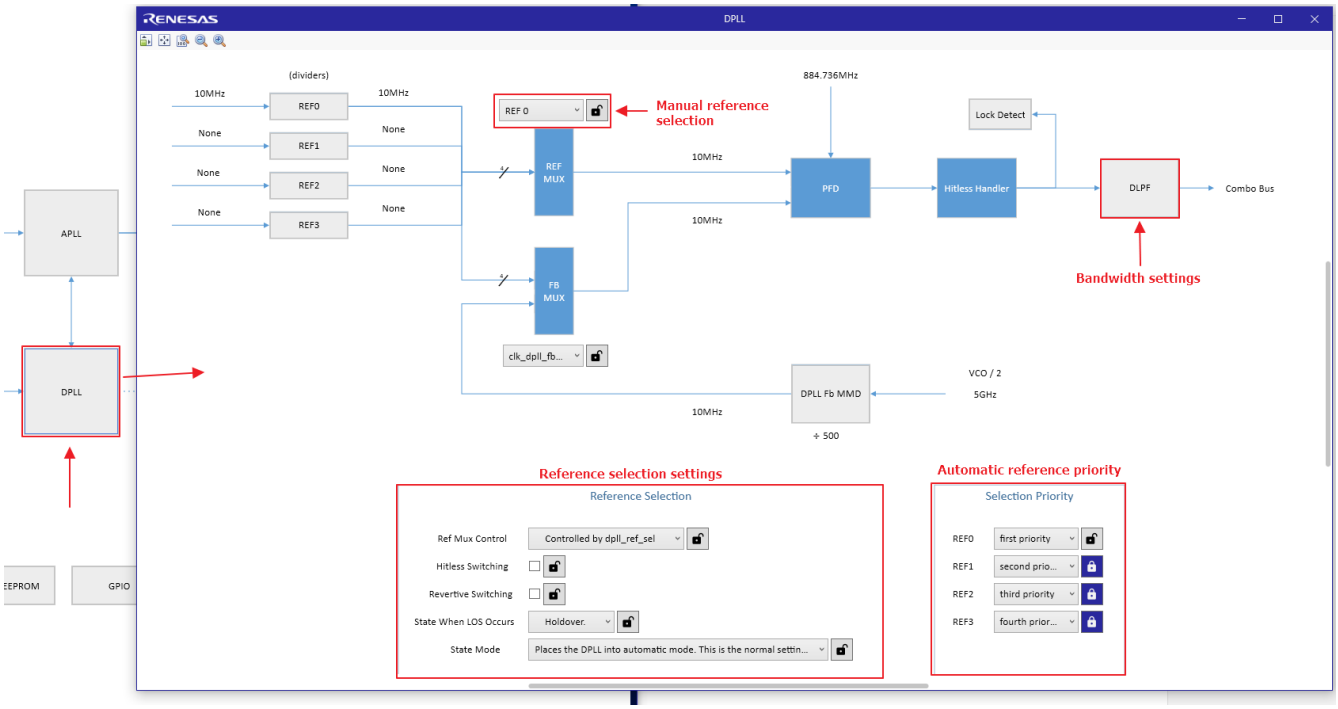

Figure 31. DPLL Block

8.8 GPIO Block

Clicking on the GPIO Block enables configuration of the GPIO function, polarity, output drive strength, and pull-up/down.

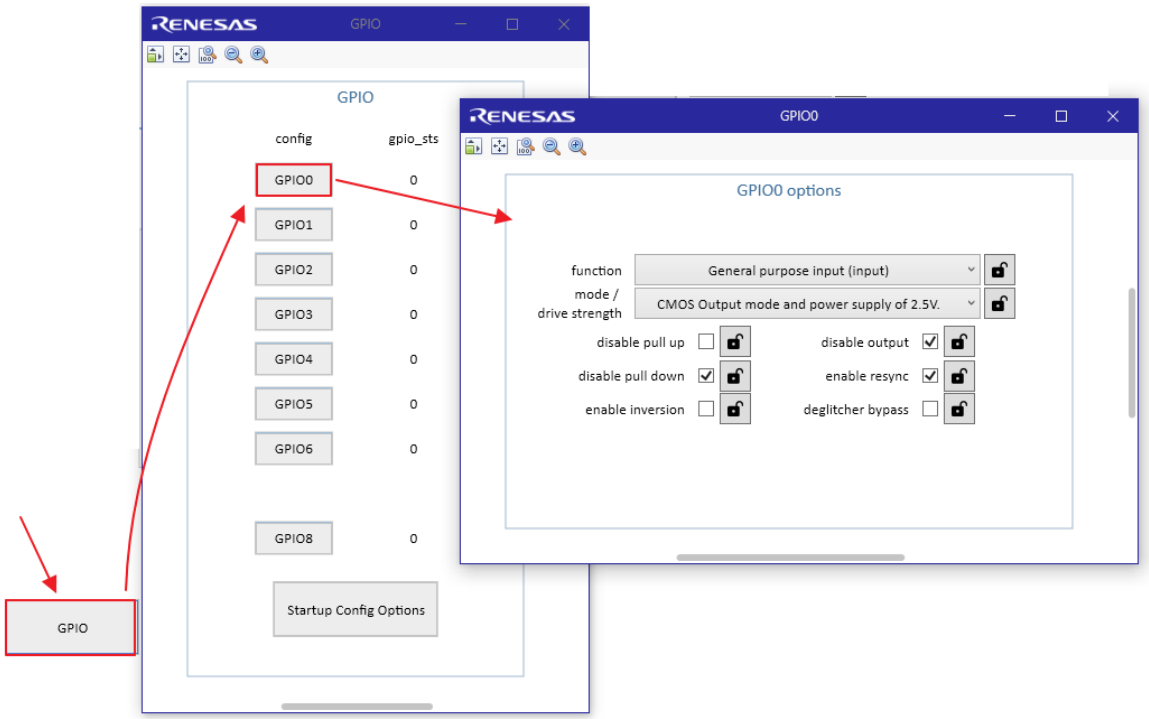

Figure 32. GPIO Block

Note: GPIO8 is indicative of the lock pin settings.

8.9 Serial Block

The Serial Block displays settings for serial communication protocol, I2C address selection, and SPI interface type.

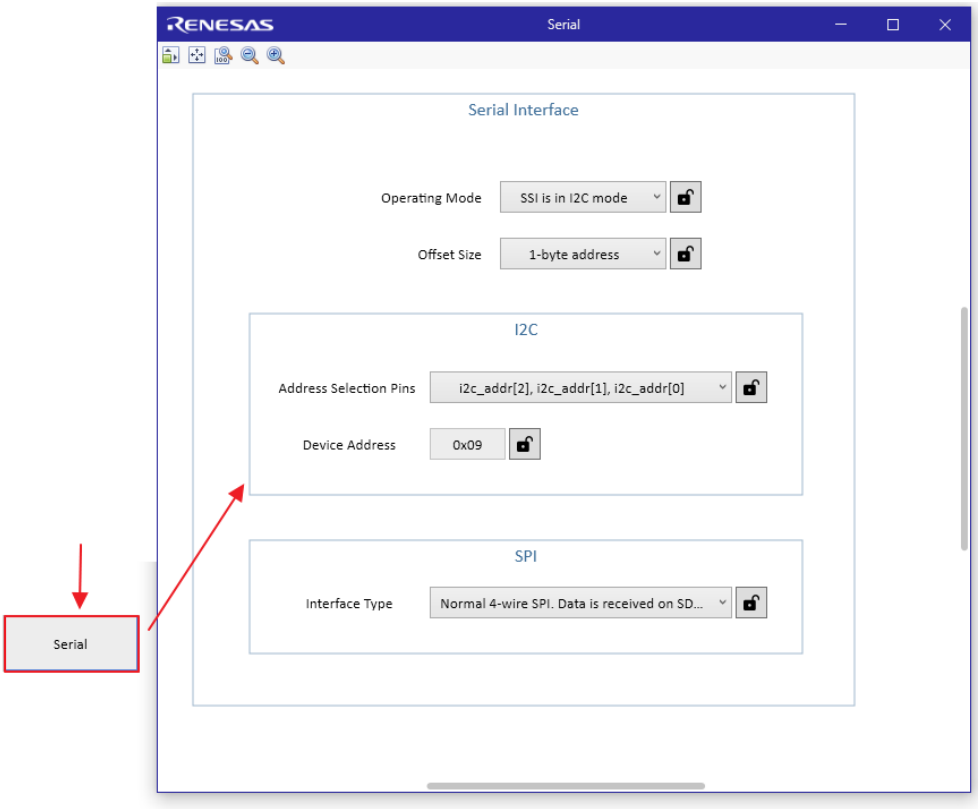

Figure 33. Serial Block

9. Device Connection

Device connection can be achieved through the bottom right corner of every page.

1. To connect a Renesas evaluation board, ensure the device is powered and connected to the working computer.
2. Click the **Not Connected** button in the corner of the screen. This will lead to a small pop-out page.
3. Click the connect symbol in the corner of the page to establish a connection to the device.

Figure 34. Device Connection

Note: RICBox Software Manual section 4 has more information about device connection features.

10. Using the Emulator to Capture Register Writes

RICBox has an emulator feature that is used to simulate a connection to the device. This feature is useful for capturing register write sequences when combined with the use of the RICBox log.

1. Click the *Not Connected* button in the corner of the screen. The Configure/Connect pop-out page appears (see .Figure 36).

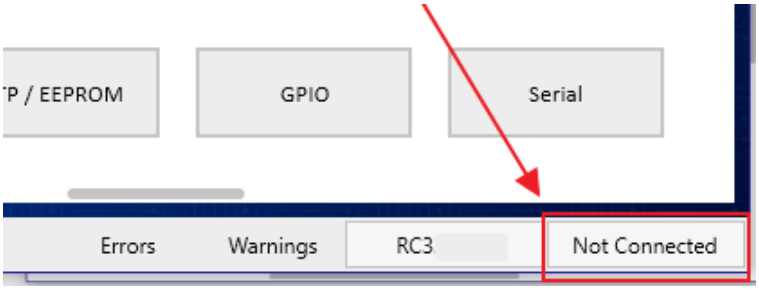

Figure 35. Not Connected Button

2. Click the *Configure* button to open the connection settings menu.

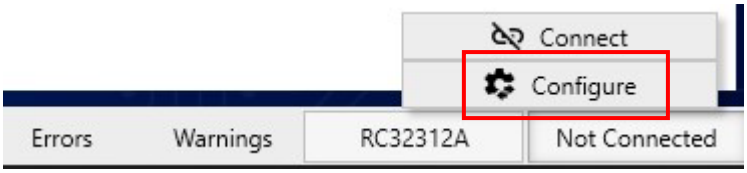

Figure 36. Configure Button

3. Select the *Manual* tab to navigate to the manual connection settings.

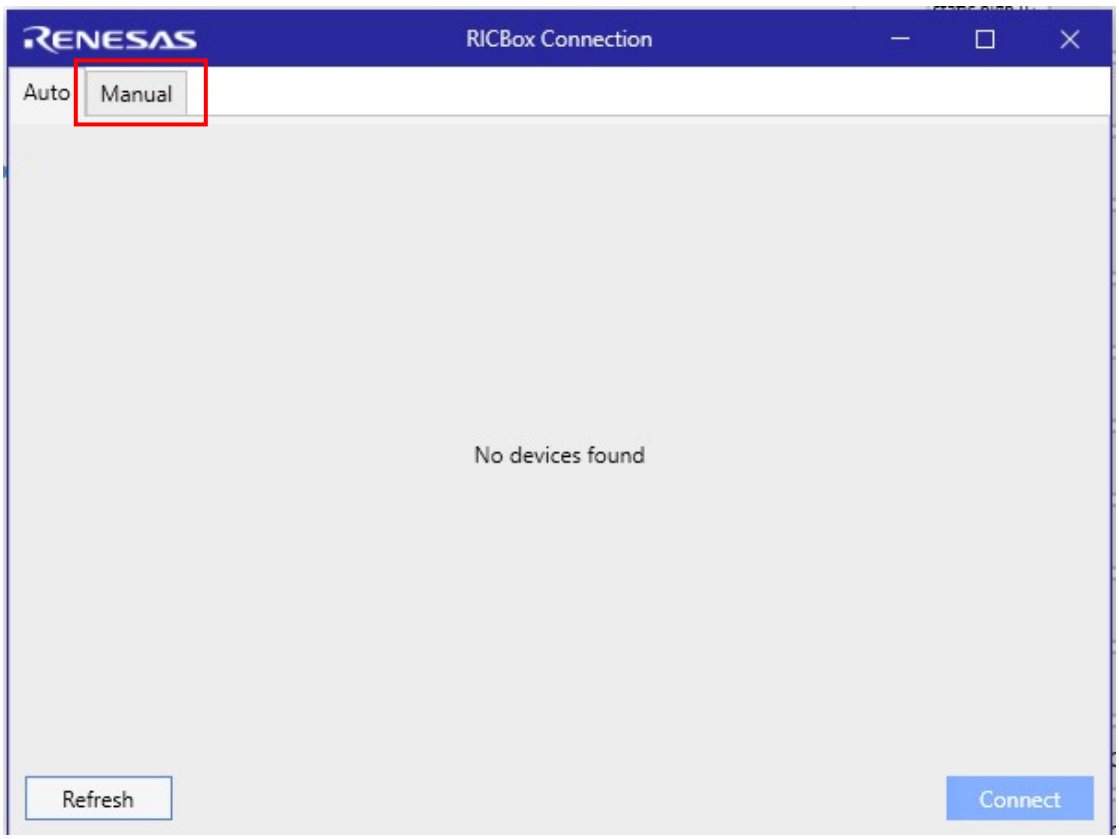

Figure 37. RICBox Connection – Manual Tab

4. Set the “Adapter” field to **Emulator**. Next, select the *Connect* button at the bottom right of the connection settings menu.

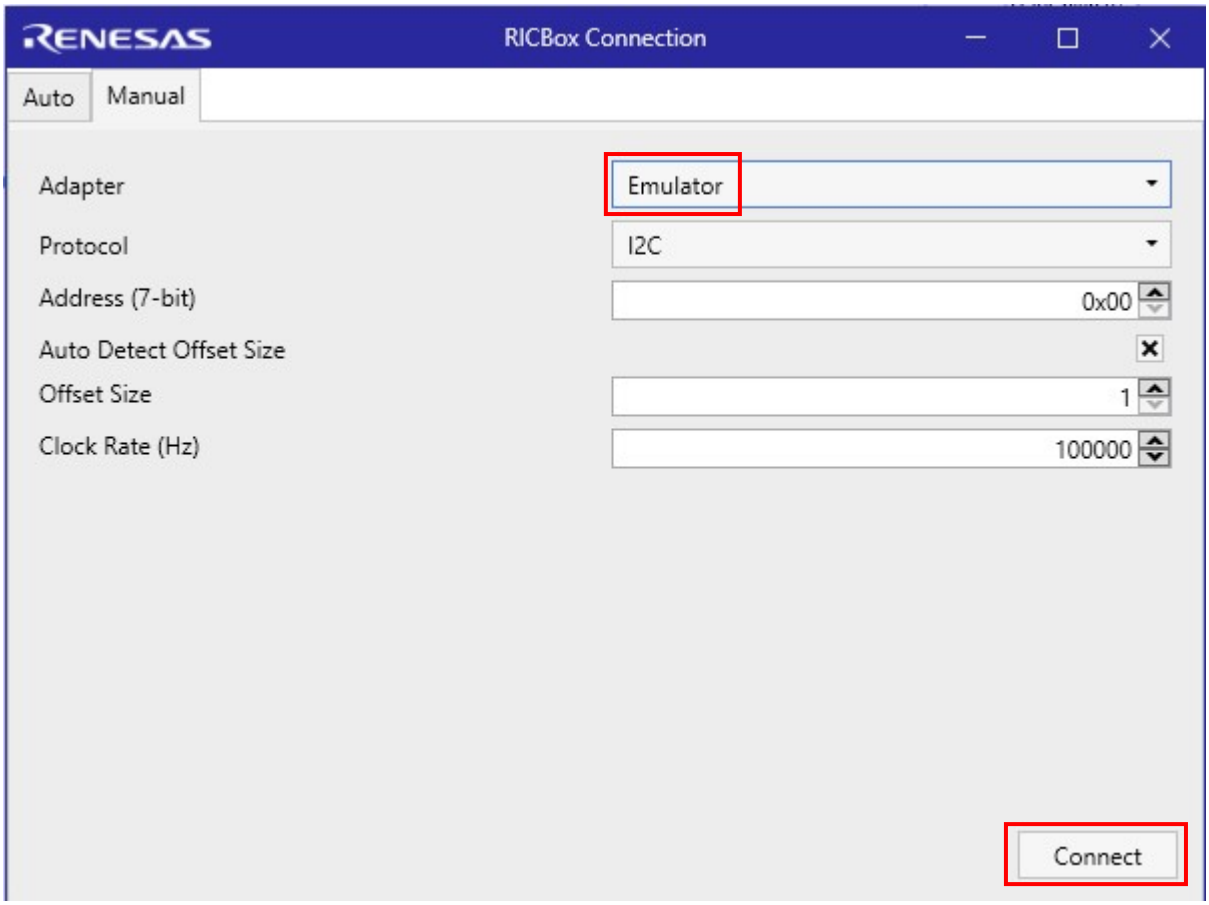

Figure 38. Emulator Field Selection

5. RICBox now shows that it is connected to a device. However, when using the Emulator, RICBox only thinks it is connected to a device.

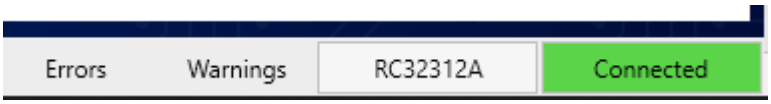

Figure 39. RICBox Connected to a Device

6. Open the connection log by selecting the *Help* menu tab, then clicking on the *Log* button.

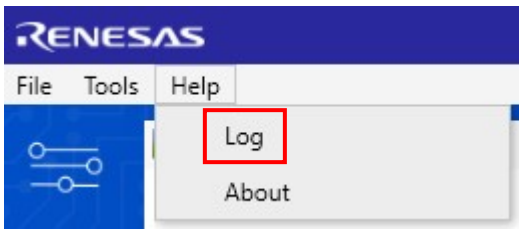

Figure 40. Help Menu – Log Button

7. Ensure that the **Debug** and **Trace** boxes in the bottom-left corner of the log window are checked.

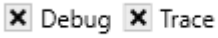

Figure 41. Log Window – Debug and Trace Check Boxes

8. Clear the log by clicking the *X* button at the bottom-right corner of the log window.

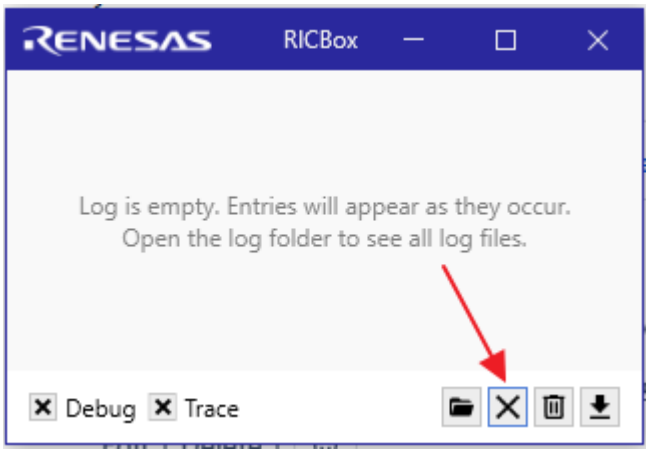

Figure 42. Log Window – Clearing the Log Entries

9. If any device settings in the GUI are changed while the log is open, the necessary register writes to make the changes are printed in the log. This is due to RICBox being connected to a device and any changes are written to that device in real-time. When using the emulator, RICBox thinks that there is a device to write to, so it sends the necessary write sequences that would be used to program the changes to a device.

   Use the mouse to select the log contents then copy/paste them into a text editor.

Figure 43. RICBox Log Contents Window

11. Common Configurable Settings

11.1 Enabling Jitter Attenuation Mode from the Block Diagram

1. Set device operation mode to **Jitter Attenuator** from the main block diagram.

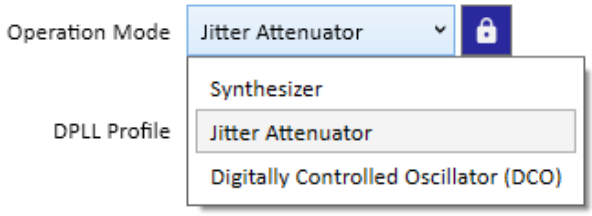

Figure 44. Operation Mode Selection

2. Set an input clock frequency.

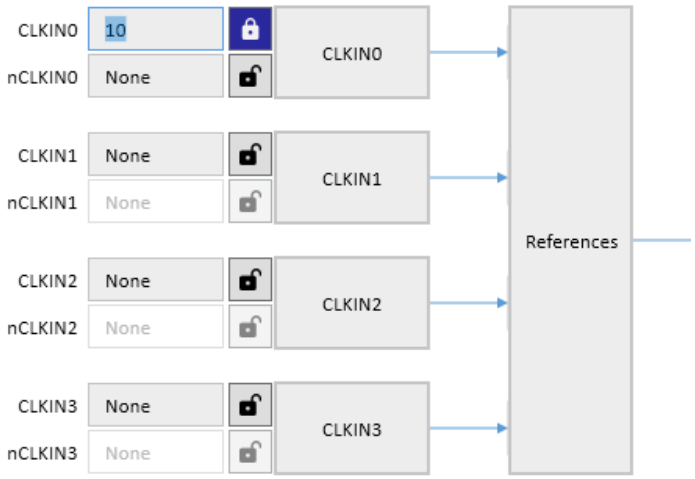

Figure 45. Set Input Clock Frequency

Note: If an input clock is not already enabled then the software will indicate an error. The error will be cleared when the input clock frequency is set.

3. Go into the CLKIN block and select the input signal type.

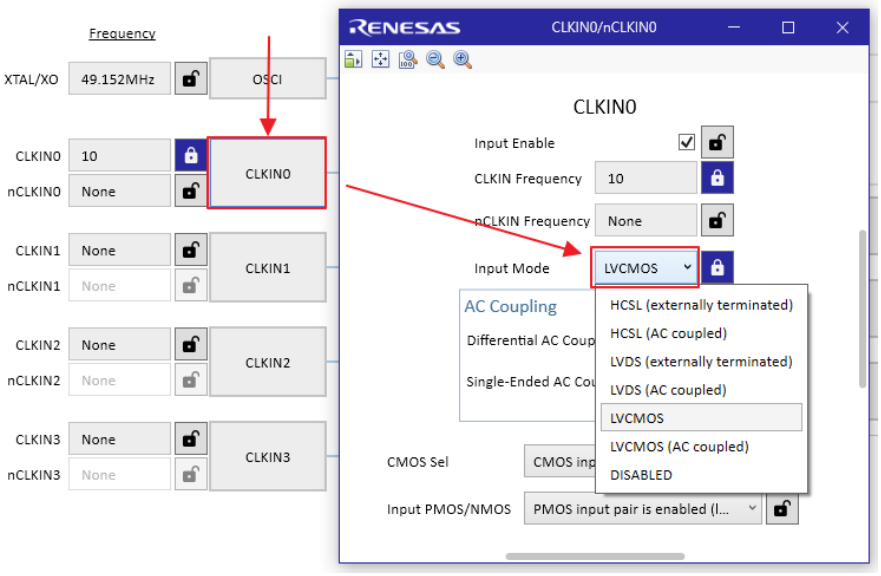

Figure 46. Set Input Clock Signal Type

Note: If an input clock signal type is not already enabled, the software will indicate a warning. This will be cleared when the input mode is set.

11.2 Saving/Programming EEPROM Images

1. Establish a connection to a device with an EEPROM attached.

Figure 47. Device Connection

2. Go to OTP/EEPROM section of the block diagram.
3. Use the configuration type dropdown menu to select **SingleConfig**.
4. Populate the Single Config dropdown menu with the configuration name that is being programmed to EEPROM.
5. Click the program button in the lower corner of the page.

   Note: The Adding Configurations to a Settings File section highlights configuration naming. RICBox Software Manual section 13 discusses multiple configuration support.

   Note: FemtoClock3 software only supports programming one configuration into EEPROM at a time.

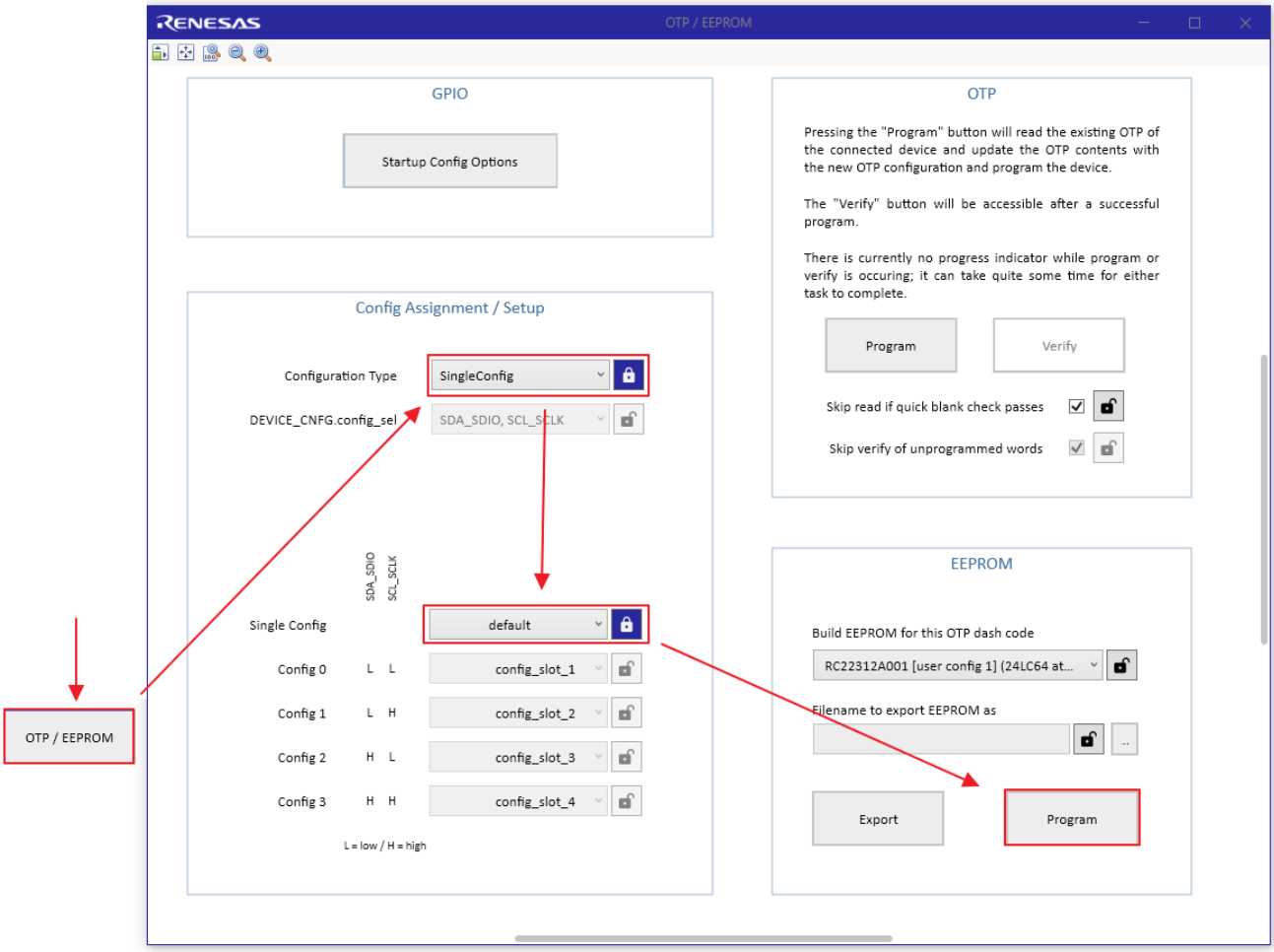

Figure 48. Programming a Connected EEPROM Device

6. Another option is to choose the save location by clicking the button next to the EEPROM filename entry box.
7. Click the **Export** button to save the EEPROM image to the specified location

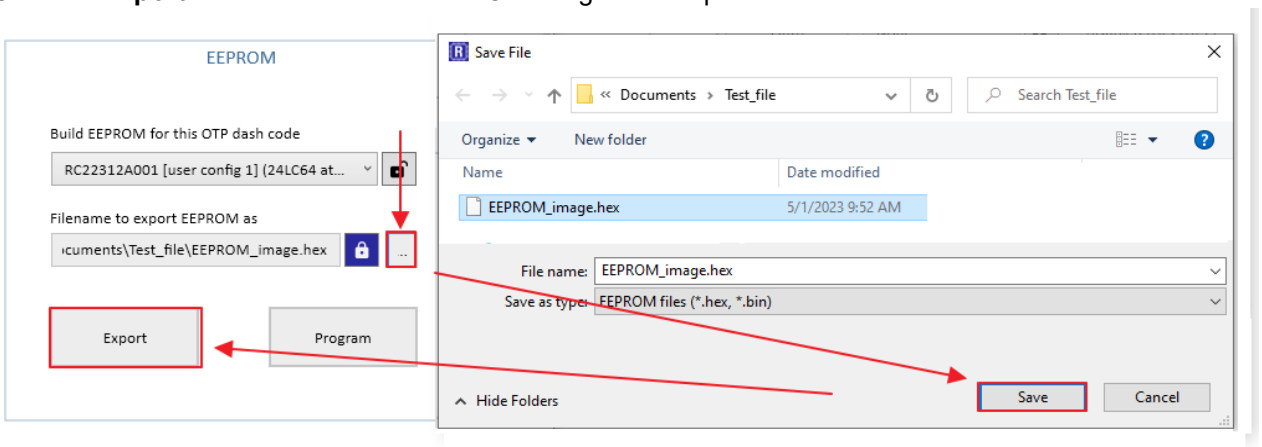

Figure 49. Saving EEPROM Image

Note: Be sure to specify the file extension as .bin or .hex when naming the file.

11.3 Enabling GPIO for Output Enable

FemtoClock3 GPIOs support output enable (OE) functionality to control output signals.

1. Click on the *GPIO* block.
2. Click the GPIO that will be used for the OE function.
3. Select the function as OE.

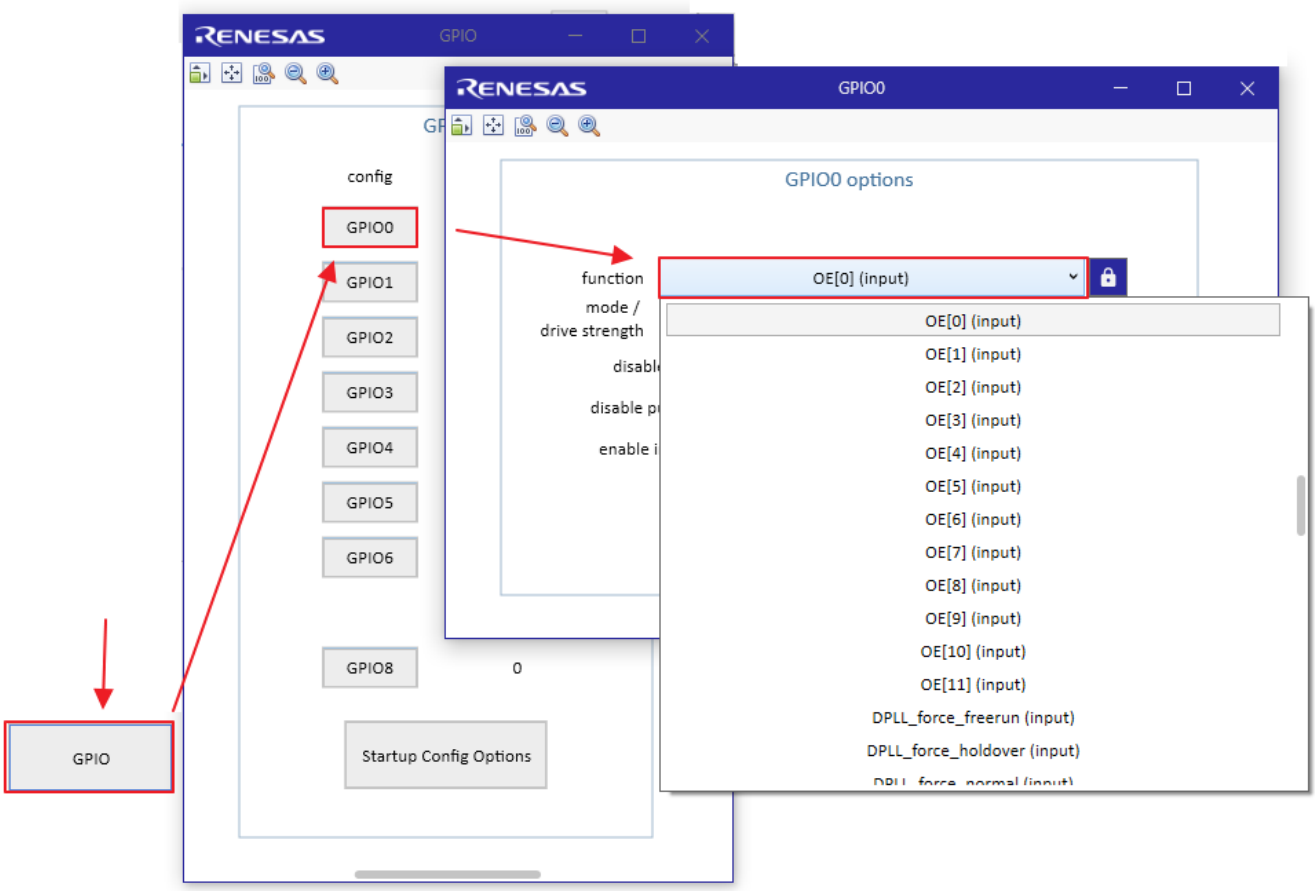

Figure 50. Configure GPIO for OE

4. Go to the specified output, click advanced, and set enable source to GPIO.

Note: Using two GPIOs to control the enable source of one output is not supported. This includes group and global OE functions.

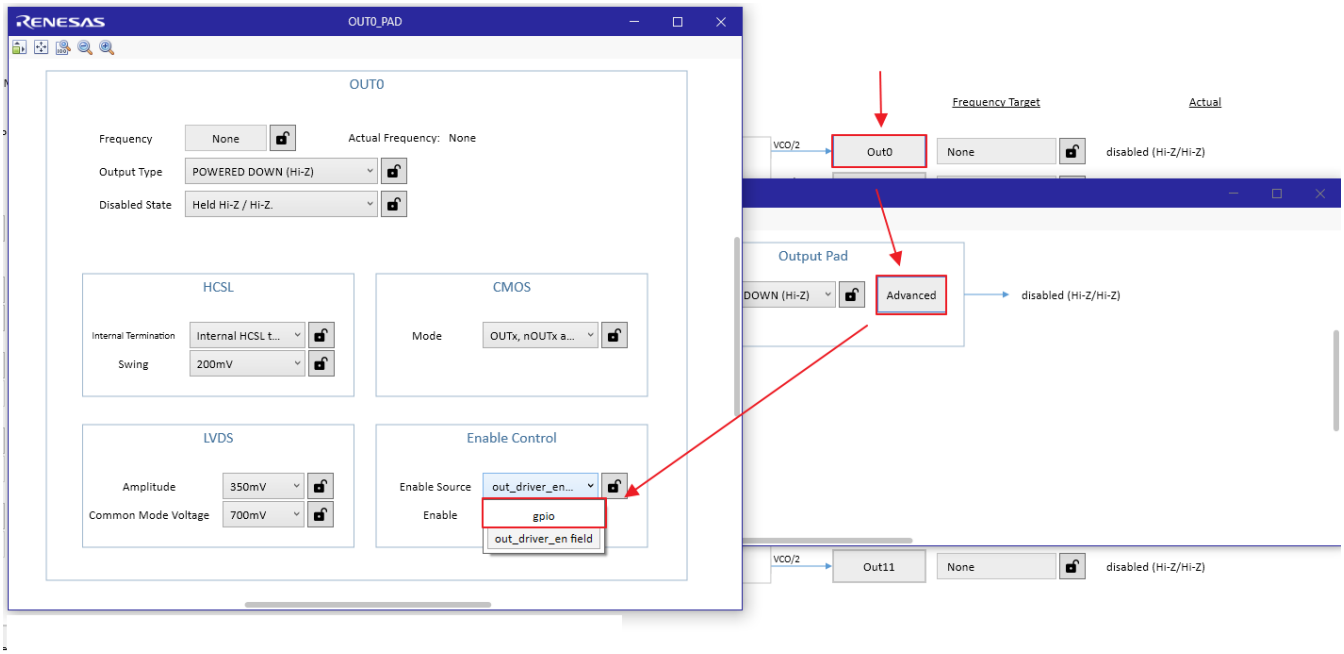

Figure 51. Configure Output Enable to GPIO Control

12. Revision History

Revision	Date	Description
1.01	Aug 7, 2024	Added the section Using the Emulator to Capture Register Writes.
1.00	Jul 6, 2023	Initial release.

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