User's Manual

Diagnostic Software Safety Manual

User's Manual

Renesas Synergy™ Platform
Renesas Synergy™ Tools & Kits
Tools: Synergy S7 Series MCU Diagnostic Software

Renesas Electronics
www.renesas.com

Rev. 1.03 Sep 2018

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(Rev.3.0-1 November 2016)

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The S7 Series MCU Diagnostic Software is not guaranteed to be error free, and the entire risk as to the results and performance of the Diagnostic Software is assumed by the User. The S7 Series MCU Diagnostic Software is provided by Renesas on an "as is" basis without warranty of any kind whether express or implied, including but not limited to the implied warranties of satisfactory quality, fitness for a particular purpose, title, and non-infringement of intellectual property rights with regard to the S7 Series MCU Diagnostic Software. Renesas expressly disclaims all such warranties.

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Precautions

This Renesas Synergy™ S7 Series MCU Diagnostic Software is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. - There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

• Ensure attached cables do not lie across the equipment.

• Reorient the receiving antenna.

• Increase the distance between the equipment and the receiver.

• Connect the equipment into an outlet on a circuit different from that which the receiver is connected.

• Power down the equipment when not in use.

• Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

• The user is advised that mobile phones should not be used within 10 m of the product when in use.

• The user is advised to take ESD precautions when handling the equipment.

The Renesas Synergy™ S7 Series MCU Diagnostic Software does not represent an ideal reference design for an end product and does not fulfill the regulatory standards for an end product.

1. Glossary

1.1 Use of Words

Use of the words "shall", "should", "must", "will", and "may" within this Specification observe the following rules:

- The word SHALL in the text expresses a mandatory requirement of the Specification
- The word SHOULD in the text expresses a recommendation or advice on implementing such a requirement of the Specification. REE expects such recommendations or advice to be followed unless good reasons are stated for not doing so.
- The word MUST in the text is used for legislative or regulatory requirements (for example, Health and Safety) with which both REE and the Supplier shall comply. It is not used to express a requirement of the Specification.
- The word WILL in the text expresses a provision or service by REE or an intention by REE in connection with a requirement of the Specification. The Supplier is implicitly authorized to rely on such service or intention.
- The word MAY in the text expresses a permissible practice or action. It does not express a requirement of the Specification.

2. Abbreviations

Ordered	Unordered
ALU	Arithmetic Logic Unit
CISC	Complex Instruction Set Computer
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DC	Direct Current
DFT	Design For Test
DM	Diagnostic Measure
DMA	Direct Memory Access (Controller)
FIT	Failure In Time
FPU	Floating Point Unit
FSCC	Functional Safety Competence Centre
HFT	Hardware Fault Tolerance
HW	Hardware
I/O	Input/Output
MCU	Microcontroller Unit
MPU	Memory Protection Unit
RAM	Random Access Memory
REE	Renesas Electronics Europe
ROM	Read-Only Memory
SC	Systematic Capability
SER	Soft Error Rate
SFF	Safe Failure Fraction
SIL	Safety Integrity Level
SRAM	Static Random Access Memory
SW	Software
WDT	Watchdog Timer

3. Document Scope

This Safety Manual specifies the user responsibilities for installation and operation in order to use the following items in safety related systems, and maintaining the specified safety integrity level:

- Renesas Diagnostics Software for Synergy S7 MCU, Version 1.1, including:
  - CPU Test, Version (see §4.1)
  - RAM Test, Version (see §4.2)
  - ROM Test, Version (see §4.3)
  - CAC Configuration, Version (see §4.4)
  - iWDT Management, Version (see §4.5)
  - LVD Configuration, Version (see §4.6).

The Renesas Diagnostics Software was developed for use with the Synergy S7 MCU following the IEC61508, 2nd Edition, targeting max. SIL3 applications. It is intended to provide diagnostic coverage for random permanent faults in the CPU, the User RAM, and the Flash ROM. It was developed in accordance with IEC61508:2010, Systematic Capability of 3 (SC 3). It can be used in safety related applications up to SIL 3 / SC 3.

The hosting MCU itself has a Hardware Fault Tolerance of 0 (HFT=0) and is a type "B" element according to IEC61508-2:2010.

This document is based on the assumption that the MCU is only used in customer applications adopting fail-silent / fail-flagging system design (fail-operational requirement for MCU is out of scope).

The Renesas Diagnostics Software User Guide [3] is a mandatory reference document for this Safety Manual and has to be followed in order to guarantee full functionality of the Diagnostics Software, avoid unwanted impact on application software, and enable Diagnostics Software to be used in safety related applications. In the following sections mainly additional information is given in order to avoid duplication of information.

4. Renesas Diagnostic Software

4.1 CPU Software Tests

4.1.1 Description of functions

The objective of the CPU Software Test is to test the correct functionality of the CPU by adopting a mainly instruction based diagnosis, with the aim of detecting permanent hardware failures of the CPU core. It is intended to be executed periodically at run-time.

All instructions listed in [2] with the exception of only BKPT, SEV, WFE, WFI, and DMB instructions, are used for the core testing. The CPU Software Test supports the Synergy family products based on the ARM® Cortex®-M4 CPU.

The CPU Software Test targets the following parts of the MCU, with a medium diagnostic coverage:

- ARM Cortex-M4 CPU Core module.

Additionally, the CPU Software Test also uses the following modules, but without the special requirement of providing a specific diagnostic coverage value:

- Interface to external modules
- Memory Protection Unit (MPU)
- Nested Vectored Interrupt Controller (NVIC).

Note: The interface modules mentioned above are tested by the RAM test and the ROM test in the Renesas Diagnostics Software.

Refer to Renesas Diagnostics Software User Guide [3] for more detailed description of the functions related to CPU Software Test.

Note: The user is responsible for the diagnostic measures required for the integrity of the interrupts.

4.1.2 Software version

All information provided in this document refers to the CPU Software Test, version 1.0.3.

4.1.3 Recommended configuration

Refer to the Renesas Diagnostic Software User Guide [3].

4.1.4 Outstanding anomalies

No outstanding anomalies of the CPU Software Test are known. Renesas will inform the customers in case of anomalies detected on this version.

4.1.5 Compatibility

The CPU Software Test is a porting of the previous PA015 project. The SW API are unchanged w.r.t. it, so no specific integration actions are needed to switch on this SW version.

4.1.6 Development environment

The CPU Software Test was developed using IAR Embedded Workbench for Synergy, functional safety version 8.23.1.17132, which is certified by 3rd party certification body TÜV SÜD to be used in safety related applications up to SIL3. You should use this development environment for building the CPU Software Test.

For detailed configuration to be used for the compiler please see [3].

4.1.7 Installation instructions

Please see [3] for instructions on how to install the CPU Software Test into the integrated system.

4.1.8 CPU Software Test diagnostic coverage validation

Renesas performed the safety validation of the CPU Software Test.

The fault injection performed involves the deliberate introduction of a fault into the netlist to evaluate the effect of a net in the netlist being shorted to Vcc or Ground, considering the stuck-at fault model. This is a common approach for fault injection and allows the Diagnostic Software to effectively detect faults to be evaluated.

Although only the stuck-at fault model is used for fault injection, the DC fault model is considered for this validation by estimating the impact of further fault models (bridge, stuck-open, stuck-on).

The diagnostic coverage value for the CPU Software Test is listed in Table 4.1. The coverage value is evaluated with the precondition that software flow control is temporally monitored.

Table 4.1 Diagnostic coverage of CPU Software Test evaluated by netlist fault injection

Diagnostic coverage value considering DC fault mode	Medium

Diagnostic coverage value is valid for the CPU Software Test including all test segments. If a different CPU Software Test configuration is used for example, by leaving out some test segments, the diagnostic coverage value decreases.

4.2 RAM Software Test

4.2.1 Description of functions

The objective of the RAM Software Test is to test the embedded RAM memory. The main features of this test are as follows:

- Whole memory check including stack(s)
  - Memory size programmable at compile time
- Block-wise implementation of the test
  - Size of the block programmable at compile time
- Support for two testing algorithms
  - Extended March C-
  - WALPAT
- Word-wise implementation of the testing algorithms supporting 32-bit width
- Support for destructive and non-destructive memory testing.

The Extended March C- test is very efficient in terms of fault coverage and execution time. The WALPAT test misses the detection of some faults that the Extended March C- test detects, but has the advantage of also detecting sense amplifier faults. Both tests provide a medium coverage for permanent random hardware faults, and the selected test should be executed periodically during the application. This coverage value is valid under the condition that, for both tests, the minimum block size chosen is not lower than 512 bytes. Transient faults (soft errors) are not covered by the RAM tests and have to be considered separately.

The diagnostic software is intended to be executed periodically at run-time, at least for the RAM memories that are not protected by parity/ECC.

For more information, see [3].

4.2.2 Software version

All information provided in this document refers to the RAM Software Test, version 1.0.1.

4.2.3 Recommended configuration

Refer to the Renesas Diagnostic Software User Guide [3].

4.2.4 Outstanding anomalies

No outstanding anomalies of the RAM Software Test are known. Renesas will inform the customers in case of anomalies detected on this version.

4.2.5 Compatibility

The RAM Software Test is a porting of the previous PA015 project. The SW API are unchanged w.r.t. it, so no specific integration actions are needed to switch on this SW version.

4.2.6 Development environment

The RAM Software Test was developed using IAR Embedded Workbench for Synergy, functional safety version 8.23.1.17132, which is certified by 3rd party certification body TÜV SÜD, to be used in safety related applications up to SIL3. The user shall use this development environment for building the RAM Software Test.

For detailed configuration to be used for the compiler, see [3].

4.2.7 Installation instructions

See [3] for instructions on how to install the RAM Software Test into the integrated system.

4.3 ROM Software Test

4.3.1 Description of functions

The objective of the ROM Software Test is to test the whole embedded ROM, adopting the CRC technique. Error detected uses the the following steps:

1. A range of addresses are chosen, which define the block under test.
2. A reference checksum value is calculated using the IAR linker and save to the ROM.
3. During the ROM Software Test execution, the CRC hardware peripheral is used to produce an actual checksum value for the ROM content under test in order to check its integrity.
4. The checksum value calculated is compared with the one stored in the ROM and an error is flagged if the two values do not match.
5. Previous steps are repeated for a different block of the ROM until whole coverage of the used ROM is obtained.

Three different CRC polynomials are supported:

- 8-bit CRC
  - x^8+x^2+x+1
- 16-bit CRC
  - $x^{16}+x^{15}+x^2+1$
  - $x^{16}+x^{12}+x^5+1$.

For more information, see [3].

The ROM test using the 8-bit CRC provides medium coverage against permanent random hardware faults, while the ROM test using the 16-bit CRC gives high coverage in relation to permanent and transient failures.

4.3.2 Software version

All information provided in this document refers to the ROM Software Test, version 1.0.1.

4.3.3 Recommended configuration

Refer to the Renesas Diagnostic Software User Guide [3].

4.3.4 Outstanding anomalies

No outstanding anomalies of the ROM Software Test are known. Renesas will inform the customers in case of anomalies detected on this version.

4.3.5 Compatibility

The ROM Software Test is a porting of the previous PA015 project. The SW API are unchanged w.r.t. it, so no specific integration actions are needed to switch on this SW version.

4.3.6 Development environment

The ROM Software Test was developed using IAR Embedded Workbench for Synergy, functional safety version 8.23.1.17132, which is certified by 3rd party certification body TÜV SÜD, to be used in safety related applications up to SIL3. The user shall use this development environment for building the ROM Software Test.

For detailed configuration to be used for the compiler, see [3].

4.3.7 Installation instructions

See [3] for instructions on how to install the ROM Software Test into the integrated system.

4.4 CAC Configuration Software

4.4.1 Description of functions

The Synergy S7 has a Clock Frequency Accuracy Measurement Circuit (CAC) that can be used to monitor the system clock frequency during run time, to detect deviations.

The objective of the CAC Configuration Software is to configure the CAC.

This software will be used to:

- Select the PCLKB as measurement target clock for the CAC
- Select sub-clock oscillator as the measurement reference clock for the CAC.

This configuration allows for detection of deviations of the main clock oscillator and PLL due to systematic or random hardware failures.

Note: To ensure effectiveness of this diagnostic measures, the application configures the CAC to generate PCLKB through the main clock oscillator and PLL[1].

Note: For the operation of the CAC, it is necessary for the reference clock, which is the sub-clock oscillator, to be supplied. The user shall enable the sub-clock oscillator through the SOSCCR register (that is, SOSCCR.SOSTP = 0b. See the User Manual [1] for details.). A loss of the reference clock can be detected by reading the CACNTBR. If this is 0x0000, the reference clock does not work. This can be used as a start-up diagnostic.

[1] Faults of muxes and dividers involved in the generation of PCLKB are also detectable. Additional measures are necessary to check the system clock (ICLK). For details, see section 4.5.

The CAC Configuration Software also enables the Synergy S7 oscillation stop detection circuit functionality. In case the main clock oscillator stops, this circuit is in charge of switching to the middle-speed on-chip oscillator and generating an NMI interrupt. This provides additional protection for helping to diagnose problems on the main clock oscillator and for fault reaction support.

Refer to the Renesas Diagnostic Support User Guide [3] for more detailed descriptions of the functions related to the CAC Configuration Software.

4.4.2 Software version

All information provided in this document refers to the CAC Configuration Software, version 1.0.2.

4.4.3 Recommended configuration

Refer to the Renesas Diagnostic Software User Guide [3].

4.4.4 Outstanding anomalies

No outstanding anomalies of the CAC Configuration Software are known. Renesas will inform the customers in case of anomalies detected on this version.

4.4.5 Compatibility

The CAC Configuration Software is a porting of the previous PA015 project. The SW API are unchanged w.r.t. it, so no specific integration actions are needed to switch on this SW version.

4.4.6 Development environment

The CAC Configuration Software was developed using IAR Embedded Workbench for Synergy, functional safety version 8.23.1.17132, which is certified by 3rd party certification body TÜV SÜD, to be used in safety related applications up to SIL3. The user shall use this development environment for building the CAC Configuration Software.

For detailed configuration to be used for the compiler, see [3].

4.4.7 Installation instructions

See [3] for instructions on how to install the CAC Configuration Software into the integrated system.

4.5 IWDT Management Software

4.5.1 Description of functions

The Synergy S7 Independent Watchdog Timer (IWDT) can be used to detect an abnormal program execution. If a program is not running as expected, the IWDT is not refreshed by software as required, and therefore, triggers a programmed action.

The IWDT also includes a windowing feature requiring the refresh to happen within a specified window rather than before a specified time. It can be configured to generate an internal reset or an NMI interrupt, if an error is detected. This Watchdog Timer is also operated on a clock that is different and independent from the one used for the CPU (ICLK). Consequently, it also protects against abnormal program execution caused by random hardware failures. In particular, it complements the CAC, providing high-level of coverage against faults of the mux generating the ICLK.

Note: The IWDT is operated by a dedicated on-chip oscillator that has a 10% tolerance. The system integrator has to consider if this tolerance is adequate for the target application.

The objective of the IWDT Management Software is to enable the IWDT peripheral and provide an API to refresh it periodically, based on the application requirements. In addition, the software provides the user with an API to check whether the IWDT initiated the last reset.

4.5.2 Software version

All information provided in this document refers to the IWDT Management Software, version 1.0.1.

4.5.3 Recommended configuration

Refer to the Renesas Diagnostic Software User Guide [3].

4.5.4 Outstanding anomalies

No outstanding anomalies of the IWDT management software are known. Renesas will inform the customers in case of anomalies detected on this version.

4.5.5 Compatibility

The IWDT Management Software is a porting of the previous PA015 project. The SW API are unchanged w.r.t. it, so no specific integration actions are needed to switch on this SW version.

4.5.6 Development environment

The IWDT Management Software was developed using IAR embedded workbench for Synergy, functional safety version 8.23.1.17132, which is certified by 3rd party certification body TÜV SÜD, to be used in safety related applications up to SIL3. The user shall use this development environment for building the IWDT management software. For detailed configuration to be used for the compiler, see [3].

4.5.7 Installation instructions

See [3] instructions on how to install the IWDT Management Software into the integrated system.

4.6 LVD Configuration Software

4.6.1 Description of functions

The Synergy S7 has a voltage detection circuit. This can be used to detect the power supply voltage (Vcc) falling below a specified voltage. The supplied sample code demonstrates using Voltage Detection Circuit 1 to generate an NMI interrupt when Vcc drops below a specified level.

The objective of the LVD Configuration Software is to configure the low voltage detection circuit peripheral according to the user setting provided by its API.

Using this software, it is possible to reach at least a medium level of coverage against permanent random hardware faults leading to Vcc going below Vdet1 threshold (under voltage, drift to lower voltage and spikes to lower voltage longer than 200 µs.)

Note: This diagnostic measure has to be accompanied by an external voltage monitoring, such as in the case of overvoltage conditions that are not detected and may lead to damage of the circuit.

4.6.2 Software version

All information provided in this document is referring to the LVD Configuration Software, version 1.0.1.

4.6.3 Recommended configuration

Refer to the Renesas Diagnostic Software User Guide [3].

4.6.4 Outstanding anomalies

No outstanding anomalies of the LVD configuration software are known. Renesas will inform the customers in case of anomalies detected on this version.

4.6.5 Compatibility

The LVD Configuration Software is a porting of the previous PA015 project. The SW API are unchanged w.r.t. it, so no specific integration actions are needed to switch on this SW version.

4.6.6 Development environment

The LVD Configuration Software was developed using IAR Embedded Workbench for Synergy, functional safety version 8.23.1.17132, which is certified by 3rd party certification body TÜV SÜD, to be used in safety related applications up to SIL3. The user shall use this development environment for building the IWDT management software. For detailed configuration to be used for the compiler, see [3].

4.6.7 Installation instructions

See [3] instructions on how to install the LVD Configuration Software into the integrated system.

4.7 Assumptions and recommendations for use of Renesas Diagnostic Software

See [3] for all safety related conditions for use of the Renesas Diagnostic Software.

4.8 User Expertise

The user needs to have expertise in embedded programming of the target MCU. Expertise on assembly programming and C level/ assembly interface is also necessary.

4.9 Degree of reliance information

4.9.1 Independent assessment

An independent assessment of the Renesas Diagnostics Software, including all related documentation and development process, with respect to the requirements of IEC61508:2010, targeting maximum SIL3 applications, was performed by TÜV Rheinland.

4.9.2 Development of environment safety guidelines

Development of Renesas Diagnostic Software followed the IAR Embedded Workbench Safety Guide [4].

4.9.3 Verification of Renesas Diagnostic Software

A thorough verification of the Renesas Diagnostics Software was performed. Verification includes:

- Software requirement verification
- Static verification
- Dynamic verification
- Verification of software requirements coverage.

For the dynamic verification, the IAR Embedded Workbench was used, which enables the implementation of efficient software tests. More than 30 test cases were re-executed for dynamic verification.

4.9.4 Further information

The Renesas Diagnostic Software was developed almost completely in assembly language with C-user interface. No complex structures are involved and branches/ jumps are avoided as much as possible. This is an important factor for avoiding systematic failures in the Renesas Diagnostic Software.

4.10 Change Control

If any changes to the CPU Software Test, RAM Software Test, or ROM Software Test are required to fulfill certain requirements of the system integrator, a related change request should be addressed to:

Renesas Electronics Europe GmbH
Industrial & Communications Business Group (ICBG)
Arcadiastrasse 10
40472 Düsseldorf
Germany

5. Appendix A: Product Variants

Table 5.1 lists all product variants that are covered by this safety manual.

Table 5.1 Product variants covered by this Safety Manual

Part Number	Family	Product Group	Product Description	Package
R7FS7G27H2A01CBD#AC0	MCU	S7G2	4 MB Code flash, 64 KB Data flash, 640 KB SRAM, -40 to +85°C	PLBG0224GA-A
R7FS7G27H2A01CBG#AC0	MCU	S7G2	4 MB Code flash, 64 KB Data flash, 640 KB SRAM, -40 to +85°C	PLBG0176GE-A
R7FS7G27H3A01CFC#AA0	MCU	S7G2	4 MB Code flash, 64 KB Data flash, 640 KB SRAM, -40 to +105°C	PLQP0176KB-A
R7FS7G27H2A01CLK#AC0	MCU	S7G2	4 MB Code flash, 64 KB Data flash, 640 KB SRAM, -40 to +85°C	PTLG0145KA-A
R7FS7G27H3A01CFB#AA0	MCU	S7G2	4 MB Code flash, 64 KB Data flash, 640 KB SRAM, -40 to +105°C	PLQP0144KA-B
R7FS7G27G2A01CBD#AC0	MCU	S7G2	3 MB Code flash, 64 KB Data flash, 640 KB SRAM, -40 to +85°C	PLBG0224GA-A
R7FS7G27G2A01CBG#AC0	MCU	S7G2	3 MB Code flash, 64 KB Data flash, 640 KB SRAM, -40 to +85°C	PLBG0176GE-A
R7FS7G27G3A01CFC#AA0	MCU	S7G2	3 MB Code flash, 64 KB Data flash, 640 KB SRAM, -40 to +105°C	PLQP0176KB-A
R7FS7G27G2A01CLK#AC0	MCU	S7G2	3 MB Code flash, 64 KB Data flash, 640 KB SRAM, -40 to +85°C	PTLG0145KA-A
R7FS7G27G3A01CFB#AA0	MCU	S7G2	3 MB Code flash, 64 KB Data flash, 640 KB SRAM, -40 to +105°C	PLQP0144KA-B
R7FS7G27G3A01CFP#AA0	MCU	S7G2	3 MB Code flash, 64 KB Data flash, 640 KB SRAM, -40 to +105°C	PLQP0100KB-B

6. References

1. Synergy S7 User's Manual: Hardware, Rev. 1.00, February 2016 (Document Reference R01UM0001EU0100).
2. Cortex - M4 Devices – Generic User guide, 16 December 2010.
3. Synergy Group: Renesas Diagnostics Software User Guide.
4. IAR Embedded Workbench Safety Guide (SafetyEW-1), February 2013, IAR Internal Reference: M13, ISUD.

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Feb 2, 2017	-	Initial version
1.01	Mar 10, 2017	§4.1.2	Updated reference CPU release.
		All	Corrected typos in header / footer.
1.02	Jul 17, 2018	References	Removed revision information from documentation
1.03	Sep 27, 2018	All	Updated the functional safety version of the IAR Embedded Workbench.
		-	Removed “ADC12 Comparator Software” and TSN “Management Software” sections.
		-	Updated latest release of CPU,RAM,ROM,CAC,IWDT and LVD tests.
		All	Replaced “S7G2” Synergy name with “S7”.
		4.9.3	Rephrased a sentence.

Synergy S7 Series MCU Diagnostic Software Safety User's Manual

Publication Date: Rev. 1.03 Sep, 2018

Published by: Renesas Electronics Corporation

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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