DA14592 SmartBond Module Development Kit

This document outlines the system design, configuration options, and supported features of DA14592 SmartBond Module Development Kit, PCB version 469-18-C.

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Terms and Definitions

BLE	Bluetooth Low Energy
CIB	Communication Interface Board
DB	Daughterboard
DEVKIT	Development Kit
JTAG	Join Test Action Group
LDO	Low Dropout
PCB	Printed Circuit Board
SDK	Software Development Kit
SMD	Surface-Mount Device
SoC	System on Chip
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

1. References

[1] DA14592, Datasheet, Renesas Electronics.

[2] DA14592MOD, Datasheet, Renesas Electronics.

[3] UM-B-167, DA1459x Pro-Development Kit, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

2. Introduction

This document describes the development kit of the DA14592 SmartBond Module (DA14592MOD).

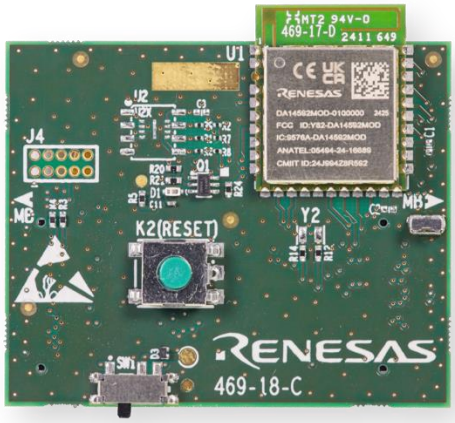

Figure 1. DA14592 SmartBond Module Daughterboard

DA14592 SmartBond Module Development Kit (DevKit) is implemented on a Daughterboard (DB) (469-18-C), and it comes with DA1459x Pro DevKit (469-16-D) and PMM2 (500-29-E), see Figure 2.

DA14592 SmartBond Module DB can also use the same combination of DA1459x Pro Devkit (469-16-D) and PMM2 (500-29-E) without modifications.

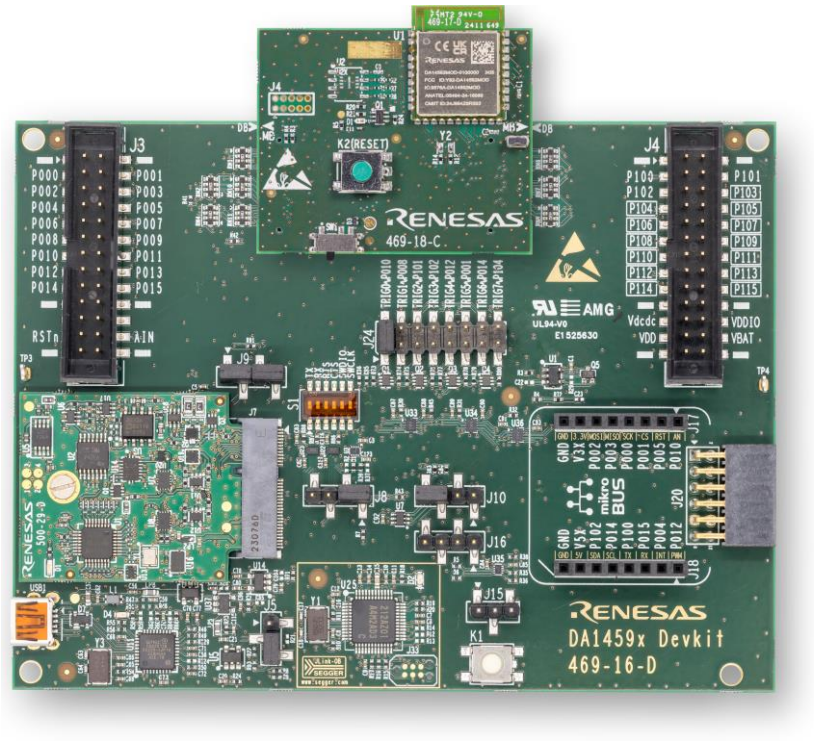

Figure 2. DA14592 SmartBond Module DevKit

The Development Kit (DevKit) is used for software development, programming, debugging, and measuring current, whereas the Daughterboard (DB) can be also used stand alone.

The block diagram, the actual board, the various sections, and settings, as well as the connectivity, are presented.

2.1 Features of DA14592 SmartBond Module DB

The features of DA14592 SmartBond Module DB include:

- Integrated Renesas DA14592 SmartBond Module
- Reset push button
- General-purpose LED
- Supply from VLDO from DA1459x Pro DevKit or from battery (coin cell)
- JTAG and UART interface over DA1459x Pro DevKit
- JTAG and UART interface over on-board connector (J4)
- External QSPI RAM option
- Stand-alone operation
- A dimension of 43x35.3 mm.

2.2 Features of DA1459x Pro-MB

- Mating connectors to connect a DA1459x Pro-DB which hosts one of the following:
  - DA14592MOD, DA14592 SmartBond Module
  - DA14592- FCQFN52
  - DA14592- WLCSP39
- A slot for attaching a power measurement module (PMM2)
- Single USB port to provide power and data interfacing to a PC (USB1)
- Headers for I/O monitoring and expandability
- Option to support MikroBUS click boards
- Provisions for automated test
- On-board basic peripherals for demo and development
- JTAG(SWD) debugger and connectivity to PC.

For detailed information on DA1459x Pro-MB, see Ref. [3].

2.3 Features of PMM2 (Power Measurement Module, 500-29-x)

- Full scale range 50 µA at 3 V
- Measure accurately down to 1 µA
- Dedicated Hibernation mode to measure down to 100 µA
- Software trigger inputs
- System voltage measurement.

The power measurement module (PMM2) is an external add-on board that is interfaced (connected) on the DA1459x Pro-MB. For detailed information on PMM2, see Ref. [3].

3. Get Started with DA14592 SmartBond Module DevKit

3.1 Hardware Components of the DevKit

The DA14592 SmartBond Module DevKit consists of the following parts:

- Pro-Motherboard, DA1459x Pro-MB. PCBA reference number 469-16-D.
- DA14592 SmartBond Module Development Daughterboard (DB). PCBA reference number 469-18-C.
- Power measurement module, PMM2. PCBA reference number 500-29-E.

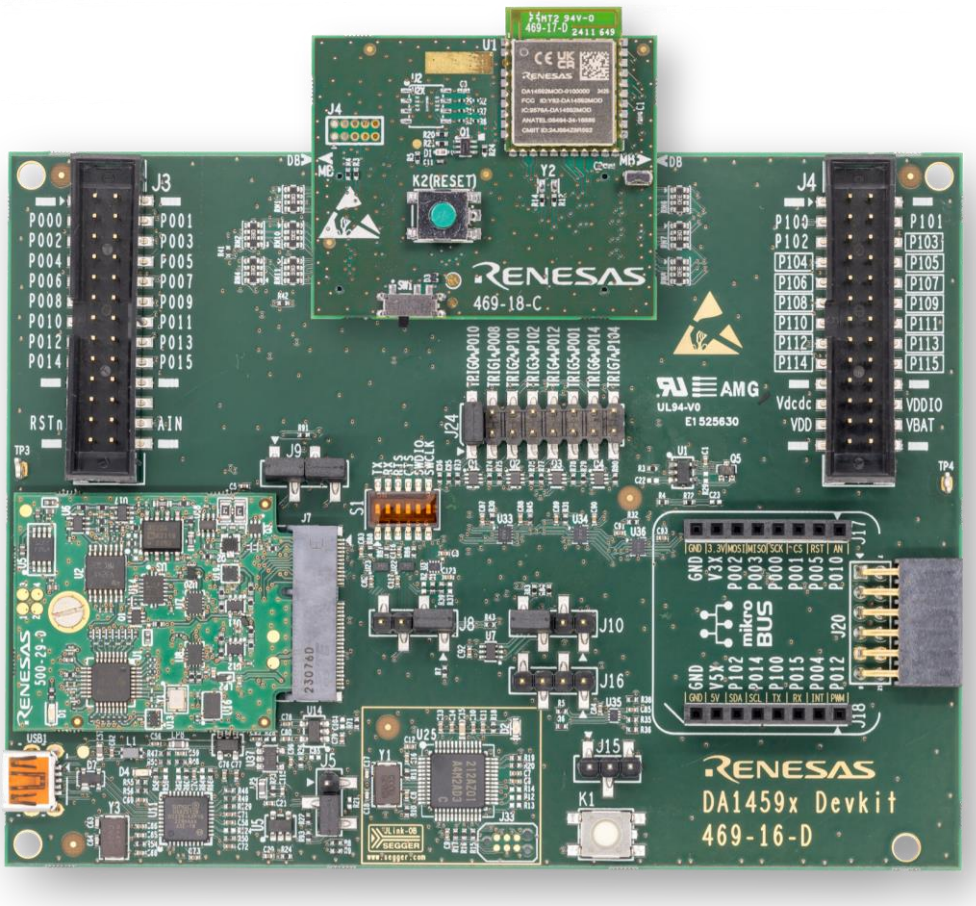

Figure 3. Mount DA14592 SmartBond Module DB to DA1459x Pro-MB with PMM2

3.2 First Steps with DA14592 SmartBond Module DevKit

The DA1459x Pro-MB, as well as DA14592 SmartBond Module DB, comes with a pre- defined default configuration. See Ref. [3] for default configuration.

3.2.1 DA14592 SmartBond Module DevKit Pro Setup

Default jumper settings applied on DA1459x Pro-MB are shown in Figure 4. System configuration and the functions enabled are presented in Table 1. Before starting the development kit, ensure that the jumper settings are according to Table 1.

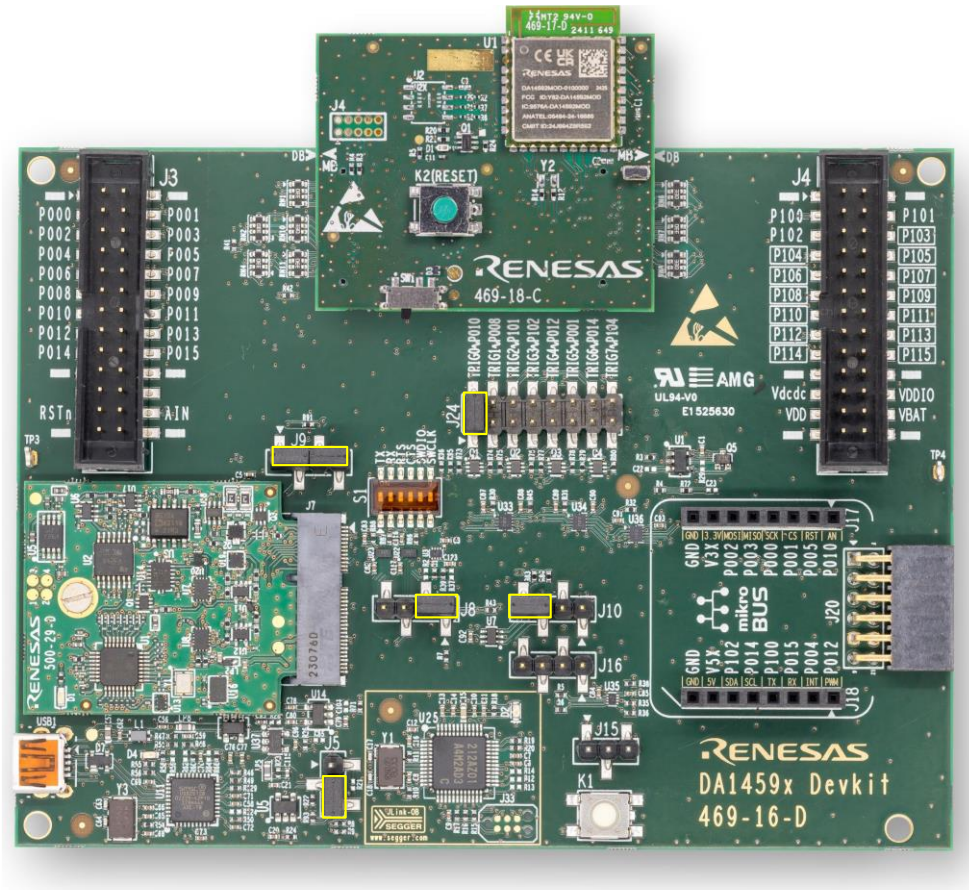

Figure 4. DA1459x Pro-MB default jumper configuration with DA14592 SmartBond Module DB attached

Table 1. Headers and jumper settings of DA1459x Pro Devkit

HDR	Function of headers	Jumper options		Default jumper setting
J5	DA1459x input voltage, generated from LDO (U5)	1.8 V	Mount pos. 1-2 Or No mount 1-2	Mounted 2-3
		3.0 V	Mount pos. 2-3	
J8	K1, general purpose push button and (pins 1-2) Force enable Power_Enable (3-4), for supplying Pro Devkit with a power source without USB data connection	Enable K1	Mount pos. 1-2	Mounted 1-2
		Force Power_Enable	Mount pos. 3-4	No mounted 3-4
J9	Power Measurement Module PMM2	PMM2 Bypass	Mount pos. 2-3	PMM2 mounted: Mounted 1-2
		PMM2 Enable	Mount pos.1-2 Mount pos. 3-4	Mounted 3-4 PMM2 no mounted: Mounted 2-3
J10	Reset source options	Activate Reset driven from serial interface (U_RSTn)	Mount pos.1-2	No mounted 1-2
		Activate Reset driven from Debugger (T_Reset)	Mount pos. 3-4	Mounted 3-4
J15		Disable I2C	No jumper Mount	-

HDR	Function of headers	Jumper options		Default jumper setting
	Enable Pullups of I2C for PMOD and MikroBUS	Power Pull-ups with 3.3 V	Mount pos.1-2	No mounted 1-2
		Power Pull-ups with 5 V	Mount pos.2-3	No mounted 3-4
J16	Enable I2C signals for PMOD and MikroBUS	Enable SDA	Mount pos.1-2	No mounted 1-2
		Enable SCL	Mount pos.3-4	No mounted 3-4
J24	Software Trigger activation	TRIG_0 mapped to P0_10	Mount pos.1-2	Mounted 1-2
		TRIG_1 mapped to P0_08	Mount pos.3-4	
		TRIG_2 mapped to P1_01	Mount pos.5-6	
		TRIG_3 mapped to P1_02	Mount pos.7-8	
		TRIG_4 mapped to P0_12	Mount pos. 9-10	
		TRIG_5 mapped to P0_01	Mount pos.11-12	
		TRIG_6 mapped to P0_14	Mount pos.13-14	
		TRIG_7 mapped to P1_04	Mount pos.15-16	

4. DA14592 SmartBond Module DB

The system on DA14592 SmartBond Module Daughterboard (DB) consists of the DA14592 Module, the power section, the general-purpose LED, the Reset button, Power switch, the Debugging and Mating connectors. The system block diagram is shown in Figure 5, and the actual component's location in Figure 6 for top side and Figure 7 for bottom side of Daughterboard.

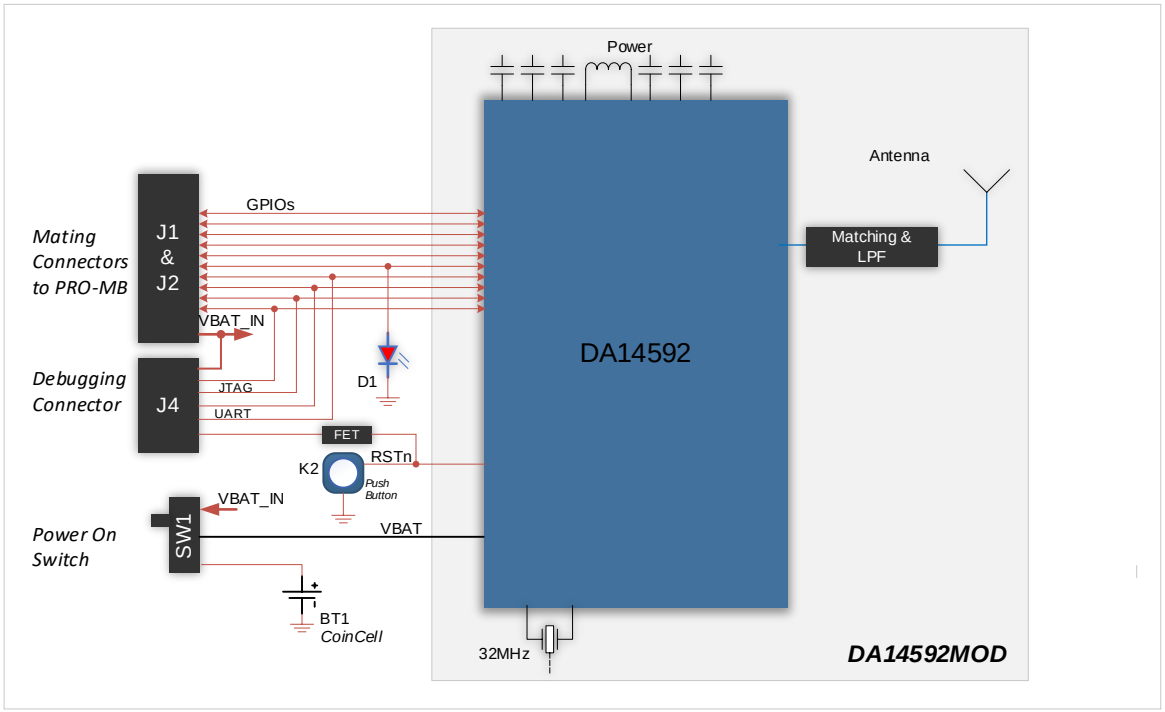

Figure 5. Block diagram of DA14592 SmartBond Module DB

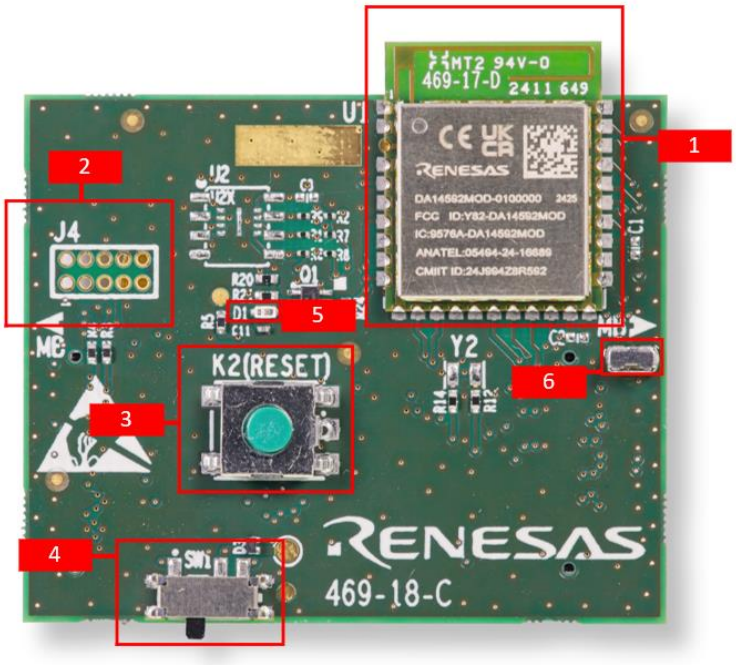

Figure 6. Top side components of DA14592 SmartBond Module DB

The marked and numbered sections of the system are:

1. DA14592 SmartBond Module (U1)

2. JTAG/2-wire UART debugger connector (J4)
3. Reset button (K2, Reset)
4. Power switch (SW1). Selection between VLDO from PRO-MB/ Coin cell.
5. General purpose LED (D1)
6. GND pad (GND)

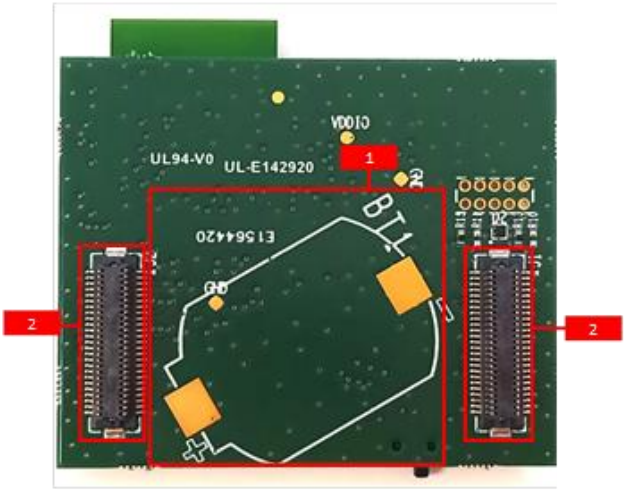

Figure 7. Bottom side of DA14592 SmartBond Module DB

The marked and numbered sections of the system, for the bottom side, are:

1. Coin cell battery (BT1, optional)
2. Interface connectors to motherboard (J1, J2)

Table 2. Test points description

Test point	Assigned to	Comments
TP6	VDDIO	Output 1.8 V power rail
TP9	VBAT	Power supply rail of VLDO of DA1459x Pro-MB or external coin cell battery
TP10	FIDUCIAL	Not electrically connected
TP11	FIDUCIAL	Not electrically connected
TP12	GND	GND
TP13	GND	GND
TP14	GND	GND
TP20	GND	GND
TP19	ESD_WARNING SIGN	Not electrically connected
TP21	FIDUCIAL	Not electrically connected
TP22	FIDUCIAL	Not electrically connected

4.1 Power Section

The power supply on the DA14592 SmartBond Module DB supports these options:

- Power supply from DA1459x Pro-MB. The supply voltage comes from VLDO setup (U5) with output voltage range to meet recommended operating conditions of DA14592 SmartBond Module. For recommended operation conditions, see Ref.[2] and for VLDO selection, see Ref.[3]
- Power supply from Coin cell battery (BT1). Battery case is mounted on bottom side of the daughterboard.

NOTE
Do not mount coin cell battery when daughterboard is supplied from DA1459x Pro-MB.

Power selection between DA1459x Pro Development Kit VLDO or Coin Cell Battery is done using SW1 power switch.

The power supply from VLDO of DA1459x Pro Development Kit allows measuring current drawn from DA14592 SmartBond Module by using the PMM2 circuit and the power profiler of Renesas's SmartSnippets Toolbox. For more information on current measurement, see Ref.[3].

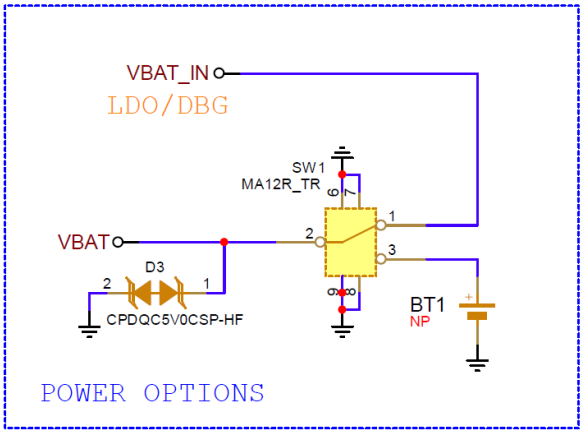

Figure 8. Power option selection for DA14592 SmartBond Module DB

Figure 9. Power option default configuration

4.2 Reset Operation

On DA14592 SmartBond Module DB there are four ways to activate Reset:

- By pressing button (K2)
- Through Debugger connector J4. As the Reset signal of J4 is active high, a nFET is added.
- Through T-Reset signal on DA1459x Pro-Motherboard. This connected directly (wired-OR)
- to DA1459x chip pin. For more information, see Ref.[3].
- Through U_RSTn signal on DA1459x Pro-Motherboard. This signal is tied together with
- T_Reset and connected directly (wired-OR) to DA1459x chip pin. This option requires additional software. By default, it is not enabled. For more information, see Ref.[3].

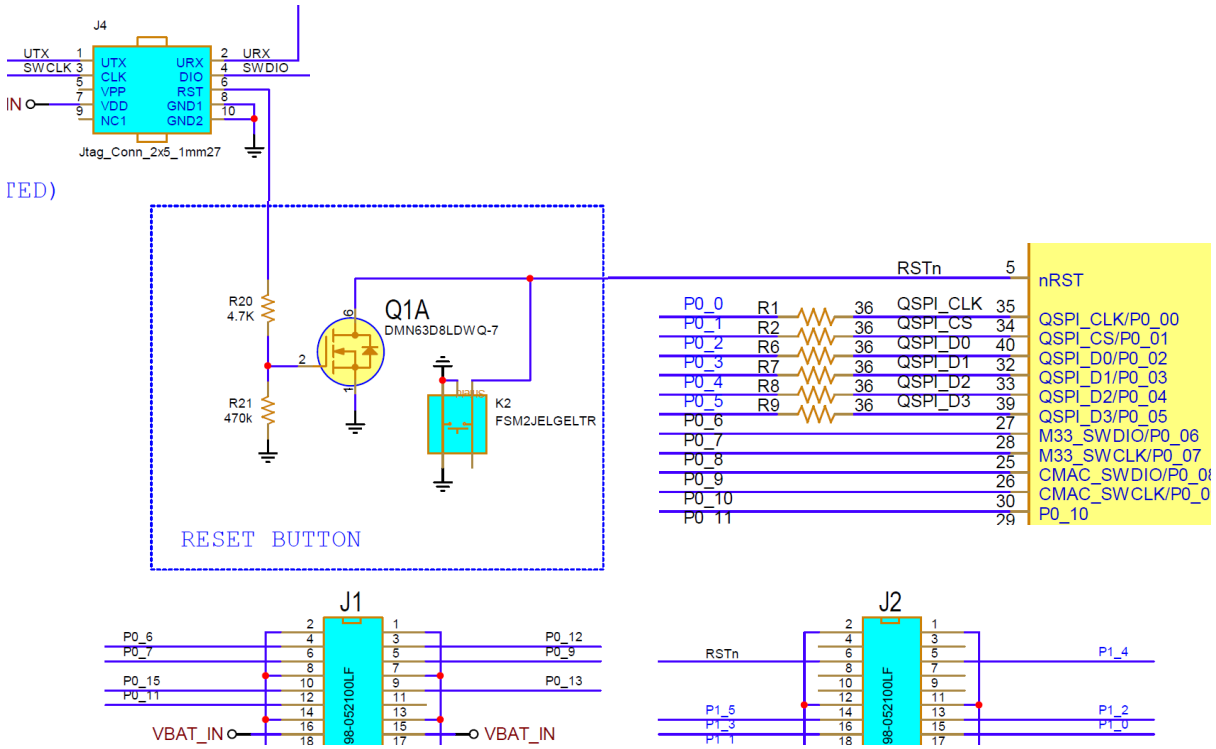

Figure 10. The Reset circuitry

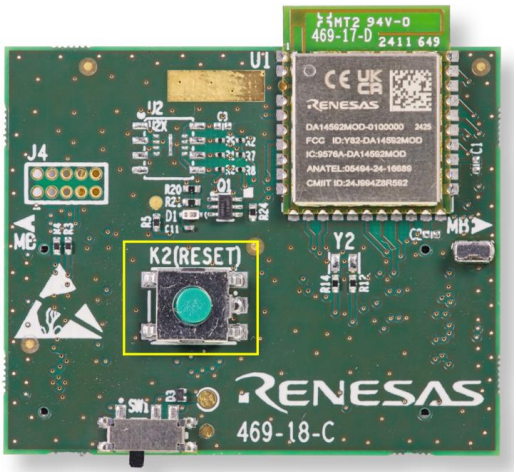

Figure 11. The Reset button on DA14592 SmartBond Module DB

4.3 General Purpose LED

LED D1 is a general-purpose LED that can be used for optical indications. LED is driven by P1_1 through a N-FET (Figure 12 and Figure 13).

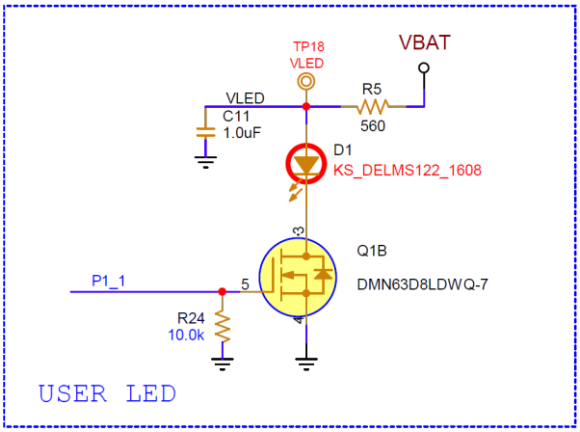

Figure 12. General purpose LED circuit on DA14592 SmartBond Module DB

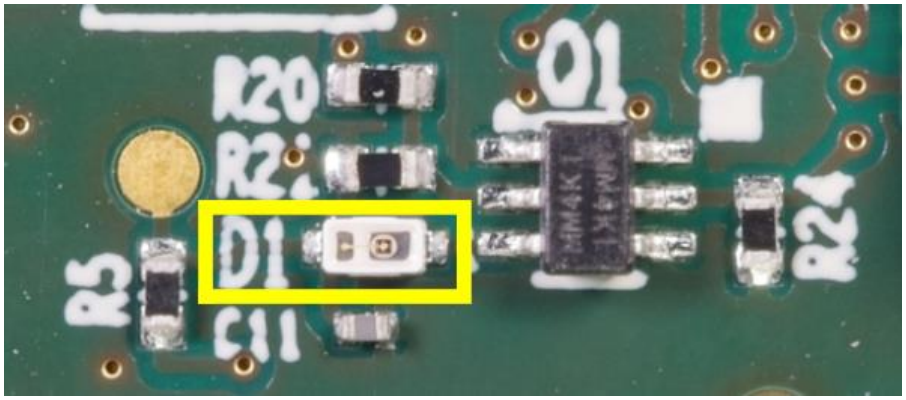

Figure 13. General purpose LED on DA14592 SmartBond Module DB

4.4 QSPI External Memory

On DA14592 SmartBond Module an optional external QSPI memory place holder, U2 is applied. By default, it is not populated as DA1459x contains an embedded flash memory. For more information on the supported memories, see Ref. [3].

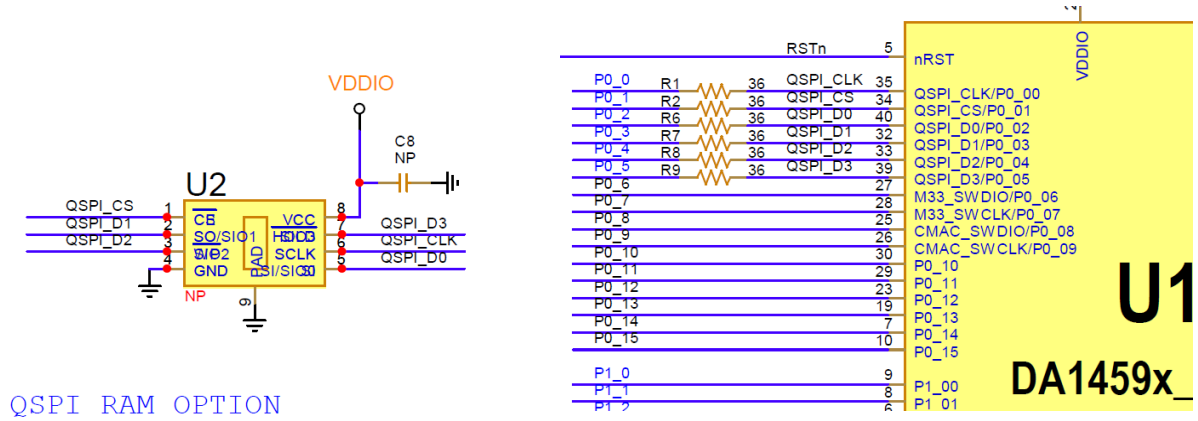

Figure 14. The external QSPI memory (U2) circuitry

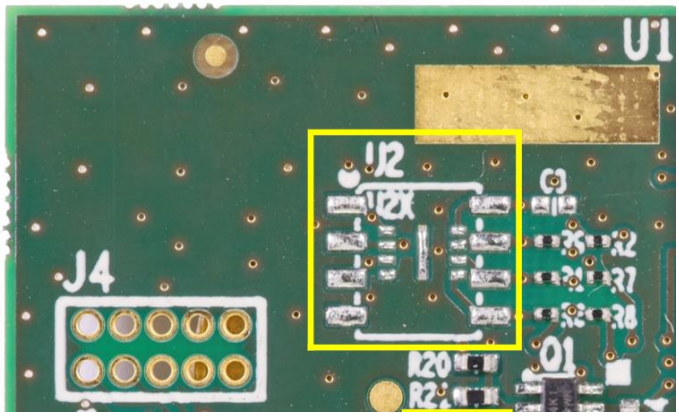

Figure 15. The external QSPI memory (U2) placeholder

4.5 Debugging Interface

On the DA14592 SmartBond Module DB there is an optional JTAG connector that can be used for debugging through SWD or for communication through UART. See signal assignment in Table 3.

As described in the datasheet, DA1459x contains two processors, an ARM Cortex-M33TM and an ARM Cortex-M0+TM. Both processors can be accessed from J4, through their SWD bus. By default, the SWD of M33 is enabled. For enabling SWD bus of M0+, two resistors must be removed (R10, R15) and two others to be mounted (R11, R13).

Table 3. Debugging header – pins assignment

Pin №	Pin function	Default signals	Optional signals	Comments
1	UTX	P0_13	-	Through 100 Ω
2	URX	P0_15	-	Through 100 Ω
3	SWCLK	P0_7 (SWCLK_M33)	P0_9 (SWCLK_M0+)	To Enable optional signal: solder R11/remove R15
4	SWDIO	P0_6 (SWDIO_M33)	P0_8 (SWDIO_M0+)	To Enable optional signal: solder R13/remove R10
5	VPP	No Connect	-	-
6	RST	RST	-	Driven to DA14592 through inverter
7	VDD	VBAT_IN	-	-
8	GND	GND	-	-
9	No Connect	No Connect	-	-
10	GND	GND	-	-

SWD of M33 is also connected to the Pro-Motherboard onboard J-Link debugger. Consequently, by enabling the SWD of M0+ connectivity on J4, you can access both processors (M33 and M0+) of DA14592.

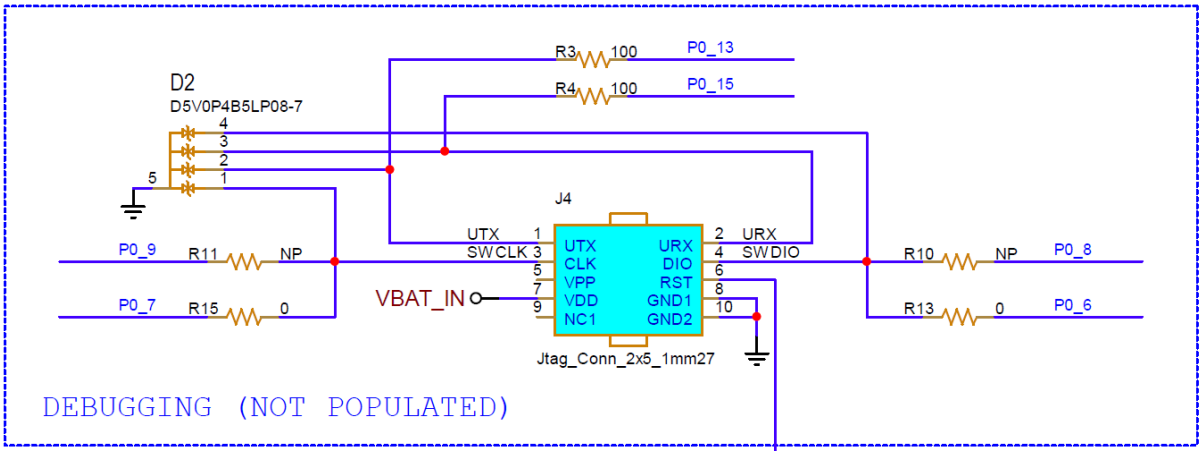

Figure 16. Debugging header (J4)

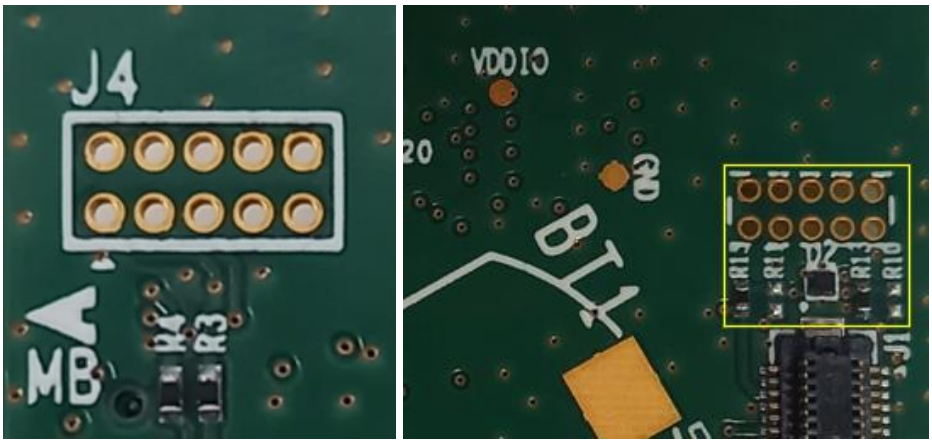

Figure 17. Debugging header (J4) top and bottom view

4.6 Interface to Motherboard

The signals of DA1459x are routed to DA14592 SmartBond Module DB through J1, J2 mating connectors, and they are distributed into the Pro-Motherboard. They are either used for debugging purposes or they are connected to MikroBUS/PMOD interfaces (Figure 18 and Figure 19). All signals are exposed to break out headers for monitoring purposes.

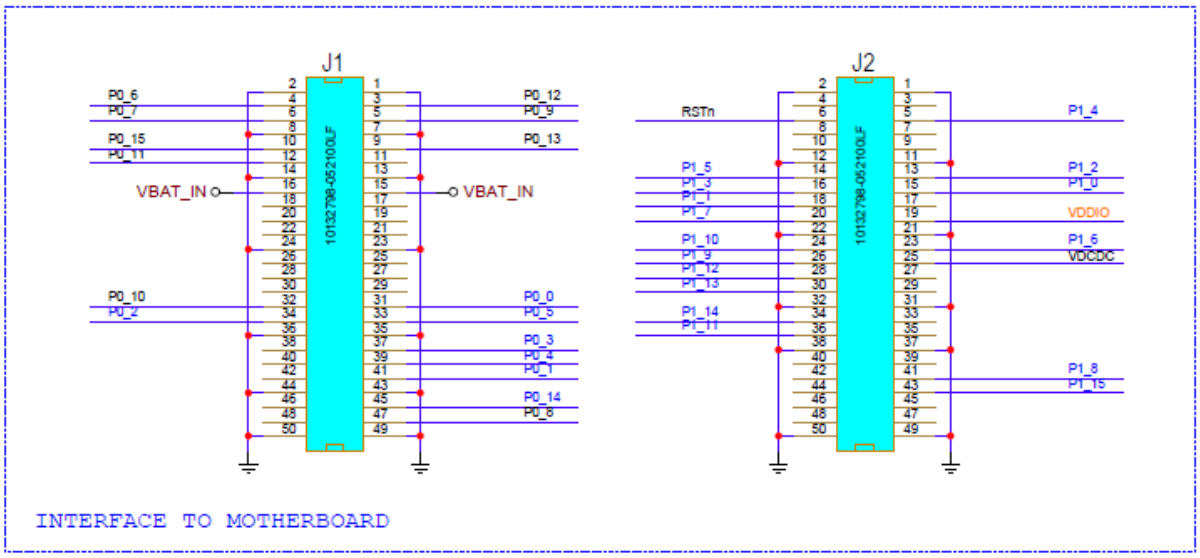

Figure 18. Interface connectors (J1, J2)

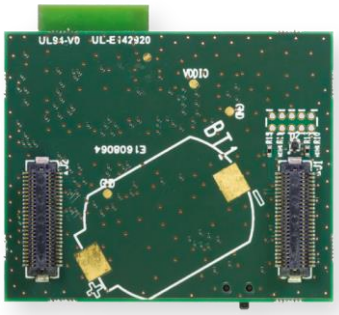

Figure 19. Interface connector on DA14592 SmartBond Module DB bottom side

Appendix A DA14592 SmartBond Module DB [469-18-C]

A.1 Schematic

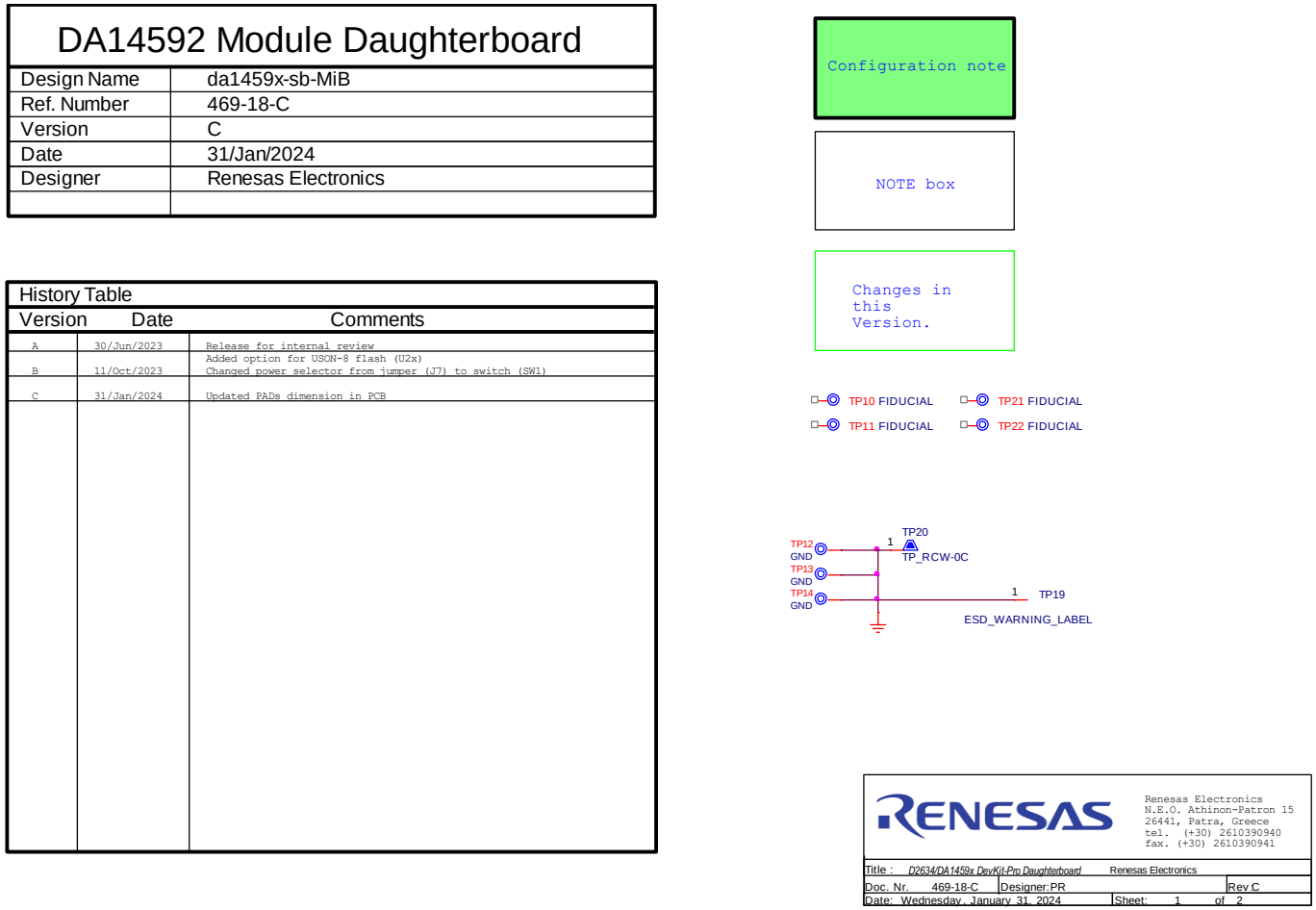

Figure 20. DA14592 SmartBond Module DB schematic – Release Note

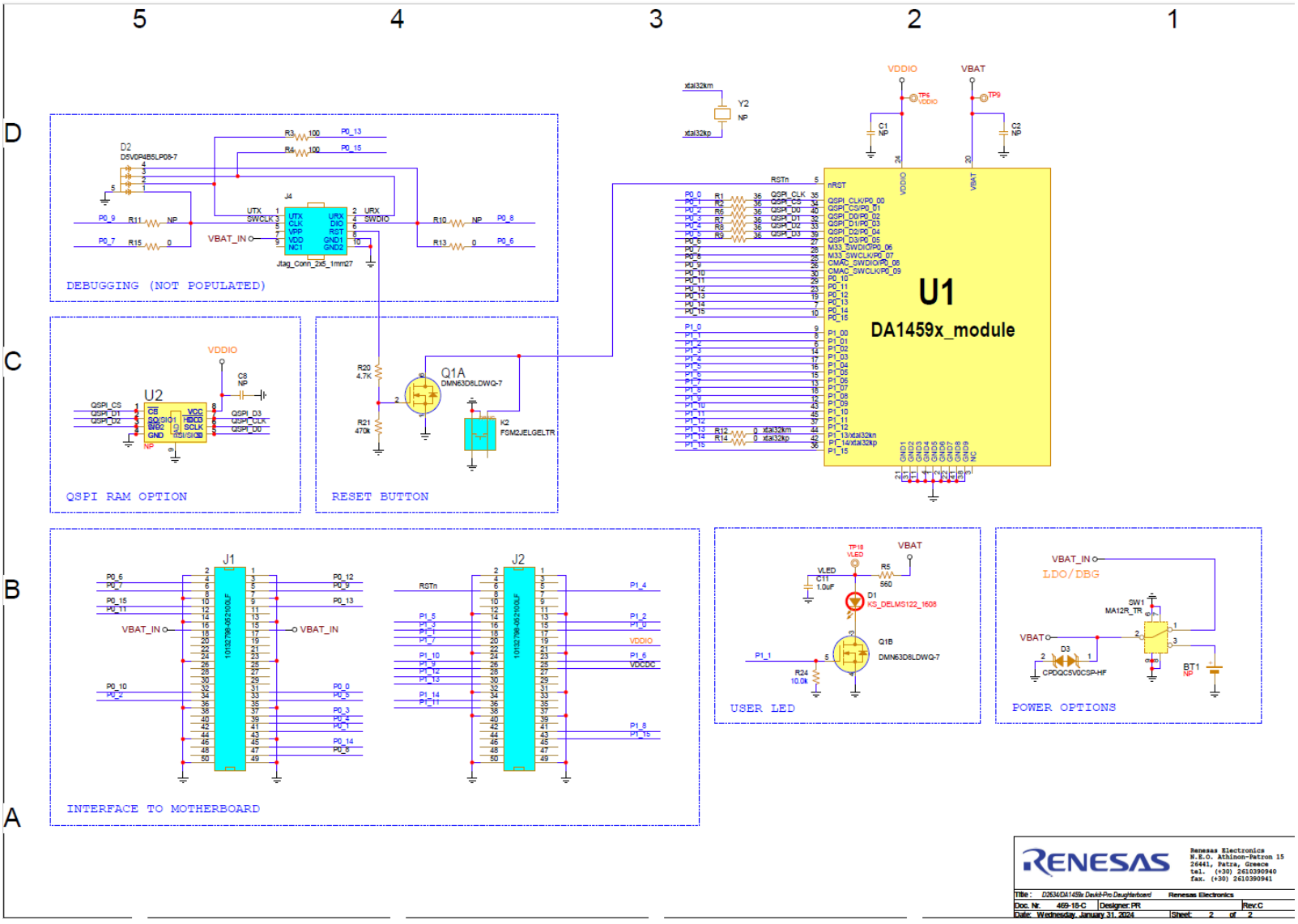

Figure 21. DA14592 SmartBond Module DB - DA1459x SoC section

A.2 Placed Components

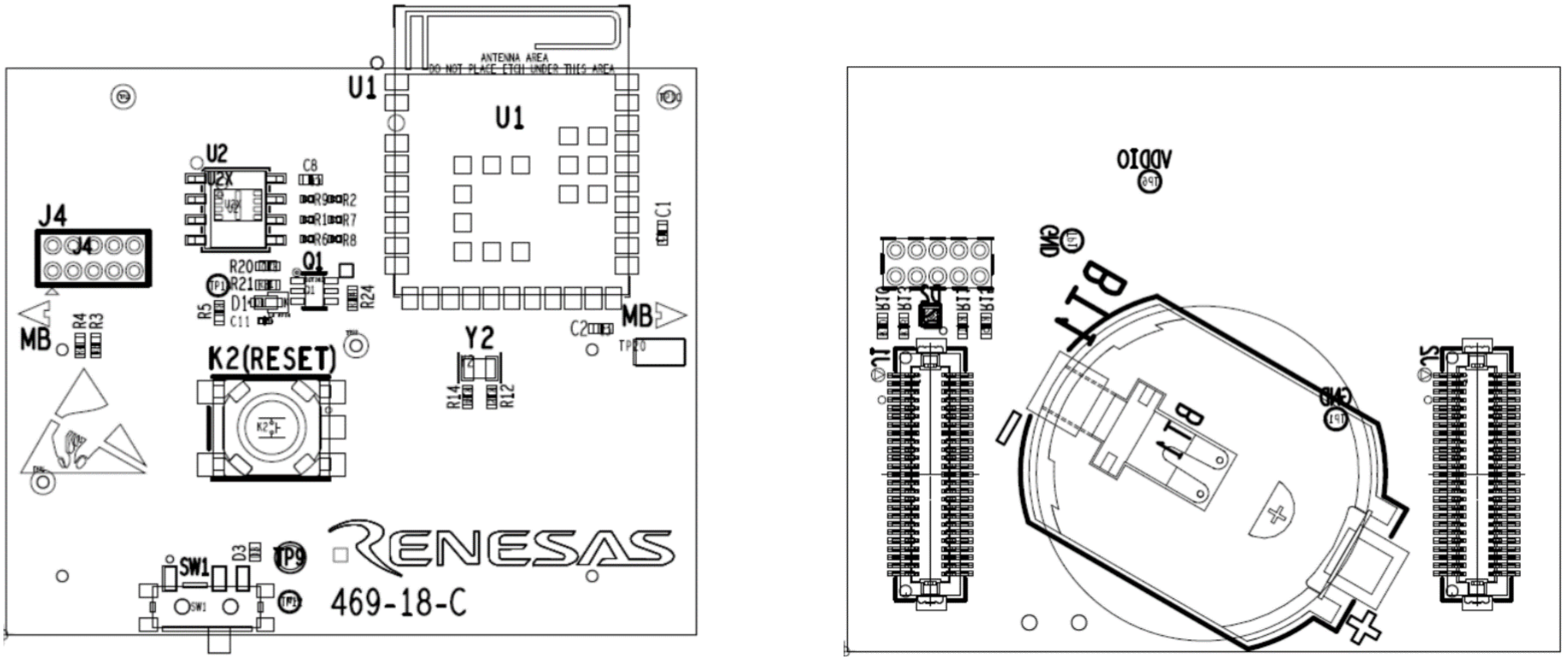

Figure 22. Components on top and bottom sides for DA14592 SmartBond Module DB [469-18-C]

5. Revision History

Revision	Date	Description
1.0	Sep 20, 2024	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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