User Manual

DA9070 / DA9073 Demo Board User Guide

UM-PM-035

Abstract

This guide describes the basic setup and operation of the DA9070 and DA9073 Demo Board. The DA9070 / 73 is a highly integrated ultra-low IQ PMIC providing battery charging, buck and boost regulators, 3 LDOs, and power path management. The DA9070 includes analog battery monitoring to support an external fuel gauge. The Demo Board is a flexible platform designed for evaluation of all the PMIC's functions and features. The DA9070/73 can be configured through I2C with SmartCanvas GUI software and the included USB hardware interface, also described in this document.

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1 References

[1] DA9070 or DA9073 Datasheet

[2] Schematic: DA9070_73_Demo_SCH.pdf

[3] PCB Layout: 320-30-A_Demo_PCB.pdf

[4] Bill of Materials: 320-30-A_Demo_BOM.xlsx

2 Jumper Configuration

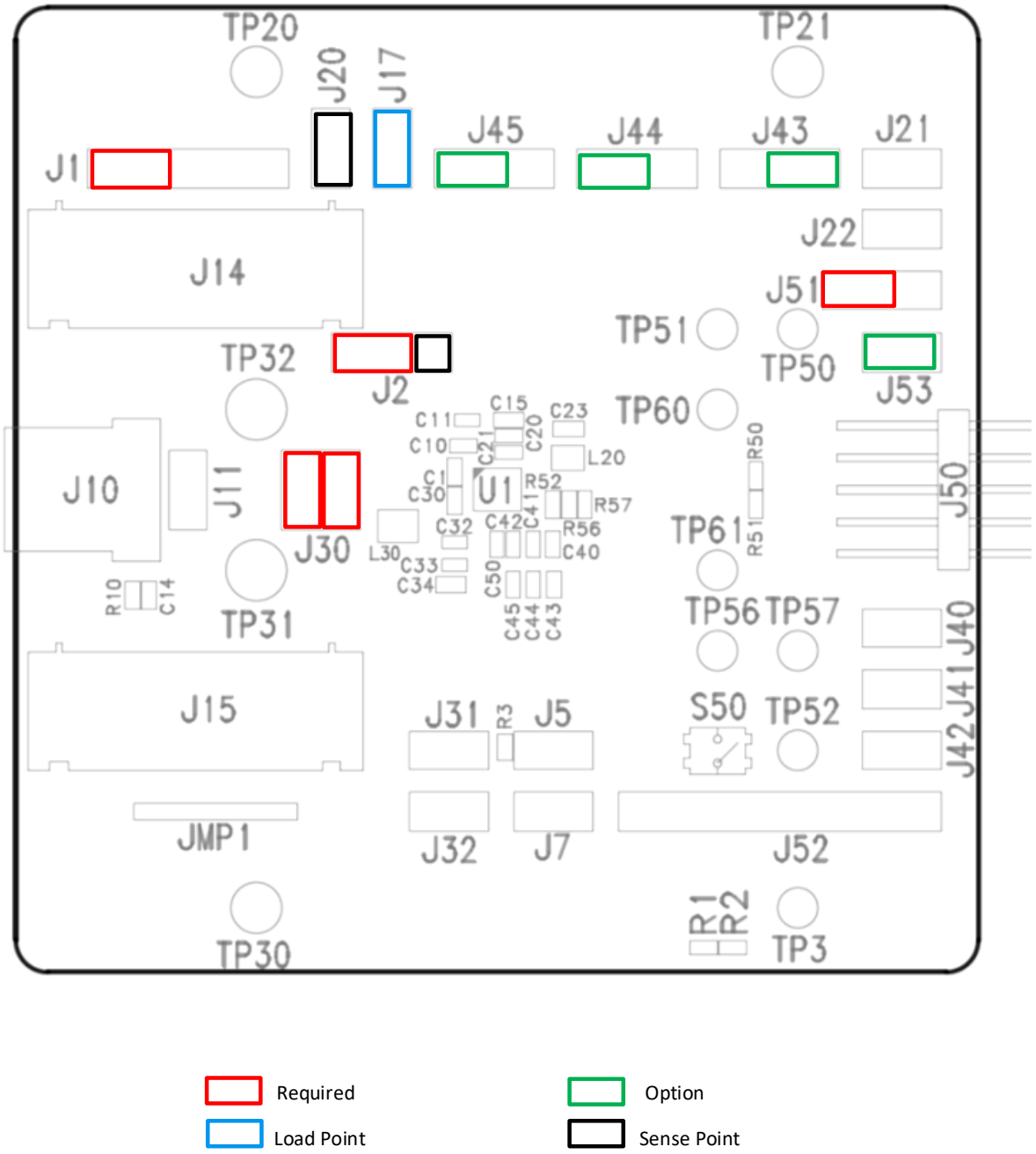

Figure 1: Typical Jumper Positions and Connection Points

Table 1: Headers and Connectors

Designator	PCB Label	Function	Comment
J1	VBAT	Battery Connection	S+ must be connected by jumper to +. NTC connection is optional
J2	IBAT	Battery input current	Jumper must be installed at pins 2 to 3
J5	I_MON	IMON signal	Battery discharge current monitor
J7	VBAT_DIV	VBAT_DIV signal	
J10	-	USB mini VDD_PWR input	USB power only
J11	VDD_PWR	VDD_PWR input	
J14	VDD_PWR	VDD_PWR positive input	banana jack
J15	PGND	VDD_PWR negative input	banana jack
J17	VDD_SYS	VDD_SYS load point	
J20	VDD_BUCK	BUCK input voltage sense	
J21	VO_BUCK	BUCK output voltage	2-pin
J22	PGND	BUCK output ground	2-pin
J30	VDD_SYS / VDD_BST	BOOST input voltage connection	
J31	VO_BOOST	BOOST output voltage	2-pin
J32	PGND	Boost output ground	2-pin
J40	VLDO0	LDO_0 output voltage	
J41	VLDO1	LDO_1 output voltage	
J42	VLDO2	LDO_2 output voltage	
J43	VO_BUCK / VDD_LDO0 / VDD_SYS	LDO_0 input select	Install at either VDD_SYS or VO_BUCK if LDO is used
J44	VO_BUCK / VDD_LDO1 / VDD_SYS	LDO_1 input select	Install at either VDD_SYS or VO_BUCK if LDO is used
J45	VO_BUCK / VDD_LDO2 / VDD_SYS	LDO_2 input select	Install at either VDD_SYS or VO_BUCK if LDO is used
J50	USB / I2C	USB/I2C module connector	
J51	VDDIO Select	VDDIO source select	Typically install jumper at Buck
J52		I/O sense points	MODE, ROUT_N, RIN_N, WD, SYS_FLT, PWR_FLT, AGND
J53	MODE	Connects MODE to I2C module	Allows GUI to control MODE pin

Table 2: Test Points

Designator	PCB Label	Function	Comment
TP3	TMP_SNS	Monitor battery temp sense voltage	
TP20, 21, 30	PGND		
TP31	VDD_BST	Optional Boost input voltage	
TP32	PGND (BST)	Optional Boost input ground	
TP50	MODE	Sense point	
TP51	VDDIO	Sense point	Can be used to connect external VDDIO supply
TP52	RIN_N	Sense point	
TP56	PWR_FLT	Sense point	
TP57	SYS_FLT	Sense point	
TP60, 61	AGND		
JMP1	GND		

3 Input Power Connections

The DA9070 / DA9073 requires 2 power connections: a battery at VBAT and a charging source at VDD_PWR (typically USB power).

EQUIPMENT NOTE
The battery connection will both sink and source current. Therefore, the supply connected to VBAT must be able to sink current. A battery emulator, source meter, bi-polar supply, battery, or similar must be used. Standard bench power supplies that cannot sink current should not be used as the VBAT supply.

If a current meter is used at J2 to monitor battery current, the meter's impedance will lower the input voltage at the DA9070 / 73 during discharging. This voltage drop should be considered during testing. A current meter will also affect the sensed battery voltage during charging. Sensed voltage is critical during charging, and therefore it is not recommended to use a series current meter.

3.1 J1: Battery Connections

The battery connects to the '+' and '–' pins at header J1. The S+ pin of J1 connects to the VBAT_SNS pin of the DA9070 / 73. This sense pin must be connected either by a jumper to '+' or directly to the battery '+' terminal.

The TMP_S pin of J1 connect to the TEMP_SNS pin of the IC, as well as the temp sense voltage divider (R1 and R2). If the battery pack includes an NTC, it should be connected to J1 here. Test pin TP3 can be used as a sense point. If there is no NTC, disable the temp sense function by register control or connect a 10k ohm resistor from TMP_SNS to ground to mimic an NTC in nominal temperature range.

The J2 header can be used for battery current sensing. A jumper must be installed between pins 2 and 3, or replaced with a current meter.

3.2 J10 or J14-15: VDD_PWR

The VDD_PWR supply can connect to either the J14/J15 banana jacks, or through the J10 mini-USB connector. Header J11 can be used as an input voltage sense point.

3.3 J43, J44, and J45: LDO Inputs

These three headers allow the input supply to each LDO to be selected as either VDD_SYS or the Buck output voltage. If an LDO is not used, this header can be left open.

3.4 J30, TP31, and TP32: VDD Boost

The boost input supply, VDD_BST, is typically taken from VDD_SYS and connected at header J30. Because the boost may require high input currents, 2 parallel jumpers are used to connect VDD_SYS to VDD_BST.

An external supply may also be used for VDD_BST by removing the J30 jumpers and connecting directly to VDD_BST and PGND at TP31 and TP32.

3.5 J17 and J20: VDD Buck

The Buck regulator takes its input directly from VDD_SYS. The input to the Buck, VDD_BUCK, can be monitored at header J20 which is kelvin connected close to the buck input caps.

4 Output Power Connections

The following headers are used for output voltage connections:

- J21: Buck Positive Output and Sense
- J22: Buck Ground Output and Sense

- J31: Boost Positive Output and Sense
- J32: Boost Ground Output and Sense

The Buck and Boost headers are each 2-pins, allowing one pair to be used for load and the other for sense.

- J40 – J42: LDO Outputs

LDO outputs are 2-pin headers and marked + and -.

- J17: VDD_SYS

VDD_SYS is the same net as VDD_BUCK and is an intermediate voltage rail which can be used as an output.

A system load can be connected to VDD_SYS at header J17. The voltage at VDD_SYS is not regulated, but will track to the higher of VBAT or VDD_PWR.

Table 3: Typical Current and Voltage Ratings

Power Input / Output	Maximum Current	Voltage Range	Note
VDD_PWR	Up to 600 mA	3.6 to 5.5 V	Operating range
VDD_PWR	-	5.5 to 20 V	Input disabled in OVP
VBAT	Up to 500 mA	0 to 4.65 V	Charging
VBAT	0.55 A to 1.75 A	2.8 to 4.65 V	Discharging
BUCK	300 mA	0.6 to 2.1 V output	
BOOST	300 mA	At 5 V output	At minimum input voltage: 2.8V
BOOST	125 mA	At 12 V output	
LDO_0	150 mA	0.8 to 3.15 V output	
LDO_1	150 mA	0.8 to 3.3 V output	
LDO_2	150 mA	0.8 to 3.3 V output	

5 I²C Interface and VDDIO selection

Before using the provided USB-I2C module, the VDDIO source must be first selected.

The VDDIO voltage must be lower than VBAT or VDD_PWR and is best supplied by the Buck output or an LDO output. The Buck output is recommended as it is enabled by default at power up (although that can be changed by OTP configuration).

Install the J51 jumper in the BUCK position and connect the USB-I2C module to the 10-pin header, J50 as shown in Figure 2. There are 2 USB-I2C module versions, both connect with the same orientation, pcb number 162-09-xx facing up as shown in Figure 2.

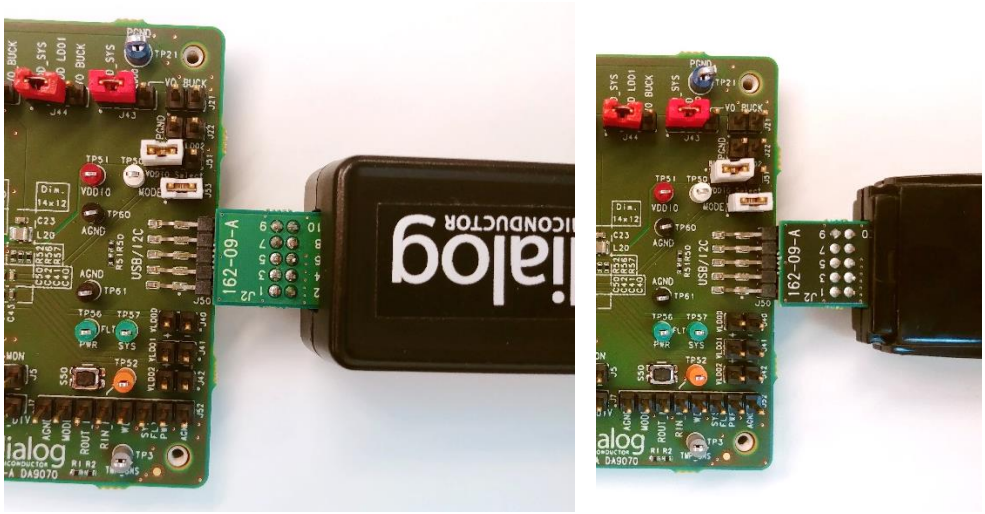

Figure 2: USB-I2C Module and VDDIO Connection

The I2C module must be connected to the host PC by USB cable. This provides both power and host communication to the module, regardless of the VDDIO supply.

When power is applied to VBAT or VDD_PWR, the Buck output will startup, powering VDDIO and allowing the GUI to communicate with the DA9070 or DA9073.

The USB-I2C module includes the following signals:

- SDA
- SCL
- MODE output (if J53 is installed)
- WD output
- PWR_FLT input
- SYS_FLT input

6 GUI

The GUI allows read/write access to all DA9070 and DA9073 registers and includes several useful features.

6.1 MAIN SCREEN

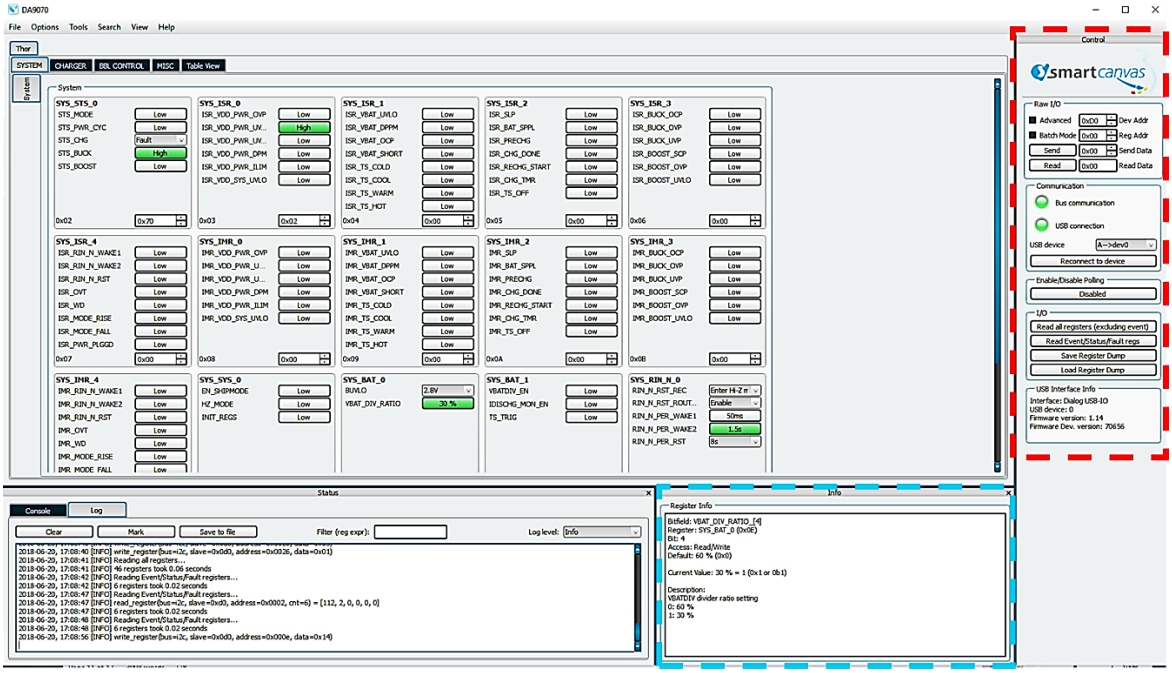

Figure 3: GUI Main Screen

The DA9070 or DA9073 GUI main screen is shown when the GUI is started. There are five tabs at the top: SYSTEM, CHARGER, BBL CONTROL (buck, boost, LDO), MISC, and Table View.

Registers can be written to directly from each of the tabs in this screen.

On the right side is the Control window. In normal operation, both the USB and Bus Communication (I2C) lights should be green.

If polling is enabled in this window, all register data will be automatically updated. This does not include interrupt (IRQ) event registers. To read the event registers, click on the Read Event button. All interrupts which have occurred since the previous READ will be high, showing all historical events. Reading the event registers a second time will READ-CLEAR any events which are no longer valid.

To update all register status without using polling, click “Read all registers”.

At the lower right is the Register Info window. Hovering over any register box in the main screen will display a description and register settings in this box.

6.2 Table View

The Table View tab shows the register map, which has a similar appearance to the map in the datasheet. Registers can be directly written to the Data column on the left.

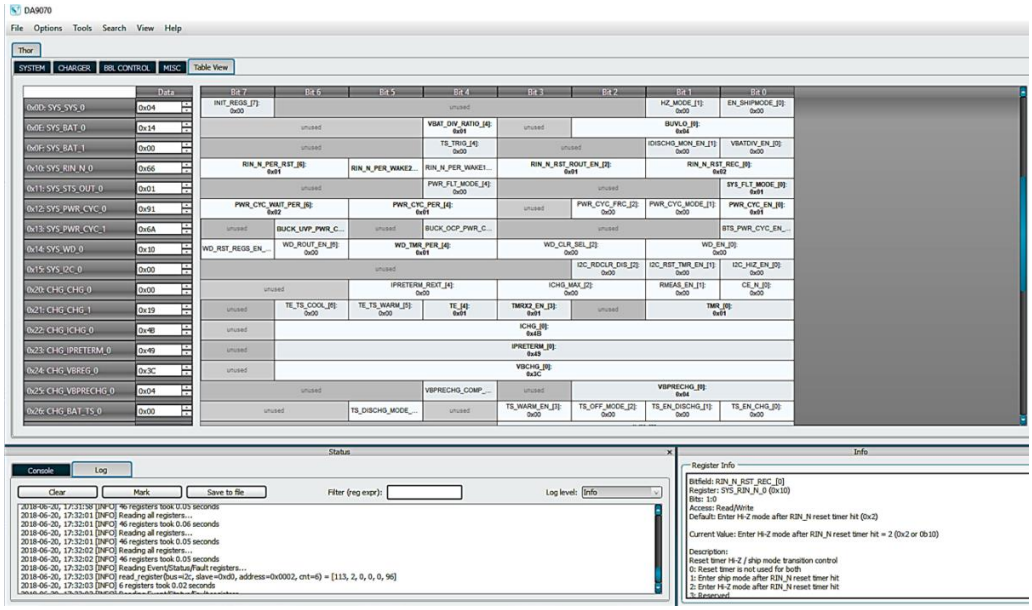

Figure 4: Table View

6.3 GPIO CONTROL

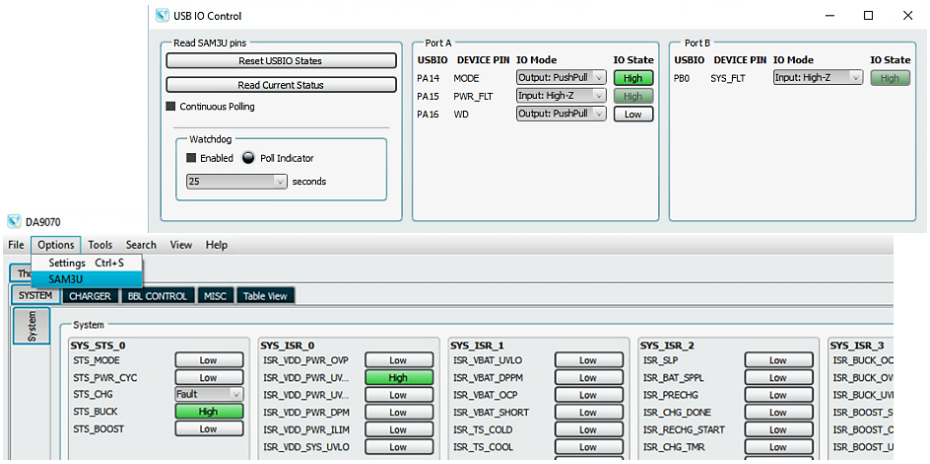

Figure 5: GPIO Window

To open the GPIO control window, select:

Options→SAM3U
This window allows you to control or monitor five functions via GPIO: MODE, PWR_FLT, SYS_FLT, and WD.
Each I/O can be configured as an input or output using the IO Mode pulldown menus. It is recommended to configure MODE and WD as push-pull outputs. The SYS_FLT and PWR_FLT signals should be configured as High-Z inputs.
To continuously read the status of the inputs, check Continuous Polling. Otherwise the state will not be updated automatically, but can be manually updated using the Read Current Status button.

- Watchdog (WD)
  When enabled, the WD GPIO will send periodic watchdog pulses to the WD pin. The WD period is selectable via the pulldown menu.
- MODE
  The MODE pin is used to enable/disable charging when VDD_PWR is plugged in.
  When the DA9070 / 73 is battery powered (VDD_PWR not plugged in), the MODE pin controls entry and exit from Hi-Z mode. Because MODE is edge triggered, the pin (or GUI button) may have to be toggled to exit Hi-Z mode after VDD_PWR is unplugged. In Hi-Z mode, I2C communication will be disabled. However the GPIO window and MODE pin control is still active and can be used to exit Hi-Z mode.
- SYS_FLT and PWR_FLT
  These pins are open drain status flags which can be read through the GUI.
  In the default configuration, SYS_FLT will show the charging status and PWR_FLT will show the status of VDD_PWR.

6.4 SEARCH

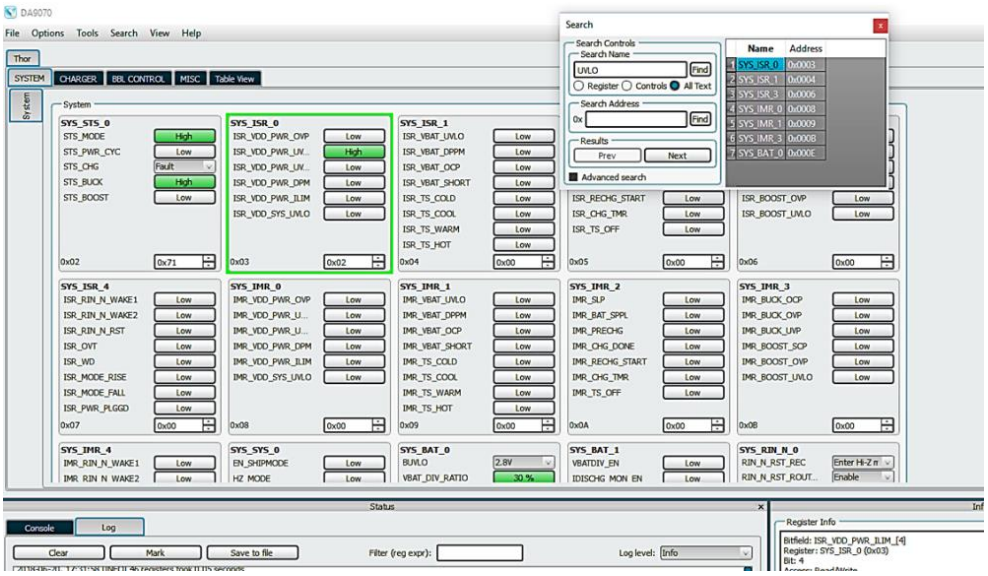

Figure 6: Search Window

To open the Search window, select:

Search→Find Register
Registers can be searched by name or register address. When the find button is clicked, the matching register in the main window will be highlighted in green. For a text search, a second window will open showing all matches.

6.5 GUI Settings

To open the Settings window, select:

Options→Settings

The settings window allows you to configure I2C address, I2C clock frequency, numerical base display, and others.

The I2C frequency can be set between 100kHz and 400kHz.

Changing the I2C address in the GUI settings does not change the I2C slave address of the DA9070 / DA9073.

7 Powering Up

Before powering up the evaluation board, confirm that VBAT and VDD_PWR connections are correct and BUCK is selected for VDDIO. The USB interface can be connected at any time.

Although either supply can be used, it is recommended that only VBAT be powered initially. This will allow you to confirm the register settings before starting charging.

Once power is applied to either input, the DA9070 / 73 will start and VDD_SYS will ramp up. Depending on the OTP configuration, one or more outputs will then start up automatically.

The GUI can be started at any time and the status indicators will turn green for USB connection and I2C communication. If the I2C indicator remains red, click ‘re-connect to IC’.

Before changing settings, click ‘Read all Registers’ and “read status/events’. Because Events are read clear, they should be read twice to confirm the present status.

All outputs, charge settings, and other functions can now be confirmed and modified if needed.

Assuming a battery is connected; simply apply power to VDD_PWR to begin charging. If charging does not start automatically, confirm the MODE status, CE_N status at register 0x20, and any interrupts which may prevent charging, such as Temp Sense.

8 Other Features

8.1 Pushbutton Reset

Switch S50 is a normally off pushbutton switch connected to the RIN_N pin. When pushed for several seconds, S50 can be used to enter Ship mode or Hi-Z mode and also to toggle the reset output pin ROUT_N. A short press of the button will then exit Ship and Hi-Z modes. Refer to the datasheet for details.

RIN_N is internally pulled high to VDD_SYS; ROUT_N is open drain and pulled up to VDDIO by R52. These signals can be monitored at the orange test points TP52 and J52.

8.2 Status Flags: SYS_FLT and PWR_FLT

The SYS_FLT and PWR_FLT pins are open drain status flags which indicate interrupts, VDD_PWR status, and charging status. Both pins are pulled up to VDDIO via R56 and R57.

The two signals can be monitored at TP56 and TP57, or at J52 pins 6 and 7. They can also be monitored in the GUI GPIO window. However, event interrupts are signaled by a 128usec pulse at the SYS_FLT pin, which is too short to be visible in the GUI.

9 Battery Monitor Features: DA9070 only

9.1 IMON (Battery Current Monitor)

The IMON function sources a current proportional to the battery discharge current to enable fuel gauging or other external current monitoring functions. The IMON current through R3 generates a voltage which can be monitored at header J5.

The IMON current is equal to battery current at 1mA/A scale, therefore an R3 value of 1k generates 1V/A at J5. The R3 value can be changed, but IMON accuracy will be degraded if the voltage rises above 1.4V.

9.2 VBAT_DIV (Battery Voltage Monitor)

Similar to IMON, VBAT_DIV is an output voltage proportional to the battery voltage. The VBAT_DIV and GND_DIV pins are connected to J7 where they can be connected to external monitoring or fuel gauging. Measurements can be made directly at the + and – pins of J7. The VBAT_DIV ratio is 30% by default and can be changed to 60% by I2C control.

10 Optional Components

For most applications, the default BOM performs well over the DA9070 and DA9073 full operating range. For additional flexibility, the evaluation board includes unpopulated and easily modified components.

- C13 is a bulk electrolytic input capacitor on VDD_PWR. Placing this capacitor may help to reduce parasitic ringing when long cables are used.
- C31 is an additional boost input capacitor. If VDD_BST is not connected to VDD_SYS, 10uF or greater is recommended here. C31 may also be required if starting the boost into a load. C31 is located on the bottom side of the PCB.
- R53, R54, and R55 can be used to set charge current, termination current, and VDD_PWR current limit without using I2C control. Refer to the datasheet for details about R_ILIM_CHG (R54), R_ITER_CHG (R55), and R_ILIM_PWR (R53). Zero ohm is installed for all three resistors which are located on the bottom side of the evaluation board.
- R1 and R2 can be modified as required by the application. R1 and R2 should be set according to the battery NTC resistor characteristics, refer to the datasheet for details.

  If no NTC is connected, the Temp Sense function can be evaluated by placing a 10kΩ resistor in parallel with R1. This will provide a voltage between the warm and cool thresholds at the TEMP_SNS pin (no fault).

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