

ISL70062SEHEV1Z

User's Manual: Evaluation Board

High Reliability

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ISL70062SEHEV1Z

Evaluation Board

The ISL70062SEHEV1Z evaluation board (shown in [Figure 3 on page 8](#)) features the [ISL70062SEH](#) 10A NMOS load switch IC. The IC is a radiation hardened, single channel load switch featuring ultra-low r_{ON} and controlled turn-on rise time for use in space power supply switching applications. The ISL70062SEH device uses a NMOS pass device as the main switch that operates across an input voltage range of 0V to ($V_{CC} - 2V$) and can support a maximum of 10A continuous current. The V_{CC} bias voltage range is from 3V to 5.5V.

The ISL70062SEHEV1Z evaluation board provides a quick and easy method to evaluate the unique ISL70062SEH NMOS load switch IC. To use this evaluation board properly requires a thorough knowledge of the operation of the IC. See the [ISL70062SEH](#) datasheet for information about the device operation, function, and performance.

This user manual explains how to configure and use the ISL70062SEHEV1Z board to evaluate the ISL70062SEH NMOS load switch IC.

Key Features

- VIN_SENSE and VOUT_SENSE turret connectors easily measure the voltage at the SWI and SWO package pins.
- Convenient test points and connections for test equipment.
- Banana jacks for power, ground, logic, and load connections.

Specifications

The evaluation board is configured and optimized for the following conditions:

- $V_{CC} = 3V$ to 5.5V
- $V_{SWI} = 0V$ to ($V_{CC} - 2V$)
- $I_{SWO} \leq 10A$
- Board temperature: +25°C

Ordering Information

Part Number	Description
ISL70062SEHEV1Z	ISL70062SEH evaluation board

Related Literature

For a full list of related documents, visit our website:

- [ISL70062SEH](#) device page

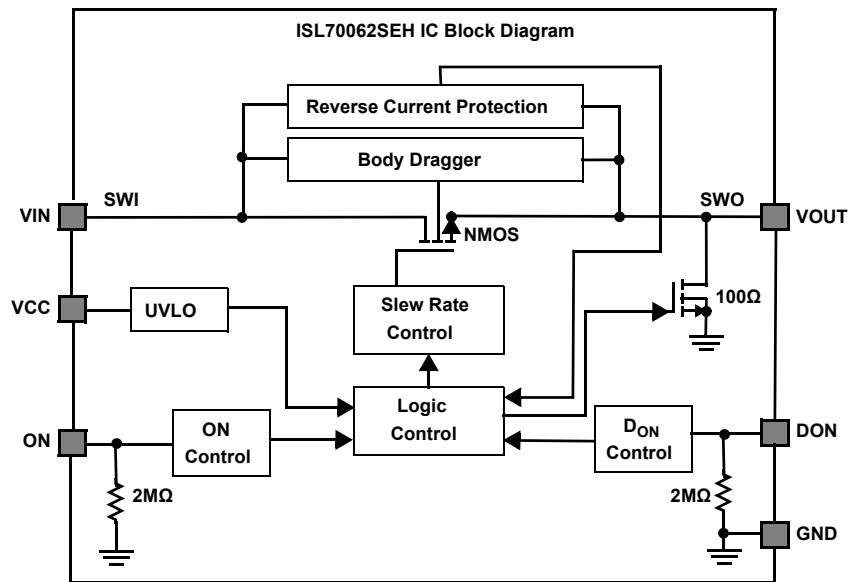
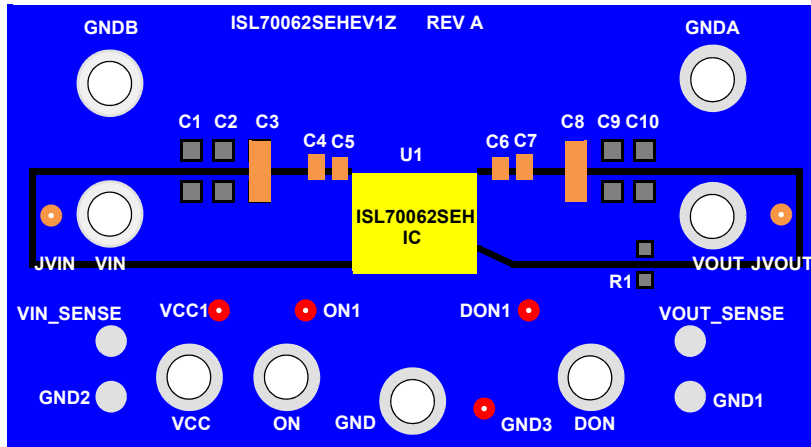


Figure 1. ISL70062SEHEV1Z Evaluation Board Block Diagram

1. Functional Description

The ISL70062SEHEV1Z evaluation board contains the ISL70062SEH radiation hardened single channel 10A NMOS load switch IC.

The ISL70062SEH device is a single channel, low voltage, high current load switch for use in space power-switching applications. The integrated circuit is a NMOS pass device with a simple logic input to turn the pass device on or off. The ISL70062SEH device is capable of 10A continuous current with a typical r_{ON} of 25m Ω with $V_{CC} = 5.5V$ and $V_{SWI} = 3.5V$ and a r_{ON} of 16m Ω with $V_{CC} = 5.5V$ and $V_{SWI} = 1.0V$. The device has a VCC pin to power the logic decoder and the level shift circuitry of the device, allowing the switching of low voltage levels. V_{CC} voltage range is 3V to 5.5V, and an internal UVLO keeps the device OFF when V_{CC} drops below 2.2V. The input voltage (V_{SWI}) range of the device is 0V to ($V_{CC} - 2V$). To reduce voltage drops and minimize inrush current, the device features an internal controlled on-time with a typical fixed rise time of 2.2ms at $V_{CC} = 5.5V$ and $V_{SW} = 3.0V$. The ISL70062SEH incorporates reverse current protection when the output voltage (V_{SWO}) increases above the V_{SWI} voltage. Additionally, there is a selectable 100 Ω MOSFET between SWO and GND to discharge the output when the main pass device is OFF. When the DON logic input = High, the discharge FET circuitry is enabled.

The ISL70062SEH is designed to operate in the harsh environment of space.

[Figure 1 on page 3](#) shows the ISL70062SEHEV1Z evaluation board block diagram with [Figure 3 on page 8](#) showing the board. The ISL70062SEHF/PROTO 14 Ld CDFP IC is soldered onto the center of the ISL70062SEHEV1Z evaluation board and is designated as U1.

The ISL70062SEHEV1Z evaluation board provides a simple platform to demonstrate the features and evaluate the performance of the ISL70062SEH load switch. The board provides easy access to the ISL70062SEH pins and convenient connectors/test points for connecting test equipment. For more information, see the schematic ([Figure 4 on page 9](#)), top layer silkscreen ([Figure 5 on page 10](#)), and "[Bill of Materials](#)" on [page 9](#). Performance data was taken using the ISL70062SEHEV1Z and basic lab equipment and is shown in [Figures 8](#) through [15](#) starting on [page 11](#).

1.1 Basic Layout

The following is the basic layout of the ISL70062SEHEV1Z (see [Figure 3 on page 8](#) or the actual board picture):

Located in the center of the board is the ISL70062SEHF/PROTO load switch IC (U1). The evaluation board has a Pin 1 dot showing how the IC should be oriented onto the evaluation board. The ISL70062SEH Pin 1 indicator lead needs to be aligned with the evaluation board Pin 1 dot indicator. The board is provided with the IC soldered onto it.

Power to bias the logic decoder and the device level-shift circuitry is located at the lower left center of the board through the banana jack labeled VCC. A DC voltage source of 3V to 5.5V must be connected between VCC and GND.

Access to the load switch SWI input of the load switch is located at the middle left side of the board through the banana jack labeled VIN. Connect a DC voltage source in the range of 0V to ($V_{CC} - 2V$) from the positive terminal to the VIN banana jack and from the negative terminal to the GNDB banana jack.

Access to the load switch ON pin of the load switch is at the banana jack labeled ON located at the lower left center of the evaluation board. Apply a digital signal in the range of 0V to V_{CC} at the ON banana jack. The ON logic input controls the state of the NMOS pass device. The ON logic input is active high. When ON = HIGH (Logic 1), the switch is ON and when ON = LOW (Logic 0), the switch is OFF.

Access to the load switch DON pin of the load switch is at the banana jack labeled DON located at the lower right center of the evaluation board. The ISL70062SEH device has a selectable discharge MOSFET circuit at the SWO output that can be activated when DON = HIGH (Logic 1). It is disabled when DON = LOW (Logic 0). The activation of this circuitry is for applications that need to quickly discharge the output of the load switch when the NMOS pass device is turned off. See the DON Logic Input section in the [ISL70062SEH](#) datasheet for a detailed description of the operation and functionality of the discharge MOSFET circuitry.

Access to the load switch SWO output is located at the middle right side of the board using the banana jack labeled VOUT. Connect a load source or resistor that draws no more than 10A of current between the VOUT banana jack and the GNDA banana jack.

The VIN_SENSE silver turret connector located at the lower left side of the board provides a connection point close to the SWI pins of the IC. The VOUT_SENSE silver turret connector located at the lower right side of the board provides a connection point close to the SWO pins of the IC. Connect a voltmeter between the VIN_SENSE and VOUT_SENSE turret connectors for precise calculation of the r_{ON} of the load switch.

1.1.1 VCC Power Supply

The ISL70062SEH requires a V_{CC} DC voltage supply in the range of 3.0V to 5.5V for proper operation. V_{CC} biases the IC. The voltage at V_{CC} should be applied before applying the VIN (SWI) voltage and the ON and DON logic voltage.

The V_{CC} power supply is connected at banana jacks VCC and GND. The power supply should be capable of delivering 100mA of current.

1.1.2 SWI Input Voltage (V_{SWI})

The ISL70062SEH SWI input voltage range is from 0V to ($V_{CC} - 2V$). The V_{SWI} drives the load connected at the SWO output when ON = HIGH (Logic 1).

The V_{SWI} power supply is connected at banana jacks VIN and GNDB. The power supply should be capable of delivering the required current to the load connected at the SWO output of the load switch. The load current should be $\leq 10A$.

1.1.3 Logic Control

The ISL70062SEH has two logic control input pins; ON (pin 7) and DON (pin 9).

The Logic 1 V_{IH} level for the logic pins is from 1.2V to V_{CC} . The Logic 0 V_{IL} level is from 0.4V to 0V. The V_{CC} voltage can be 3.0V to 5.5V.

The ON logic input turns the load switch ON and OFF. When ON = LOW (Logic 0) the switch is OFF. When ON = HIGH (Logic 1), the switch is ON.

The DON logic input activates or deactivates the internal MOSFET output discharge circuitry of the load switch. When DON = LOW (Logic 0), the discharge MOSFET circuitry is deactivated (non-functional). When DON = HIGH (Logic 1), the discharge MOSFET circuitry is activated. During normal operation, when the discharge circuitry is activated, a 100 Ω internal resistor gets connected at the SWO side of the switch to ground when the NMOS load switch is turned OFF (ON logic pin = LOW (Logic 0)). The activation of this circuitry is for applications that need to quickly discharge the output of the load switch when the NMOS pass device is turned off. See the DON Logic Input section in the [ISL70062SEH](#) datasheet for a detailed description of the operation and functionality of the discharge MOSFET circuitry. **Note:** The DON pin has an internal 2M Ω pull-down resistor to ground and it can be left floating if this discharge function is not to be evaluated.

The ON and DON logic pins are controlled by connecting your logic drivers at the ON and DON banana jacks on the evaluation board. Test points ON1 and DON1 are available to monitor the voltage levels at the logic pins with a voltmeter or oscilloscope. The ON and DON logic inputs have an internal 2M Ω pull-down resistor to ground and they can be left floating.

1.1.4 Test Points

For ease in connecting probes to make measurements, the board has various test points available (see [Table 1](#)).

Table 1. Test Points

Designator	Description
GND1 - GND3	Ground test point
VCC1	VCC test point

Table 1. Test Points (Continued)

Designator	Description
JVIN	VIN (SWI) test point
JVOUT	VOUT (SWO) test point
VIN_SENSE	SWI sense test point (Measurement point close to the IC SWI pins)
VOUT_SENSE	SWO sense test point (Measurement point close to the IC SWO pins)
ON1	ON logic input test point
DON1	DON logic input test point

Table 2. Board Component Definitions

Designator	Description
U1	ISL70062SEHL/PROTO CLCC IC
GND, GNDA, GNDB	Ground connection
VCC	VCC power supply connection ($3V_{DC}$ to $5.5V_{DC}$)
VIN	VIN (V_{SWI}) supply connection ($0V_{DC}$ to $(VCC - 2V_{DC})$)
VOUT	VOUT (SWO) output load connection
ON	ON logic input
DON	DON logic input
C1 - C3	SWI input channel capacitors (C1 and C2 not populated on the evaluation board)
C4 - C5	SWI input decoupling capacitors
C6 - C7	SWO output decoupling capacitors
C8 - C10	SWO output channel capacitors (C9 and C10 not populated on the evaluation board)
R1	Output load resistor connection to ground (not populated on the evaluation board)

1.2 Quick Start Guide

1.2.1 Required Equipment

The following equipment is needed to operate the board:

- Two 5.5V DC power supplies capable of delivering 100mA
- One 3.5V DC power supply capable of delivering 10A
- One voltmeter (Keithley 2000 multimeter or equivalent)
- One ammeter (Keithley 2000 multimeter or equivalent)
- One 3.5Ω resistor (10W)

1.2.2 Configuring and Using the Board

1. Configure the board as shown in [Figure 2 on page 7](#). Start with all supplies (V1, V2, V3) in the disabled state.
2. Set the 5.5V DC supply (V1) connected at the VCC banana jack to 5.5V. This provides the bias for the IC. Enable the supply.
3. Set the 3V DC supply (V2) connected at the ON banana jack to 0V, which turns the load switch OFF. Enable this supply.
4. Set the 3.5V DC supply (V3) connected at the VIN banana jack (SWI input) to 3.5V. Enable the supply.
5. Check that the load switch is in the OFF state and the current through the ammeter is at $\sim 0A$.
6. Increase the 3V DC supply (V2) at the ON banana jack to 3V. This turns the load switch ON. The ammeter should now read $\sim 1A$.

7. Read VDIFF voltmeter connected between VIN_SENSE and VOUT_SENSE, which gives the voltage directly across the load switch IC. Calculate the r_{ON} of the load switch by dividing the VDIFF voltage by the current through the ammeter. The r_{ON} calculated should be approximately 25m Ω .
8. To vary the output load resistance, replace the load resistor with a DC Electronic Load, such as a Chroma 63102A. By varying the output load resistance to draw current from 0A up to 10A through the load switch, you can measure the r_{ON} of the load switch at various loads and V_{IN} voltage conditions.

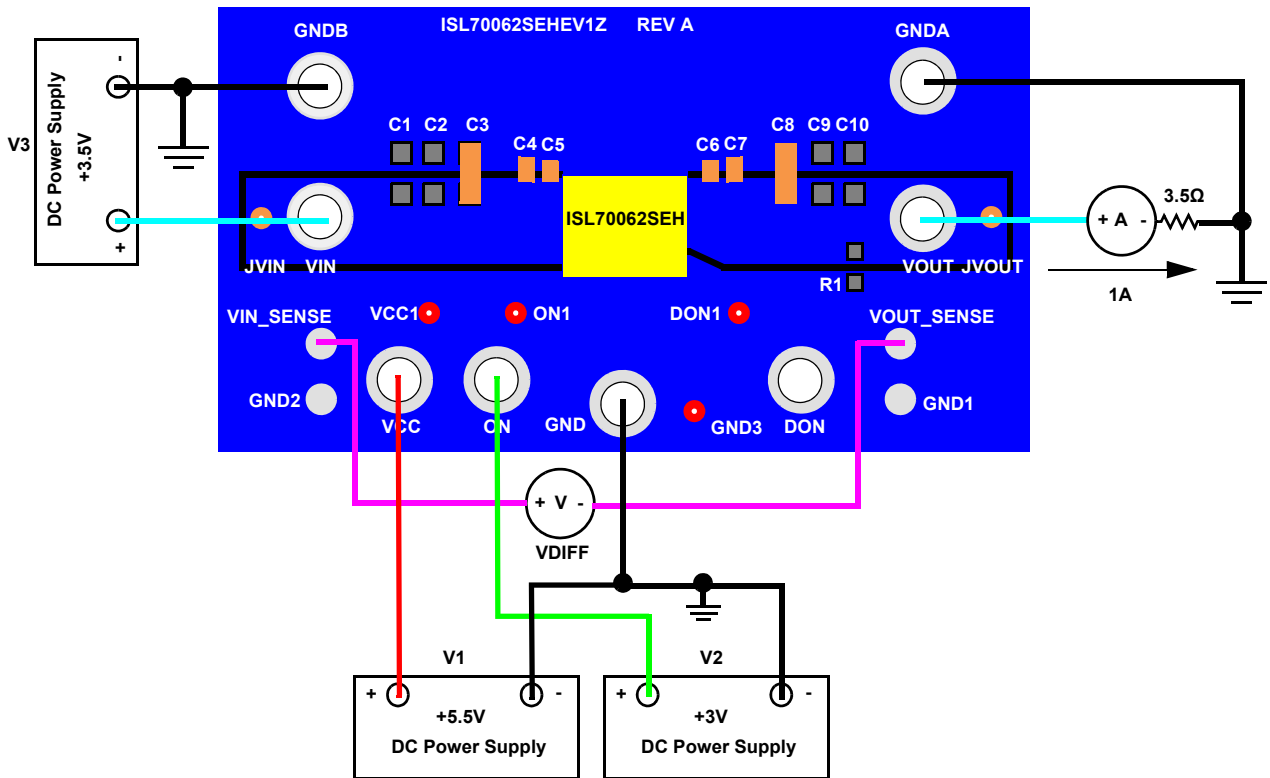


Figure 2. Basic Evaluation Test Setup for Functional Operation Testing

2. PCB Layout Information

This section contains the evaluation board picture, schematic, bill of materials, and board layout.

2.1 ISL70062SEHEV1Z Evaluation Board

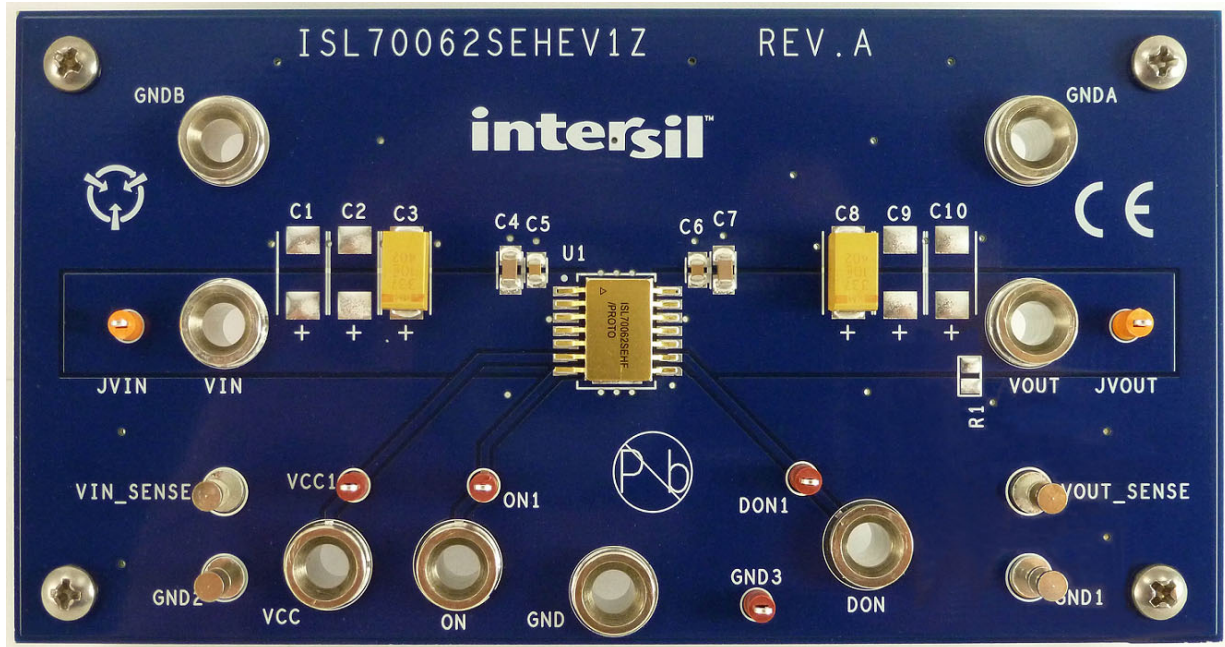


Figure 3. ISL70062EHEV1Z Evaluation Board (Top View)

2.2 ISL70062SEH Circuit Schematic

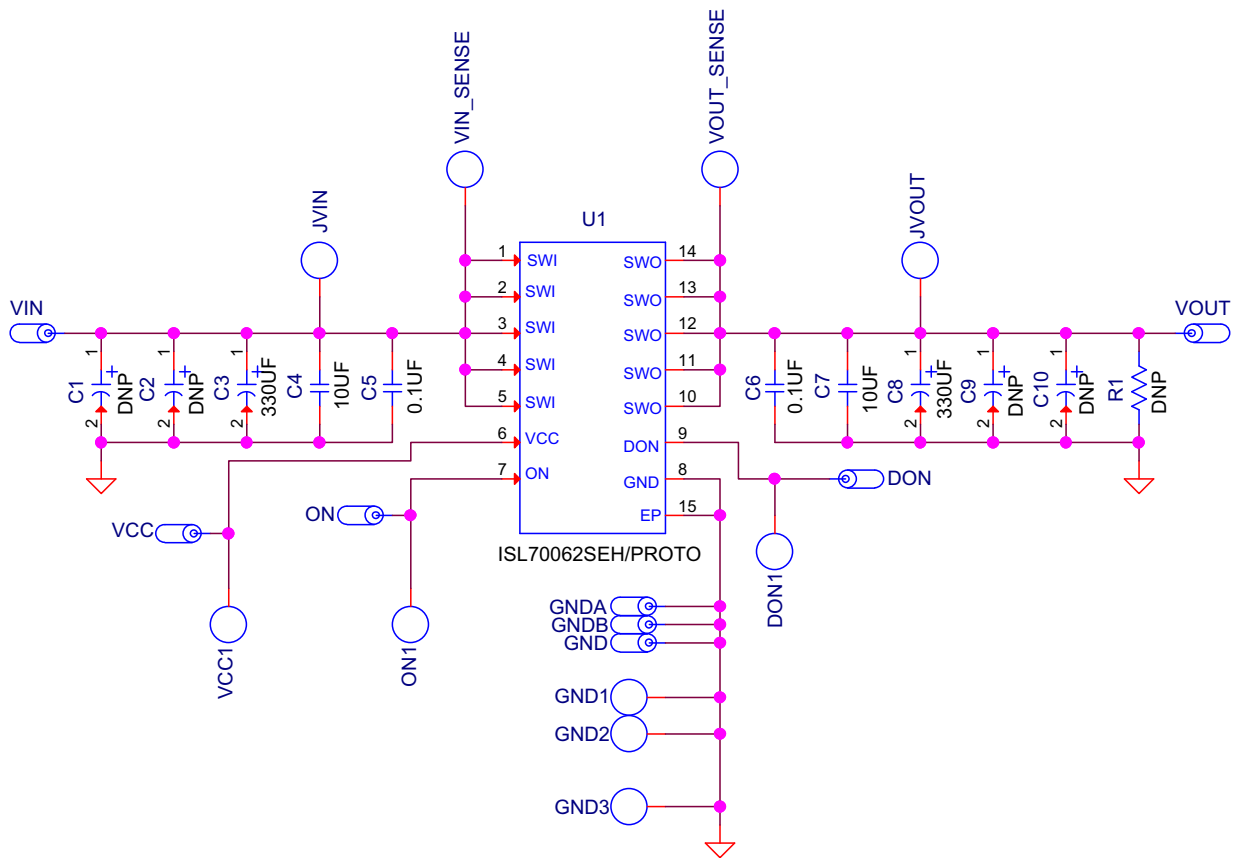


Figure 4. ISL70062SEHEV1Z Evaluation Board Schematic

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
4	GND1, GND2, VIN_SENSE, VOUT_SENSE	Test Point Turret, 0.150 Pad, 0.100 Thole, CONN-TURRET, Terminal Post, TH, ROHS	Keystone	1514-2
3	ON1, DON1, GND3	Test Point, Miniature, Red, 0.100 Pad, 0.040 Thole	Keystone	5000
2	JVIN, JVOUT	Test Point, Miniature, Orange, 0.100 Pad, 0.040 Thole	Keystone	5003
8	VCC, ON, DON, GND, VIN, GNDA, GNDB, VOUT	Banana Plug, Solder Mount, L = 0.218in	Keystone	575-8
2	C5, C6	Multilayer CAP, 0.1µF	Generic	H1046-00104-50V5
2	C4, C7	Multilayer CAP, 10µF	Generic	H1065-00106-25V10
2	C3, C8	CAP, SMD, 330µF, Tantalum, Ultra-Low ESR, High Capacitance	Kemet	T530X337M010ATE005
1	R1	Resistor, Metal Film Chip, (Not Populate)	Generic	H2506-DNP-DNP-1
4	C1, C2, C9, C10	CAP, Tantalum, Ultra-Low ESR 30mΩ (Not Populate)	AVX	TPME157K016R0030-DNP
1	U1	Radiation Hardened 10A NMOS Load Switch	Renesas	ISL70062SEHF/PROTO

2.4 Board Layout

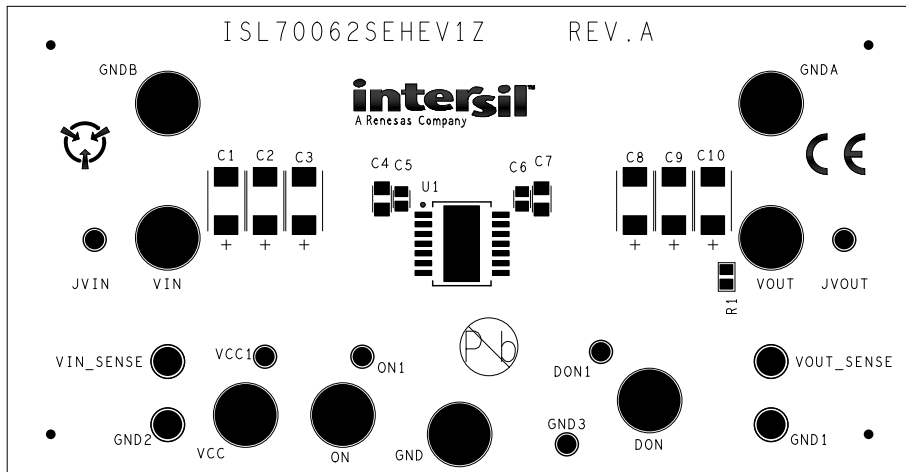


Figure 5. Top Layer Silk Screen

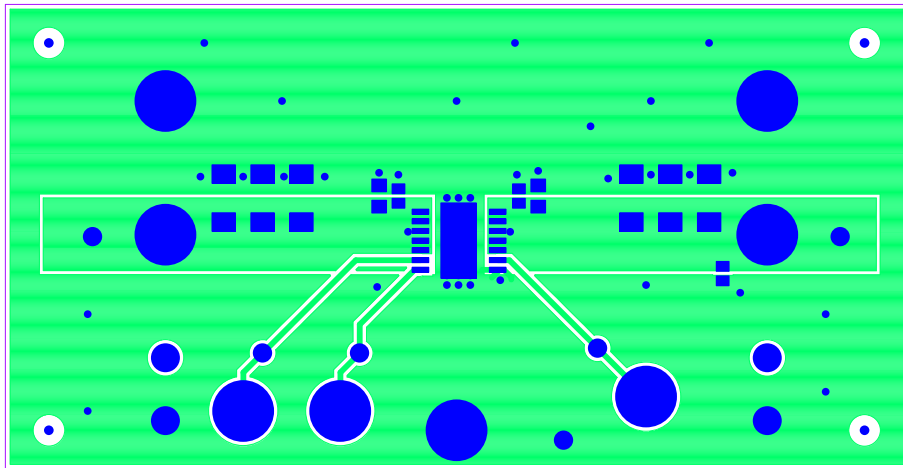


Figure 6. Top Layer

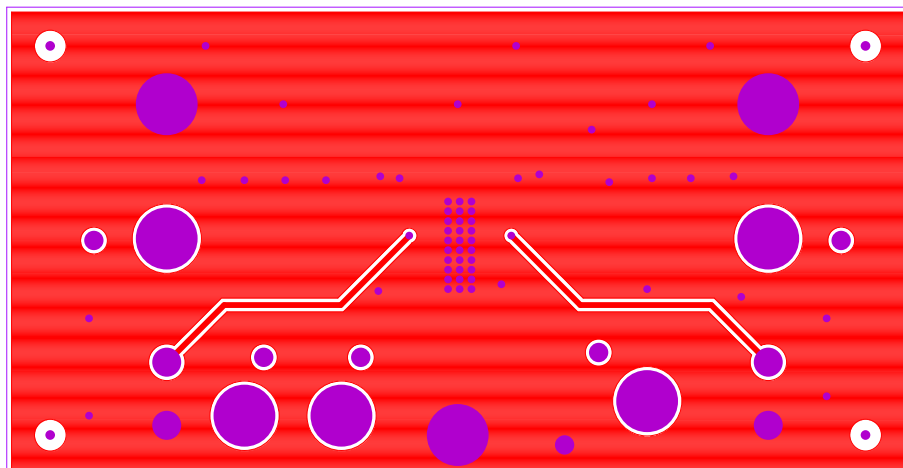


Figure 7. Bottom Layer

3. Typical Performance Curves

Unless otherwise noted, $V_{SWI} = 5.5V$; $I_{SWO} = 1A$; $C_{SWI} = 10\mu F$, $C_L = 1\mu F$, $T_A = +25^\circ C$

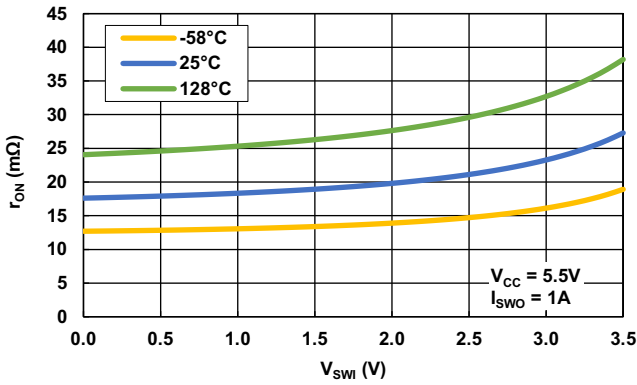


Figure 8. r_{ON} vs V_{SWI} vs Temperature

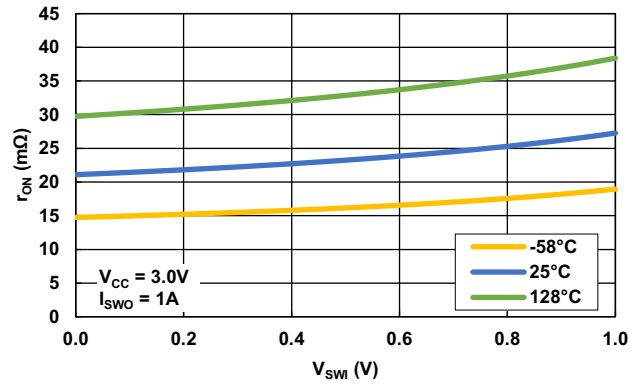


Figure 9. r_{ON} vs V_{SWI} vs Temperature

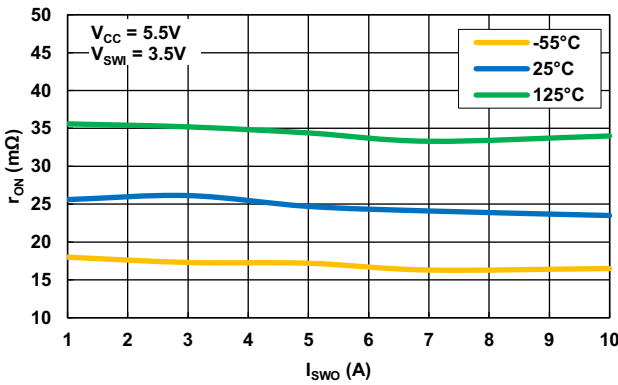


Figure 10. r_{ON} vs I_{SWO} vs Temperature

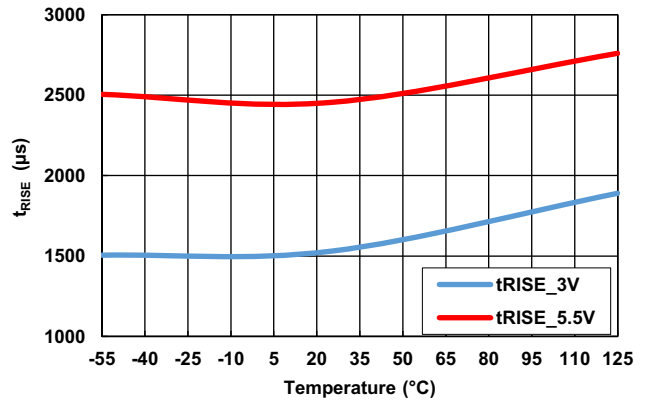


Figure 11. t_{RISE} vs Temperature vs V_{CC}

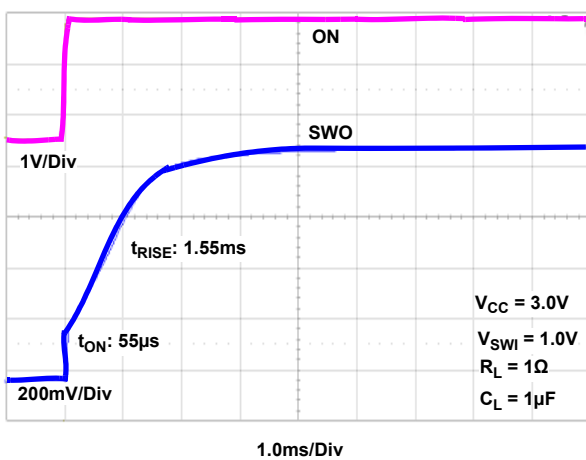


Figure 12. Turn-On Waveform

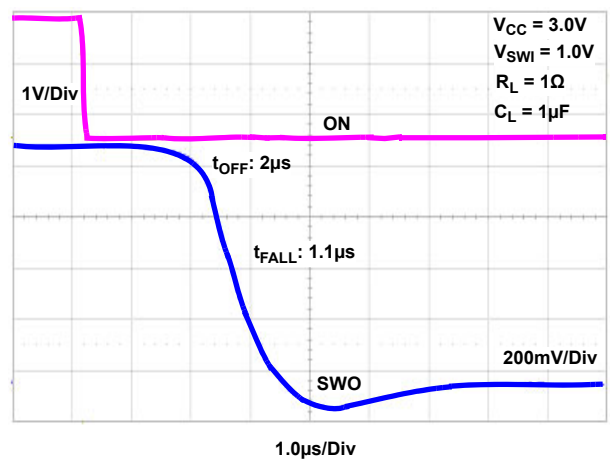


Figure 13. Turn-Off Waveform

Unless otherwise noted, $V_{SWI} = 5.5V$; $I_{SWO} = 1A$; $C_{SWI} = 10\mu F$, $C_L = 1\mu F$, $T_A = +25^\circ C$ (Continued)

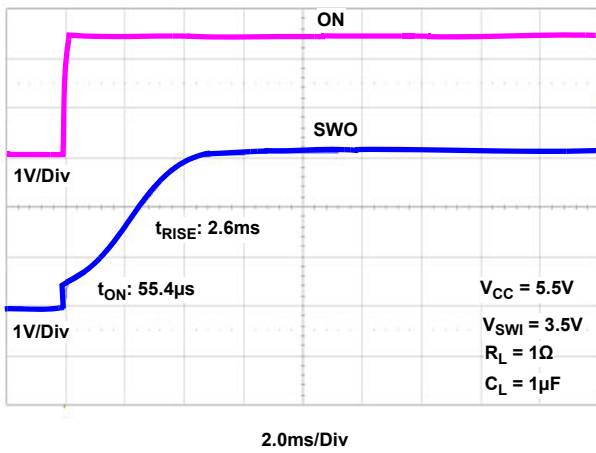


Figure 14. Turn-On Waveform

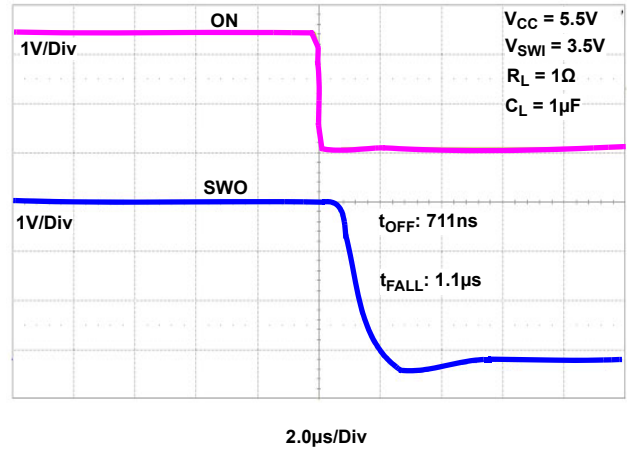


Figure 15. Turn-Off Waveform

4. Revision History

Rev.	Date	Description
1.00	Oct.28.19	Initial release

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