

ISL71010BM25EV1Z

User's Manual: Evaluation Board

High Reliability

1. Overview

The ISL71010BM25EV1Z evaluation board measures the performance of the high precision 2.5V [ISL71010B25](#) voltage reference. The reference has a wide input voltage range from 4V to 30V and an initial accuracy of $\pm 0.05\%$. The voltage noise of $1.9\mu\text{V}_{\text{p-p}}$ in the 0.1Hz to 10Hz range and maximum output voltage temperature coefficient of 10ppm/ $^{\circ}\text{C}$ makes the ISL71010B25 ideal for high end applications.

The evaluation board includes voltage input test points (VIN and GND) for a power supply input, as well as a pair of test points for the output (VOUT and GND). The resistor location designated as R2 and the capacitor location designated as C3 allow VOUT output load testing. The R2 resistor location accepts surface mount or through-hole style resistors and C3 comes populated with a 0.1 μF load capacitor. Additionally, an R-C damper network can be connected to VOUT by installing a jumper at J1.

1.1 Key Features

- Voltage input test points for power supply connection
- Convenient output test points to measure the voltage reference VOUT
- R2 and C3 allow for VOUT output load testing
- An additional R-C damper network can be connected at VOUT by installing a jumper at J1

1.2 Specifications

This evaluation board is configured and optimized for the following conditions:

- VIN = 4V to 30V
- 10 μF and 0.1 μF input decoupling capacitors, 1nF compensation capacitor, and 0.1 μF load capacitor
- R2 load resistance of $\geq 125\Omega$
- Selectable 10 μF and 2.21k Ω damper network at the output by installing a jumper at J1
- Board temperature: +25 $^{\circ}\text{C}$

1.3 Ordering Information

| Part Number | Output Voltage (V) | Description |
|------------------|--------------------|------------------|
| ISL71010BM25EV1Z | 2.5V | Evaluation board |

1.4 Related Literature

For a full list of related documents, visit our website:

- [ISL71010B25](#) product page

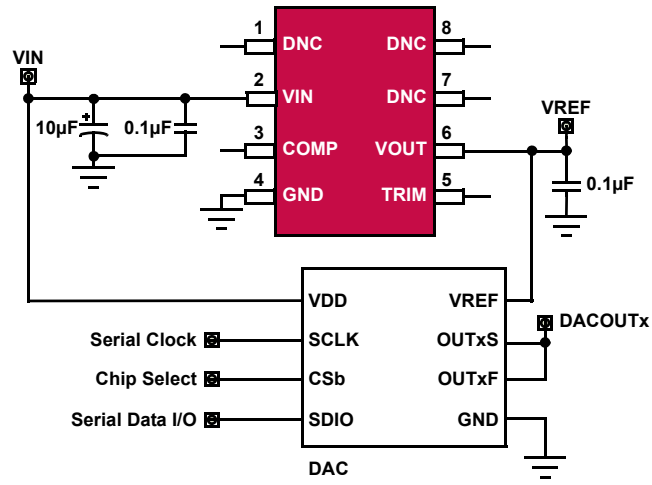


Figure 1. ISL71010BM25EV1Z Block Diagram

2. Functional Description

The ISL71010BM25EV1Z evaluation board provides a simple platform to demonstrate the features and evaluate the performance of the ISL71010B25 voltage reference. It provides easy access to the ISL71010B25 IC pins. The schematic, bill of materials, and top silkscreen for the board are available on [pages 6](#) through [8](#).

[Figures 8](#) through [18](#) show performance data taken using the ISL71010BM25EV1Z evaluation board and basic lab equipment.

The following sections explain how to use the evaluation board.

2.1 Basic Layout of the Evaluation Board

[Figure 3 on page 6](#) shows the basic layout of the evaluation board.

[Figure 4](#) shows the evaluation board schematic. The ISL71010BM25EV1Z contains the ISL71010BMB25Z voltage reference (U1), input decoupling capacitors (C1, C2), a compensation capacitor (C5), and a load capacitor (C3). Different resistor values can be applied at (R2) for testing of the voltage reference at different loads. The R2 resistor location accepts surface mount or through-hole style resistors.

The power supply leads attach to TP1 and TP2 (VIN, GND). The ISL71010B25 IC requires a DC supply in the range of 4.0V to 30V for proper operation. The power supply should be capable of delivering 100mA of current.

The output is measured at test points TP3 and TP4 (VOUT, GND), and is best measured with a high precision voltmeter, such as the Keysight 3458A digital multimeter, 8 1/2 digits.

The R-C damper network (R1, C4) is populated and can be connected to the reference output by adding a shunt to the R-C jumper (J1). The damper network improves stability by reducing transient load ringing with high value (>0.47 μ F) load capacitance.

Table 1. Board Components List

| Designator | Value | Description |
|------------|----------------|------------------------|
| C1 | 10 μ F | Bypass Capacitor |
| C2 | 0.01 μ F | Bypass Capacitor |
| C3 | 0.1 μ F | Load Capacitor |
| C4 | 10 μ F | Damper Capacitor |
| C5 | 1nF | Compensation Capacitor |
| R1 | 2.21k Ω | Damper Resistor |
| R2 | DNP | Optional Load Resistor |
| U1 | ISL71010BMB25Z | SOIC 8-Pin Package |
| J1 | DNP | Damper Jumper |

2.2 Operating Range

The ISL71010B25 IC requires a V_{IN} DC supply in the range of 4.0V to 30V for proper operation. The power supply should be capable of delivering 100mA of current.

The ISL71010B25 IC V_{OUT} can source 20mA of current and sink -10mA of current. For normal operation, the R2 load resistor should be selected to be $\geq 125\Omega$.

Note: With V_{OUT} shorted to ground, the IC will limit the current to ≤ 75 mA.

2.3 Quick Start Guide

- (1) Gather the external supply and equipment needed to operate the board:
 - (a) 4V to 30V DC power supply
 - (b) Precision Voltmeter (Agilent 3458A digital multimeter or equivalent)
- (2) Attach the evaluation board to a DC power supply at test points TP1 and TP2 labeled VIN and GND as shown in [Figure 2](#). Place the positive terminal at VIN (TP1) and the negative terminal at GND. The supply should be capable of delivering 4V to 30V of power and 100mA of current.
- (3) Connect a precision voltmeter at test points TP3 and TP4 labeled VOUT and GND as shown in [Figure 2](#).
- (4) Set the supply voltage to 5V.
- (5) Turn the DC power supply ON. The voltmeter should read $2.5V \pm 0.05\%$.
- (6) Change the DC power supply voltage to 10V. The voltmeter should continue to read 2.5V.
- (7) Vary the DC power supply voltage over the range of 4V to 30V. The voltmeter should continue to read 2.5V.
- (8) Performance at different resistive loads can be evaluated by changing R2 with different resistor values.

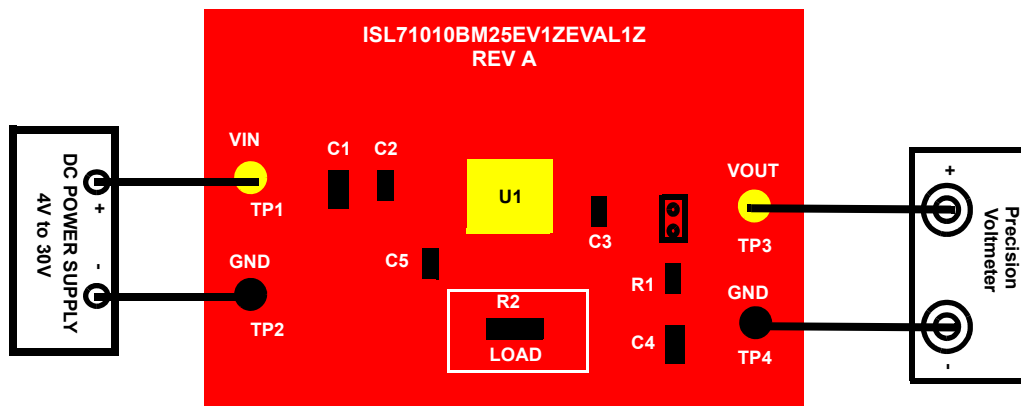


Figure 2. Basic Evaluation Test Setup Block Diagram (Measuring Voltage Reference VOUT)

3. PCB Layout Guidelines

3.1 ISL71010BM25EV1Z Evaluation Board

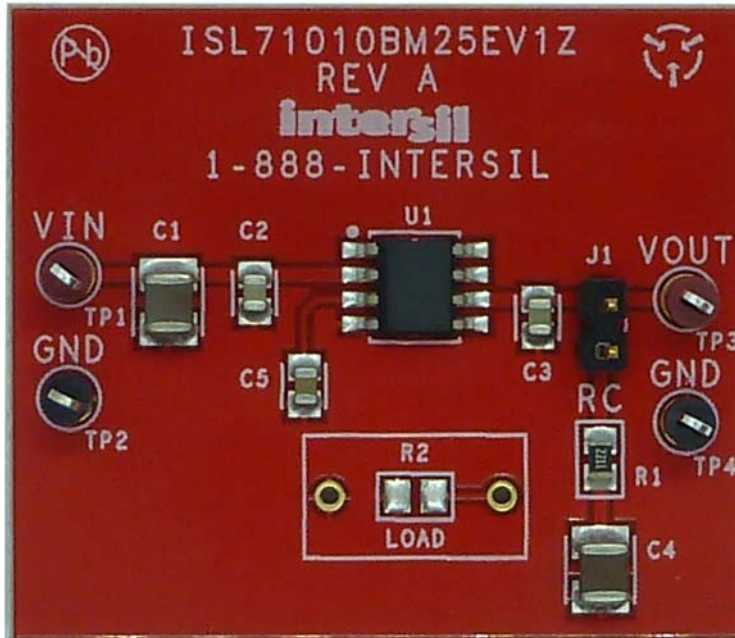


Figure 3. ISL71010BM25EV1Z Evaluation Board

3.2 ISL71010BM25EV1Z Evaluation Board Schematic

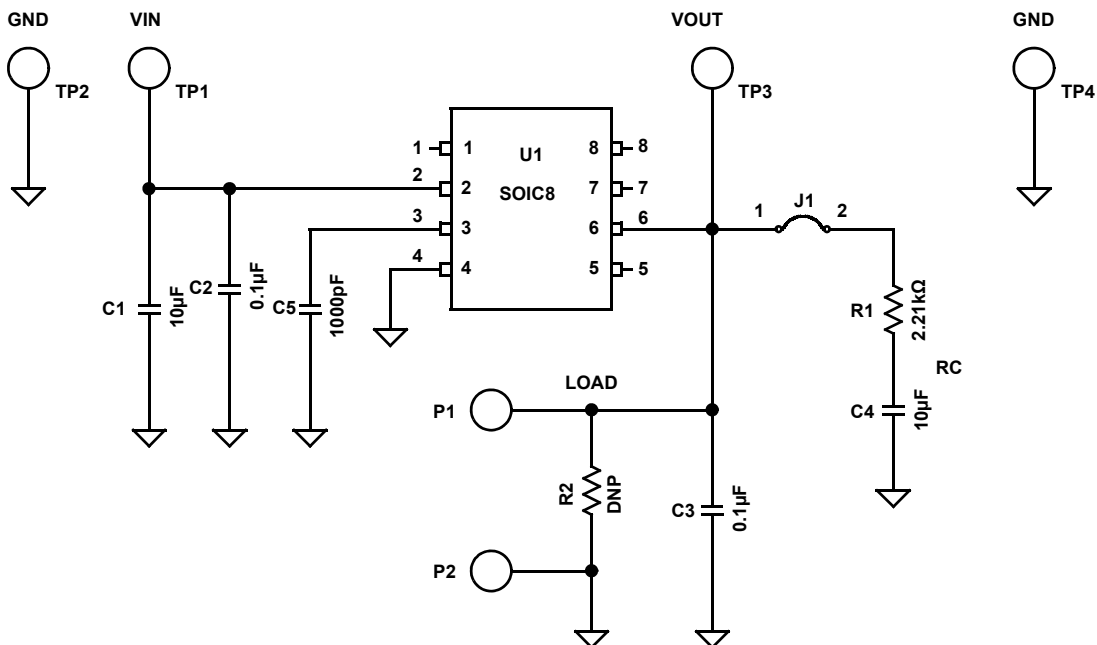


Figure 4. ISL71010BM25EV1Z Evaluation Board Schematic

3.3 Bill of Materials

| Qty | Reference Designator | Description | Mfr | Manufacturer Part Number |
|-----|----------------------|--|------------------|--------------------------|
| 1 | - | PWB-PCB, ISL71010BM25EV1Z, Rev A, ROHS | IMAGINEERING INC | ISL71010BM25EV1ZREVAPCB |
| 1 | C5 | CAP, SMD, 0805, 1000pF, 50V, 10%, X7R, ROHS | PANASONIC | ECJ-2VB1H102K |
| 2 | C2,C3 | CAP, SMD, 0805, 0.1µF, 50V, 10%, X7R, ROHS | KEMET | C0805C104K5RACTU |
| 2 | C1,C4 | CAP, SMD, 1210, 10µF, 50V, 10%, X5R, ROHS | TAIYO YUDEN | UMK325BJ106KM-T |
| 2 | TP1, TP3 | CONN - MINI TEST PT, VERTICAL, RED, ROHS | KEYSTONE | 5000 |
| 2 | TP2, TP4 | CONN - MINI TEST PT, VERTICAL, BLK, ROHS | KEYSTONE | 5001 |
| 1 | J1 | CONN-HEADER, 1X2, RETENTIVE, 2.54mm, 0.230X0.120, ROHS | BERG/FCI | 69190-202HFL |
| 1 | U1 | IC - PREC. VOLTAGE REFERENCE, 8P, SOIC, 2.5VOUT, ROHS | INTERSIL | ISL71010BMB25Z-TK |
| 1 | R2 | RESISTOR, SMD, 0805, DNP | - | - |
| 1 | R1 | RESISTOR, SMD, 0805, 2.21KΩ, 1/8W, 1%, TF, ROHS | YAGEO | RC0805FR-072K21L |
| 1 | Place assy in bag | BAG, STATIC, 2X3, ZIP LOC | - | 2X3-STATIC-BAG |
| 1 | - | LABEL-DATE CODE_LINE 1: YRWK/REV#, LINE 2: BOM NAME | INTERSIL | LABEL-DATE CODE |

3.4 Board Layout

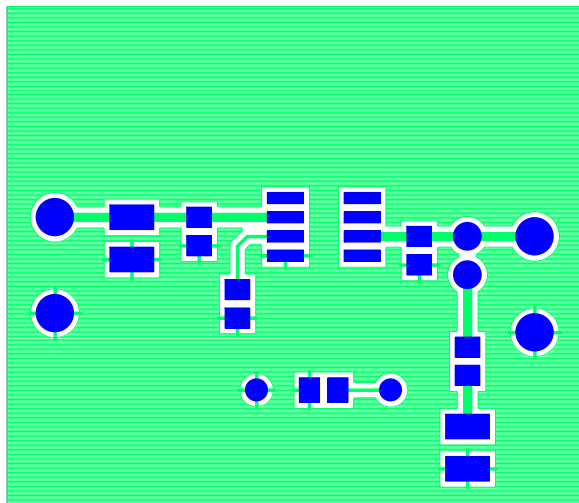


Figure 5. Top Layer

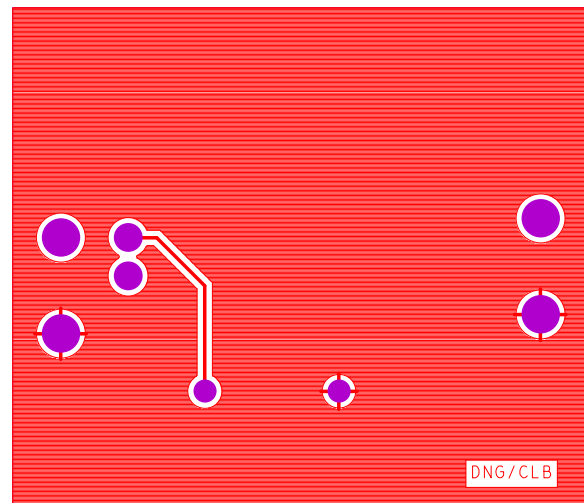


Figure 6. Bottom Layer

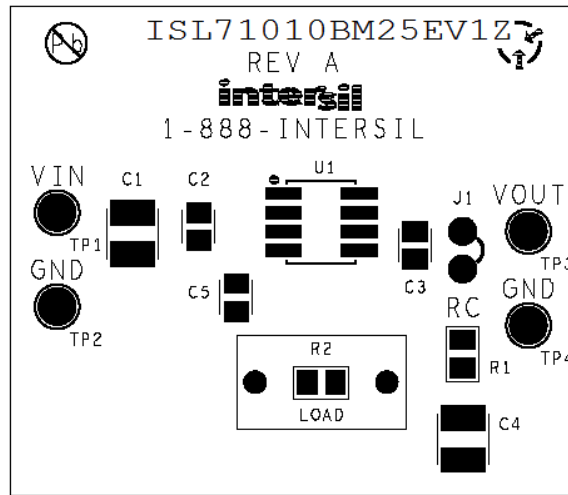


Figure 7. Top Layer Silk Screen

4. Typical Performance Curves

Recommended operation conditions, unless noted: $V_{IN} = 5V$, $I_{OUT} = 0mA$, $C_{OUT} = 0.1\mu F$, $COMP = 1nF$, $T_A = +25^\circ C$

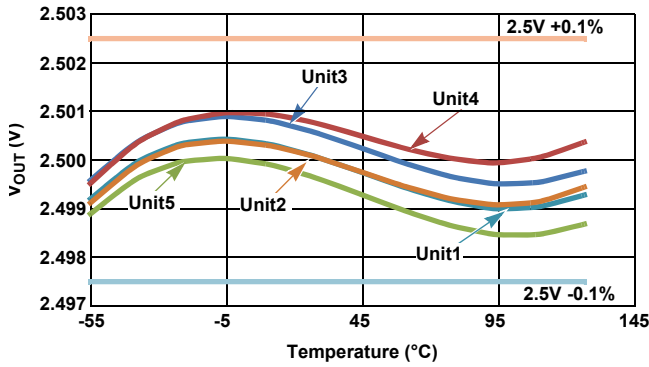


Figure 8. V_{OUT} vs Temperature, Five Units

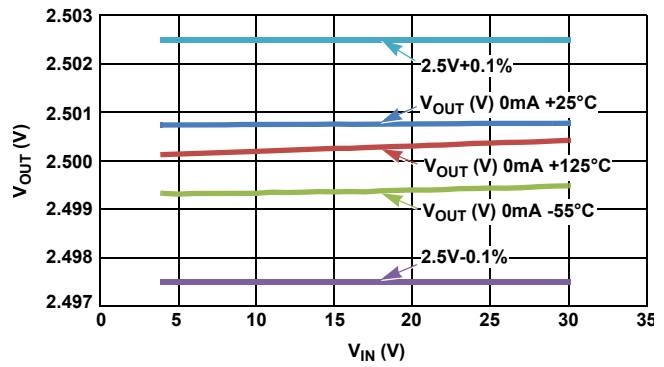


Figure 9. V_{OUT} Accuracy Over Temperature

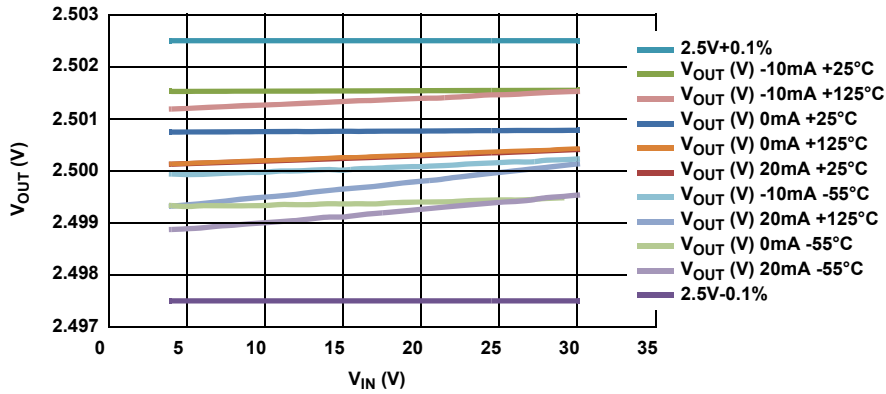


Figure 10. V_{OUT} vs V_{IN} at 0mA, 20mA, and -10mA

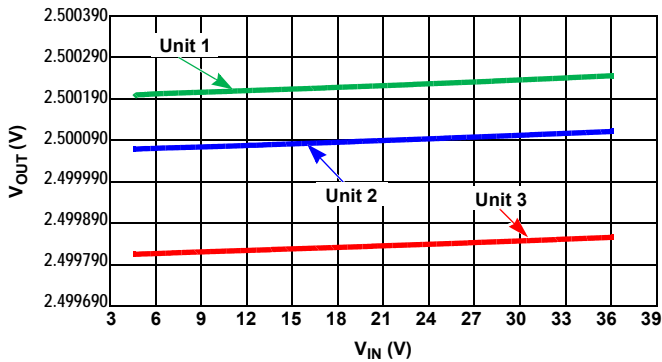


Figure 11. Line Regulation, Three Units

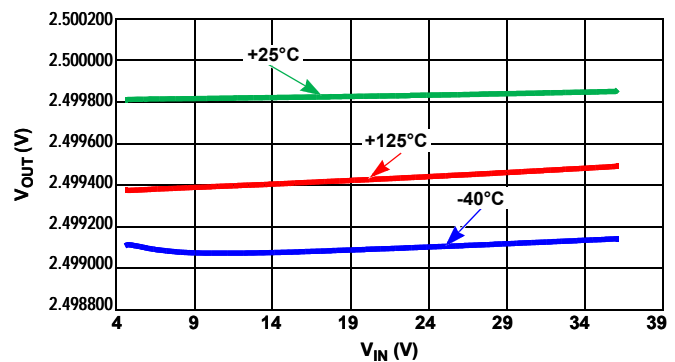


Figure 12. Line Regulation, Three Temperatures

Recommended operation conditions, unless noted: $V_{IN} = 5V$, $I_{OUT} = 0mA$, $C_{OUT} = 0.1\mu F$, $COMP = 1nF$, $T_A = +25^\circ C$ (Continued)

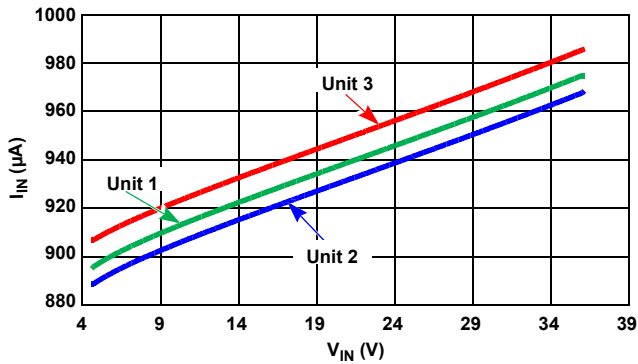


Figure 13. I_{IN} vs V_{IN} , Three Units

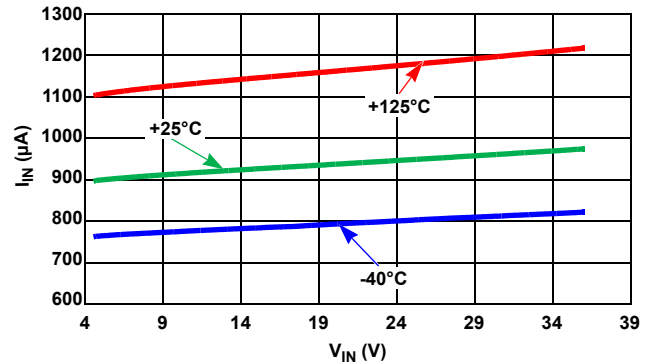


Figure 14. I_{IN} vs V_{IN} , Three Temperatures

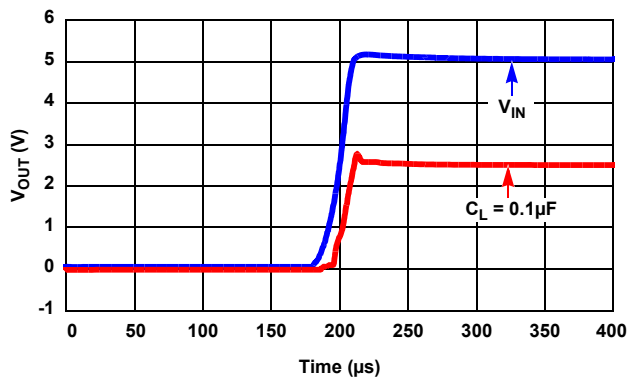


Figure 15. Turn-On Time with $0.1\mu F$

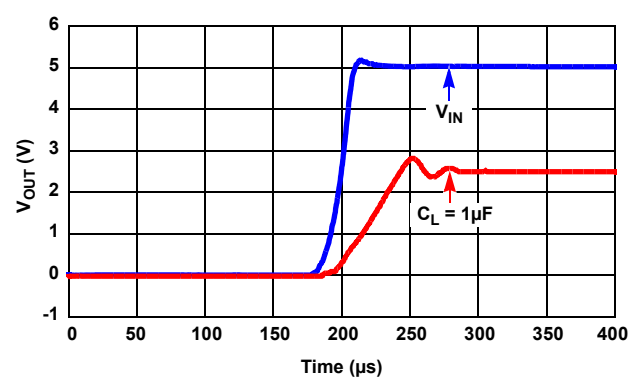


Figure 16. Turn-On Time with $1\mu F$

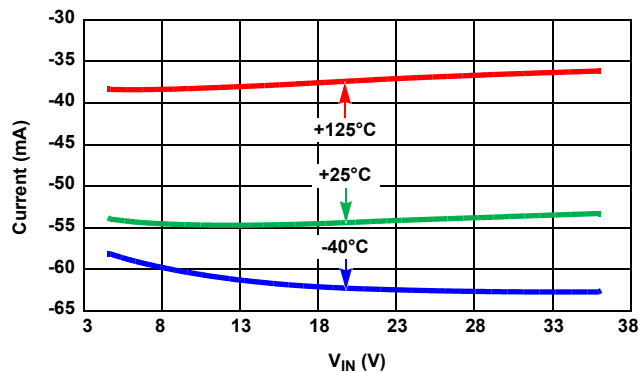


Figure 17. Short-Circuit to GND

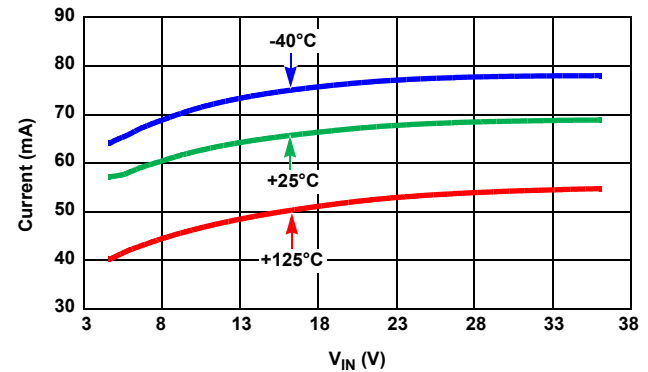


Figure 18. Short-Circuit to V_{IN}

5. Revision History

| Rev. | Date | Description |
|------|-------------|-----------------|
| 0.00 | Nov 2, 2017 | Initial release |

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(Rev.1.0 Mar 2020)

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