

ISL71830SEHEV1Z

Evaluation Board

UG039  
Rev.0.00  
August 17, 2015

**Description**

The [ISL71830SEH](#) is a radiation tolerant, 16-channel high ESD protected multiplexer that is fabricated using Intersil's proprietary P6SOI (Silicon On Insulator) process technology to provide excellent reliability. It operates with a single supply voltage ranging from 3.0V to 5.5V. This evaluation board is designed to provide easy access to the capabilities of the part.

The evaluation board has a DIP switch, which provides a convenient way to address all 16 channels without the need for extra supplies. There's also a BNC input available that will allow you to drive the address pins with a signal generator.

**Specifications**

This board has been configured and optimized for the following operating conditions:

- $V_+ = 3.0V$  to  $5.5V$
- $V_{REF} = 3.0V$  to  $5.5V$

**Key Features**

- Jumper selectable input source for each input
- DIP switch to conveniently select 1 of 16 channels
- BNC input for dynamic addressing
- Multiple loading options with jumpers on VOUT
- Convenient power connection
- On-board enable switch

**References**

[ISL71830SEH](#) Datasheet

**Ordering Information**

PART NUMBER	DESCRIPTION
ISL71830SEHEV1Z	Evaluation board for the ISL71830SEH

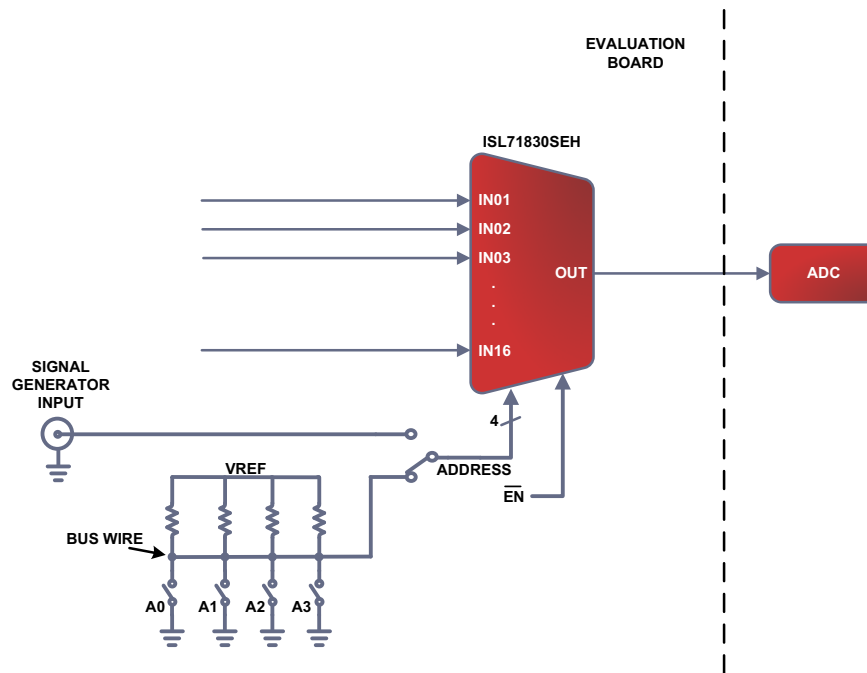


FIGURE 1. ISL71830SEHEV1Z BLOCK DIAGRAM

## ISL71830SEHEV1Z Evaluation Board

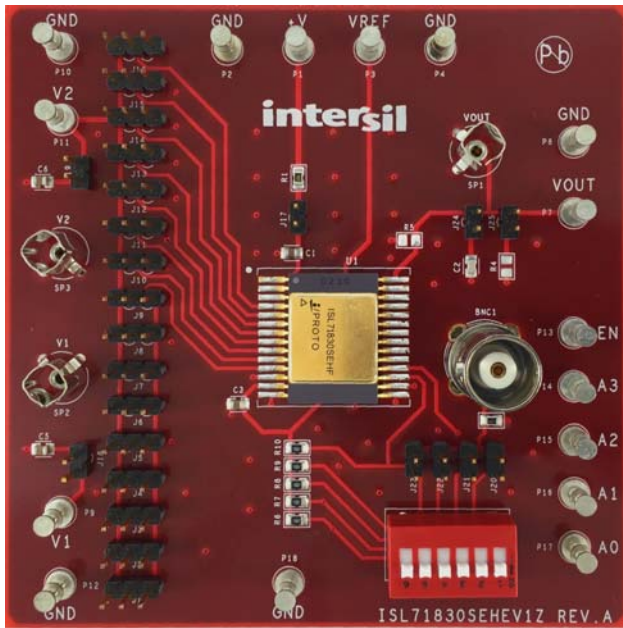


FIGURE 2. TOP SIDE



FIGURE 3. BOTTOM SIDE

### Power Supplies

This board has power supply inputs for  $V_+$  and  $V_{REF}$ . There are no requirements for sequencing on these supplies, but it is recommended that the supplies come up relatively at the same time. In-line resistors are provided to  $V_+$  with decoupling capacitors close to the part for  $V_+$  and  $V_{REF}$ . The in-line resistors are 100 $\Omega$  but can be changed by the user for additional power supply filtering or to limit the rise time of the supply voltages.

The voltage ranges for  $V_+$  and  $V_{REF}$  are +3V to +5.5V. The ISL71830SEH is a rail-to-rail mux and should be able to accommodate any input signal with a voltage level between or equal to the supplies voltages.  $V_{REF}$  is used to set the decoder logic levels.

### PCB Layout Guidelines

The ISL71830SEHEV1Z PCB layout has been optimized for ease of testing. When incorporating the ISL71830SEH into a system there are a few guidelines that can ensure optimal electrical and noise performance.

- Analog circuits can conduct noise through paths that connect it to the “outside world”. These paths include the  $V_+$ ,  $V_{REF}$ , the input to any switch and the output. It is important to make sure these paths are kept away from known noise sources.
- It is recommended to decouple the power supply pins ( $V_+$  and  $V_{REF}$ ) for power supply filtering. If the traces to the supply lines are long, it is recommended to use a larger 1 $\mu$ F capacitor at the point of entry for the supply and a smaller capacitor, like a 0.1 $\mu$ F, close to the part to reduce high frequency perturbations.

# ISL71830SEHEV1Z Circuit Schematic

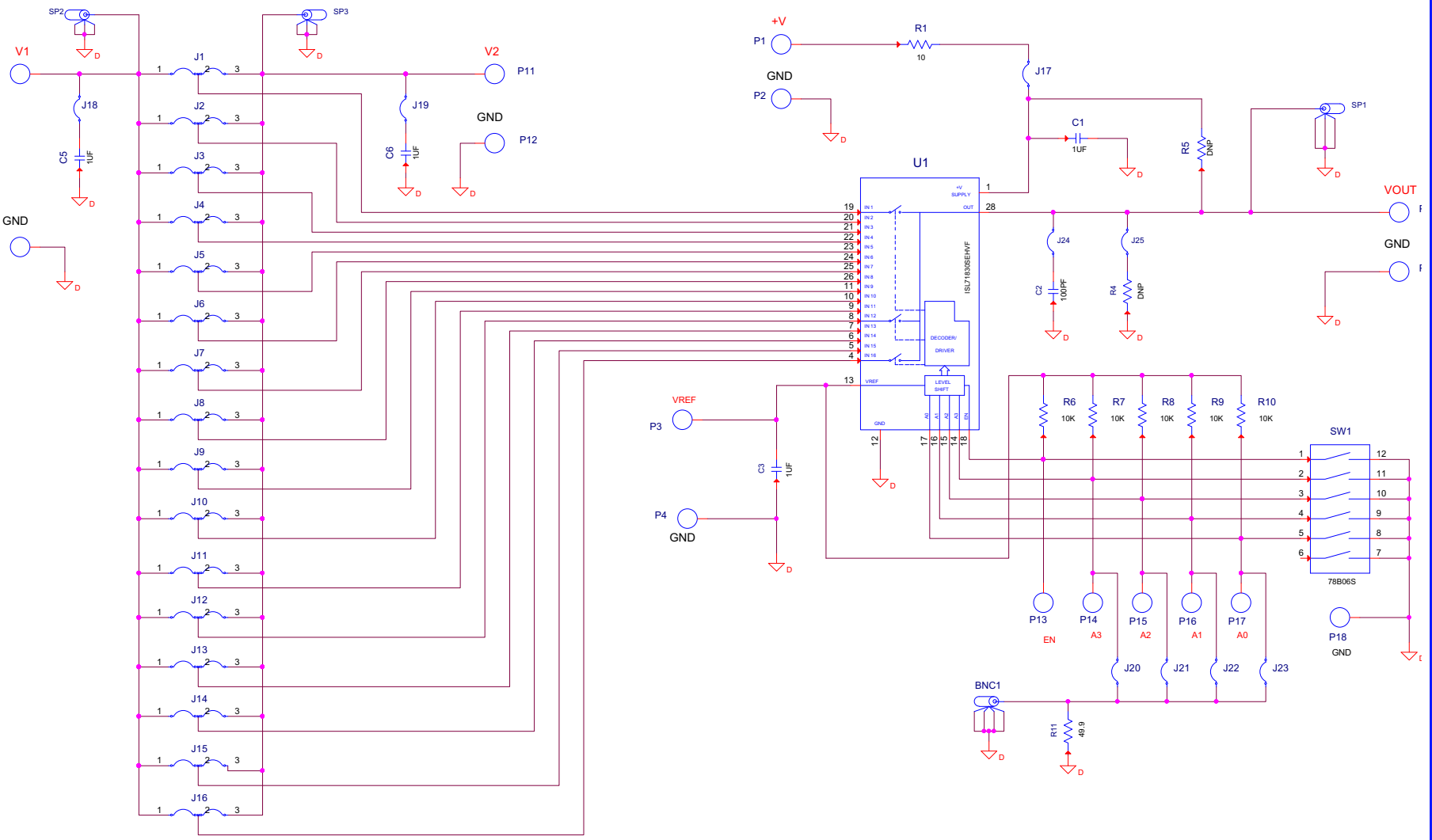


FIGURE 4. ISL71830SEHEV1Z SCHEMATIC

## Bill of Materials

ITEM	QTY	REFERENCE DESIGNATOR	VALUE	TOL (%)	RATING	TYPE	PCB FOOTPRINT	MANUFACTURER	MANUFACTURER PART NUMBER
1	1	C4	100pF	5	50V	X7R	0805	PANASONIC	ECU-V1H101JCG
2	5	C1, C2, C3, C5, C6	1 $\mu$ F	10	25V	X7R	0805	AVX	08053C105KAT2A
3	2	R4, R5	DNP	1	DNP		0805	GENERIC	
4	2	R1, R2	10 $\Omega$	1	1/10W		0805	VENKEL	CR0805-8W-10R0FT
5	5	R6, R7, R8, R9, R10	10K $\Omega$	1	1/10W		0805	VENKEL	CR0805-8W-1002FT(Pb-free)
6	1	R11	49.9 $\Omega$	1	1/10W		0805	ROHM	MCR10EZH49R9
7	3	SP1-SP3					CONN	TEKTRONIX	131-4353-00
8	18	P1-P4, P7-P18					THOLE	KEYSTONE	1514-2
9	1	BNC1					CONN	AMPHENOL	31-5329-51RFX
10	1	SW1					DIP	GRAYHILL	78B06S
11	1	U1					28CDFP	INTERSIL	ISL71830SEH/PROTO
12	16	J1-J16					THOLE	BERG/FCI	68000-236HLF
13	10	J17-J26						BERG/FCI	69190-202HLF
14	4	Bottom four corners						3M	SJ-5003SPBL

# Board Layout - 4 Layers

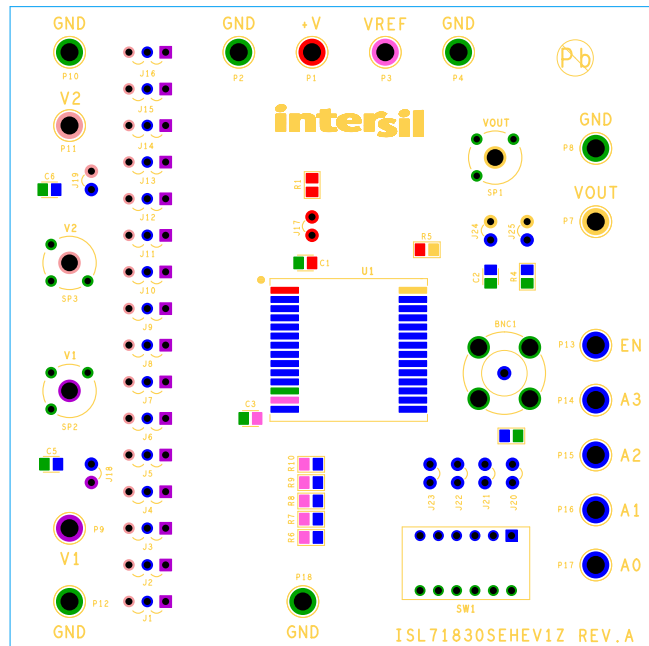


FIGURE 5. SILKSCREEN TOP

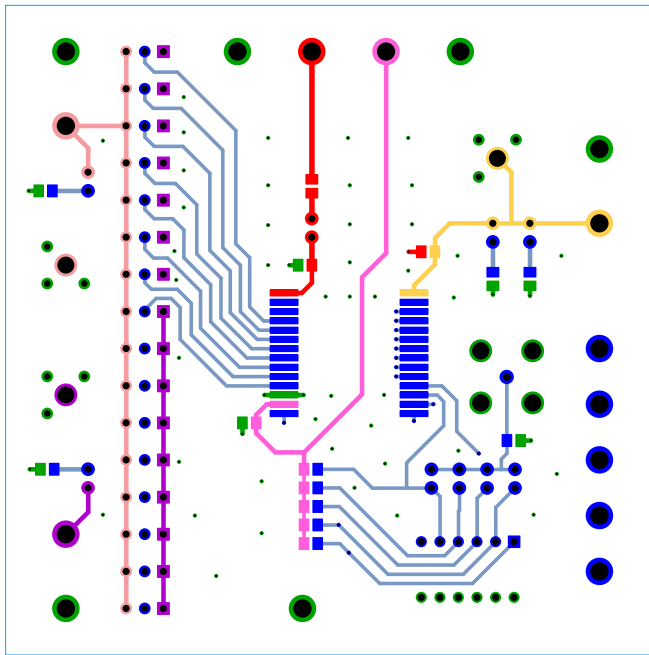


FIGURE 6. TOP LAYER

## Board Layout - 4 Layers (Continued)

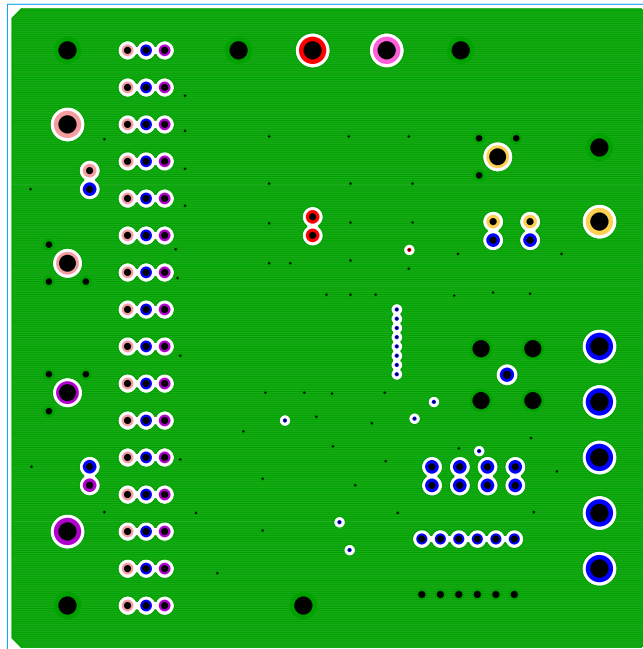


FIGURE 7. PCB - INNER LAYER 1 (TOP VIEW)

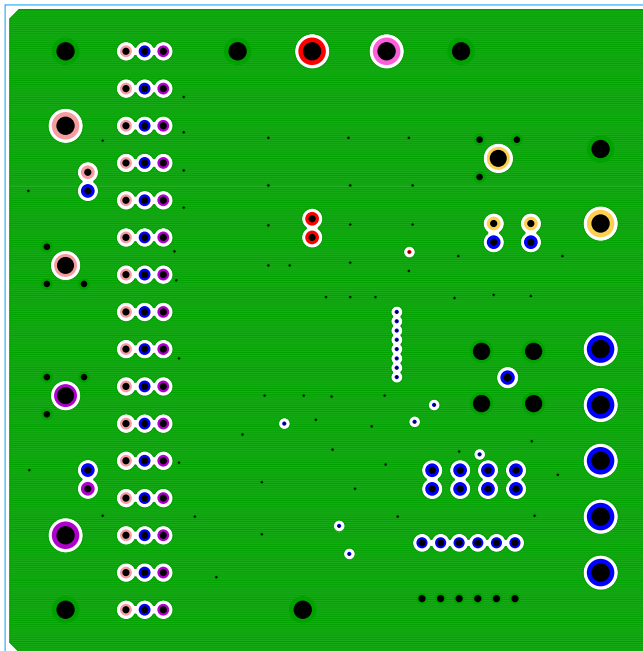


FIGURE 8. PCB - INNER LAYER 2 (TOP VIEW)

## Board Layout - 4 Layers (Continued)

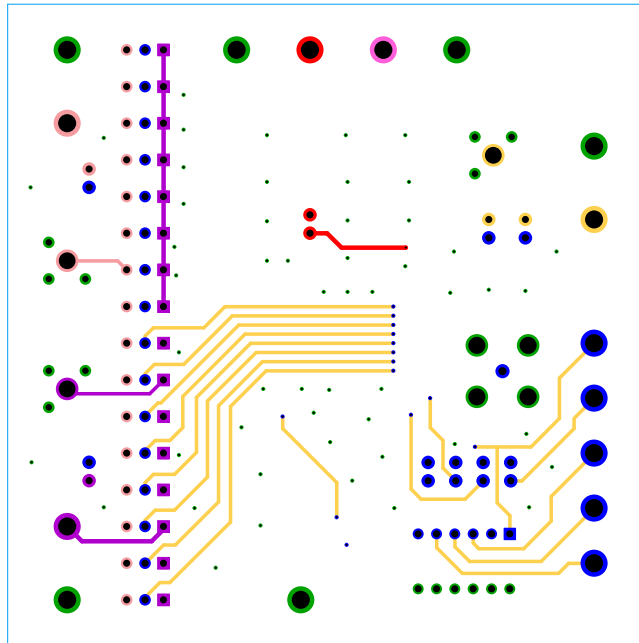


FIGURE 9. PCB - BOTTOM LAYER (TOP VIEW)

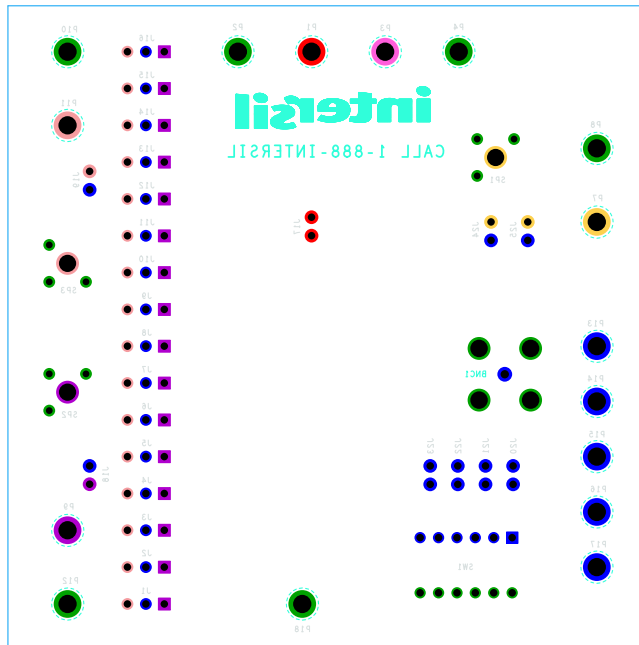


FIGURE 10. SILKSCREEN BOTTOM

# Typical Performance Curves

Unless otherwise noted:  $V_+ = +15V$ ,  $V_- = -15V$ ,  $V_{REF} = 5.0V$ ,  $T_A = +25^\circ C$

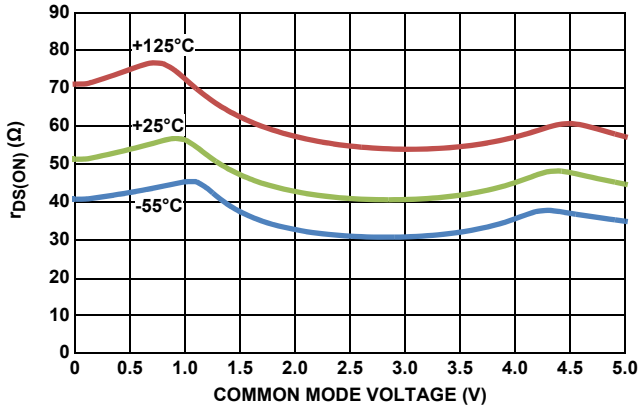


FIGURE 11.  $r_{DS(ON)}$  vs COMMON MODE VOLTAGE ( $V_S = 5V$ )

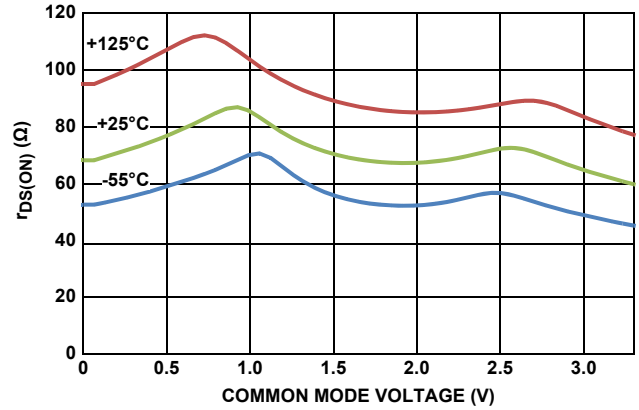


FIGURE 12.  $r_{DS(ON)}$  vs COMMON MODE VOLTAGE ( $V_S = +3.3V$ )

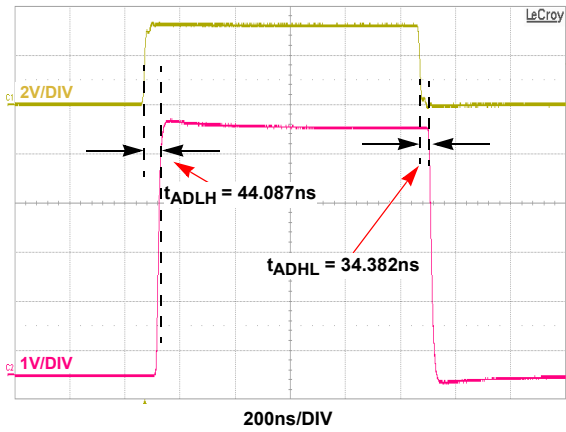


FIGURE 13. ADDRESS PROPAGATION DELAY

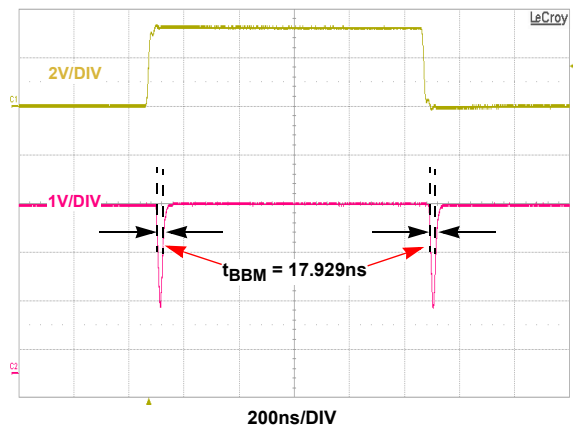


FIGURE 14. BREAK-BEFORE-MAKE DELAY

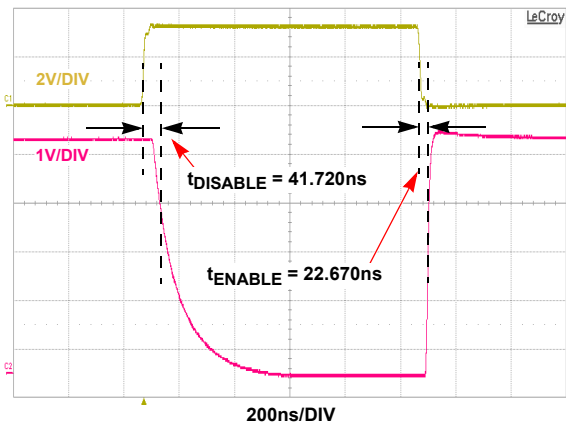


FIGURE 15. ENABLE/DISABLE PROPAGATION DELAY

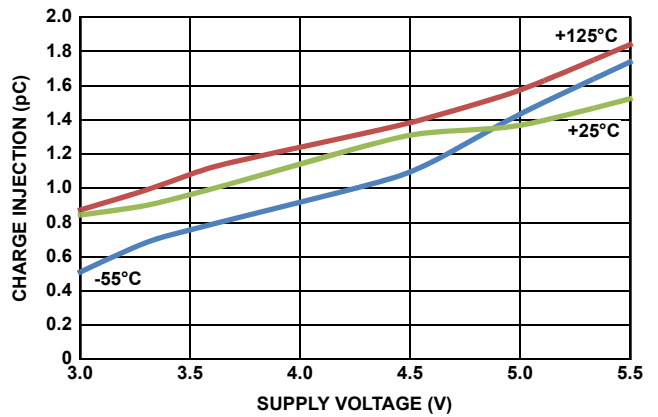


FIGURE 16. CHARGE INJECTION



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