

ISL71841SEHEV1Z

Evaluation Board

UG037  
Rev.0.00  
June 16, 2015

**Description**

The [ISL71841SEH](#) is a radiation hardened, 32-channel high ESD protected multiplexer that is fabricated using Intersil's proprietary P6SOI (Silicon On Insulator) process technology to mitigate single-event effects and total ionizing dose. It operates with a dual supply voltage ranging from  $\pm 10.8V$  to  $\pm 16.5V$ . This evaluation board is designed to provide easy access to the capabilities of the part.

The evaluation board has a set of toggle switches, which provides a convenient way to address all 32 channels without the need for extra supplies. There's also a BNC input available that will allow you to drive the address pins with a signal generator.

**Specifications**

This board has been configured and optimized for the following operating conditions:

- $V^+ = +10.8V$  to  $+16.5V$
- $V^- = -10.8V$  to  $-16.5V$
- $V_{REF} = 4.5V$  to  $5.5V$

**Key Features**

- Jumper selectable input source for each input
- Toggle switches to conveniently select 1 of 32 channels
- BNC input for dynamic addressing
- Multiple loading options with jumpers on VOUT
- Convenient power connection
- On-board enable switch

**References**

[ISL71841SEH](#) Datasheet

**Ordering Information**

PART NUMBER	DESCRIPTION
ISL71841SEHEV1Z	Evaluation board for the ISL71841SEH

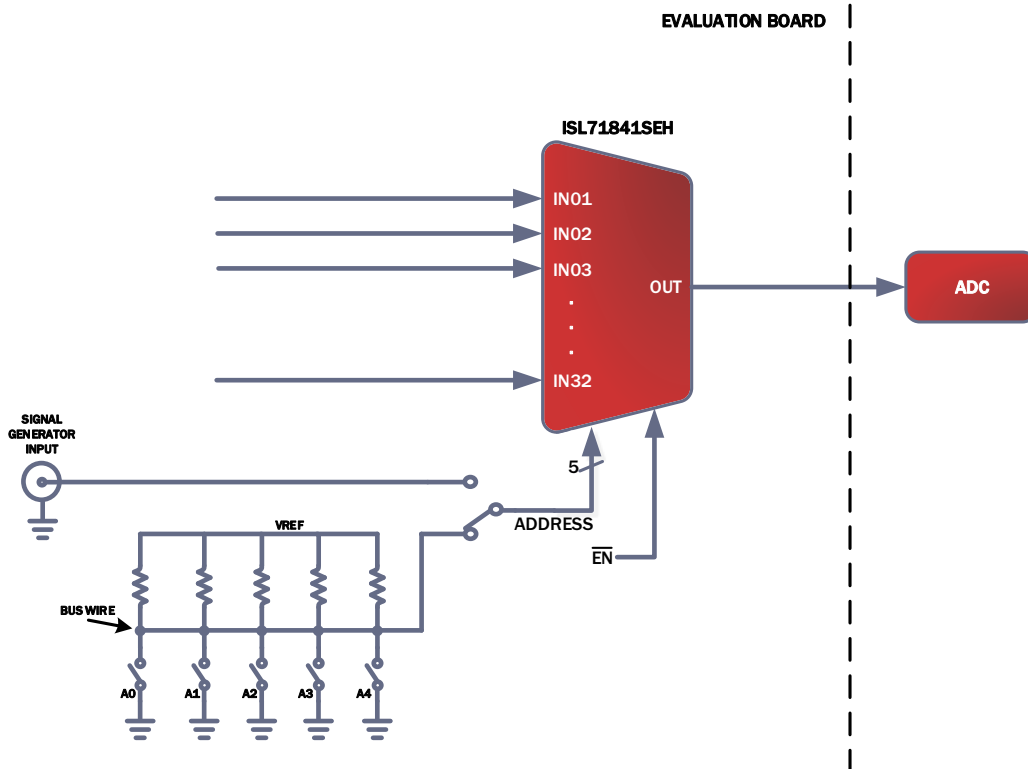


FIGURE 1. ISL71841SEHEV1Z BLOCK DIAGRAM

# ISL71841SEHEV1Z Evaluation Board



FIGURE 2. TOP SIDE



FIGURE 3. BOTTOM SIDE

## Operating Range

This board has power supply inputs for  $V^+$ ,  $V^-$  and  $V_{REF}$ . There's no requirements for sequencing on these supplies, but it is recommended that the supplies come up relatively at the same time. In-line resistors are provided to  $V^+$  and  $V^-$  with decoupling capacitors close to the part for  $V^+$ ,  $V^-$  and  $V_{REF}$ . The in-line resistors are 100 $\Omega$  but can be changed by the user for additional power supply filtering or to limit the rise time of the supply voltages.

The voltage ranges for  $V^+$  is +10.8V to +16.5V and the range for  $V^-$  is -10.8V to -16.5V.  $V_{REF}$  ranges from 4.5V to 5.5V. The ISL71841SEH is a rail-to-rail mux and should be able to accommodate any input signal with a voltage level between or equal to the supplies voltages.  $V_{REF}$  is used to set the decoder logic levels.

## PCB Layout Guidelines

The ISL71841SEHEV1Z PCB layout has been optimized for ease of testing. When incorporating the ISL71841SEH into a system there are a few guidelines that can ensure optimal electrical and noise performance.

- Analog circuits can conduct noise through paths that connect it to the “outside world”. These paths include the  $V^+$ ,  $V^-$ ,  $V_{REF}$ , input to any switch and the output. It is important to make sure these paths are kept away from known noise sources.
- It is recommended to decouple the power supply pins ( $V^+$ ,  $V^-$  and  $V_{REF}$ ) for power supply filtering. If the traces to the supply lines are long, it is recommended to use a larger 1 $\mu$ F capacitor at the point of entry for the supply and a smaller capacitor, like a 0.1 $\mu$ F, close to the part to reduce high frequency perturbations.



## Bill of Materials

ITEM	QTY	REFERENCE DESIGNATOR	VALUE	TOL (%)	RATING	TYPE	PCB FOOTPRINT	MANUFACTURER	MANUFACTURER PART NUMBER
1	1	C6	100pF	5%	100V	X7R	0805	AVX	08051C101JAT4A
2	3	SP1-SP3	-	-	-	-	CONN	TEKTRONIX	131-4353-00
3	17	TP1-TP17	-	-	-	-	THOLE	KEYSTONE	1514-2
4	1	J28	-	-	-	-	CONN	AMPHENOL	31-5329-52RFX
5	1	J19	-	-	-	-	IN-LINE	Generic	CONN-1X8
6	5	C1-C5	1μF	10%	50V	X7R	0805	MURATA	GRM21BR71H105KA12L
7	6	SW1-SW6	-	-	-	-	SPST	C&K	GT12MSCBETR
8	1	R3	DNP	1%	DNP	-	0805	GENERIC	H2506-DNP-DNP-1
9	6	R4-R9	10k	1%	1/10W	-	0603	GENERIC	H2511-01002-1/10W1
10	1	R10	49.9k	1%	1/16W	-	0603	GENERIC	H2511-04992-1/16W1
11	2	R1, R2	10	1%	1/10W	-	0805	GENERIC	H2512-00100-1/10W1
12	1	U1	-	-	-	-	CQFP	INTERSIL	ISL71841SEHF/PROTO
13	32	J2-J17, J29-J44	-	-	-	-	THOLE	GENERIC	JUMPER-3-100
14	10	J1, J18, J20-J27	-	-	-	-	THOLE	GENERIC	JUMPER2_100

## Board Layout - 4 Layers

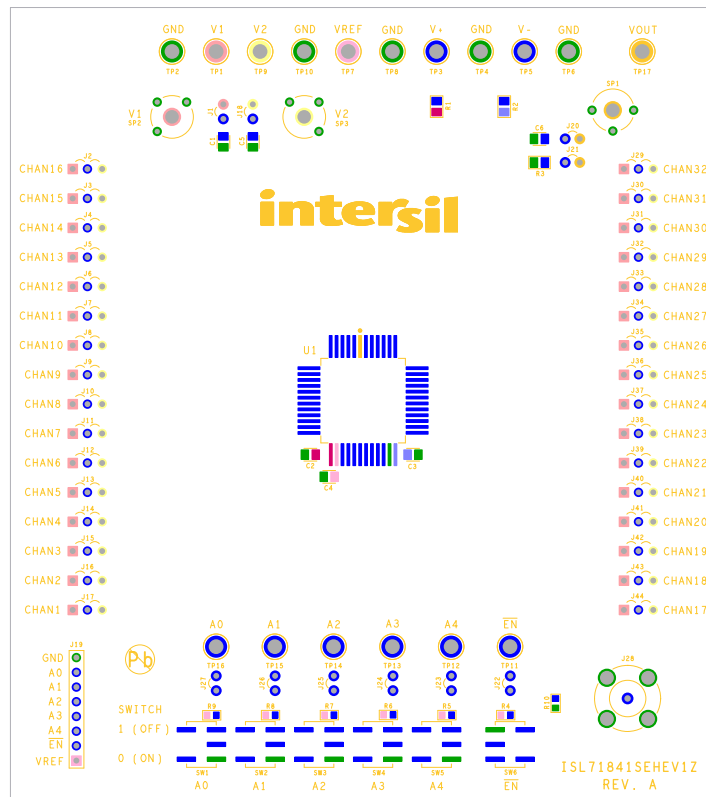


FIGURE 5. SILKSCREEN TOP

## Board Layout - 4 Layers (Continued)

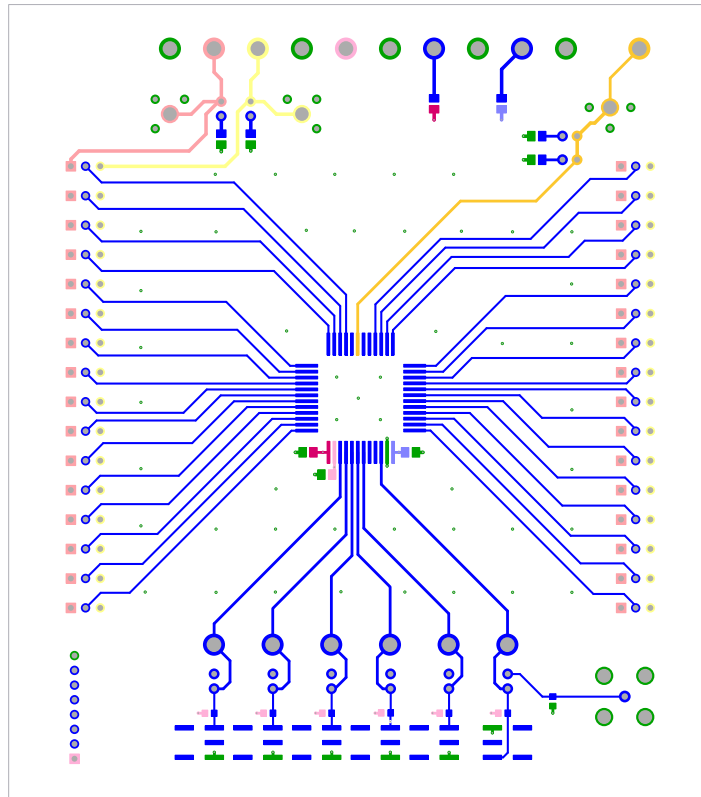


FIGURE 6. TOP LAYER

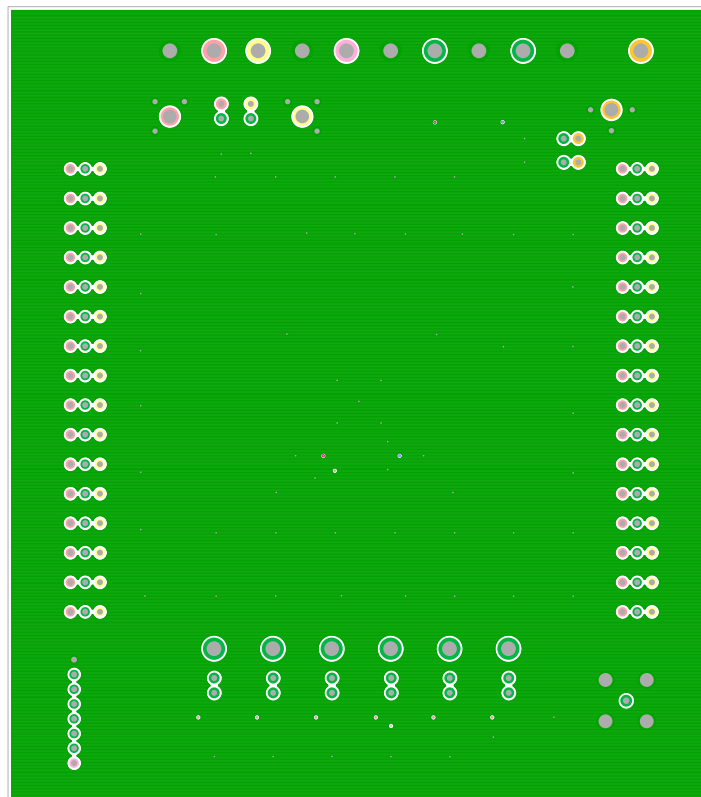


FIGURE 7. PCB - INNER LAYER 1 (TOP VIEW)

## Board Layout - 4 Layers (Continued)

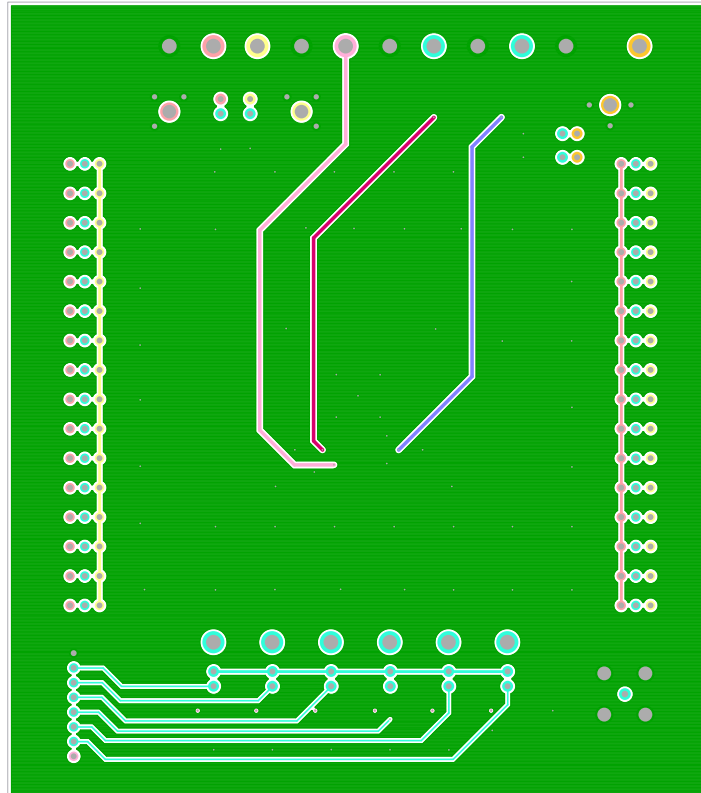


FIGURE 8. PCB - INNER LAYER 2 (TOP VIEW)

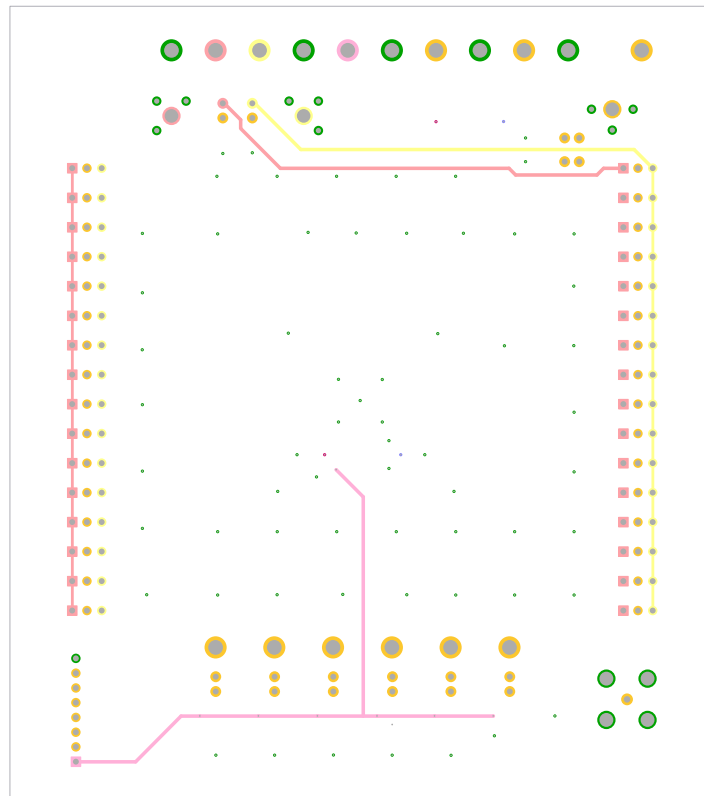


FIGURE 9. PCB - BOTTOM LAYER (TOP VIEW)

## Board Layout - 4 Layers (Continued)

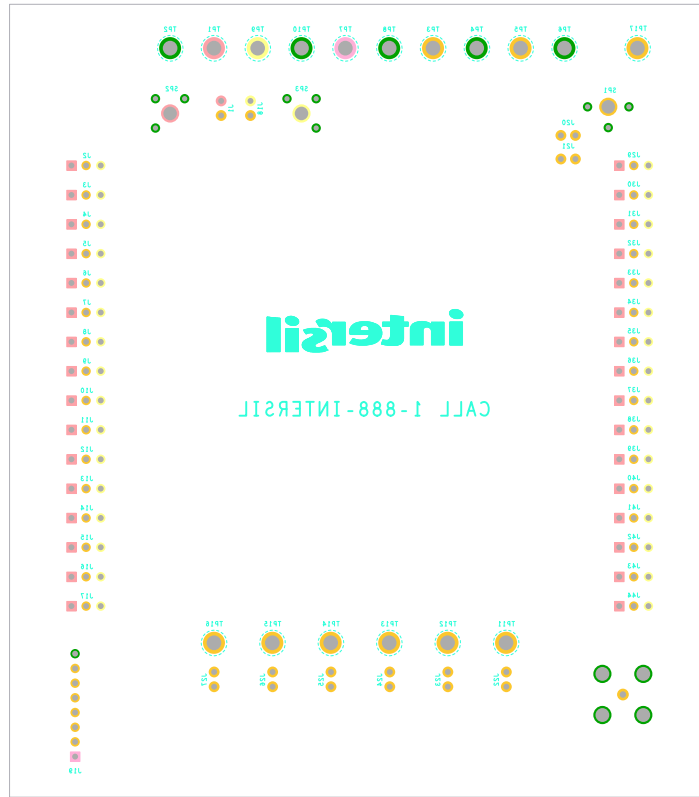


FIGURE 10. SILKSCREEN BOTTOM

## Typical Performance Curves

Unless otherwise noted:  $V^+ = +15V$ ,  $V^- = -15V$ ,  $V_{REF} = 5.0V$ ,  $T_A = +25^\circ C$

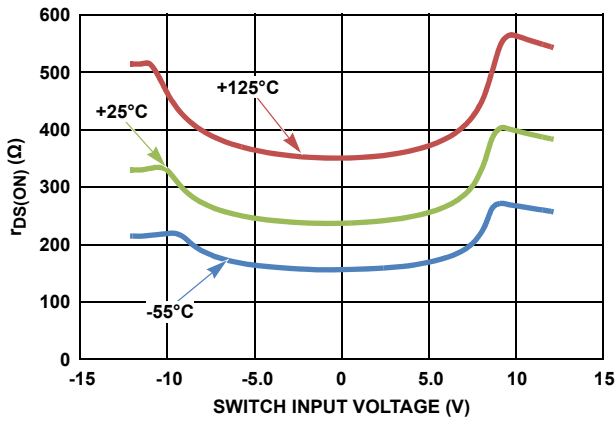


FIGURE 11.  $r_{DS(ON)}$  vs SWITCH INPUT VOLTAGE ( $V_{\pm} = \pm 12.0V$ )

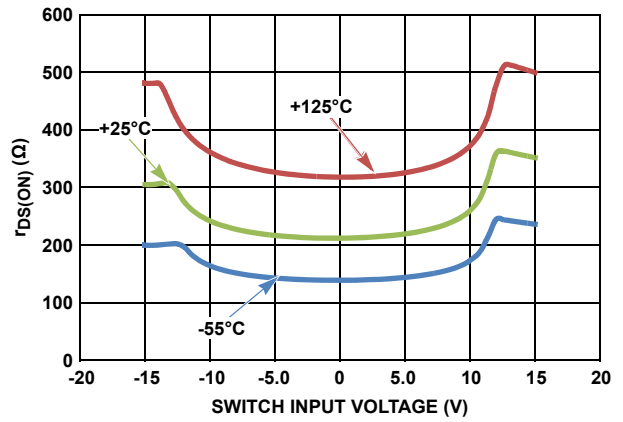


FIGURE 12.  $r_{DS(ON)}$  vs SWITCH INPUT VOLTAGE ( $V_{\pm} = \pm 15.0V$ )



# Typical Performance Curves

Unless otherwise noted:  $V^+ = +15V$ ,  $V^- = -15V$ ,  $V_{REF} = 5.0V$ ,  $T_A = +25^\circ C$  (Continued)

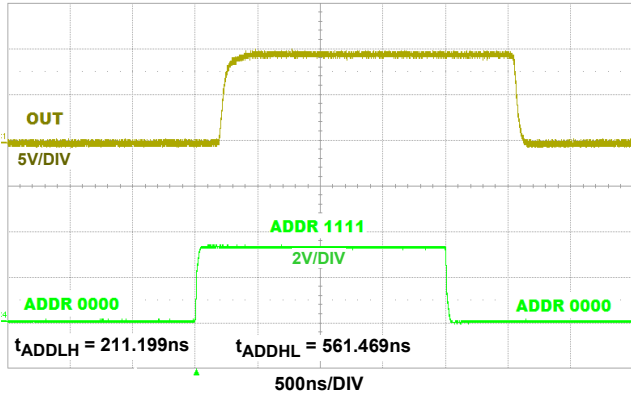


FIGURE 13. TYPICAL ADDRESS TO OUTPUT DELAY ( $V_{\pm} = \pm 15V$ ,  $+25^\circ C$ )

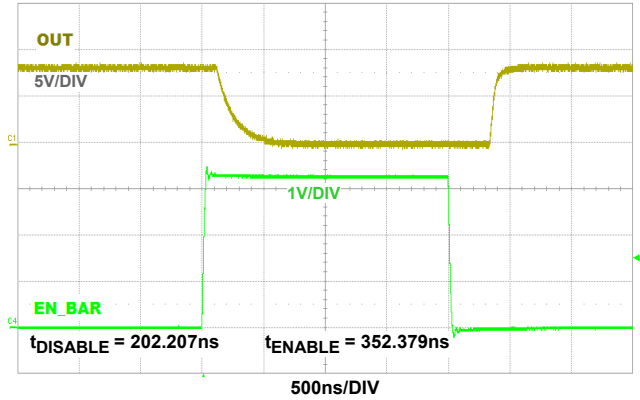


FIGURE 14. TYPICAL ENABLE TO OUTPUT DELAY ( $V_{\pm} = \pm 15V$ ,  $+25^\circ C$ )

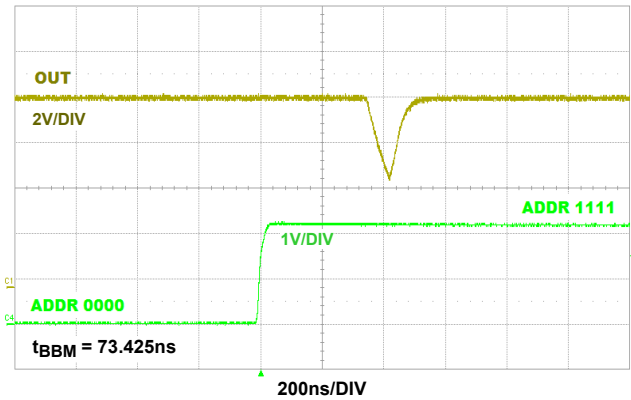


FIGURE 15. TYPICAL BREAK BEFORE MAKE DELAY ( $V_{\pm} = 15V$ ,  $+25^\circ C$ )

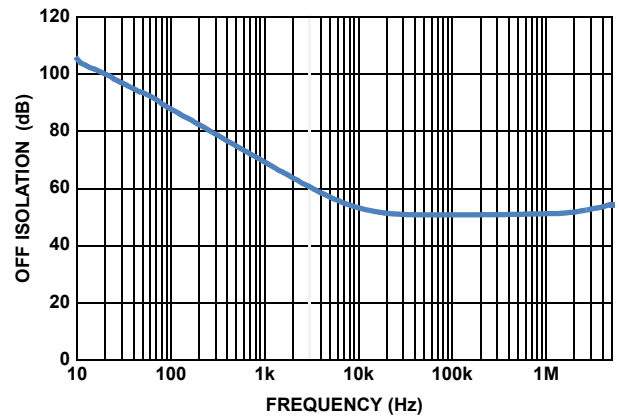


FIGURE 16. OFF ISOLATION ( $V_{\pm} = \pm 15V$ ,  $+25^\circ C$ )

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