User's Manual

ISL8210MEVAL1Z

User's Manual: Evaluation Board

Industrial Analog and Power

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1. Overview

The ISL8210MEVAL1Z evaluation board (shown in Figures 4 and 5) is designed for evaluating the ISL8210M. The ISL8210M is a single channel, synchronous step-down DC/DC power supply module that is capable of delivering up to 10A of continuous current. The proprietary Renesas R4 Technology control scheme has extremely fast transient performance, accurately regulated frequency control, and all internal compensation. The ISL8210M includes four setting up pins (SETx) for module configuration and allows for easy R4 loop optimization that results in fast transient performance across a wide range of applications, including all ceramic output filters. The ISL8210M integrates the controller, all power components, and most passive components. The device requires only a few external components to operate, which significantly reduces design complexity and board space, and it optimizes for high power density applications without the need for airflow or a heatsink.

The ISL8210MEVAL1Z evaluation board is a 3 x 3 inch six-layer FR4 board with 2oz. copper on all layers. The ISL8210MEVAL1Z operates from a single 4.5V to 15V wide input power rail and offers adjustable output voltages down to 0.5V and efficiencies of up to 95%. The ISL8210MEVAL1Z comes with placeholders for pin-strap resistors to set up output voltage, PFM/PWM mode, temperature compensation (TCOMP), switching frequency (f_{SW}), AV gain, OCP retry/latch-off, ultrasonic PFM enable, soft-start ramp rate, RR impedance, and AV gain multiplier (1x or 2x).

By default, the ISL8210MEVAL1Z is set to a 1V output voltage with a 400kHz switching frequency, 49 AV gain, and 200kΩ RR.

1.1 Key Features

- Input voltage range: 4.5V to 15V, capable of delivering up to 10A of continuous current and up to 95% conversion efficiency
- Adjustable output voltage: 0.5V to 5V with ±1.5% load/line/temperature regulation with remote sense
- Proprietary Renesas R4 Technology
- Programmable V_{OUT}, PFM/PWM mode, TCOMP, f_{SW}, AV gain, OCP retry/latchoff, ultrasonic PFM enable, soft-start ramp rate, RR, and AV gain multiplier
- Startup into precharged load
- Dedicated enable pin and PGOOD indicator
- Comprehensive fault protection for high system reliability: over-temperature protection, output overcurrent and short-circuit protection, output overvoltage and undervoltage protection, open remote sense protection, input UVLO and power sequence, and fault reset
- Thermally enhanced 12mm x 11mm x 5.3mm HDA package

1.2 Specifications

The ISL8210MEVAL1Z is configured and optimized for the following operating conditions:

- V_{IN} = 4.5V to 15V
- V_{OUT} = 1V
- $I_{OUT-MAX}$ = 10A
- f_{SW} = 400kHz
- AV gain multiplier = 2x, AV gain = 49, RR = 200kΩ
- TCOMP = +5°C

1.3 Ordering Information

Part Number	Description
ISL8210MEVAL1Z	10A high efficiency step-down power module evaluation board

1.4 Related Literature

For a full list of related documents, visit our website:

- ISL8210M device page

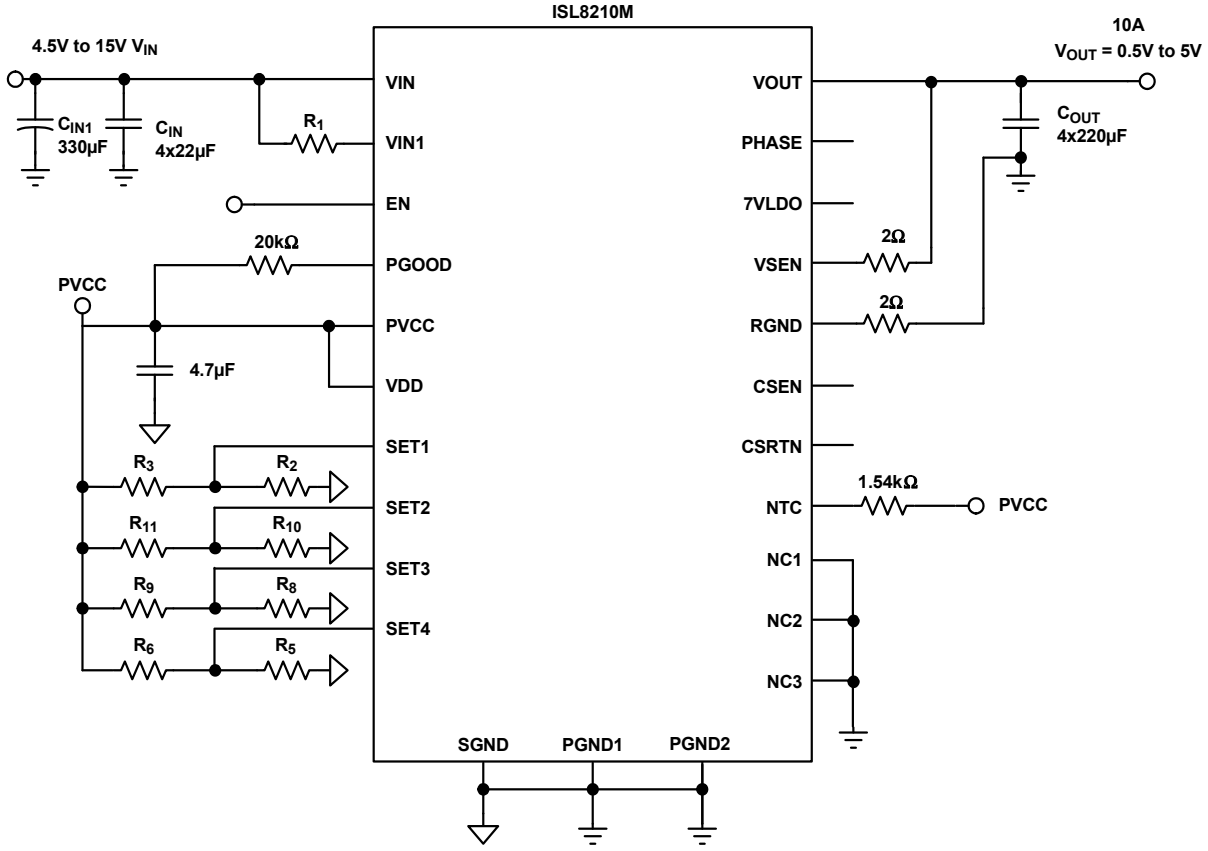

Figure 1. ISL8210MEVAL1Z Block Diagram

1.5 Recommended Testing Equipment

- DC power supply with minimum 15V/10A source current capability
- Electronic loads capable of sinking current up to 10A
- Digital Multimeters (DMMs)
- Oscilloscope with bandwidth greater than 100MHz

2. Functional Description

The ISL8210MEVAL1Z evaluation board provides the peripheral circuitry to evaluate the ISL8210M feature set. The ISL8210MEVAL1Z includes several connectors, test points, and external pin-strap resistors that simplify ISL8210M validation. Figure 4 on page 23 shows the top of the ISL8210MEVAL1Z. Figure 5 on page 23 shows the bottom of the ISL8210MEVAL1Z.

2.1 Quick Start Guide

(1) Disable the module by toggling the mechanical switch SW_1 to **2-3** as shown in Figure 4.

(2) Connect the DC input power supply to banana sockets J_4 and J_3 and the electronic load to sockets J_{14} and J_{15}. Ensure that the polarity for the power leads is correct and the input voltage is within the ISL8210MEVAL1Z's operating range of 4.5V to 15V. Use test points TP_1 (VIN) and TP_3 (GND) to accurately measure the input voltage.

(3) Toggle the mechanical switch SW_1 to **1-2** to enable the module.

(4) Turn on the DC input power supply.

(5) Probe test points TP_3 (VOUT) and TP_4 (PGND) to observe the output voltage. The output voltage should read 1V.

(6) Adjust the input voltage, V_{IN}, within the specified range and observe the output voltage. The output voltage variation should be within ±1.5%.

(7) Adjust the load current to within the specified range of 0A to 10A and observe the output voltage. The output voltage variation should be within ±1.5%.

(8) To change V_{OUT}, disconnect the ISL8210MEVAL1Z from the setup and populate 1% standard 0402 resistors at the R_2 and R_3 placeholder locations on the bottom layer. Use Table 1 on page 5 as a reference for programming different output voltages. See the "ISL8210M Design Guide Matrix of Typical Applications" table in the ISL8210M datasheet for recommended values in typical applications.

(9) To change PFM/PWM mode and TCOMP, disconnect the ISL8210MEVAL1Z from the setup and populate 1% standard 0402 resistors at the R_{10} and R_{11} placeholder locations on the bottom layer. Use Table 2 on page 11 as a reference for customizing module specifications. Renesas recommends using +5°C as the TCOMP.

(10) To change OCP retry/latchoff, f_{SW}, AV gain and ultrasonic PFM enable, disconnect the ISL8210MEVAL1Z from the setup and populate 1% standard 0402 resistors at the R_8 and R_9 placeholder locations on the bottom layer. Use Table 3 on page 17 as a reference for customizing module specifications. See the "ISL8210M Design Guide Matrix of Typical Applications" table in the ISL8210M datasheet for recommended values in typical applications.

(11) To change the soft-start ramp rate, RR, and AV gain multiplier, disconnect the ISL8210MEVAL1Z from the setup and populate 1% standard 0402 resistors at the R_5 and R_6 placeholder locations on the bottom layer. Use Table 4 on page 20 as a reference for customizing module specifications. See the "ISL8210M Design Guide Matrix of Typical Applications" table in the ISL8210M datasheet for recommended values in typical applications.

2.2 Thermal Considerations and Current Derating

Proper board layout is critical so that the module can operate safely and deliver the maximum allowable power. For the board to operate properly at high ambient temperature environments and carry full load current, carefully design the board layout to maximize thermal performance. For best thermal performance, use enough trace width, copper weight, and proper connectors.

The ISL8210MEVAL1Z is capable of operating at 10A full load current at room temperature without the need for additional cooling systems. However, if the ISL8210MEVAL1Z needs to operate at elevated ambient temperatures, the available output current needs to be derated. See the derated current curves in the ISL8210M datasheet to determine the maximum output current that the ISL8210MEVAL1Z can supply.

2.3 Programming the Resistor Reader

This section contains information about operating the resistor reader with the ISL8210M's four setting up pins (SET1, SET2, SET3, and SET4) to customize module specifications. See the "Definition of SET Pins" table in the ISL8210M datasheet for detailed descriptions of each setting up pin.

Table 1. SET1 Resistor Reader

R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
49.9	12.4	0.500
45.3	12.7	0.508
42.2	13.3	0.516
38.3	13.3	0.523
35.7	13.7	0.531
34	14.3	0.539
31.6	14.7	0.547
29.4	15	0.555
28	15.4	0.562
26.7	16.2	0.570
25.5	16.5	0.578
24.3	17.4	0.586
23.2	17.8	0.594
22.1	18.2	0.602
21	19.1	0.609
20	19.6	0.617
19.6	20.5	0.625
18.7	21.5	0.633
18.2	22.6	0.641
17.4	23.2	0.648
16.9	24.3	0.656
16.5	26.1	0.664
15.8	26.7	0.672
15.4	28.7	0.680
15	30.1	0.688
14.7	32.4	0.695
14	34	0.703
13.7	36.5	0.711

Table 1. SET1 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
13.3	39.2	0.719
13	43.2	0.727
107	26.7	0.734
97.6	27.4	0.742
90.9	28.7	0.750
82.5	28.7	0.758
76.8	29.4	0.766
71.5	30.1	0.773
68.1	31.6	0.781
63.4	32.4	0.789
Open	10	0.797
57.6	34.8	0.805
54.9	35.7	0.812
52.3	37.4	0.820
49.9	38.3	0.828
47.5	39.2	0.836
45.3	41.2	0.844
Open	21.5	0.852
42.2	44.2	0.859
40.2	45.3	0.867
39.2	48.7	0.875
37.4	49.9	0.883
36.5	52.3	0.891
Open	34.8	0.898
34	57.6	0.906
33.2	61.9	0.914
32.4	66.5	0.922
30.9	68.1	0.930
30.1	73.2	0.938
29.4	78.7	0.945
Open	52.3	0.953
28	93.1	0.961
174	43.2	0.969
158	44.2	0.977
147	46.4	0.984
133	46.4	0.992
Open	75	1.000
118	49.9	1.008
110	51.1	1.016
102	52.3	1.023
97.6	53.6	1.031

Table 1. SET1 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
93.1	56.2	1.039
Open	105	1.047
84.5	60.4	1.055
80.6	61.9	1.062
76.8	63.4	1.070
73.2	66.5	1.078
69.8	68.1	1.086
68.1	71.5	1.094
Open	147	1.102
63.4	78.7	1.109
60.4	80.6	1.117
59	84.5	1.125
57.6	90.9	1.133
54.9	93.1	1.141
53.6	100	1.148
52.3	105	1.156
49.9	110	1.164
48.7	118	1.172
47.5	127	1.180
46.4	137	1.188
45.3	150	1.195
Open	499	1.203
237	66.5	1.211
221	69.8	1.219
200	69.8	1.227
187	71.5	1.234
178	75	1.242
165	76.8	1.250
154	78.7	1.258
147	80.6	1.266
140	84.5	1.273
133	86.6	1.281
127	90.9	1.289
121	93.1	1.297
115	95.3	1.305
110	100	1.312
105	102	1.320
102	107	1.328
97.6	110	1.336
95.3	118	1.344
10	Open	1.352

Table 1. SET1 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
88.7	127	1.359
86.6	137	1.367
82.5	140	1.375
80.6	150	1.383
78.7	162	1.391
75	165	1.398
73.2	178	1.406
71.5	191	1.414
69.8	205	1.422
68.1	226	1.430
374	93.1	1.438
340	95.3	1.445
316	100	1.453
287	100	1.461
267	102	1.469
255	107	1.477
237	110	1.484
221	113	1.492
21.5	Open	1.500
200	121	1.508
191	124	1.516
182	130	1.523
174	133	1.531
165	137	1.539
158	143	1.547
150	147	1.555
147	154	1.562
140	158	1.570
137	169	1.578
130	174	1.586
127	182	1.594
124	196	1.602
118	200	1.609
115	215	1.617
113	232	1.625
110	243	1.633
105	255	1.641
102	274	1.648
100	294	1.656
97.6	324	1.664
523	130	1.672

Table 1. SET1 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
475	133	1.680
442	140	1.688
402	140	1.695
374	143	1.703
357	150	1.711
332	154	1.719
309	158	1.727
294	162	1.734
280	169	1.742
267	174	1.750
255	182	1.758
243	187	1.766
232	191	1.773
221	200	1.781
210	205	1.789
34.8	Open	1.797
196	226	1.805
191	237	1.812
182	243	1.820
178	255	1.828
174	274	1.836
165	280	1.914
162	301	1.992
158	324	2.070
154	340	2.148
147	357	2.227
143	383	2.305
140	412	2.383
137	453	2.461
732	182	2.469
665	187	2.477
619	196	2.484
576	200	2.492
52.3	Open	2.500
499	210	2.508
464	215	2.516
432	221	2.523
412	226	2.602
392	237	2.68
374	243	2.758
357	255	2.836

Table 1. SET1 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
340	261	2.914
324	267	2.992
75	Open	3.000
309	280	3.070
301	294	3.148
287	301	3.227
274	309	3.281
267	332	3.289
105	Open	3.297
249	357	3.305
243	383	3.312
232	392	3.320
226	422	3.328
221	453	3.406
215	475	3.484
205	499	3.562
200	536	3.641
196	576	3.719
191	634	3.797
1000	249	3.875
909	255	3.953
845	267	4.031
768	267	4.109
715	274	4.188
665	280	4.266
634	294	4.344
590	301	4.422
562	309	4.500
536	324	4.578
511	332	4.656
487	348	4.734
464	357	4.812
442	365	4.891
422	383	4.969
402	392	4.977
392	412	4.984
374	422	4.992
147	Open	5.000
348	464	5.008
499	Open	0.000

Table 2. SET2 Resistor Reader

R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Compensation (°C)
29.4	15	Enabled	+30
28	15.4	Enabled	+30
26.7	16.2	Enabled	+30
25.5	16.5	Enabled	+30
24.3	17.4	Enabled	+30
23.2	17.8	Enabled	+30
22.1	18.2	Enabled	+30
21	19.1	Enabled	+30
Open	10	Enabled	+30
Open	10	Enabled	+30
45.3	12.7	Enabled	+30
42.2	13.3	Enabled	+30
38.3	13.3	Enabled	+30
35.7	13.7	Enabled	+30
34	14.3	Enabled	+30
31.6	14.7	Enabled	+30
20	19.6	Enabled	+30
19.6	20.5	Enabled	+30
18.7	21.5	Enabled	+30
18.2	22.6	Enabled	+30
17.4	23.2	Enabled	+30
16.9	24.3	Enabled	+30
16.5	26.1	Enabled	+30
15.8	26.7	Enabled	+30
15.4	28.7	Enabled	+30
15	30.1	Enabled	+30
14.7	32.4	Enabled	+30
14	34	Enabled	+30
13.7	36.5	Enabled	+30
13.3	39.2	Enabled	+30
13	43.2	Enabled	+30
10	Open	Enabled	+30
63.4	32.4	Enabled	+15
60.4	33.2	Enabled	+15
57.6	34.8	Enabled	+15
54.9	35.7	Enabled	+15
52.3	37.4	Enabled	+15
49.9	38.3	Enabled	+15
47.5	39.2	Enabled	+15
45.3	41.2	Enabled	+15

Table 2. SET2 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Compensation (°C)
Open	21.5	Enabled	+15
107	26.7	Enabled	+15
97.6	27.4	Enabled	+15
90.9	28.7	Enabled	+15
82.5	28.7	Enabled	+15
76.8	29.4	Enabled	+15
71.5	30.1	Enabled	+15
68.1	31.6	Enabled	+15
43.2	42.2	Enabled	+15
42.2	44.2	Enabled	+15
40.2	45.3	Enabled	+15
39.2	48.7	Enabled	+15
37.4	49.9	Enabled	+15
36.5	52.3	Enabled	+15
34.8	54.9	Enabled	+15
34	57.6	Enabled	+15
33.2	61.9	Enabled	+15
32.4	66.5	Enabled	+15
30.9	68.1	Enabled	+15
30.1	73.2	Enabled	+15
29.4	78.7	Enabled	+15
28.7	84.5	Enabled	+15
28	93.1	Enabled	+15
21.5	Open	Enabled	+15
102	52.3	Enabled	+5
97.6	53.6	Enabled	+5
93.1	56.2	Enabled	+5
88.7	57.6	Enabled	+5
84.5	60.4	Enabled	+5
80.6	61.9	Enabled	+5
76.8	63.4	Enabled	+5
73.2	66.5	Enabled	+5
Open	34.8	Enabled	+5
174	43.2	Enabled	+5
158	44.2	Enabled	+5
147	46.4	Enabled	+5
133	46.4	Enabled	+5
124	47.5	Enabled	+5
118	49.9	Enabled	+5
110	51.1	Enabled	+5

Table 2. SET2 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Compensation (°C)
69.8	68.1	Enabled	+5
68.1	71.5	Enabled	+5
64.9	73.2	Enabled	+5
63.4	78.7	Enabled	+5
60.4	80.6	Enabled	+5
59	84.5	Enabled	+5
57.6	90.9	Enabled	+5
54.9	93.1	Enabled	+5
53.6	100	Enabled	+5
52.3	105	Enabled	+5
49.9	110	Enabled	+5
48.7	118	Enabled	+5
47.5	127	Enabled	+5
46.4	137	Enabled	+5
45.3	150	Enabled	+5
34.8	Open	Enabled	+5
154	78.7	Enabled	Off
147	80.6	Enabled	Off
140	84.5	Enabled	Off
133	86.6	Enabled	Off
127	90.9	Enabled	Off
121	93.1	Enabled	Off
115	95.3	Enabled	Off
110	100	Enabled	Off
Open	52.3	Enabled	Off
261	64.9	Enabled	Off
237	66.5	Enabled	Off
221	69.8	Enabled	Off
200	69.8	Enabled	Off
187	71.5	Enabled	Off
178	75	Enabled	Off
165	76.8	Enabled	Off
105	102	Enabled	Off
102	107	Enabled	Off
97.6	110	Enabled	Off
95.3	118	Enabled	Off
90.9	121	Enabled	Off
88.7	127	Enabled	Off
86.6	137	Enabled	Off
82.5	140	Enabled	Off

Table 2. SET2 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Compensation (°C)
80.6	150	Enabled	Off
78.7	162	Enabled	Off
75	165	Enabled	Off
73.2	178	Enabled	Off
71.5	191	Enabled	Off
69.8	205	Enabled	Off
68.1	226	Enabled	Off
52.3	Open	Enabled	Off
221	113	Disabled	+30
210	115	Disabled	+30
200	121	Disabled	+30
191	124	Disabled	+30
182	130	Disabled	+30
174	133	Disabled	+30
165	137	Disabled	+30
158	143	Disabled	+30
Open	75	Disabled	+30
374	93.1	Disabled	+30
340	95.3	Disabled	+30
316	100	Disabled	+30
287	100	Disabled	+30
267	102	Disabled	+30
255	107	Disabled	+30
237	110	Disabled	+30
150	147	Disabled	+30
147	154	Disabled	+30
140	158	Disabled	+30
137	169	Disabled	+30
130	174	Disabled	+30
127	182	Disabled	+30
124	196	Disabled	+30
118	200	Disabled	+30
115	215	Disabled	+30
113	232	Disabled	+30
110	243	Disabled	+30
105	255	Disabled	+30
102	274	Disabled	+30
100	294	Disabled	+30
97.6	324	Disabled	+30
75	Open	Disabled	+30

Table 2. SET2 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Compensation (°C)
309	158	Disabled	+15
294	162	Disabled	+15
280	169	Disabled	+15
267	174	Disabled	+15
255	182	Disabled	+15
243	187	Disabled	+15
232	191	Disabled	+15
221	200	Disabled	+15
Open	105	Disabled	+15
523	130	Disabled	+15
475	133	Disabled	+15
442	140	Disabled	+15
402	140	Disabled	+15
374	143	Disabled	+15
357	150	Disabled	+15
332	154	Disabled	+15
210	205	Disabled	+15
205	215	Disabled	+15
196	226	Disabled	+15
191	237	Disabled	+15
182	243	Disabled	+15
178	255	Disabled	+15
174	274	Disabled	+15
165	280	Disabled	+15
162	301	Disabled	+15
158	324	Disabled	+15
154	340	Disabled	+15
147	357	Disabled	+15
143	383	Disabled	+15
140	412	Disabled	+15
137	453	Disabled	+15
105	Open	Disabled	+15
432	221	Disabled	+5
412	226	Disabled	+5
392	237	Disabled	+5
374	243	Disabled	+5
357	255	Disabled	+5
340	261	Disabled	+5
324	267	Disabled	+5
309	280	Disabled	+5

Table 2. SET2 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Compensation (°C)
Open	147	Disabled	+5
732	182	Disabled	+5
665	187	Disabled	+5
619	196	Disabled	+5
576	200	Disabled	+5
523	200	Disabled	+5
499	210	Disabled	+5
464	215	Disabled	+5
301	294	Disabled	+5
287	301	Disabled	+5
274	309	Disabled	+5
267	332	Disabled	+5
255	340	Disabled	+5
249	357	Disabled	+5
243	383	Disabled	+5
232	392	Disabled	+5
226	422	Disabled	+5
221	453	Disabled	+5
215	475	Disabled	+5
205	499	Disabled	+5
200	536	Disabled	+5
196	576	Disabled	+5
191	634	Disabled	+5
147	Open	Disabled	+5
590	301	Disabled	Off
562	309	Disabled	Off
536	324	Disabled	Off
511	332	Disabled	Off
487	348	Disabled	Off
464	357	Disabled	Off
442	365	Disabled	Off
422	383	Disabled	Off
Open	499	Disabled	Off
1000	249	Disabled	Off
909	255	Disabled	Off
845	267	Disabled	Off
768	267	Disabled	Off
715	274	Disabled	Off
665	280	Disabled	Off
634	294	Disabled	Off

Table 2. SET2 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	PFM	Temperature Compensation (°C)
402	392	Disabled	Off
392	412	Disabled	Off
374	422	Disabled	Off
365	453	Disabled	Off
348	464	Disabled	Off
340	487	Disabled	Off
324	511	Disabled	Off
316	536	Disabled	Off
309	576	Disabled	Off
301	604	Disabled	Off
287	634	Disabled	Off
280	681	Disabled	Off
274	732	Disabled	Off
267	787	Disabled	Off
261	866	Disabled	Off
499	Open	Disabled	Off

Table 3. SET3 Resistor Reader

R_{UP} (kΩ)	R_{DW} (kΩ)	Ultrasonic PFM	Fault Behavior	f_{SW} (kHz)	AV Gain	
					1x	2x
Open	10	Disabled	Retry	300	42	84
49.9	12.4	Disabled	Retry	300	36.5	73
45.3	12.7	Disabled	Retry	300	30.5	61
42.2	13.3	Disabled	Retry	300	24.5	49
38.3	13.3	Disabled	Retry	300	19	38
35.7	13.7	Disabled	Retry	300	13	26
34	14.3	Disabled	Retry	300	7	14
31.6	14.7	Disabled	Retry	300	1	2
29.4	15	Disabled	Retry	400	42	84
28	15.4	Disabled	Retry	400	36.5	73
26.7	16.2	Disabled	Retry	400	30.5	61
25.5	16.5	Disabled	Retry	400	24.5	49
24.3	17.4	Disabled	Retry	400	19	38
23.2	17.8	Disabled	Retry	400	13	26
22.1	18.2	Disabled	Retry	400	7	14
21	19.1	Disabled	Retry	400	1	2
20	19.6	Disabled	Retry	500	42	84
19.6	20.5	Disabled	Retry	500	36.5	73
18.7	21.5	Disabled	Retry	500	30.5	61
18.2	22.6	Disabled	Retry	500	24.5	49

Table 3. SET3 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	Ultrasonic PFM	Fault Behavior	f_{SW} (kHz)	AV Gain	
					1x	2x
17.4	23.2	Disabled	Retry	500	19	38
16.9	24.3	Disabled	Retry	500	13	26
16.5	26.1	Disabled	Retry	500	7	14
15.8	26.7	Disabled	Retry	500	1	2
15.4	28.7	Disabled	Retry	600	42	84
15	30.1	Disabled	Retry	600	36.5	73
14.7	32.4	Disabled	Retry	600	30.5	61
14	34	Disabled	Retry	600	24.5	49
13.7	36.5	Disabled	Retry	600	19	38
13.3	39.2	Disabled	Retry	600	13	26
13	43.2	Disabled	Retry	600	7	14
10	Open	Disabled	Retry	600	1	2
Open	21.5	Disabled	Retry	700	42	84
107	26.7	Disabled	Retry	700	36.5	73
97.6	27.4	Disabled	Retry	700	30.5	61
90.9	28.7	Disabled	Retry	700	24.5	49
82.5	28.7	Disabled	Retry	700	19	38
76.8	29.4	Disabled	Retry	700	13	26
71.5	30.1	Disabled	Retry	700	7	14
68.1	31.6	Disabled	Retry	700	1	2
63.4	32.4	Disabled	Retry	850	42	84
60.4	33.2	Disabled	Retry	850	36.5	73
57.6	34.8	Disabled	Retry	850	30.5	61
54.9	35.7	Disabled	Retry	850	24.5	49
52.3	37.4	Disabled	Retry	850	19	38
49.9	38.3	Disabled	Retry	850	13	26
47.5	39.2	Disabled	Retry	850	7	14
45.3	41.2	Disabled	Retry	850	1	2
43.2	42.2	Disabled	Retry	1000	42	84
42.2	44.2	Disabled	Retry	1000	36.5	73
40.2	45.3	Disabled	Retry	1000	30.5	61
39.2	48.7	Disabled	Retry	1000	24.5	49
37.4	49.9	Disabled	Retry	1000	19	38
36.5	52.3	Disabled	Retry	1000	13	26
34.8	54.9	Disabled	Retry	1000	7	14
34	57.6	Disabled	Retry	1000	1	2
Open	34.8	Disabled	Latch	300	42	84
174	43.2	Disabled	Latch	300	36.5	73
158	44.2	Disabled	Latch	300	30.5	61
147	46.4	Disabled	Latch	300	24.5	49

Table 3. SET3 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	Ultrasonic PFM	Fault Behavior	f_{SW} (kHz)	AV Gain	
					1x	2x
133	46.4	Disabled	Latch	300	19	38
124	47.5	Disabled	Latch	300	13	26
118	49.9	Disabled	Latch	300	7	14
110	51.1	Disabled	Latch	300	1	2
102	52.3	Disabled	Latch	400	42	84
97.6	53.6	Disabled	Latch	400	36.5	73
93.1	56.2	Disabled	Latch	400	30.5	61
88.7	57.6	Disabled	Latch	400	24.5	49
84.5	60.4	Disabled	Latch	400	19	38
80.6	61.9	Disabled	Latch	400	13	26
76.8	63.4	Disabled	Latch	400	7	14
73.2	66.5	Disabled	Latch	400	1	2
69.8	68.1	Disabled	Latch	500	42	84
68.1	71.5	Disabled	Latch	500	36.5	73
64.9	73.2	Disabled	Latch	500	30.5	61
63.4	78.7	Disabled	Latch	500	24.5	49
60.4	80.6	Disabled	Latch	500	19	38
59	84.5	Disabled	Latch	500	13	26
57.6	90.9	Disabled	Latch	500	7	14
54.9	93.1	Disabled	Latch	500	1	2
53.6	100	Disabled	Latch	600	42	84
52.3	105	Disabled	Latch	600	36.5	73
49.9	110	Disabled	Latch	600	30.5	61
48.7	118	Disabled	Latch	600	24.5	49
47.5	127	Disabled	Latch	600	19	38
46.4	137	Disabled	Latch	600	13	26
45.3	150	Disabled	Latch	600	7	14
34.8	Open	Disabled	Latch	600	1	2
Open	52.3	Disabled	Latch	700	42	84
261	64.9	Disabled	Latch	700	36.5	73
237	66.5	Disabled	Latch	700	30.5	61
221	69.8	Disabled	Latch	700	24.5	49
200	69.8	Disabled	Latch	700	19	38
187	71.5	Disabled	Latch	700	13	26
178	75	Disabled	Latch	700	7	14
165	76.8	Disabled	Latch	700	1	2
154	78.7	Disabled	Latch	850	42	84
147	80.6	Disabled	Latch	850	36.5	73
140	84.5	Disabled	Latch	850	30.5	61
133	86.6	Disabled	Latch	850	24.5	49

Table 3. SET3 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	Ultrasonic PFM	Fault Behavior	f_{SW} (kHz)	AV Gain	
					1x	2x
127	90.9	Disabled	Latch	850	19	38
121	93.1	Disabled	Latch	850	13	26
115	95.3	Disabled	Latch	850	7	14
110	100	Disabled	Latch	850	1	2
105	102	Disabled	Latch	1000	42	84
102	107	Disabled	Latch	1000	36.5	73
97.6	110	Disabled	Latch	1000	30.5	61
95.3	118	Disabled	Latch	1000	24.5	49
90.9	121	Disabled	Latch	1000	19	38
88.7	127	Disabled	Latch	1000	13	26
86.6	137	Disabled	Latch	1000	7	14
82.5	140	Disabled	Latch	1000	1	2

Table 4. SET4 Resistor Reader

R_{UP} (kΩ)	R_{DW} (kΩ)	SS Rate (mV/µs)	RR (kΩ)	AVMLTI
Open	105	0.157	200	1
332	154	0.157	200	2
309	158	0.157	400	1
221	200	0.157	400	2
210	205	0.157	600	1
165	280	0.157	600	2
162	301	0.157	800	1
105	Open	0.157	800	2
Open	147	0.315	200	1
464	215	0.315	200	2
432	221	0.315	400	1
309	280	0.315	400	2
301	294	0.315	600	1
232	392	0.315	600	2
226	422	0.315	800	1
147	Open	0.315	800	2
Open	499	0.625	200	1
634	294	0.625	200	2
590	301	0.625	400	1
422	383	0.625	400	2
402	392	0.625	600	1
316	536	0.625	600	2
309	576	0.625	800	1
499	Open	0.625	800	2
Open	10	1.25	200	1

Table 4. SET4 Resistor Reader (Continued)

R_{UP} (kΩ)	R_{DW} (kΩ)	SS Rate (mV/µs)	RR (kΩ)	AVMLTI
31.6	14.7	1.25	200	2
29.4	15	1.25	400	1
21	19.1	1.25	400	2
20	19.6	1.25	600	1
15.8	26.7	1.25	600	2
15.4	28.7	1.25	800	1
10	Open	1.25	800	2
Open	21.5	2.5	200	1
68.1	31.6	2.5	200	2
63.4	32.4	2.5	400	1
45.3	41.2	2.5	400	2
43.2	42.2	2.5	600	1
34	57.6	2.5	600	2
33.2	61.9	2.5	800	1
21.5	Open	2.5	800	2
Open	34.8	5	200	1
110	51.1	5	200	2
102	52.3	5	400	1
73.2	66.5	5	400	2
69.8	68.1	5	600	1
54.9	93.1	5	600	2
53.6	100	5	800	1
34.8	Open	5	800	2
Open	52.3	10	200	1
165	76.8	10	200	2
154	78.7	10	400	1
110	100	10	400	2
105	102	10	600	1
82.5	140	10	600	2
80.6	150	10	800	1
52.3	Open	10	800	2

3. PCB Layout Guidelines

The ISL8210MEVAL1Z is a 3x3 inch six-layer FR-4 board with 2oz. copper on all layers. The board can be used as a single 10A reference design. For board layout information, see Figures 7 through 14 starting on page 27.

The ISL8210MEVAL1Z board layout is optimized for electrical performance, low loss, and good thermal performance. For similar performance in designs using the ISL8210M, use the following layout design tips:

3.1 Layout Considerations

(1) Renesas recommends using a six-layer PCB board. Use the top and bottom layer to route VIN and VOUT. Use a full ground plane in the internal layers (underneath the module) with shared SGND and PGND to simplify the layout design. Use another full ground plane directly above the bottom layer. Use the other internal layers to route the remote sense and PGOOD signals.

(2) Place the input capacitors and high frequency decoupling ceramic capacitors between VIN and PGND as close to the module as possible. The loop formed by the input capacitors, VIN, and PGND must be as small as possible to minimize high frequency noise. Place the output ceramic capacitors close to VOUT. Use a copper plane to connect the output ceramic capacitors to the load to avoid any parasitic inductances and resistances. See Figures 2 and 3 for an example layout.

(3) Use large copper planes for power paths (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress. Use multiple vias to connect the power planes in different layers.

(4) Do not oversize the copper planes for the PHASE planes. Because the PHASE planes are subjected to very high dv/dt, the parasitic capacitor formed between these planes and the surrounding circuitry tends to couple the switching noise. Ensure that none of the sensitive signal traces are routed close to the PHASE plane.

(5) Place the PVCC and VIN1 bypass capacitors underneath the PVCC and VIN1 pins and connect their grounds to the SGND. For the external pin-strap resistor dividers connected to SET1, SET2, SET3, and SET4, connect the low side dividers' ground to the SGND. If a local decoupling capacitor is used to bias these resistor dividers, place the decoupling capacitor close to the dividers and connect the capacitor's ground to the SGND. See Figure 3 for an example layout.

(6) Connect remote sensing traces to the regulation point to achieve a tight output voltage regulation. Route the remote sensing traces in parallel underneath the PGND layer and avoid routing the sensing trace near noisy planes such as PHASE. Place 2Ω resistors close to both VSEN and RGND to dampen the noise on the traces.

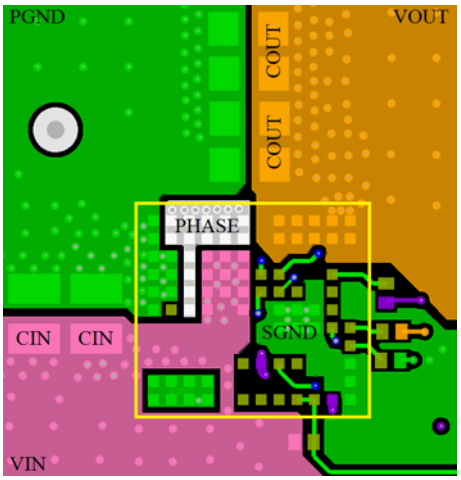

Figure 2. Layout Example - Top Layer

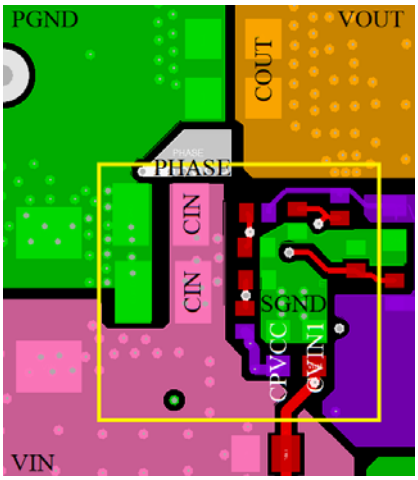

Figure 3. Layout Example - Bottom Layer

Figure 4. Top of Board

Figure 5. Bottom of Board

3.2 Schematic

RESISTOR READER

SET1 BOOT VOLTAGE=1V, R3=OPEN; R2=75K OHMS

SET2 PFM DISABLED, TCOMP=5C, R11=OPEN; R10=147K OHMS

SET3 RETRY,400KHZ,AV49 AND 25KHZ CLAMP DISABLED, R9= 25.5K OHMS; R8= 16.5K OHMS

SET4 SS= 0.157MV/US, RR=200KOHM AND AVMULTI=2X, R6= 332K OHMS;R5=154K OHMS

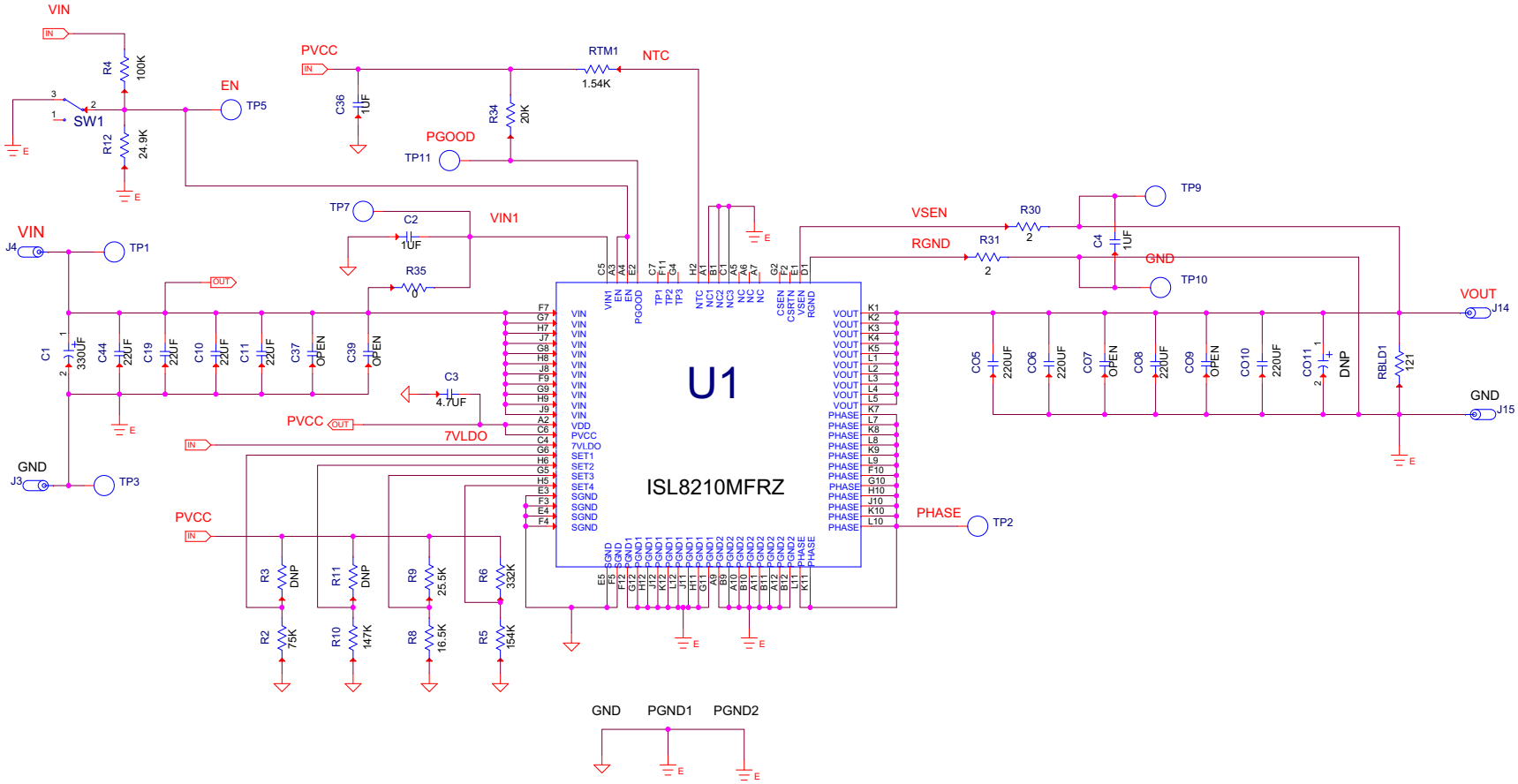

Figure 6. Schematic

3.3 Bill of Materials

Reference Designators	Qty	Value	Tol.	Voltage	Power	Package Type	Manufacturer	Part Number	Description
C1	1	330µF	±20%	16V		2917	Kemet	T521X337M016ATE025	POSCAP
C2, C36	2	1µF	±10%	25V		0603	Taiyo Yuden	TMK107BJ105KA-T	Ceramic Capacitor
C10, C11, C19, C44	4	22µF	±10%	25V		1210	Murata	GRM32ER71E226KE15L	Ceramic Capacitor
C3	1	4.7µF	±10%	10V		0603			Ceramic Capacitor
C4	1	1µF	±10%	16V		0603	TDK	C1608X7R1C105K	Ceramic Capacitor
CO5, CO6, CO8, C10	4	220µF	±20%	6.3V		1206	Murata	GRM31CR60J227ME11L	Ceramic Capacitor
C37, C39, CO7, CO9, CO11	5								DNP
J3, J15	2						Cinch Connectivity Solutions	111-0703-001	Binging Post (Black)
J4, J14	2						Cinch Connectivity Solutions	111-0702-001	Binging Post (Red)
RBLD1	1	121Ω	±1%		1/10W	0805			Thick Film Chip Resistor
RTM1	1	1.54kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R2	1	75kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R4	1	100kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R5	1	154kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R6	1	332kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R8	1	16.5kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R9	1	25.5kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R10	1	147kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R12	1	24.9kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R30, R31	2	2Ω	±1%		1/16W	0402	Vishay	CRCW04022R00FKED	Thick Film Chip Resistor
R34	1	20kΩ	±1%		1/16W	0402			Thick Film Chip Resistor
R35	1	0Ω	±1%		1/10W	0805			Thick Film Chip Resistor
R3, R11	2								DNP

Reference Designators	Qty	Value	Tol.	Voltage	Power	Package Type	Manufacturer	Part Number	Description
SW1	1						C&K	GT11MSCBE	Switch Toggle SPDT 0.4VA 20V
TP1-TP3, TP5, TP7, TP9-TP11	8					Through Hole	Keystone	5002	Miniature PC Test Point, Silver Plating 0.040” (1.02mm) Hole Diameter Mounting Type
U1	1					12x11 HDA	Renesas	ISL8210MFRZ	10A Step-Down Power Module

3.4 Board Layout

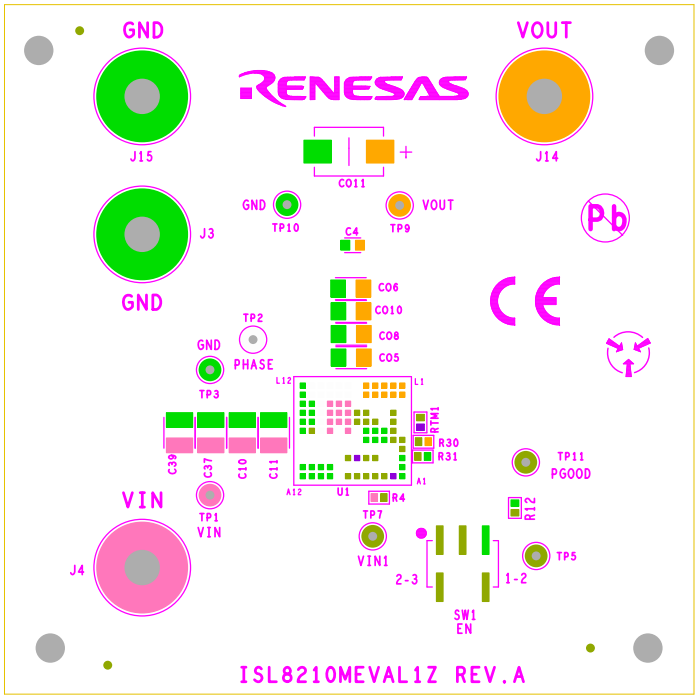

Figure 7. Silkscreen Top

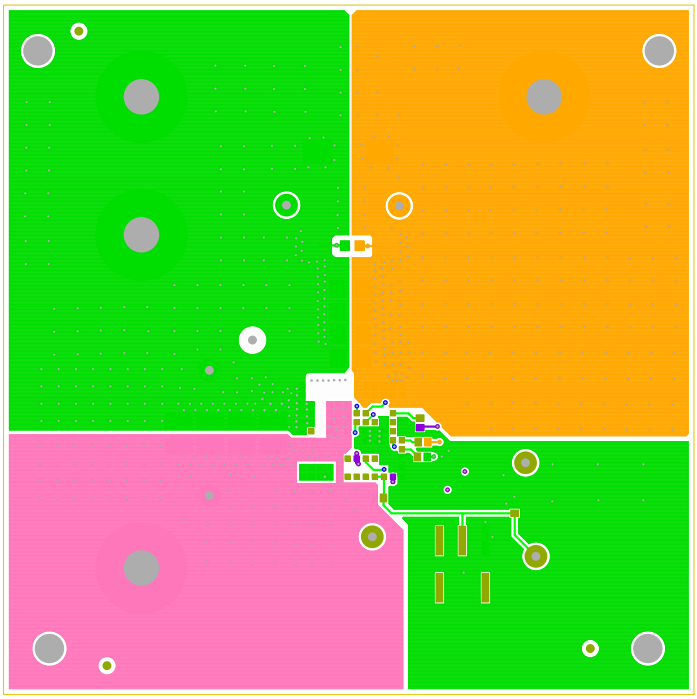

Figure 8. Top Layer Component Side

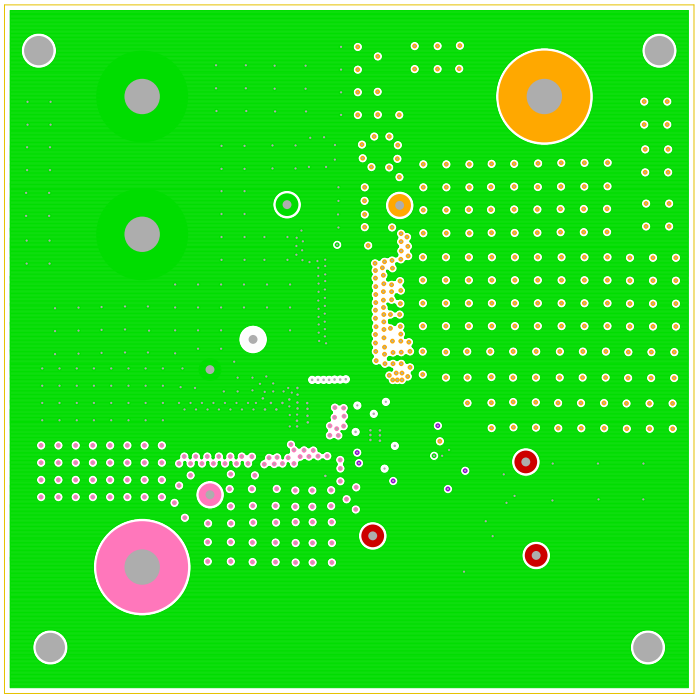

Figure 9. Inner Layer 2

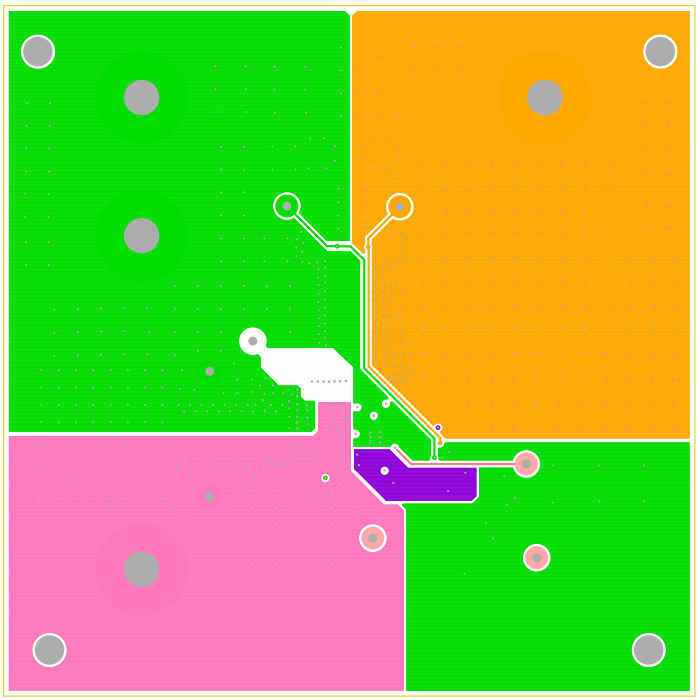

Figure 10. Inner Layer 3

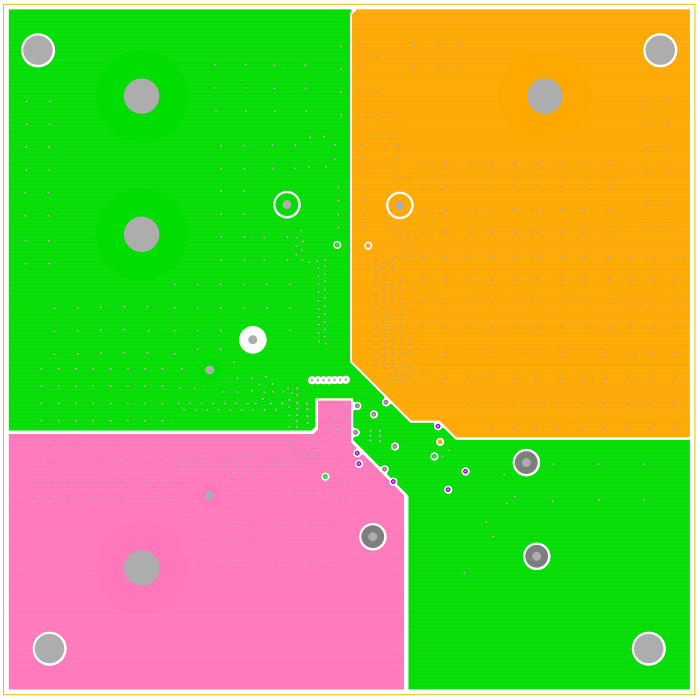

Figure 11. Inner Layer 4

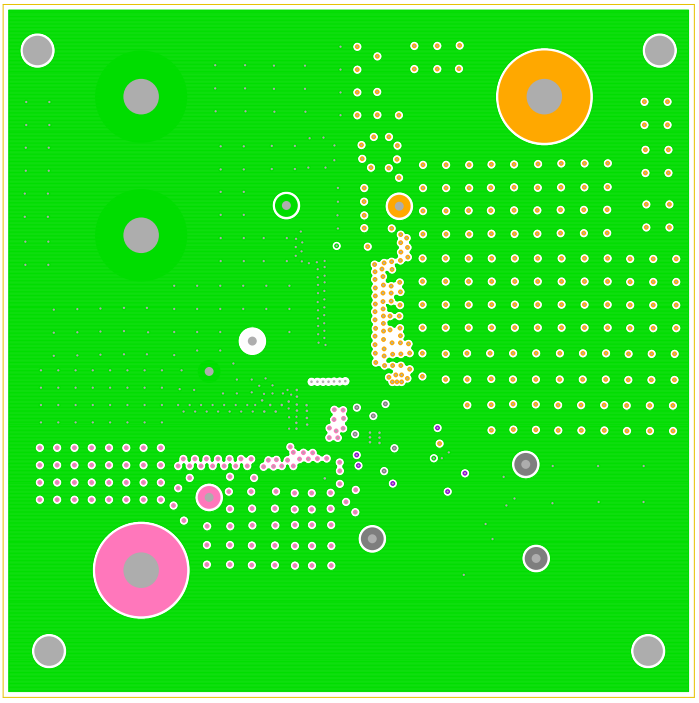

Figure 12. Inner Layer 5

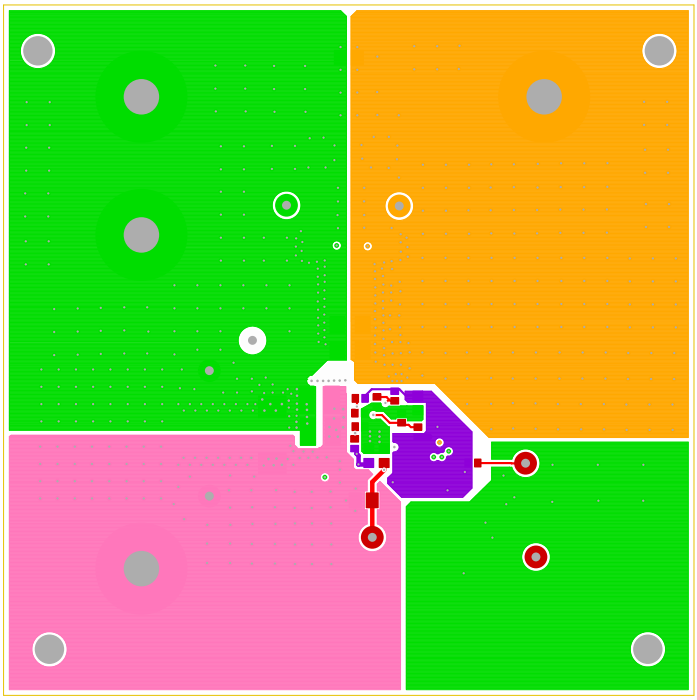

Figure 13. Bottom Layer Solder Side

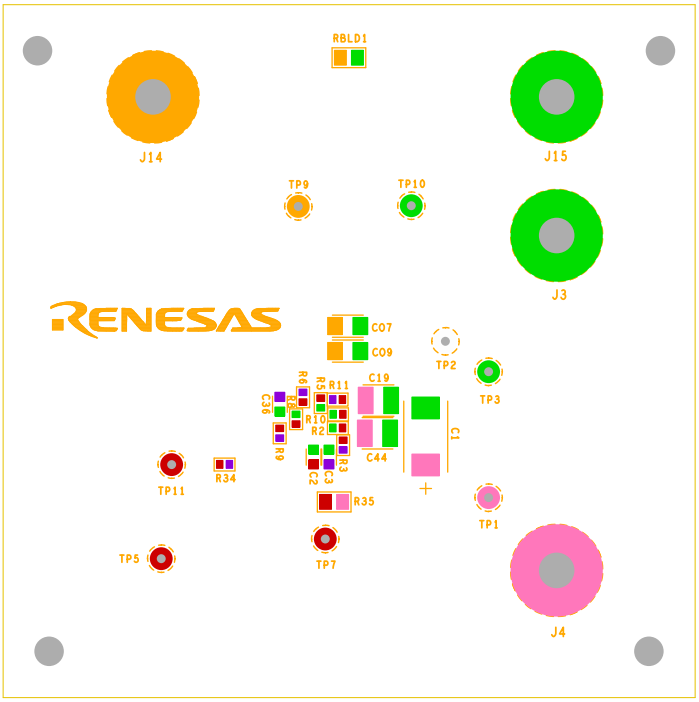

Figure 14. Silkscreen Bottom

4. Typical Performance Data

The following data was acquired using the ISL8210MEVAL1Z at +25°C ambient temperature and free air 0LFM. See the "ISL8210M Design Guide Matrix of Typical Applications" table in the ISL8210M datasheet for recommended configurations of different output voltages.

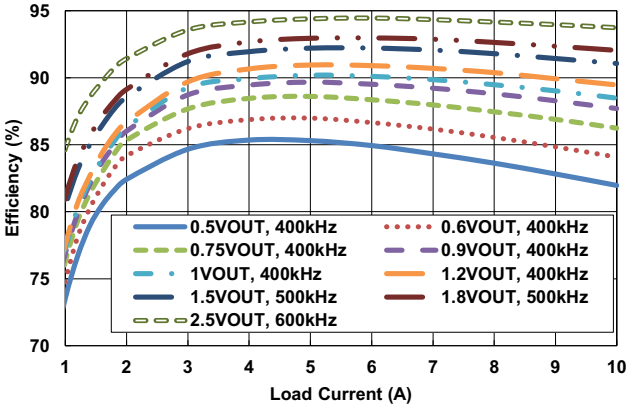

Figure 15. Efficiency vs Load Current at $5V_{IN}$ (PWM)

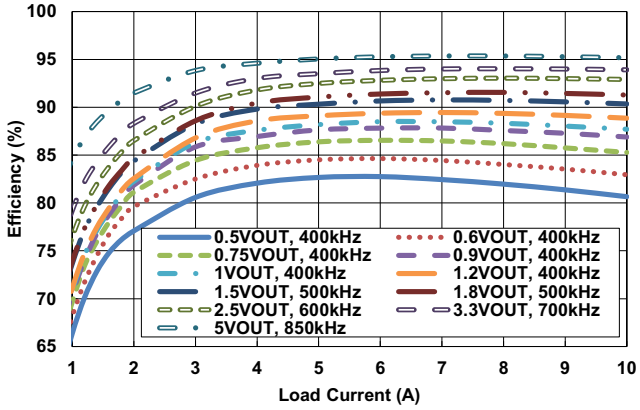

Figure 16. Efficiency vs Load Current at $8V_{IN}$ (PWM)

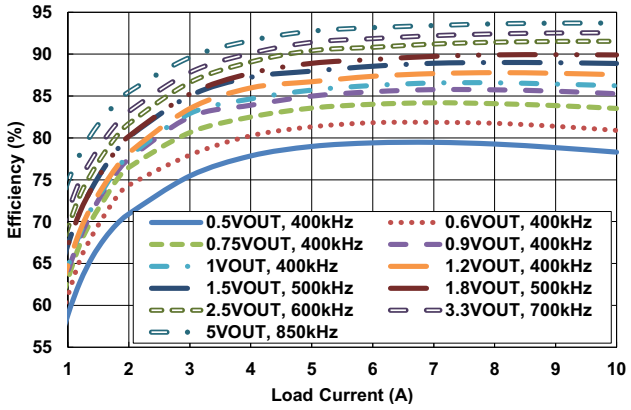

Figure 17. Efficiency vs Load Current at $12V_{IN}$ (PWM)

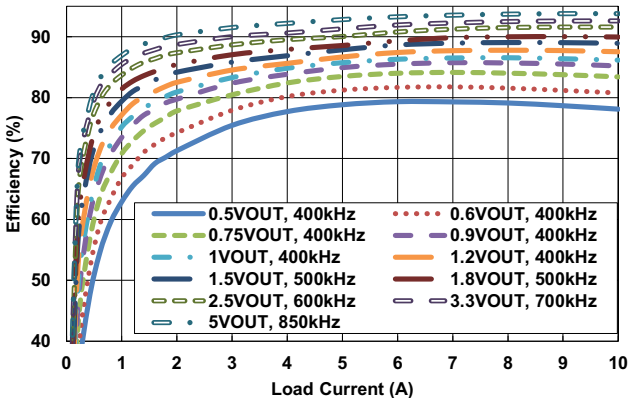

Figure 18. Efficiency vs Load Current at $12V_{IN}$ (PFM)

5. Typical Performance Curves

Operating conditions: V_{IN} = 12V, f_{SW} = 400kHz, AV gain = 49, RR = 200kΩ, C_{OUT} = 4 x 220µF Ceramic, PWM mode, unless otherwise noted.

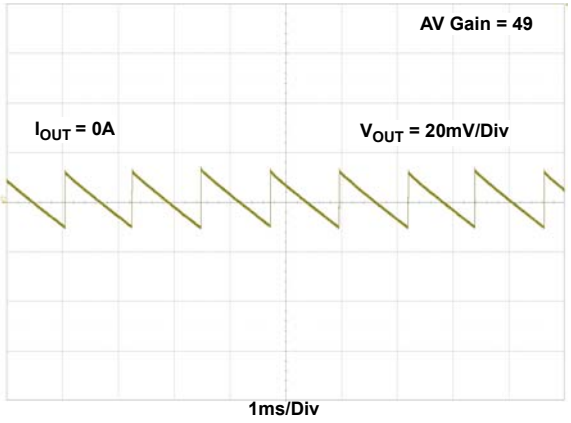

Figure 19. Output Ripple, V_{IN} = 12V, V_{OUT} = 1V, PFM Mode

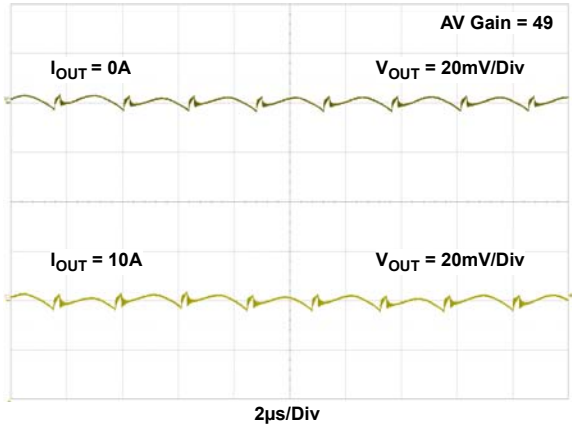

Figure 20. Output Ripple at $12V_{IN}$ and $1V_{OUT}$, 400kHz

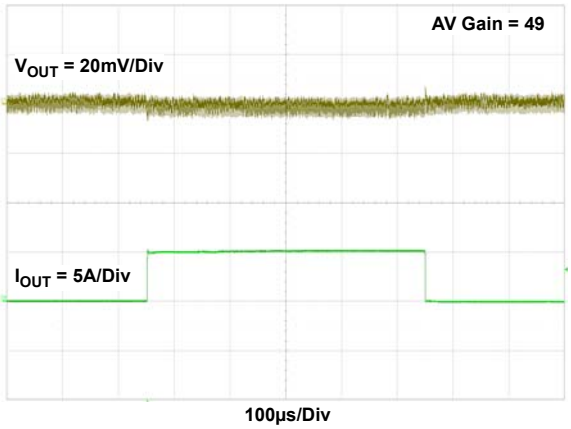

Figure 21. Load Transient Response at $1V_{OUT}$, 400kHz

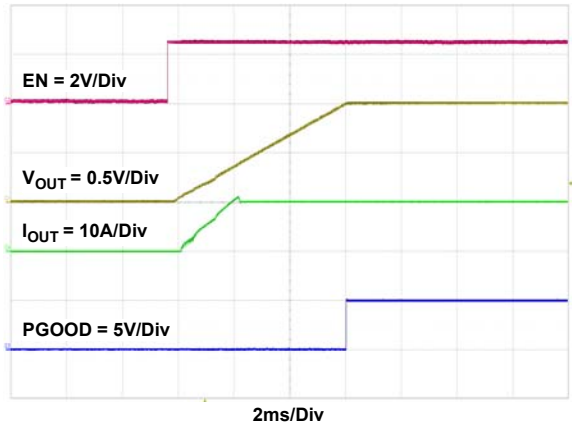

Figure 22. Start-Up Waveform, I_{OUT} = 10A

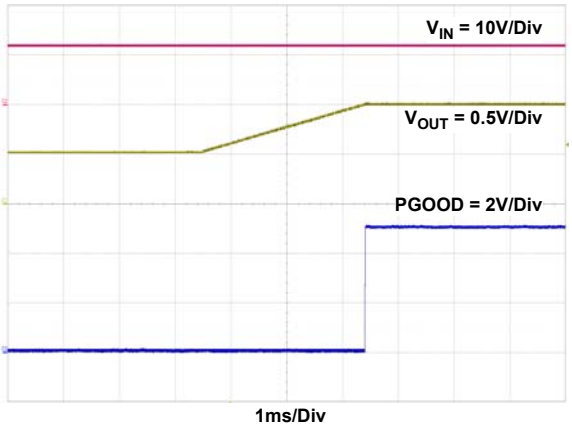

Figure 23. Prebiased Power-Up Waveform, Prebiased Voltage = 0.5V, V_{OUT} = 1V, I_{OUT} = No Load

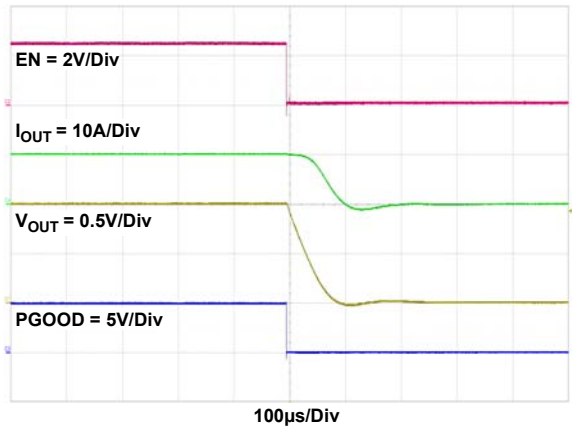

Figure 24. Shutdown Waveform, I_{OUT} = 10A

Operating conditions: V_{IN} = 12V, f_{SW} = 400kHz, AV gain = 49, RR = 200kΩ, C_{OUT} = 4 x 220µF Ceramic, PWM mode, unless otherwise noted. **(Continued)**

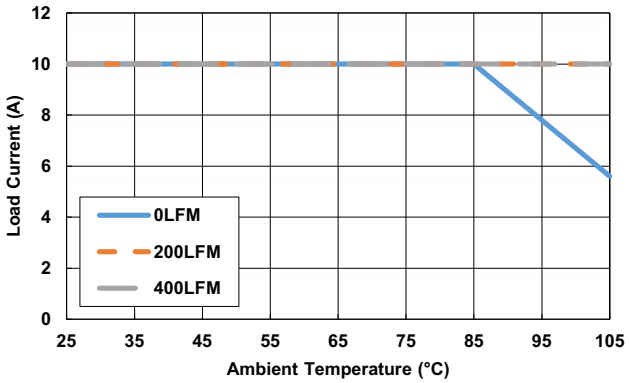

Figure 25. Derating Curve, V_{OUT} = 1V

6. Revision History

Rev.	Date	Description
1.01	Feb 13, 2019	Updated Figures 1, 2, and 3.
1.00	Feb 12, 2019	Initial release

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