ISL85012EVAL1Z

12A Evaluation Board User Guide

UG093
Rev.0.00
Oct 3, 2016

Description

The ISL85012 features integrated power switches that are capable of delivering 12A of continuous current within a 3.5mmx3.5mm package. The board is used to evaluate the performance of the ISL85012, high efficiency synchronous buck regulator.

Specifications

This board has been configured and optimized for the following operation conditions:

- V_{IN} = 4.5V to 18V
- V_{OUT} = 1.8V
- I_{OUTmax} = 12A
- f_{SW} = 600kHz
- Peak efficiency = 90%
- Output ripple <1% of the output voltage
- Transient response: ±5% (25% to 75% load 1.6A/µs)
- Operating junction temperature range: -40°C to +125°C

Key Features

- Small, compact design
- Switch selectable EN (enabled/disabled)
- Jumper selectable MODE (auto-DCM/forced-PWM)
- Jumper selectable OCP MODE (hiccup/latch-off)
- Jumper selectable default frequency (600kHz/300kHz)
- Connectors and test points for easy probing

Related Literature

- For a full list of related documents please visit our web page
  - ISL85012 product page

Ordering Information

PART NUMBER	DESCRIPTION
ISL85012EVAL1Z	Evaluation Board for ISL85012

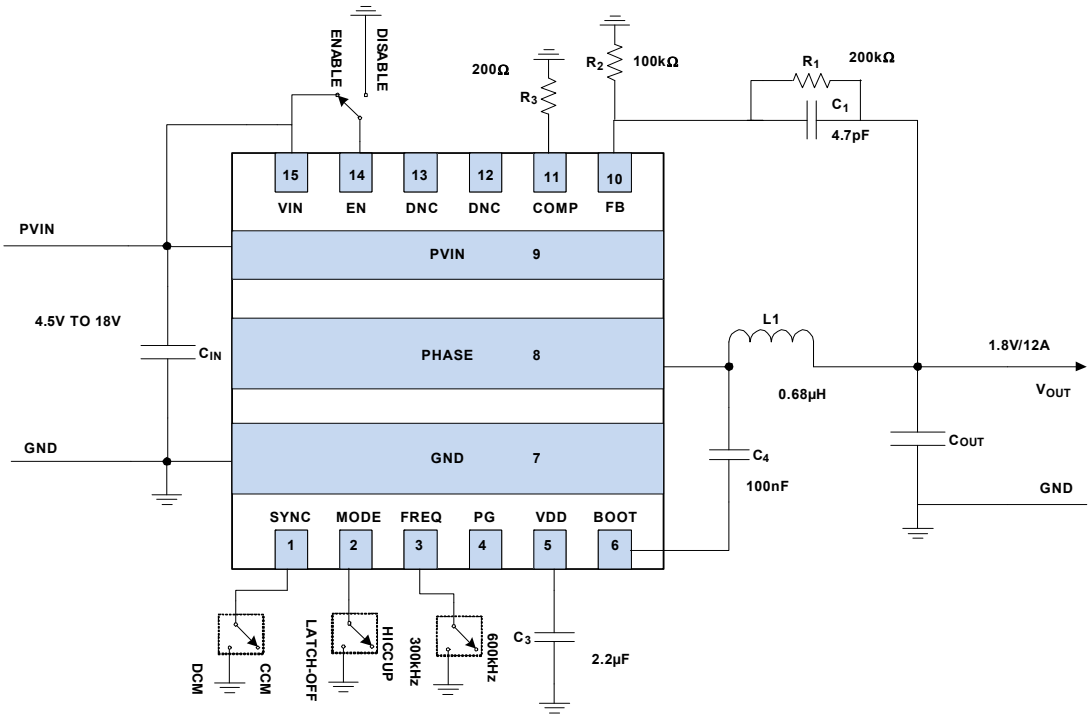

FIGURE 1. BLOCK DIAGRAM

Quick Setup Guide

1. Ensure that the circuit is correctly connected to the supply (PVIN/GND) and loads (VOUT/GND) prior to applying any power.
2. Verify there is no jumper connected.
3. Verify that the switch is enabled.
4. Turn on the power supply setting at 12V.
5. Verify the output voltage is 1.8V.

Recommended Equipment

The following materials are recommended to perform testing:

- 0V to 25V power supply with at least 15A source current capability
- Electronic loads capable of sinking current up to 20A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope
- Signal generator

Evaluating Other Output Voltages

The ISL85012EVAL1Z output is preset to 1.8V. The output voltages are programmable by the external resistor divider that scales the feedback relative to the internal reference voltage. The output voltage programming resistor, R_5, will depend on the value chosen for the feedback resistor, R_4, and the desired regulator output voltage, V_{OUT}. The value for the feedback resistor, R_4, is typically between 10kΩ and 400kΩ, as shown in Equation 1.

$$R_2 = \frac{R_1 \cdot 0.6V}{V_{OUT} - 0.6V} \quad \text{(EQ. 1)}$$

If the output voltage desired is 0.6V, then R_5 is left unpopulated. R_1 is still required to set the low frequency pole of the modulator compensation. The recommended values for different output applications are summarized in Table 2.

Switch/Jumper Control

The ISL85012EVAL1Z evaluation board contains a switch and jumpers for various controls of the ISL85012 circuitries. Table 1 details this function.

TABLE 1. SWITCH SETTINGS

SW/JUMP	FUNCTION
SW5	Enable/Disable
J10	Select frequency 600kHz/300kHz
J16	Select OCP behavior Hiccup/Latch-off
J17	Select light-load operation mode CCM/DCM

TABLE 2. DESIGN TABLE FOR DIFFERENT OUTPUT VOLTAGE

V_{OUT} (V)	0.9	1	1.2	1.5	1.8	2.5	3.3	5
V_{IN} (V)	4.5 to 18	4.5 to 18	4.5 to 18	4.5 to 18	4.5 to 18	4.5 to 18	4.5 to 18	6 to 18
Frequency (kHz)	300	300	300	600	600	600	600	600
Compensation	Internal	Internal	Internal	Internal	Internal	Internal	Internal	Internal
C_{IN} (µF)	3x22	3x22	3x22	3x22	3x22	3x22	3x22	3x22
C_{OUt} (µF)	2x560 + 4x100	2x330 + 3x100	2x330 + 3x100	4x100	3x100	4x47	4x47	4x47
L_1 (µH)	0.68	0.68	1	0.68	0.68	1	1	1.5
R_1 (kΩ)	100	100	147	150	200	301	365	365
R_2 (kΩ)	200	150	147	100	100	95.3	80.6	49.9
C_1 (pF)	DNP	DNP	DNP	10	4.7	4.7	3.3	3.3

NOTES:

1. The design table is referencing the schematic shown in Figure 1.
2. Ceramic capacitors are selected for 22µF and 100µF in the table.
3. 560µF (14mΩ) and 330µF (10mΩ) are selected low ESR conductive polymer aluminum solid capacitors.
4. Inductor 7443340068 (0.68µH), 7443340100 (1µH) and 7443340150 (1.5µH) from Wurth Electronics are selected for the above applications.
5. Recommend to keep the inductor peak-to-peak current less than 5A.

PCB Layout Consideration

A multilayer printed circuit board is recommended. Figure 2 shows the recommended top layer layout.

1. Place the input ceramic capacitors between PVIN and GND pins. Put them as close to the pins as possible.
2. A 1µF decoupling input ceramic capacitor is recommended. Place it as close to the VIN pin as possible.
3. A 2.2µF decoupling ceramic capacitor is recommended for VDD pin. Place it as close to the VDD pin as possible.
4. The entire inner Layer 1 is recommended to be GND plane in order to reduce noise coupling.
5. The switching node (PHASE) plane needs to be kept away from the feedback network. Place the resistor divider close to the IC.
6. Put three to five VIAs on the GND pin to connect the GND plane of other layers for better thermal performance. This allows the heat to move away from the IC. Keep the VIAs small, but not so small that their inside diameter prevents solder wicking through the holes during reflow. An 8 mil hole with 15 mil diameter VIAs are used on the evaluation board. Do not use “thermal relief” patterns to connect the VIAs. It is important to have a complete connection of the plated through-hole to each plane.

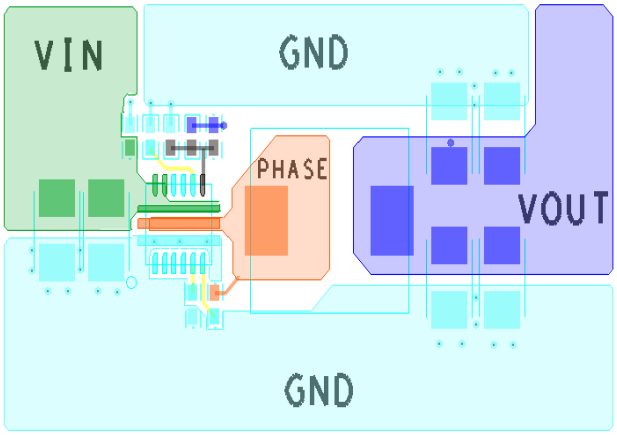

FIGURE 2. RECOMMENDED TOP LAYER LAYOUT

ISL85012EVAL1Z Evaluation Board

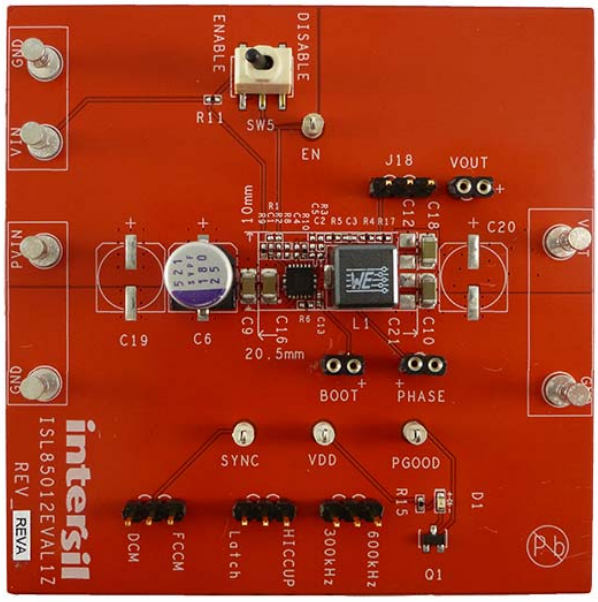

FIGURE 3. TOP VIEW

FIGURE 4. BOTTOM VIEW

ISL85012EVAL1Z Schematic

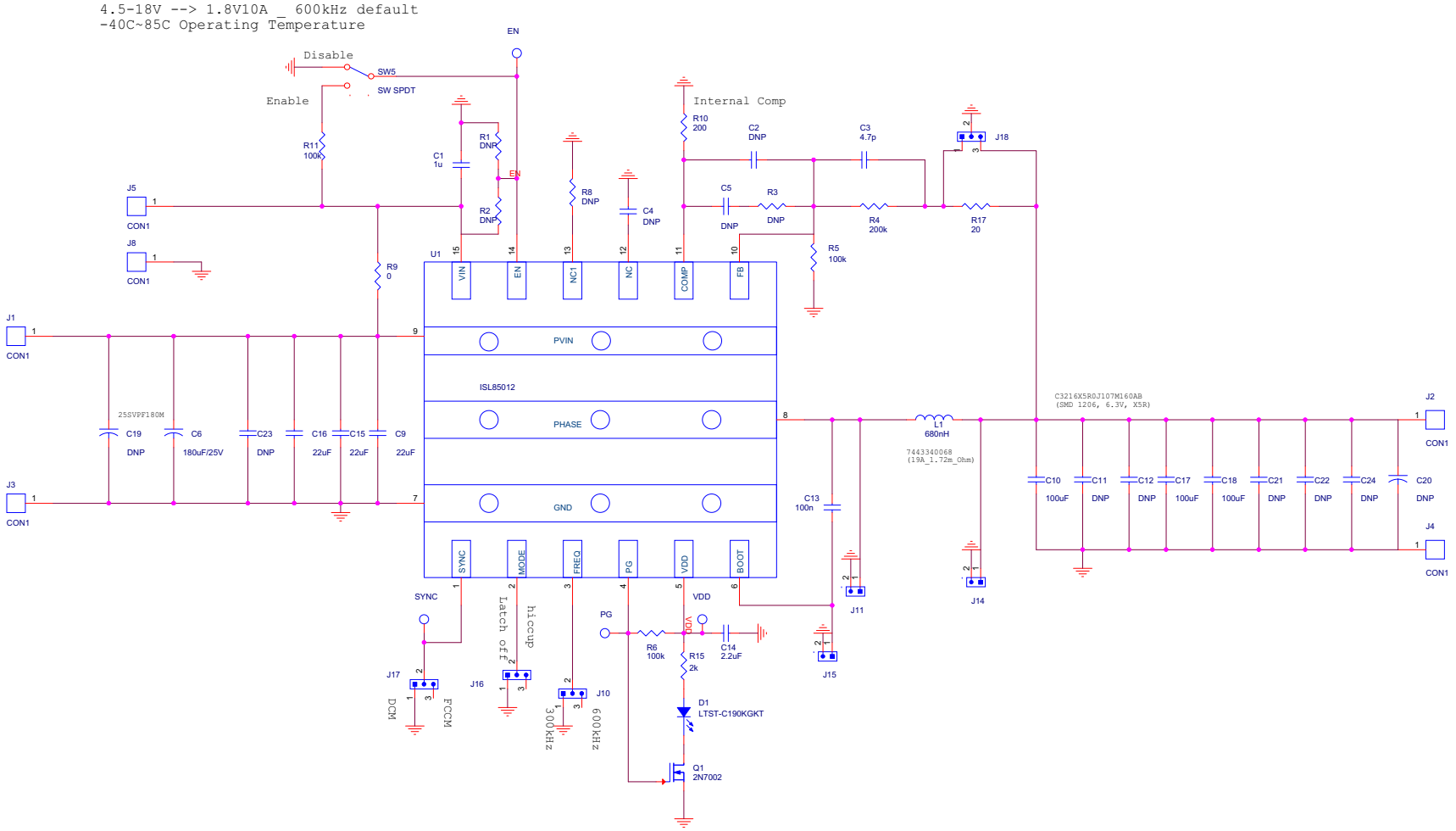

FIGURE 5. SCHEMATIC

Bill of Materials

MANUFACTURER PART	QTY	UNIT	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER
ISL85012EVAL1ZREVE01PCB	1	ea	SEE LABEL-GENERIC	PWB-PCB, ISL85012EVAL1Z, REVE01, ROHS	SHENZHEN MULTILAYER PCB TECHNOLOGY CO., LTD
25SVPF180M	1	ea	C6	CAP-OSCON, SMD, 8.3x9, 180µF, 25V, 20%, 16mΩ, ROHS	SANYO
C1005X7R1H104K	1	ea	C13	CAP, SMD, 0402, 0.1µF, 50V, 10%, X7R, ROHS	TDK
C1005X5R1E105K050BC	1	ea	C1	CAP, SMD, 0402, 1.0µF, 25V, 10%, X5R, ROHS	TDK
C1005X5R1E225K050BC	1	ea	C14	CAP, SMD, 0402, 2.2µF, 25V, 10%, X5R, ROHS	TDK
04025A4R7CAT2A	1	ea	C3	CAP, SMD, 0402, 4.7PF, 50V, 0.25pF, NPO, ROHS	AVX
	0	ea	C2, C4, C5	CAP, SMD, 0402, DNP-PLACE HOLDER, ROHS	
GRM31CR60J107ME39L	3	ea	C10, C17, C18	CAP, SMD, 1206, 100µF, 6.3V, 20%, X5R, ROHS	MURATA
GRM31CR61E226KE15L	3	ea	C9, C15, C16	CAP, SMD, 1206, 22µF, 25V, 10%, X5R, ROHS	MURATA
	0	ea	C11, C12, C21, C22, C23, C24	CAP, SMD, 1206, DNP-PLACE HOLDER, ROHS	
1514-2	6	ea	J1, J2, J3, J4, J5, J8	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE
310-43-164-41-001000	3	ea	BOOT, PHASE, VOUT	CONN-BRD-BRD, TH, 1x2, SKTSTRIP-1x64, 2.54mm, TIN, ROHS	MILL-MAX
5002	4	ea	VDD, SYNC, PGOOD, EN	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE
NRPN401PAEN-RC	4	ea	J10, J16, J17, J18	CONN-HEADER, 1x3, BRKAWY-1x40, 2mm PITCH, 3.6MATINGx2.8, GOLD, ROHS	SULLINS
LTST-C190KGKT	1	ea	D1	LED, SMD, 0603, GREEN CLEAR, 2V, 20mA, 571nm, 35mcd, ROHS	LITEON/VISHAY
7443340068	1	ea	L1	COIL-PWR CHOKE, SMD, 8.4x7.9, 0.68µH, 20%, 19A, 1.78mΩ, ROHS	WURTH ELEKTRONIK
ISL85012FRZ	1	ea	U1	IC-12A BUCK REGULATOR, 15P, TDFN, 3.5x3.5, ROHS	INTERSIL
2N7002-7-F	1	ea	Q1	TRANSISTOR, N-CHANNEL, 3LD, SOT-23, 60V, 115mA, ROHS	DIODES, INC.
ERJ2RKF20R0	1	ea	R17	RES, SMD, 0402, 20Ω, 1/16W, 1%, TF, ROHS	PANASONIC
CR0402-16W-00T	1	ea	R9	RES, SMD, 0402, 0Ω, 1/16W, 5%, TF, ROHS	VENKEL
ERJ2RKF1003	3	ea	R5, R6, R11	RES, SMD, 0402, 100K, 1/16W, 1%, TF, ROHS	PANASONIC
ERJ-2RKF2000X	1	ea	R10	RES, SMD, 0402, 200Ω, 1/16W, 1%, TF, ROHS	PANASONIC

Bill of Materials

MANUFACTURER PART	QTY	UNIT	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER
ERJ-2RKF2001	1	ea	R15	RES, SMD, 0402, 2k, 1/16W, 1%, TF, ROHS	PANASONIC
MCR01MZPF2003	1	ea	R4	RES, SMD, 0402, 200k, 1/16W, 1%, TF, ROHS	ROHM
	0	ea	R1, R2, R3, R8	RES, SMD, 0402, DNP, DNP, DNP, TF, ROHS	
GT11MSCBE	1	ea	SW5	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-NONE-ON, ROHS	ITT INDUSTRIES/C&K DIVISION
SJ-5003SPBL	4	ea	Bottom four corners w/o covering silkscreen.	BUMPONS, 0.44inW x 0.20inH, DOMETOP, BLACK	3M
212403-013	1	ea	Place assy in bag	BAG, STATIC, 5x8, ZIPLOC, ROHS	INTERSIL
	0	ea	C19, C20	DO NOT POPULATE OR PURCHASE	
LABEL-DATE CODE	1	ea	AFFIX TO BACK OF BOARD.	LABEL-DATE CODE_LINE 1: YRWK/REV#, LINE 2: BOM NAME	INTERSIL
	1	ea	RE-LABEL REV_E01 SILKSCREEN TO: REVA.	LABEL, GENERIC	

PCB Layout

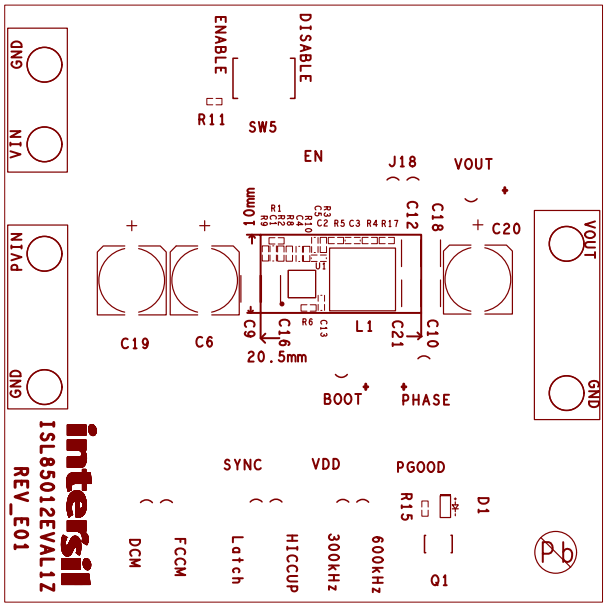

FIGURE 6. SILKSCREEN LAYER

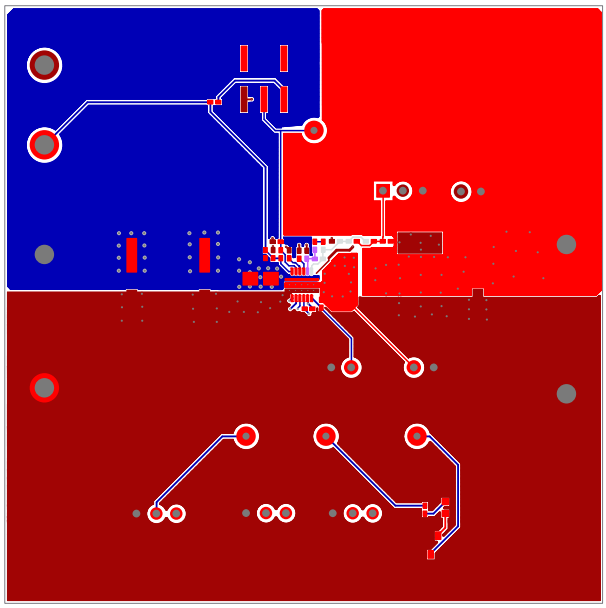

FIGURE 7. TOP LAYER

PCB Layout (Continued)

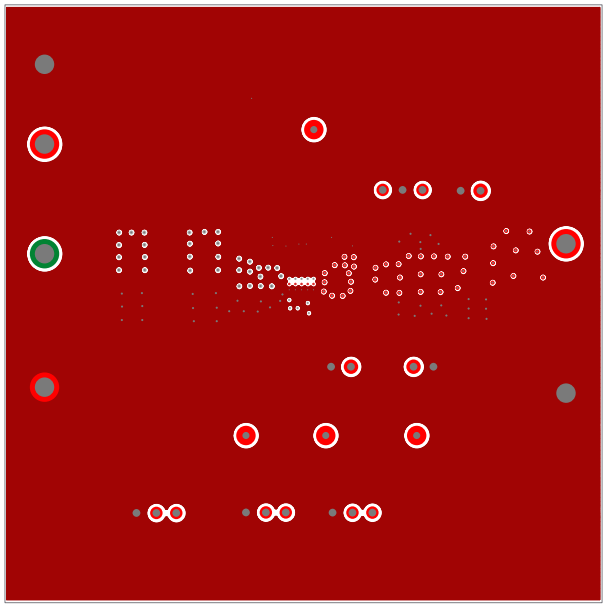

FIGURE 8. LAYER 2

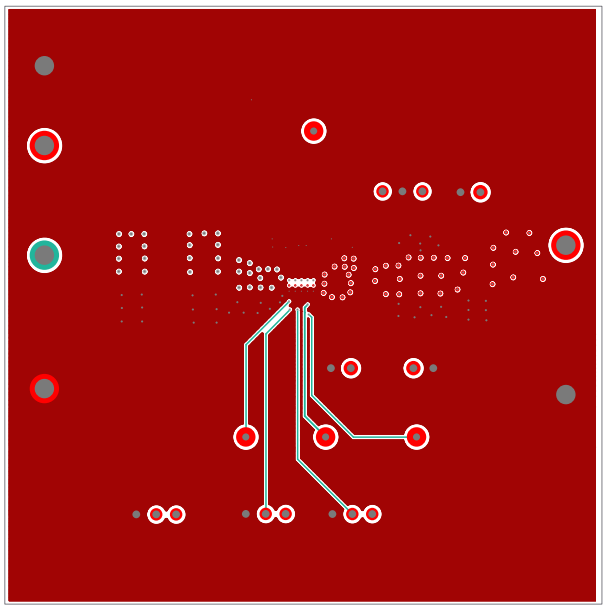

FIGURE 9. LAYER 3

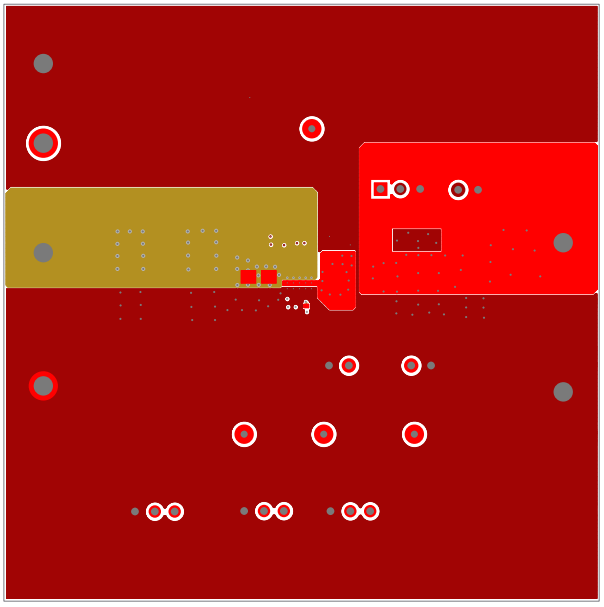

FIGURE 10. BOTTOM LAYER

Typical Performance Curves

V_{IN} = 12V, V_{OUT} = 1.8V, Frequency = 600kHz, CCM, T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = +25°C.

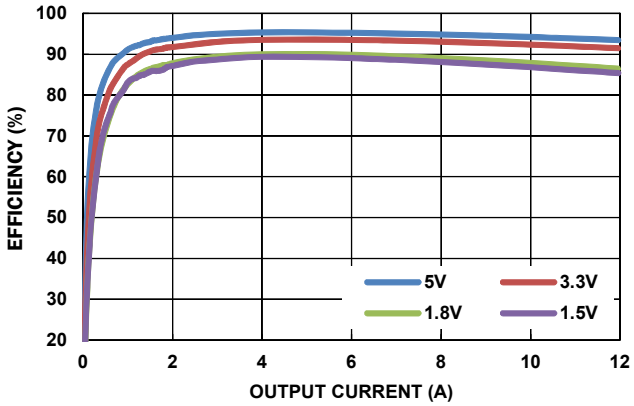

FIGURE 11. EFFICIENCY vs LOAD (V_{IN} = 12V, CCM, 600kHz)

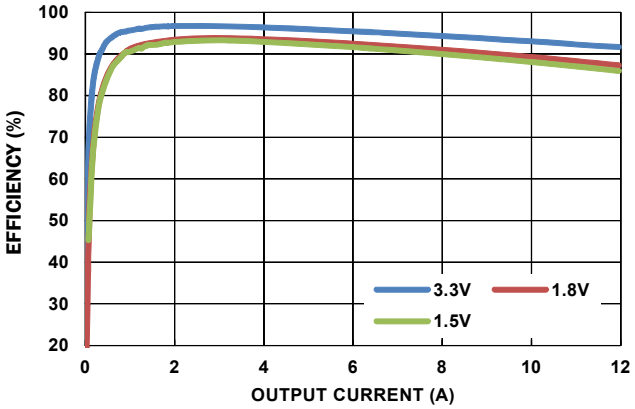

FIGURE 12. EFFICIENCY vs LOAD (V_{IN} = 5V, CCM, 600kHz)

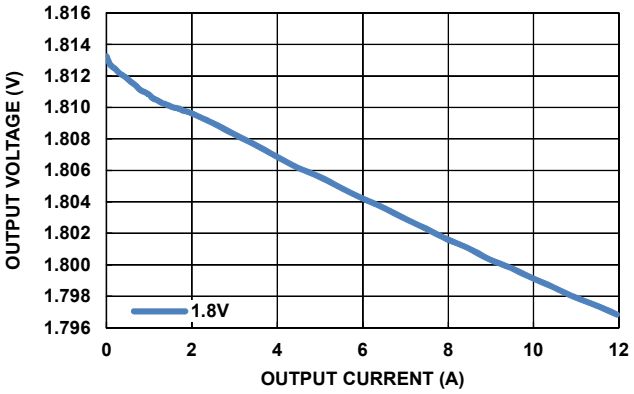

FIGURE 13. V_{OUT} REGULATION vs LOAD (V_{IN} = 12V, CCM, 600kHz)

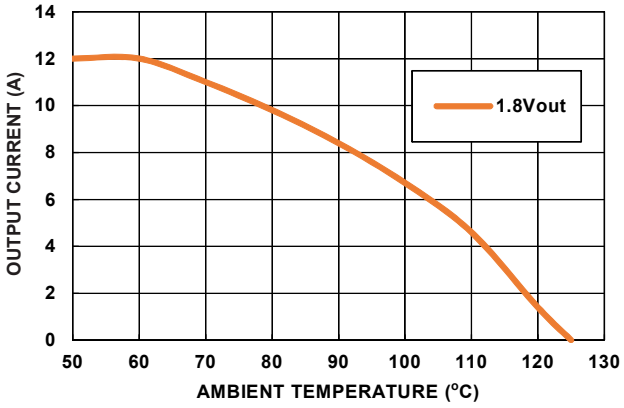

FIGURE 14. DE-RATING CURVE (NO AIRFLOW)

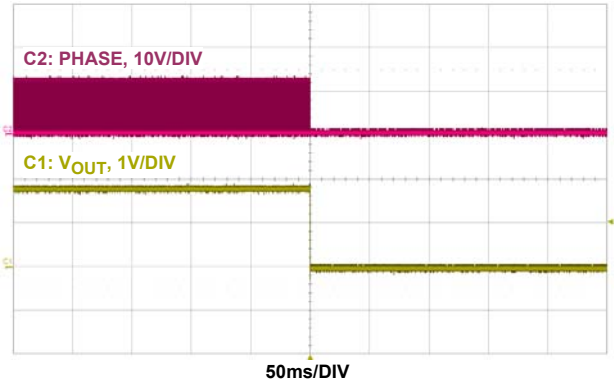

FIGURE 15. LATCH-OFF OCP (V_{IN} = 12V, V_{OUT} = 1.8V, 600kHz, CCM)

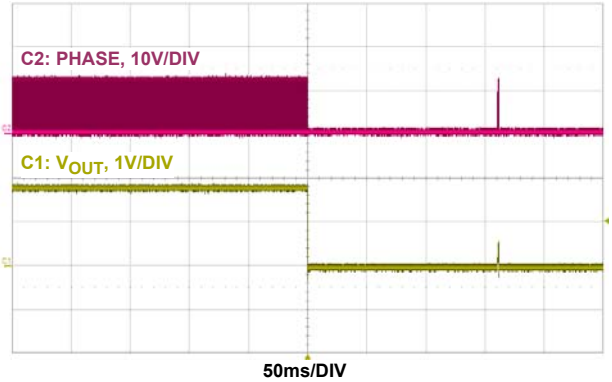

FIGURE 16. HICCUP OCP (V_{IN} = 12V, V_{OUT} = 1.8V, 600kHz, CCM)

Typical Performance Curves

V_{IN} = 12V, V_{OUT} = 1.8V, Frequency = 600kHz, CCM, T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

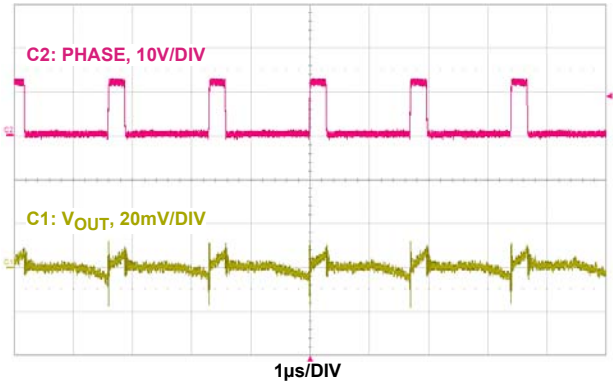

FIGURE 17. OUTPUT VOLTAGE RIPPLE (V_{IN} = 12V, V_{OUT} = 1.8V AT 12A, 600kHz, CCM)

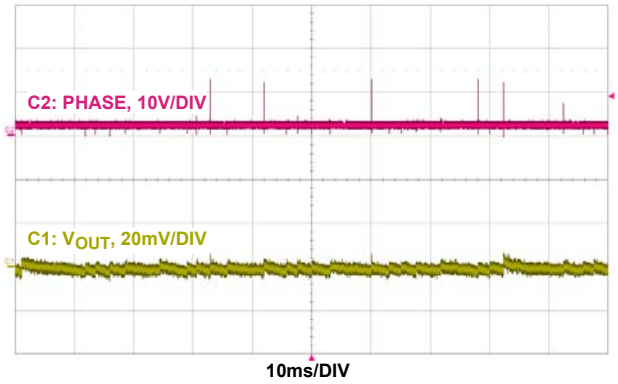

FIGURE 18. OUTPUT VOLTAGE RIPPLE (V_{IN} = 12V, V_{OUT} = 1.8V AT 0A, 600kHz, DCM)

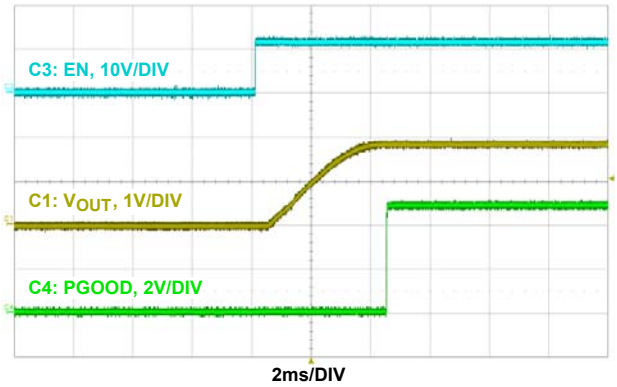

FIGURE 19. START-UP BY EN (V_{IN} = 12V, V_{OUT} = 1.8V AT 12A, 600kHz, CCM)

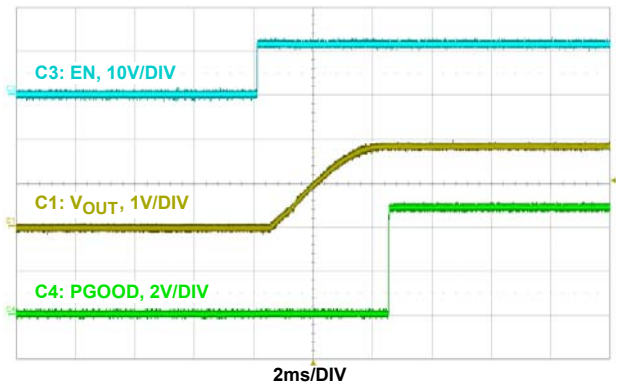

FIGURE 20. START-UP BY EN (V_{IN} = 12V, V_{OUT} = 1.8V AT 0A, 600kHz, DCM)

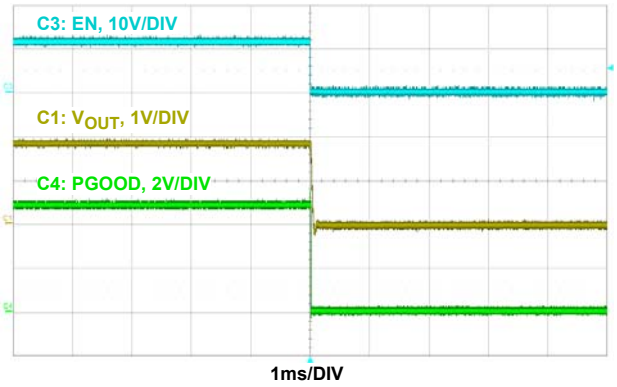

FIGURE 21. SHUTDOWN BY EN (V_{IN} = 12V, V_{OUT} = 1.8V AT 12A, 600kHz, CCM)

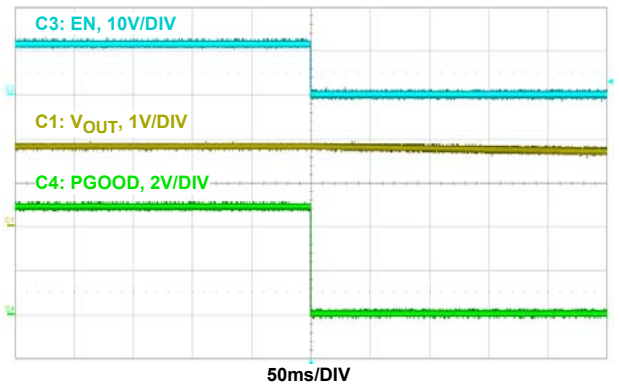

FIGURE 22. SHUTDOWN BY EN (V_{IN} = 12V, V_{OUT} = 1.8V AT 0A, 600kHz, DCM)