

ISLVERSALDEMO3Z

The ISLVERSALDEMO3Z demonstration board provides power management for the AMD Space Grade Versal ACAP AI Edge VC2302 using Renesas' Radiation Tolerant Power Management devices. The Versal ACAP system requires various supply rails, including the core, digital, analog, and DDR memory. The ISLVERSALDEMO3Z provides all these rails for the user to evaluate the performance against the Versal ACAP DC and AC electrical specifications.

Power Supply Specifications

- +12V_{DC} ±10% (Banana Jack Connectors)

Features

- Fully qualified radiation tolerant power solution
 - All power management devices are qualified to Renesas Rad Tolerant Screening and QCI Flow (R34TB0004EU)
- Designed to power AMD's Versal AI Edge Adaptive SoC, XQRVE2302
- Includes regulators for all VE2302 rails, DDR4 memory and general +5V bus
- Power supply sequencing for power up and down for increased system reliability
- All DC-DC switching converters are clock synchronized

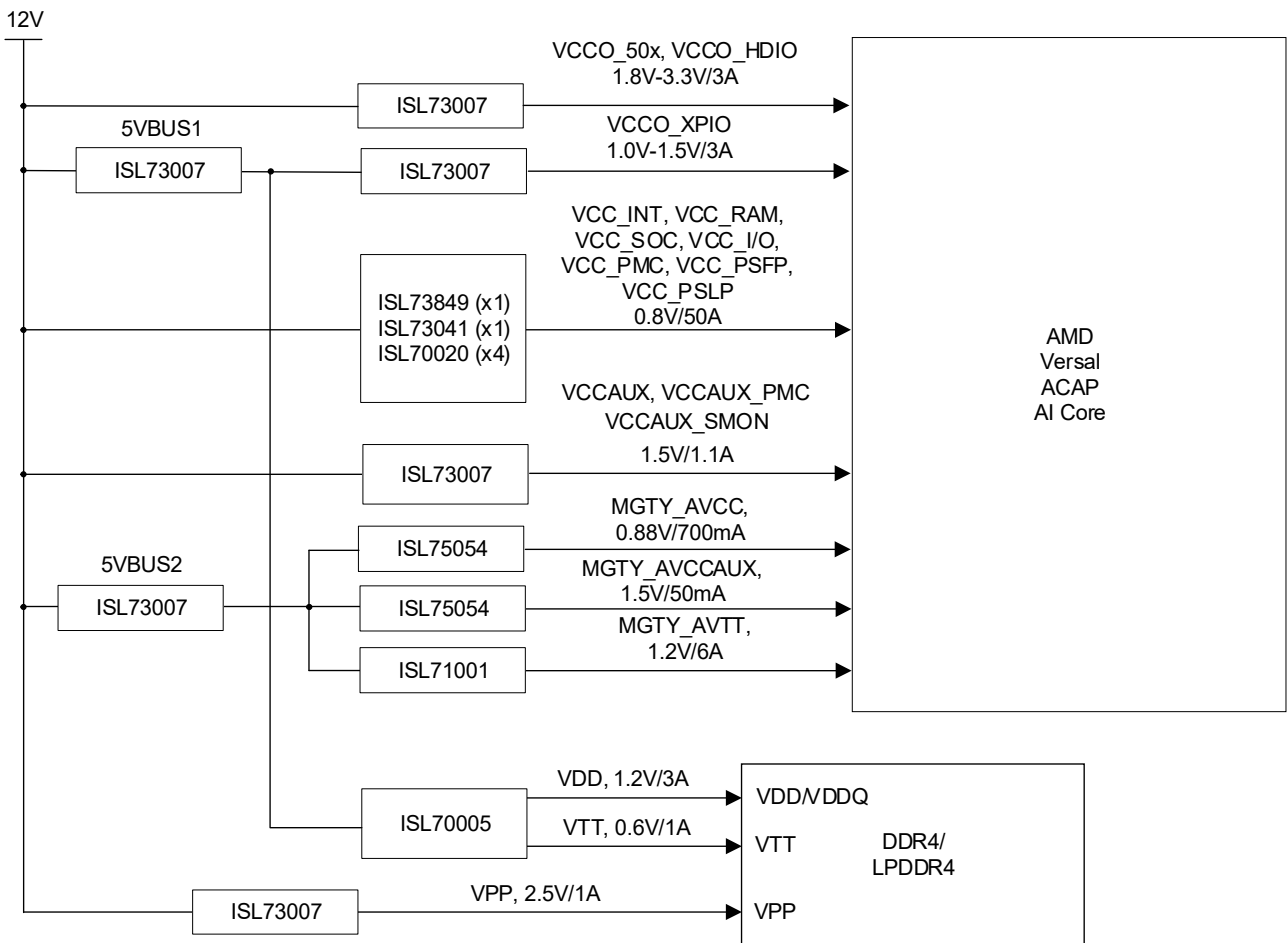


Figure 1. AMD Space Grade Versal ACAP AI Edge VC2302 Power Management Block Diagram

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1. Functional Description

1.1 Power Tree

The power tree diagram is shown in Figure 2 and the AMD Versal ACAP supply rail requirements are listed in Table 1. The power management solution is developed for the No Power Management (Minimum Rails) application of the AMD Versal ACAP, which requires individual supplies for most of the rails and a specific power sequencing.

The ISLVERSALDEMO3Z demonstration board operates on a +12V DC power supply. Two front end DC/DC regulators provide two +5.0V system rails that power all the other POL DC/DC regulators, the ISL74420 Quad Clock Fanout chips, and some minor supporting circuitry.

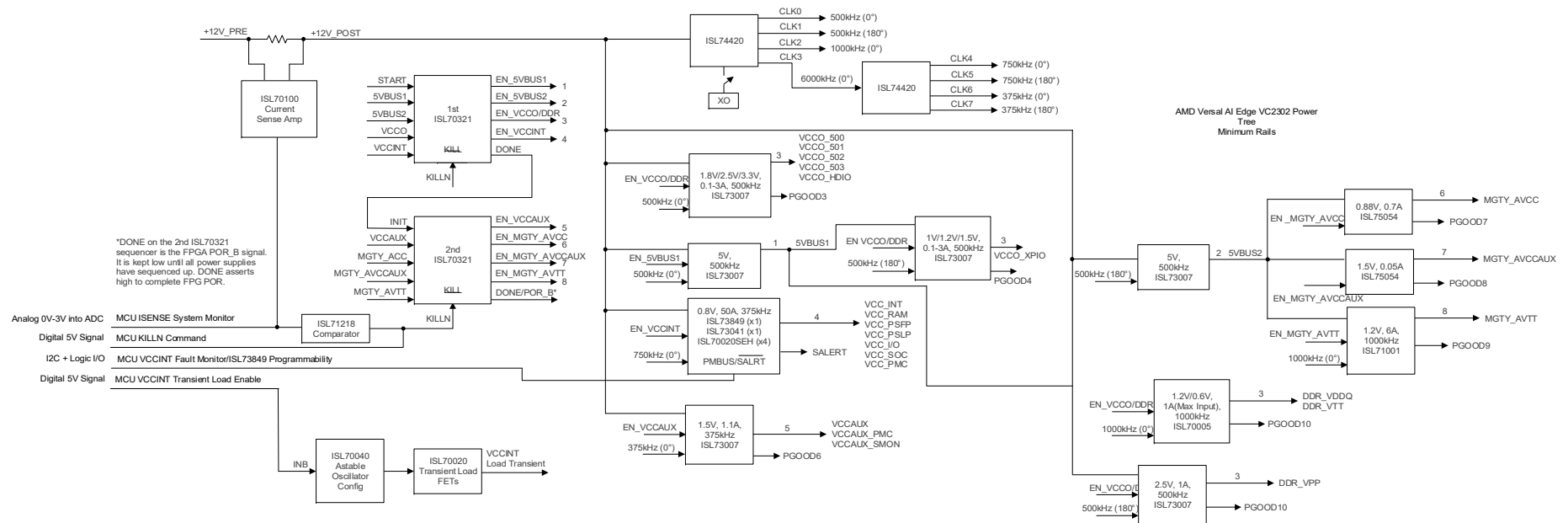


Figure 2. Renesas Radiation Tolerant Power Tree for AMD Space Grade Versal ACAP AI Edge VC2302

Table 1. AMD Space Grade Versal ACAP AI Edge VC2302 Power Management Specifications

Power Sequencing	Rail Voltage	Rail Name	Current Demand	DC Tol	AC Tol	Renesas Solution
1	5.0V	5VBUS1				ISL73007M
2	5.0V	5VBUS2				ISL73007M
3	1.8V, 2.5V or 3.3V	VCCO_500, VCCO_501, VCCO_502, VCCO_503, VCCO_HDIO	3A	±1%	+3%/-5% for 3.3V, ±5% otherwise	ISL73007M
	1.0V to 1.5V	VCCO_XPIO	3A	±1%	±5%	ISL73007M
	1.2V/0.6V	DDR_VDDQ, DDR_VTT	3A/1A	±5%	±5%	ISL70005SEH
	2.5V	DDR_VPP	1A	±5%	±5%	ISL73007M
4	0.8V	VCCINT, VCC_RAM, VCC_SOC, VCC_I/O, VCC_PMC, VCC_PSLP, VCC_PFSF	40A	±1%	±17mV	(1) ISL73849M + (1) ISL71441M + (4) ISL70020
5	1.5V	VCCAUX, VCCAUX_SMON, VCCAUX_PMC	3A	±1%	±2%	ISL73007M
6	0.88	MGTY_AVCC	0.7A	±2%	10mVpp	ISL75054M
7	1.5V	MVGTY_AVCCAUX	0.05A	±2%	10mVpp	ISL75054M
8	1.2V	MVGTY_AVTT	6A	±2%	10mVpp	ISL71001M

1.2 Renesas Power Management Solution

The most prominent power supply rail for the AMD Versal ACAP is the VCC_INT core rail, which consumes up to 40A while delivering 0.8V. This is provided by the Renesas Radiation Tolerant Point-of-Load Regulator that consists of: (1) ISL73849M PWM Controller, (1) ISL71441M GaN FET Driver, and a ISL70020SEH 40V, 65A, 3.5mΩ GaN FET in a die bump package.

The other digital and analog rails for the Versal ACAP are provided by the ISL73007M and ISL71001M Integrated FET Synchronous Buck Regulators, and ISL75054M Ultra Low-Noise LDO. The DDR4 memory VDD and VTT rails external to the Versal ACAP is powered with the ISL70005SEH Synchronous Buck Regulator + Source/Sink LDO and the ISL73007M.

The power sequencing, which is critical for the No Power Management operation of the AMD Versal ACAP, is handled by two ISL70321SEH quad sequencers. [Table 2](#) shows the full list of Renesas radiation tolerant power management parts used in the ISLVERSALDEMO3Z.

Table 2. Renesas Radiation Tolerant Parts used on ISLVERSALDEMO3Z

Device Name	Description	Used For
ISL73849M	12V PWM Dual-Phase Controller with PMBus	0.8V VCC_INT Core Rail
ISL71441M	12V GaN Half-Bridge Driver	
ISL70020SEH	40V, 65A, 3.5mΩ GaN FET (bump die)	
ISL70001ASEH	5V, 6A Integrated FET Synchronous Buck	VCC Aux Rail
ISL73007M	12V, 3A Integrated FET Synchronous Buck	Various Digital and Analog Rails, DDR4 Memory Supply Rail, 5V System Rails
ISL75054M	12V, 1A Ultra Low-Noise LDO	Analog Rails
ISL70005SEH	5V, 3A Synchronous Buck + 1A Source and Sink LDO	DDR4 Memory Supply Rails
ISL70321SEH	Quad Channel Supply Sequencer	Supply Rail Sequencing and Monitoring
ISL71218M	Dual 36V Precision Rail-to-Rail Output Operational Amplifier	Buffer for DDR VREF

1.3 Adjustable Output Voltages

The AMD Versal ACAP specifies different operating voltage on certain digital rails; for example, the VCCO_XPIO and VCCO_50x rails can be set for different digital logic I/O levels required by the user. The ISLVERSALDEMO3Z includes the necessary jumpers to change the feedback resistors to set the different output voltage.

The VCCO_50x rail can be adjusted for 1.8V, 2.5V, or 3.3V. See [Table 3](#).

Table 3. VCCO_50x Adjustments

V _{OUT} (V)	Jumper Status
1.8	Both JP201 and J202 open
2.5	Jumper JP201
3.3	Jumper JP202

The VCCO_XPIO rail can be adjusted for 1.0V, 1.2V, or 1.5V. See [Table 4](#).

Table 4. VCCO_XPIO Adjustments

V _{OUT} (V)	Jumper Status
1.0	Both JP251 and JP252 Open
1.2	Jumper JP251
1.5	Jumper JP252

1.4 Output Voltage Monitor Test Points and Load Transient Generators

The ISLVERSALDEMO3Z provides test points for monitoring the output voltage and terminals to apply an external load current. Most output rails also provide an on-board transient load step generator. The on-board transient load generator can be turned on by an on-board switch (SW) to automatically generate load steps. The load transient generator is enabled or disabled with the switch. The load transient generator circuit has a jumper test-point so that the user can connect an external pulse generator to override the disabled state to generate load steps with custom duty cycles. [Table 5](#) summarizes output rail monitoring, test points, and load transient generator input control for the supply rails.

Table 5. Output Rail Test Points and Transient Load Control Input Connection

ISLVERSALDEMO3Z Rail Name	Oscilloscope VOUT Test Point (2pin jumper)	VOUT DC Test Point/External Load Access (VOUT/GND)	Transient Load Generator Control (SW/JP)
ISL73007_5VBUS1	TP651	J651/J652	
ISL73007_5VBUS2	TP701	J701/J702	
ISL73007_VCCO_50X_HDIO	TP201	J201/J202	SW201/JP203
ISL73007_VCCO_XPIO	TP251	J251/J252	SW251/JP253
ISL73005_DDR_VDD	TP501	J503/J504	
ISL73005_DDR_VTT	TP502	J501/J506	
ISL73006_DDR_VPP	TP502	J551/J552	
ISL73849_VCCINT	TP1	TERM1/TERM2	SW1/JP1
ISL73007_VCCAUX	TP301	J301/J302	SW301/JP301
ISL75054_MGTY_AVCC	TP401	J401/J402	SW401/JP401
ISL75054_MGTY_AVCCAUX	TP351	J351/J352	SW351/JP351
ISL71001_MGTY_AVTT	TP451	J451/J452	SW451/JP451

The transient load generator comprises a FET driver controlling a common source NFET that pulls a load resistor to GND to provide a transient load to the supply rail. The ISL73849_VCCINT 0.8V core rail uses an ISL71040MRTZ GaN FET driver, while all other load generators use the HIP2211 half-bridge driver. There are switches (SW) throughout that can enable or disable the transient load generator circuit for a specific rail. When the switch is in the up direction, the generator is enabled. When the transient load generator is enabled, supporting circuitry automatically generates ~500µs load step pulses in ~5ms periods. *Note:* the ISL73849_VCCINT transient load generator requires an additional 0V to 5V control signal to enable the load step (VCCINT_LOAD_ENB). The circuit generates ~300µs load step pulses in ~3ms pulses.

When the switch is in the down direction, a 10kΩ pull-down to ground disables the load generator circuit. A jumper test-point is in parallel with the 10kΩ, which allows connecting an external pulse generator. A 0V to 5V logic control signal can switch the transient load where 0V turns the load off, and 5V turns the load on.

The automatically generated load step pulses and period can also be altered by changing two resistors and a capacitor. Use [Equation 1](#) to set the ON-time and [Equation 2](#) to set the OFF-time. For HIP2211, the V_{IH} is 2.08V typical and the V_{IL} is 1.22V typical. For the ISL71040M the V_{IH} is 1.7V typical and the V_{IL} is 1.4V typical. By default, for all the HIP2211 load transient circuits R_{ON} is 124Ω, R_{OFF} is 7.15kΩ, and C is 10µF. By default, for the ISL71040M load transient circuit R_{ON} is 261Ω, R_{OFF} is 17.4kΩ, and C is 10µF. [Table 7](#) shows which resistors and capacitor correspond to each load transient generator circuits for [Equation 1](#) and [Equation 2](#).

$$(EQ. 1) \quad R_{ON} = \frac{t_{ON}}{-C \times \ln\left(\frac{V_{IL}}{V_{IH}}\right)}$$

where:

- R_{ON} is the active ON-time resistor.
- t_{ON} is the required active ON-time.
- C is the active ON-charge and active OFF-discharge capacitor.
- V_{IH} is FET driver input high level voltage.
- V_{IL} is the FET driver input low-level voltage.

$$(EQ. 2) \quad R_{OFF} = \frac{t_{OFF}}{-C \times \ln\left(\frac{V_{IH} - 12V}{V_{IL} - 12V}\right)} - R_{ON}$$

where:

- R_{OFF} is the active OFF-time resistor.
- t_{ON} is the required active OFF-time.
- C is the active ON-charge and active OFF-discharge capacitor.
- V_{IH} is FET driver input high-level voltage.
- V_{IL} is the FET driver input low-level voltage.

Table 6. Switching Converter Clock Synchronization

ISLVERSALDEMO3Z Rail Name	Clock Node Name	Frequency, Phase
ISL73007_5VBUS1	500kHz_CLK0	500kHz, 0°
ISL73007_5VBUS2	500kHz_CLK1	500kHz, 180°
ISL73007_VCCO_50X_HDIO	500kHz_CLK0	500kHz, 0°
ISL73007_VCCO_XPIO	500kHz_CLK1	500kHz, 180°
ISL73849_VCCINT	750kHz_CLK4	750kHz, 0°
ISL73007_VCCAUX	375kHz_CLK7	375kHz, 0°
ISL71001_MGTY_AVTT	1000kHz_CLK2	1000kHz
ISL70005_DDR_VDD	1000kHz_CLK2	1000kHz
ISL73007_DDR_VPP	500kHz_CLK1	500kHz, 180°

Table 7. Load Transient t_{ON} and t_{OFF} Resistors and Capacitor

ISLVERSALDEMO3Z Rail Name	R_{ON}	R_{OFF}	C
ISL73007_VCCO_50X_HDIO	R217	R216	C214
ISL73007_VCCO_XPIO	R267	R266	C264
ISL73849_VCCINT	R34	R33	C137
ISL73007_VCCAUX	R314	R313	C316
ISL75054_MGTY_AVCC	R411	R410	C412
ISL75054_MGTY_AVCCAUX	R362	R361	C362
ISL71001_MGTY_AVTT	R465	R465	C483

Figure 3 through Figure 8 show the input connection to all the transient load generator controls on the ISLVERSALDEMO3Z. The load comprises multiple parallel 2W-rated, 2512-sized resistors. *Note:* The ISL75054_MGTY_AVCCAUX uses a single 1/8W-rated, 0805-sized resistor.

The transient load generator is intended for pulse load operation only where the frequency and duty cycle of the load do not exceed the power dissipation of the resistors.

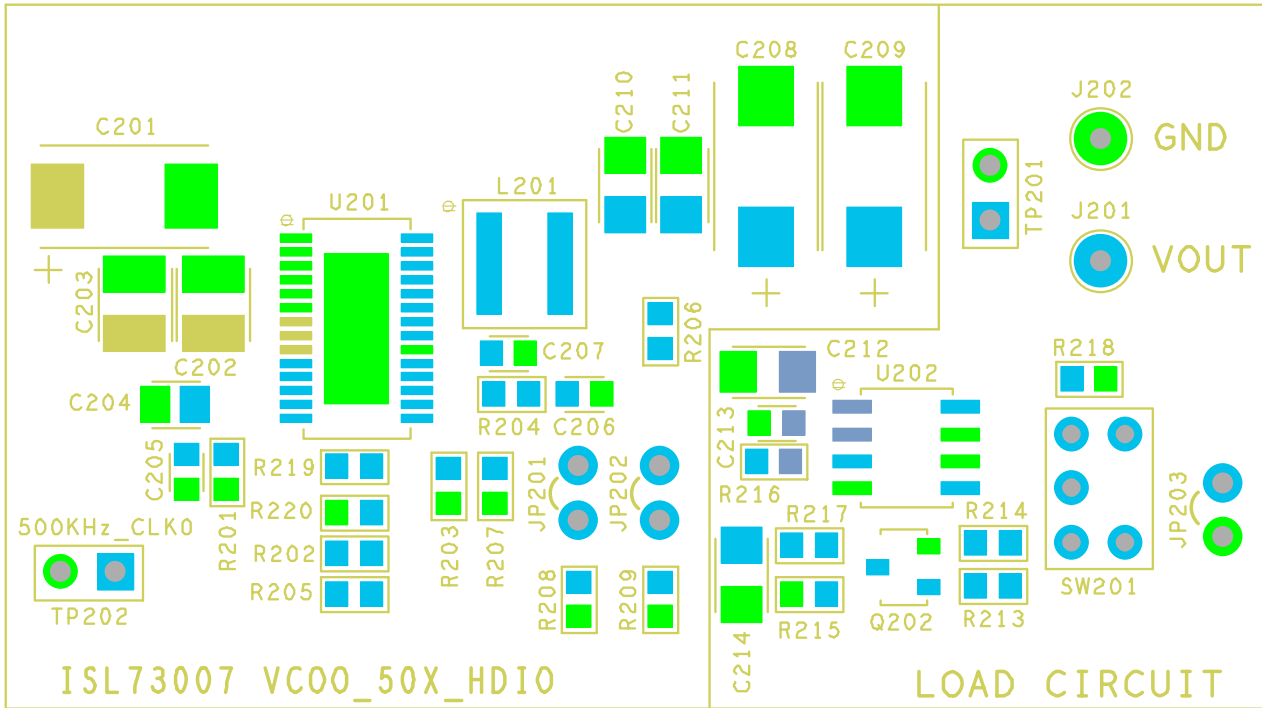


Figure 3. ISL73007_VCCO_50X_HDIO Load Generator Input Orientation

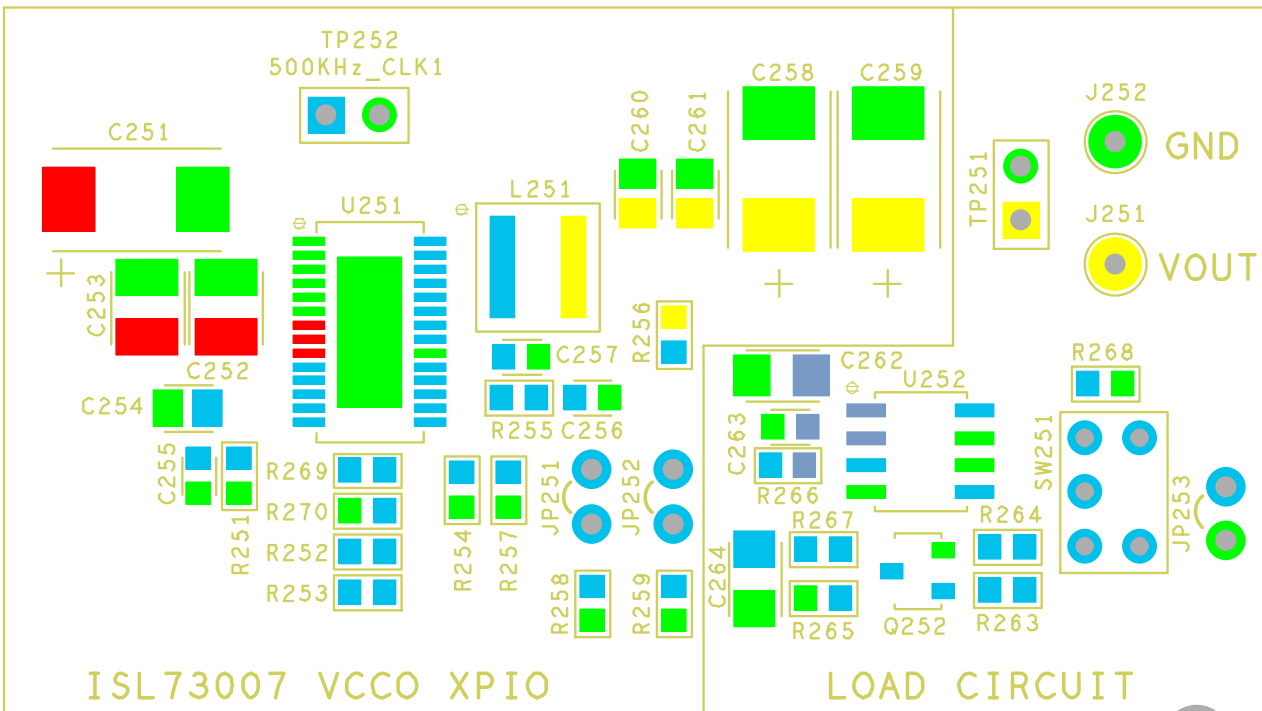


Figure 4. ISL73007_VCCO_XPIO Load Generator Input Orientation

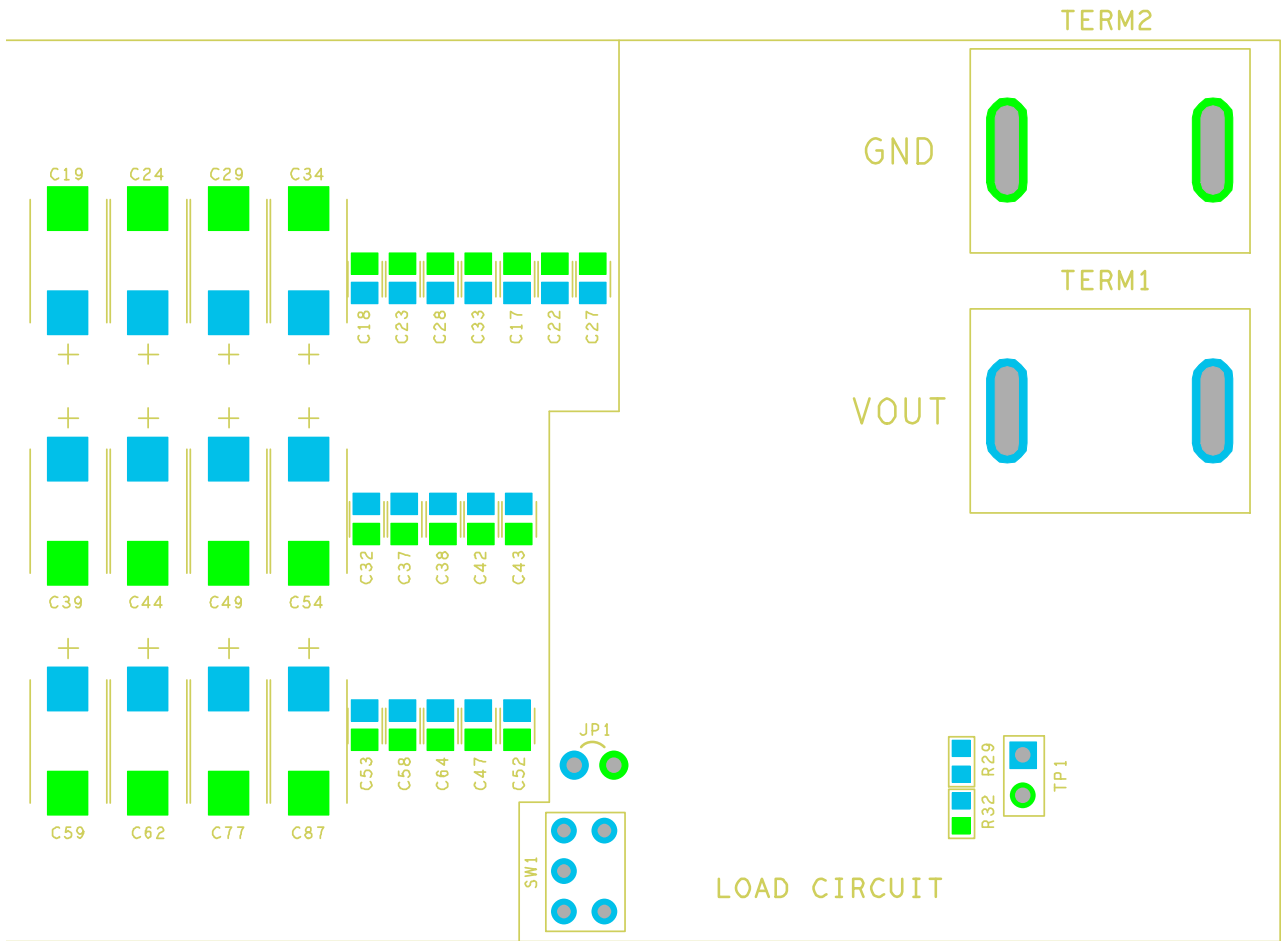


Figure 5. ISL73849_VCCINT Load Generator Input Orientation

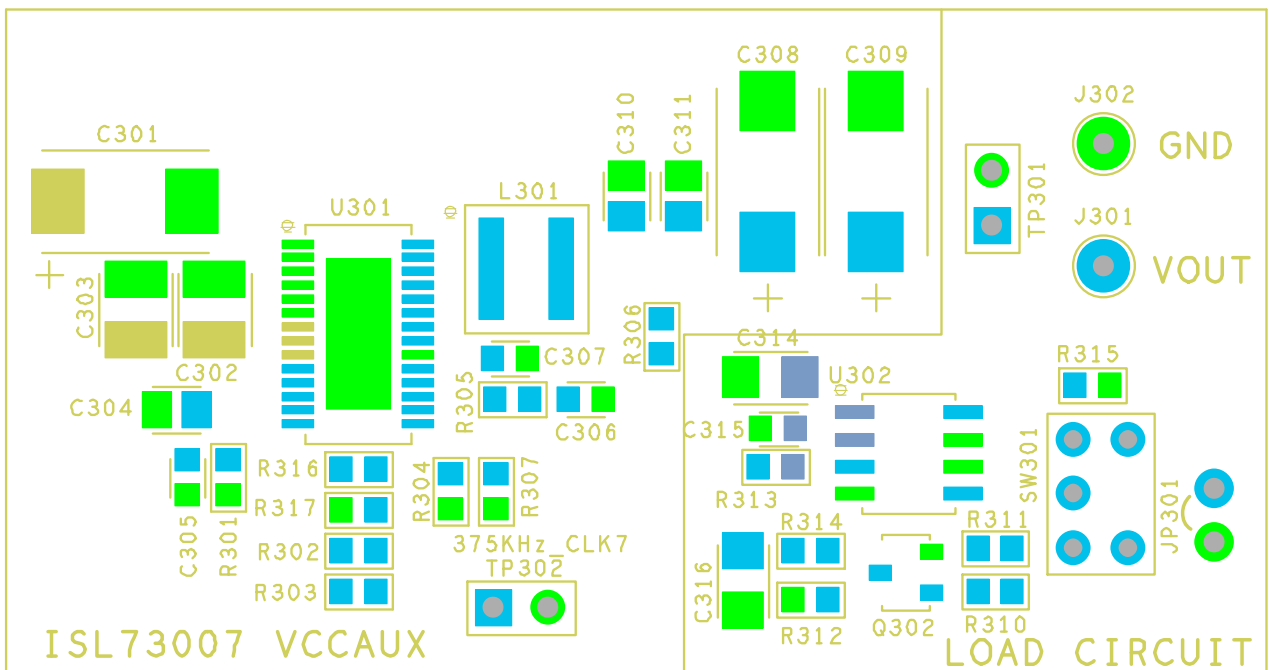


Figure 6. ISL73007_VCCAUX Load Generator Input Orientation

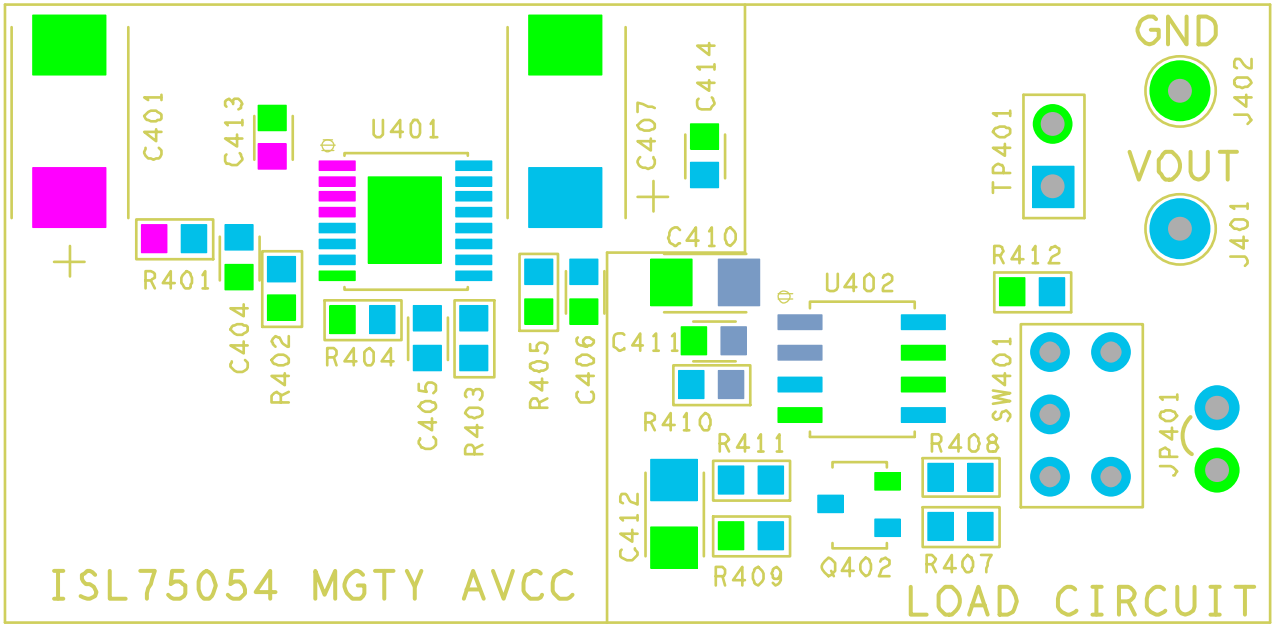


Figure 7. ISL75054_MGTY_AVCC Load Generator Input Orientation

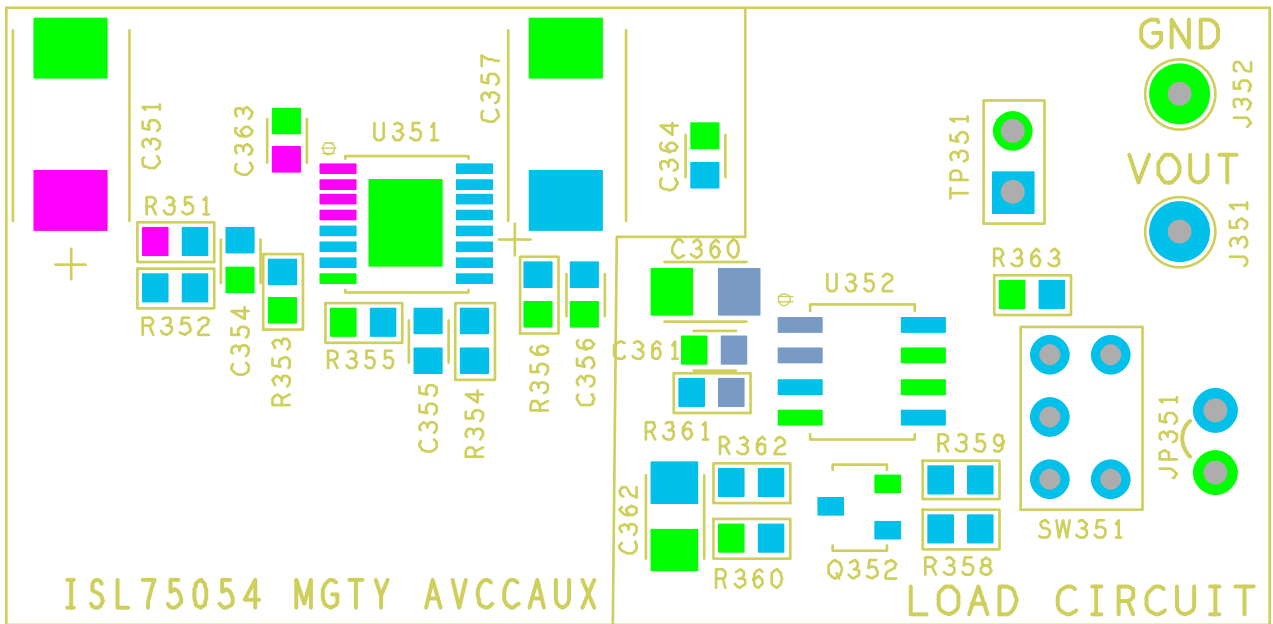


Figure 8. ISL75054_MGTY_AVCCAUX Load Generator Input Orientation

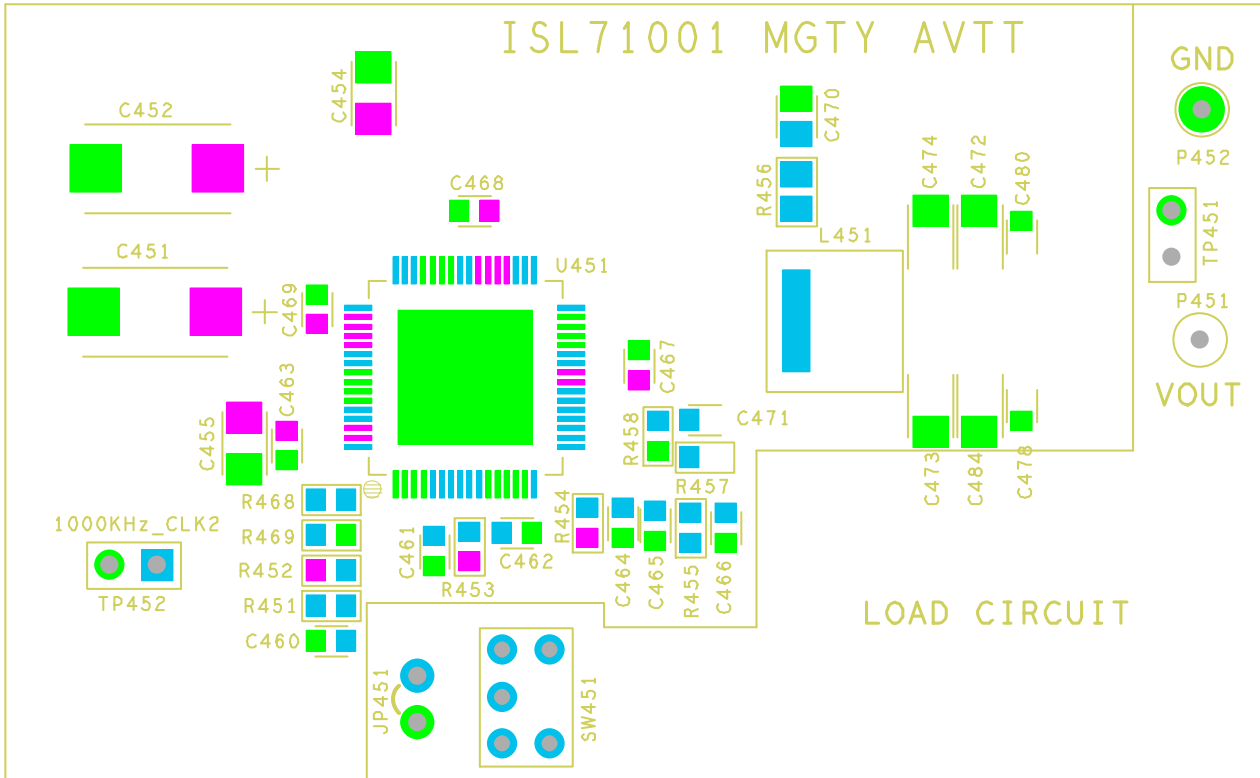


Figure 9. ISL71001_MGTY_AVTT Load Generator Input Orientation

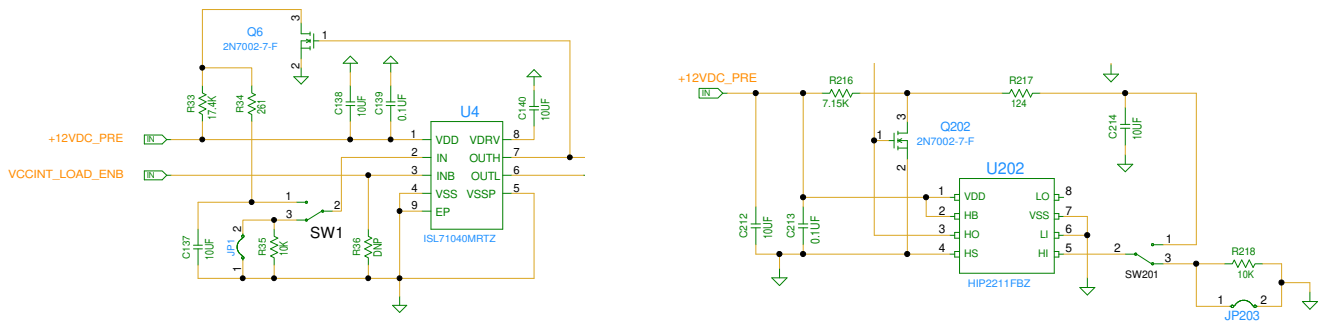


Figure 10. Schematic of Transient Load Generator FET Drivers

1.5 0.8V/40A Core Rail Design

The 0.8V/40A VCC_INT core rail is delivered by the discrete design of one ISL73849M PWM Controller, one ISL71441M GaN FET Driver, and four ISL70020SEH 40V GaN FETs in the bump die package. Each PWM Controller is a dual-phase IC but only one phase is being used for the ISLVERSALDEMO3Z to eliminate an extra GaN FET and GaN FET-based half-bridge and reduce the overall footprint of the VCC_INT rail.

1.6 Power Sequence and Monitoring

The two ISL70321SEH quad rail sequencers handle the power sequencing and monitoring of all supply rails. When a sequence up or down is initiated, the supply rails are enabled or disabled in a sequence, shown in Figure 11 and Figure 12.

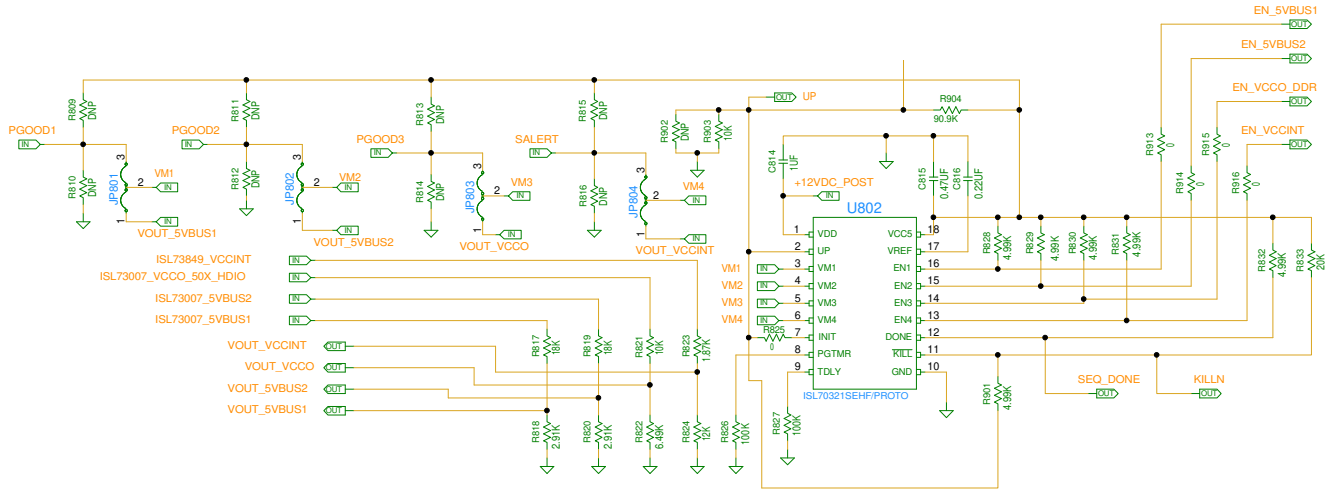


Figure 11. Power Sequencer 1 DONE signal for Versal POR_B Control

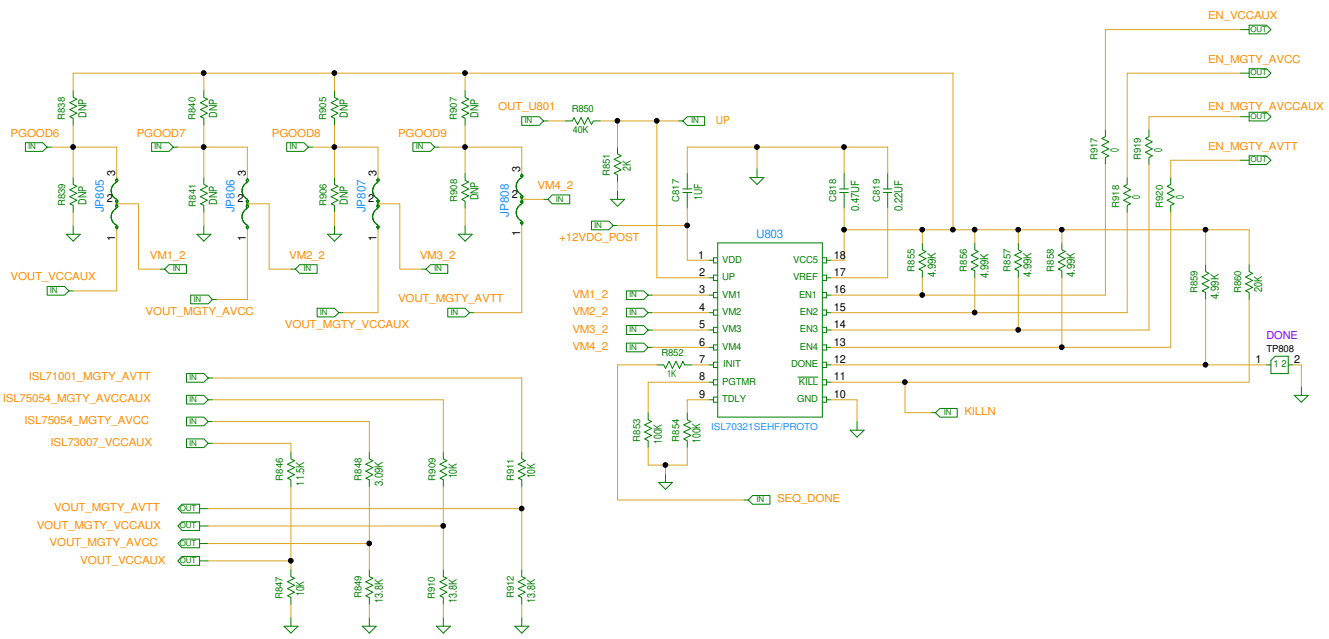


Figure 12. Power Sequencer 2 DONE signal for Versal POR_B Control

U803, the second sequencer's DONE pin, signifies the completion of the entire power-up sequence. As described in the AMD Power Estimator (XPE) design tool for the Versal ACAP, the POR_B signal for the ACAP must be asserted low during the power-up of the PMC domains. After the PMC domains have powered up, the POR_B signal must be asserted high to complete the Power-On Reset (POR). Therefore, the DONE signal of the second sequencer can be used for the POR_B of the Versal ACAP. Access to the DONE signal is provided on TP808.

1.7 Power LED Indicators

LED indicators are provided for visual detection of when certain rails have powered up. The 12V LED is always on when +12V power is applied to the board. All other LEDs are on when the PGOOD signal for that rail pulls high.

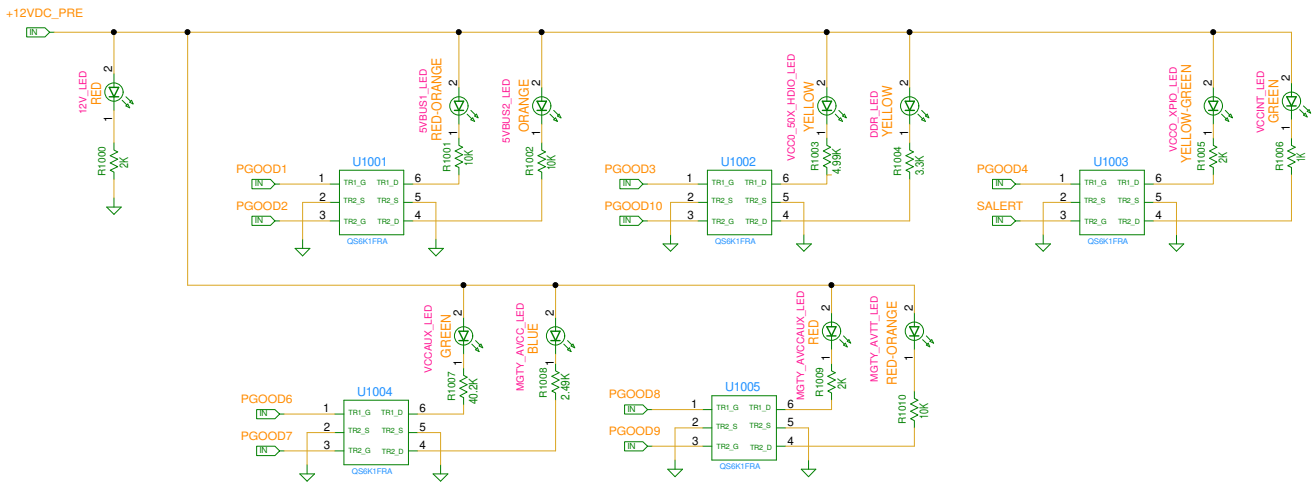


Figure 13. Power LED Indicator

1.8 12V Power Supply and Sequencing Initialization

The +12VDC power supply to the ISLVERSALDEMO3Z is provided by banana jack inputs to the board. Back-to-back PMOS FETs prevent reverse current flow back to the power supply. Mechanical switch SW801 turns the power on and off for the board.

Power sequence initialization is provided by push button switch SW802 and the CD4027B JK flip flop. Pushing the button switch provides one pulse, which latches the JK flip flop high and low, alternatively with every push. The main power switch SW801 also controls the RESET pin of the JK flip flop. When the power switch is thrown off, the RESET signal triggers a power-down sequence of the two ISL70321SEH sequencers instead of an uncontrolled shutdown of the power rails. At the same time, a large RC time constant to the gate of Q602 PMOS delays the turn-off of the 12V supply to the board for the power-down sequence to complete.

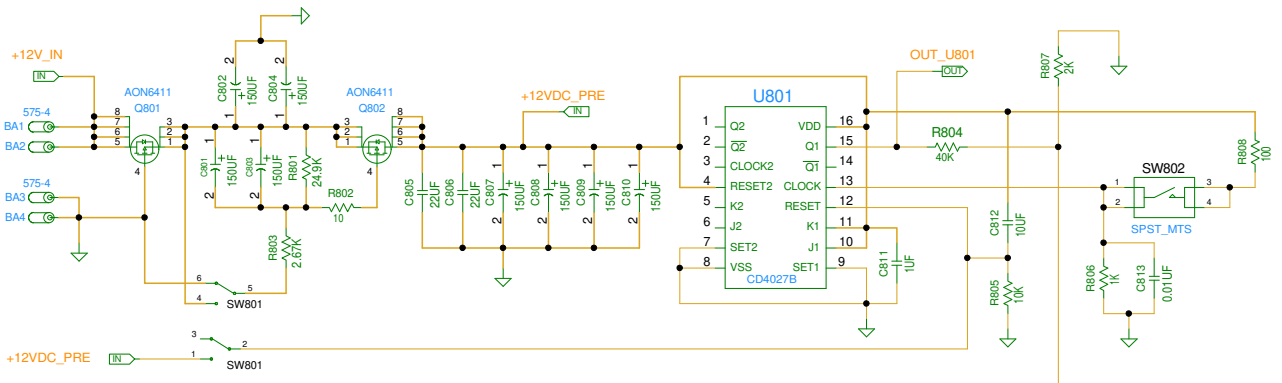


Figure 14. Power Sequence Initialization Circuit

The VCCO_XPIO_LED stays on for the longest duration during a power-off sequence. This happens because the previous rail being sequenced down that the ISL70321SEH monitors is the ISL73849_VCCINT rail, which has an extremely large output capacitance that is slowly discharged. Until the sensed voltage on ISL73849_VCCINT falls below the 600mV internal reference, the sequencer does not power down the next rail, which is driven by the EN_VCCO_DDR signal and its PGOOD4 signal is driving the VCCO_XPIO_LED.

1.9 Switching Converter Clock Synchronization

All the DC/DC converters on the ISLVERSALDEMO3Z are clock synchronized with two ISL74420s configured as a Clock controller and Clock target. The circuit generates 0V to 5V clocks at various frequencies and phases to the different rails. U601 is the Clock controller and generates two 500kHz clocks 180° out-of-phase with each other, one 1MHz clock and one 6MHz clock. The 6MHz clock is used as the oscillator of the U602 Clock target, which divides the 6MHz clock down to generate two 750kHz clocks 180° out-of-phase with each other, and two 375kHz clocks 180° out-of-phase with each other. Table 8 lists the clocks and the associated Renesas DC/DC converters.

Table 8. Switching Converter Clock Synchronization

ISLVERSALDEMO3Z Rail Name	Clock Node Name	Frequency, Phase
ISL73007_5VBUS1	500kHz_CLK0	500kHz, 0°
ISL73007_5VBUS2	500kHz_CLK1	500kHz, 180°
ISL73007_VCCO_50X_HDIO	500kHz_CLK0	500kHz, 0°
ISL73007_VCCO_XPIO	500kHz_CLK1	500kHz, 180°
ISL73849_VCCINT	750kHz_CLK4	750kHz, 0°
ISL73007_VCCAUX	375kHz_CLK7	375kHz, 0°
ISL71001_MGTY_AVTT	1000kHz_CLK2	1000kHz
ISL70005_DDR_VDD	1000kHz_CLK2	1000kHz
ISL73007_DDR_VPP	500kHz_CLK1	500kHz, 180°

The U601 clock controller needs a 48MHz oscillator. This clock is generated automatically internally on the chip, but it can also be provided by an external oscillator. To demonstrate this, a 48MHz crystal oscillator is included in the circuit with an enable/disable switch (SW601). When the switch is in the up direction, the external oscillator feeds U601. When the switch is in the down direction, the external oscillator is disabled and U601 relies on its internal 48MHz clock.

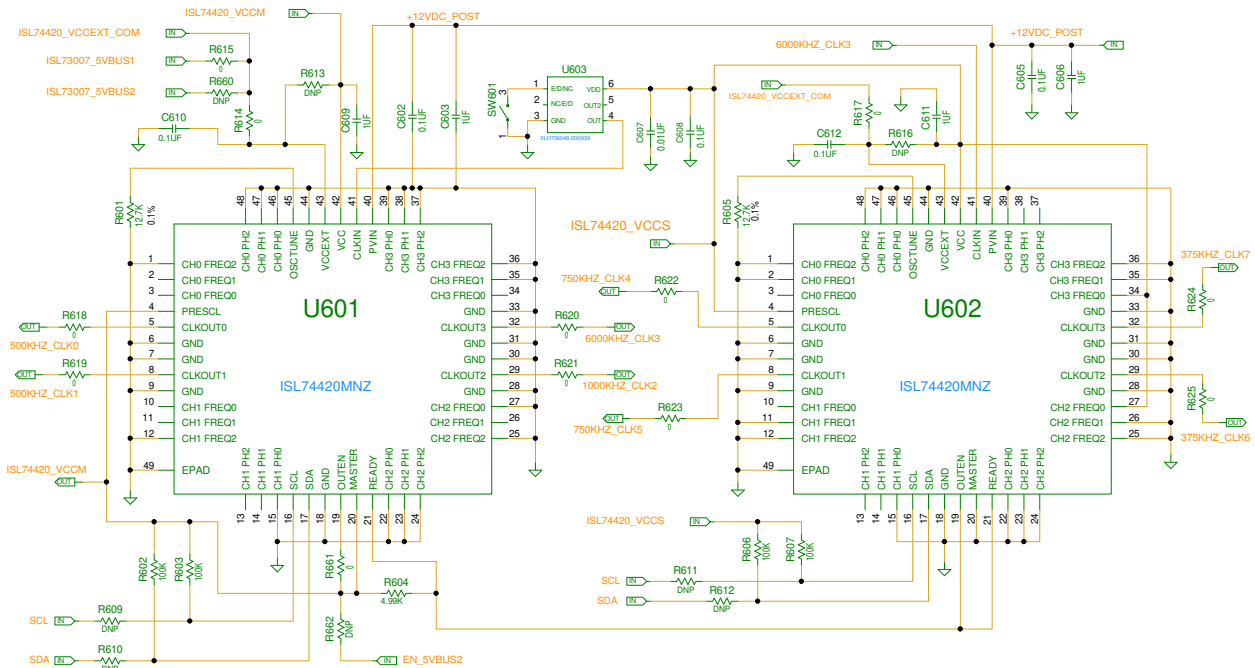


Figure 15. ISL74420 Octal Clock Circuit

1.10 +12V Bus Current Sensing and KILL Comparator

The total +12V bus supply current to the Versal rails can be monitored as a voltage (ADC_ISENSE) through the ISL70100 current-sense amplifier. The circuit converts 0A to 25A to an output voltage of 0V to 2.25V. The output voltage range can be easily scaled by adjusting the output load resistor R953 using [Equation 3](#).

$$(EQ. 3) \quad R_{OUT} = \frac{V_{OUT(MAX)}}{300\mu A}$$

where:

- R_{OUT} is the output load scaling resistor in ohms.
- V_{OUT} is the required maximum output voltage in volts.

Use [Equation 4](#) to convert the ADC_ISENSE output voltage to +12V bus supply current.

$$(EQ. 4) \quad I_{SENSE} = \frac{ADC_{ISENSE}}{R_{SENSE} \times R_{OUT} \times 0.002A/V}$$

where:

- * I_{SENSE} is the 12V bus supply current in amps.
- * R_{SENSE} is the 12V bus current sense resistance in ohms.
- * R_{OUT} is the output load scaling resistor in ohms from [Equation 3](#).

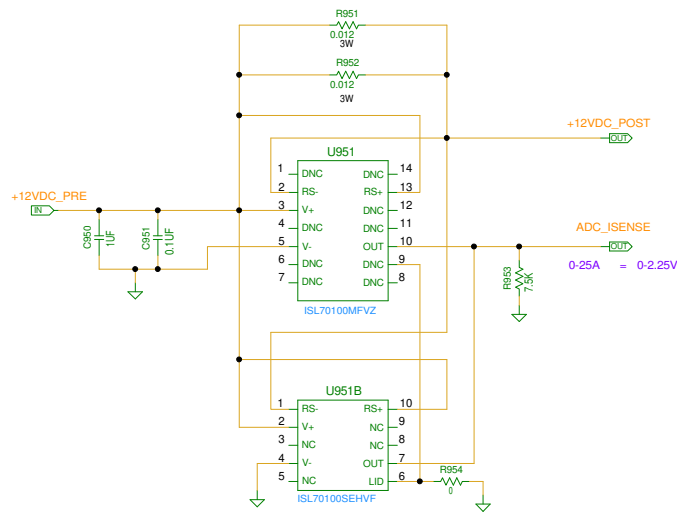


Figure 16. ISL70100 Current-Sense Amplifier

ADC_ISENSE goes to the ISL71218 comparator, which disables all the power outputs simultaneously by pulling the KILL pins low on the ISL70321 power sequencers. KILL is pulled low by the comparator when ADC_ISENSE is greater or equal to 2.02V (VIH). When ADC_ISENSE is less than or equal to 1.78V (VIL) the KILL pins are released and the Versal rails automatically powers up sequentially again. R975, R976, and R977 can be adjusted to change VIH and VIL. Use [Equation 5](#) to calculate the resistors for the required VIH threshold.

$$(EQ. 5) \quad R_{976} = \frac{R_{977} \times R_{975} \times (12V - V_{IH})}{R_{977} \times V_{IH} - R_{975} \times (12V - V_{IH})}$$

where:

- R976 is the top resistor in the comparator non-inverting input voltage-divider reference in volts.

- R975 is the bottom resistor in the comparator non-inverting input voltage divider reference in volts. Renesas recommends using the 10kΩ installed by default.
- R977 is the hysteresis resistor in ohms. Make this resistor 5 to 50 times larger than R975.
- V_{IH} is the required comparator high level threshold in volts.

When the V_{IH} resistors are determined, the V_{IL} threshold can be calculated using Equation 6. Verify the hysteresis (V_{IH}- V_{IL}) is acceptable. If it is not, increase R977 and recalculate R976 and V_{IL}.

$$(EQ. 6) \quad V_{IL} = \frac{R977 \times R976 \times 12V}{R976 \times (R977 + R975) - R977 \times R975}$$

- V_{IL} is the comparator low-level threshold in volts, which releases KILL indicating no fault.
- R977 is the hysteresis resistor in ohms.
- R976 is the top resistor in the comparator non-inverting input voltage-divider reference in ohms.
- R975 is the bottom resistor in the comparator non-inverting input voltage divider reference in ohms.

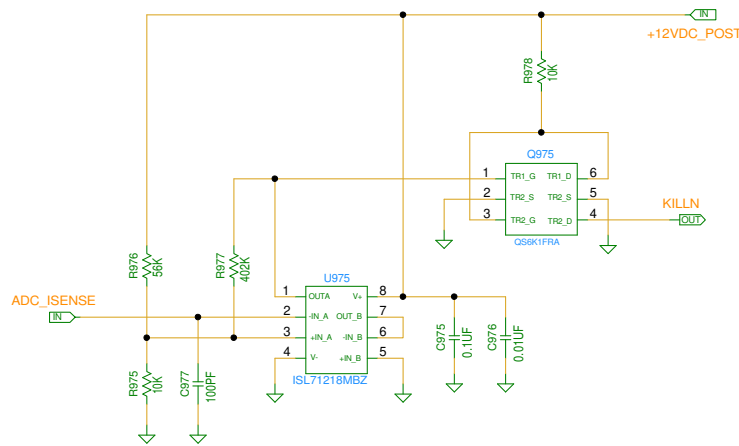


Figure 17. ISL71218 KILL Comparator

To avoid the KILL Comparator output from affecting the bias point of the power-sequencer circuit when there is no fault, Q975 is used as an open-drain output when there is no fault, and pulls KILL low when there is a fault.

1.11 All Voltage Rail Monitoring

The J801 40-pin header provides a convenient access point to monitor all the DC rails generated by the Renesas radiation tolerant point-of-load regulators and linear regulators. Figure 18 shows the pinouts of the voltage rails.

Note: Only use J801 for DC voltage monitoring. Renesas does not recommend attempting to measure the rail voltages for steady-state ripple or transient load step for meeting AMD Versal power management rail requirements because J801 is routed a long distance away from the output capacitors for those rails and does not provide accurate voltages at this measurement point.

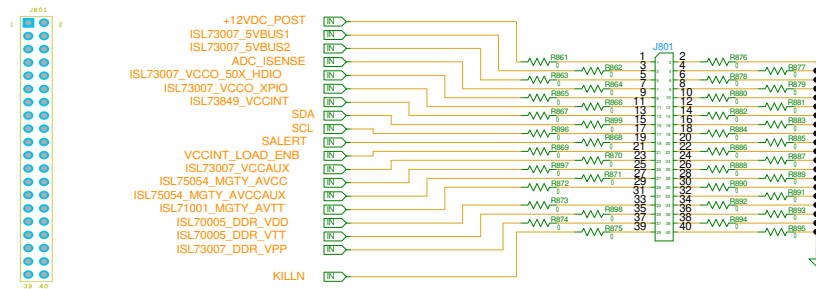


Figure 18. Voltage Rail Pinout

3. Typical Performance Graphs

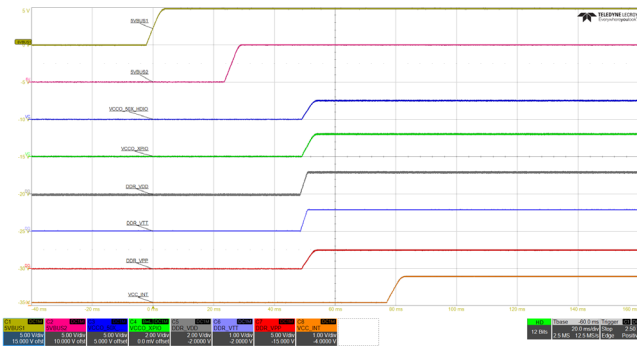


Figure 21. Power-Up Sequencing, Ch1-8

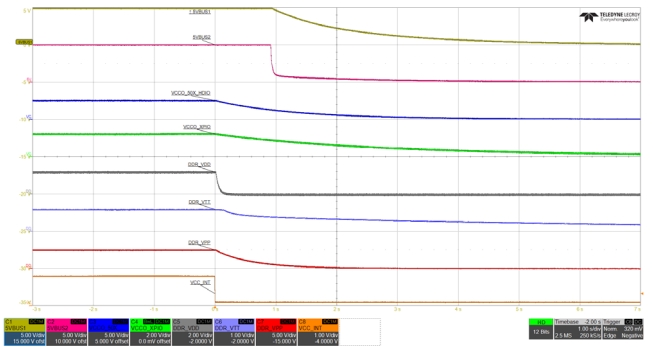


Figure 22. Power-Down Sequencing, Ch1-8

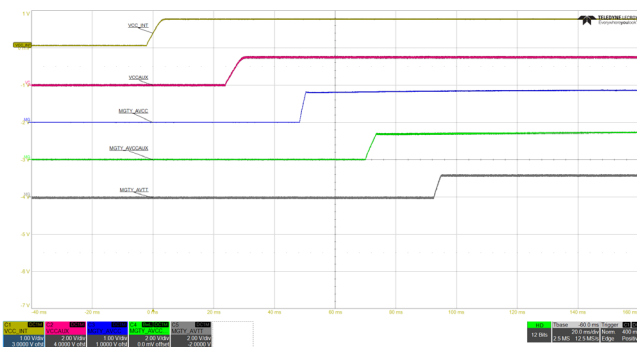


Figure 23. Power-Up Sequencing, Ch9-13

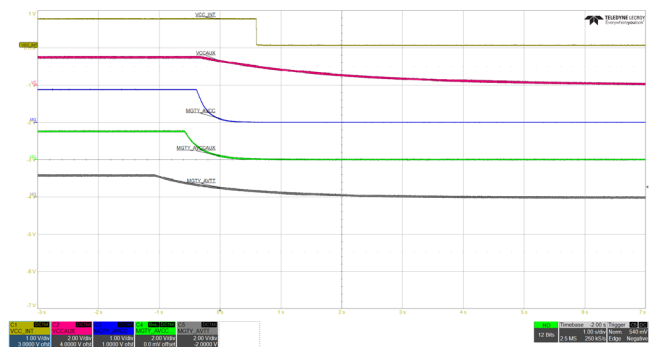


Figure 24. Power-Down Sequencing, Ch9-13

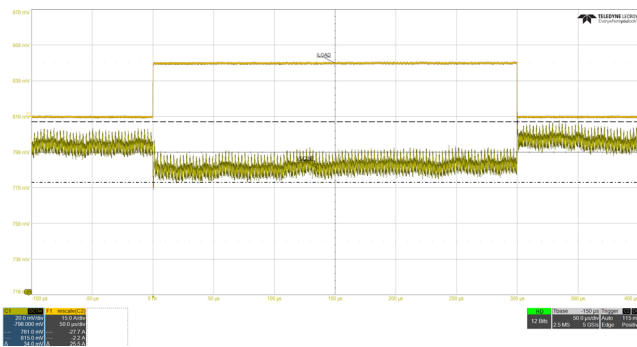


Figure 25. ISL73849_VCCINT_Rail 24A Load Step Transient with $\pm 17\text{mV}$ Compliance Window

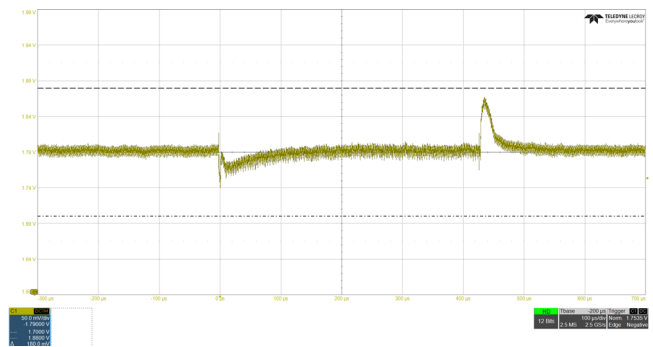


Figure 26. ISL73007_VCCO_50X_HDIO 1.8V Rail 1.11A Load Step with $\pm 90\text{mV}$ Compliance Window

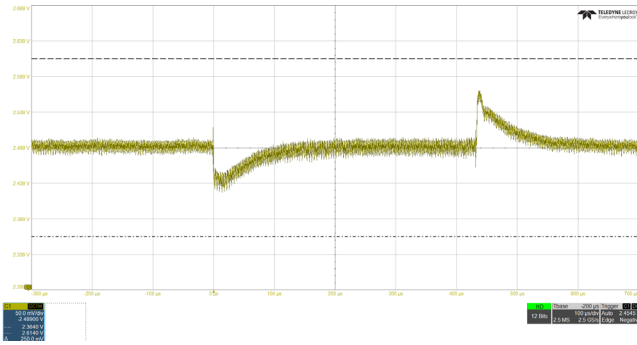


Figure 27. ISL73007_VCCO_50X_HDIO 2.5V Rail 2.78A Load Step with $\pm 250\text{mV}$ Compliance Window

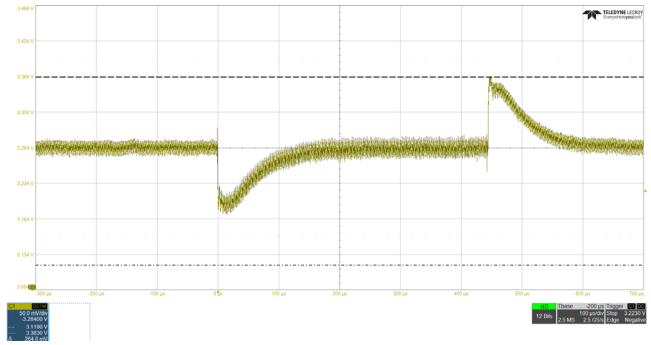


Figure 28. ISL73007_VCCO_50X_HDIO 3.3V Rail 3.67A Load Step with $+99\text{mV}/-165\text{mV}$ Compliance Window

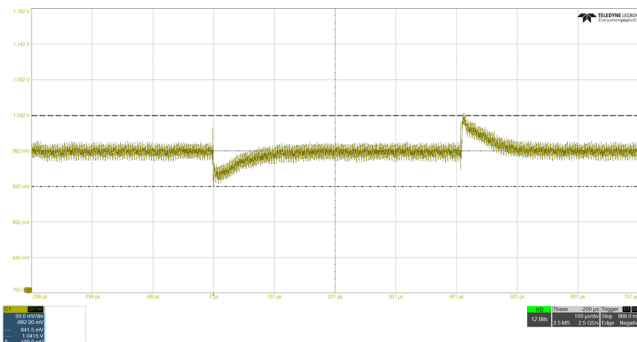


Figure 29. ISL73007_VCC_XPIO 1V Rail 2.5A Load Step with $\pm 50\text{mV}$ Compliance Window

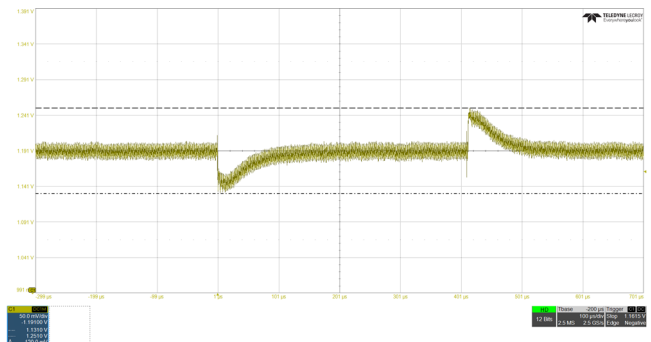


Figure 30. ISL73007_VCC_XPIO 1.2V Rail 3A Load Step with $\pm 60\text{mV}$ Compliance Window

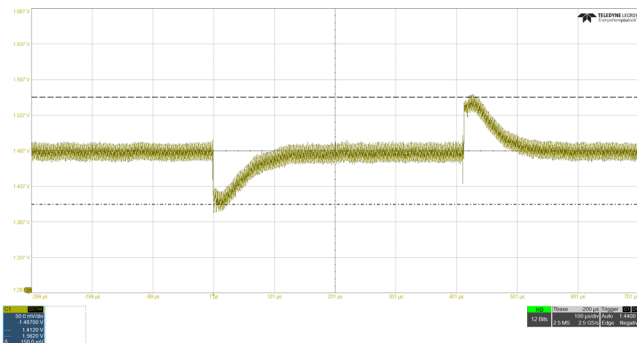


Figure 31. ISL73007_VCC_XPIO 1.5V Rail 3.75A Load Step with $\pm 75\text{mV}$ Compliance Window

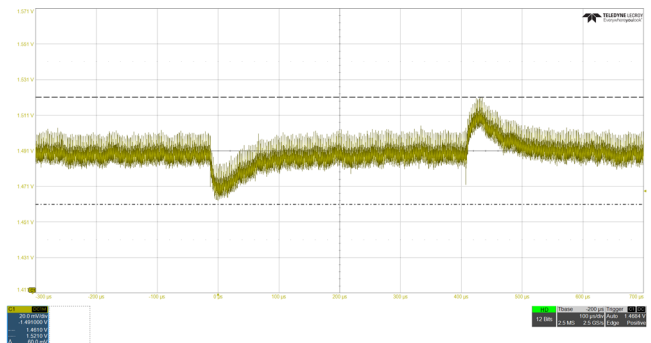


Figure 32. ISL73007_VCCAUX 1.5V Rail 1.136A Load Step with $\pm 30\text{mV}$ Compliance Window

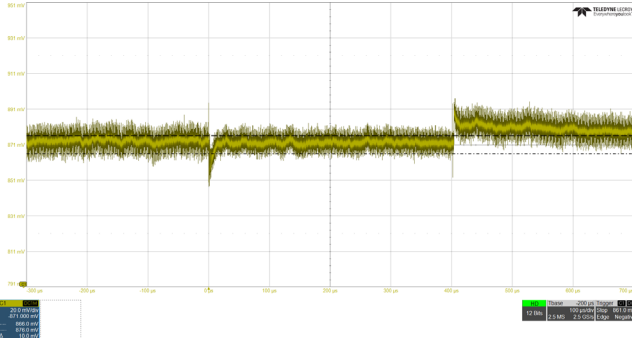


Figure 33. ISL75054_MGTY_AVCC 0.88V Rail 0.707A Load Step with +10mVpp Compliance Window

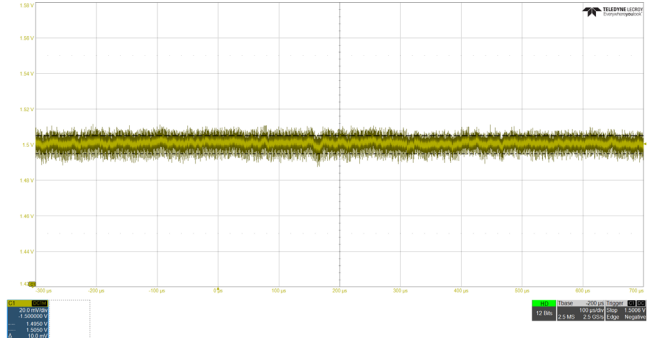


Figure 34. ISL75054_MGTY_AVCCAUX 1.5V Rail 50mA Load Step with +10mVpp Compliance Window

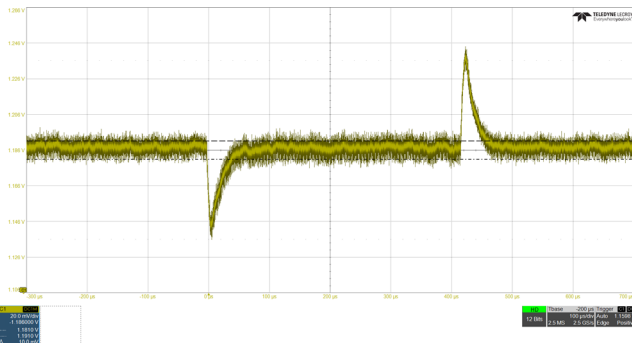


Figure 35. ISL75054_MGTY_AVTT 1.2V Rail 6A Load Step with +10mVpp Compliance Window

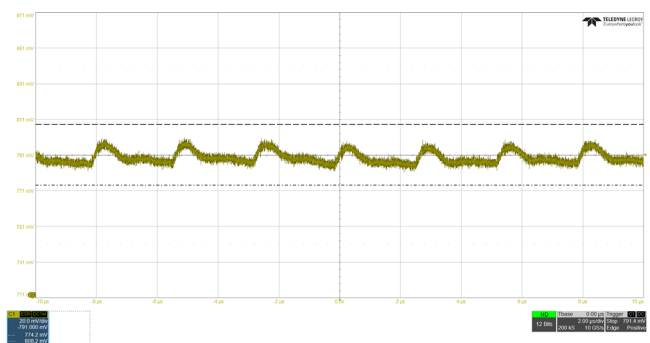


Figure 36. ISL73849_VCCINT Rail Steady State Ripple at 25A with ±17mV Compliance Window

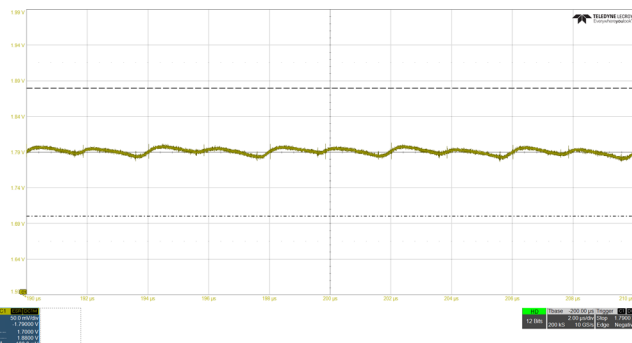


Figure 37. ISL73007_VCCO_50X_HDIO 1.8V Rail Steady State Ripple at 3A with ±90mV Compliance Window

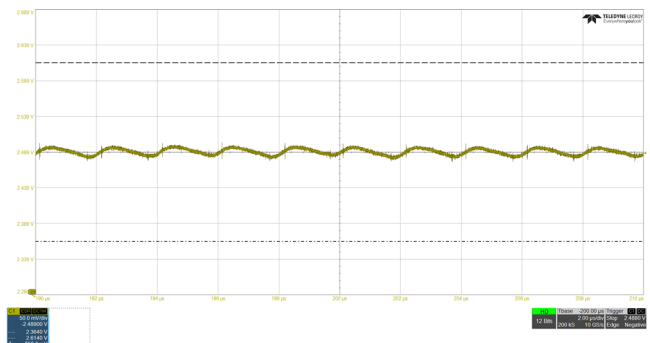


Figure 38. ISL73007_VCCO_50X_HDIO 2.5V Rail Steady State Ripple at 3A with ±75mV Compliance Window

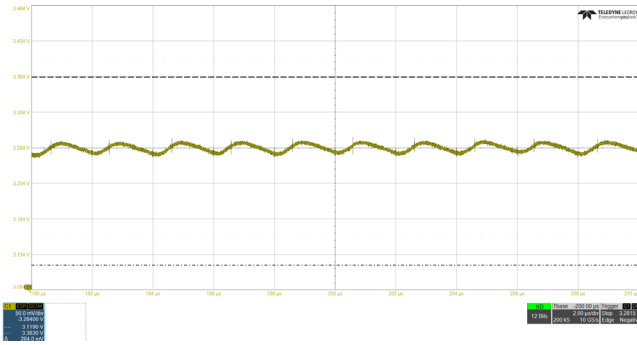


Figure 39. ISL73007_VCCO_50X_HDIO 3.3V Rail Steady State Ripple at 3A with +99mV/-165mV Compliance Window

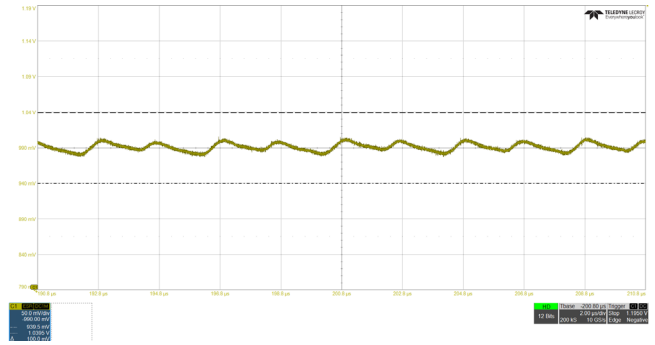


Figure 40. ISL73007_VCCO_XPIO 1V Rail Steady State Ripple at 3A with ±50mV Compliance Window

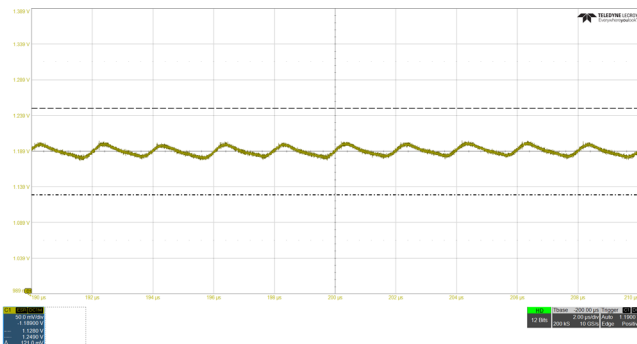


Figure 41. ISL73007_VCCO_XPIO 1.2V Rail Steady State Ripple at 3A with ±60mV Compliance Window

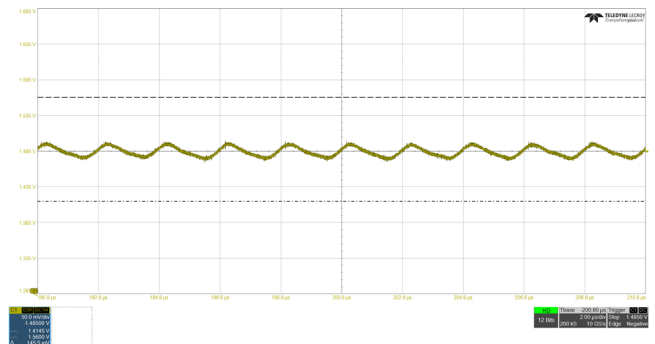


Figure 42. ISL73007_VCCO_XPIO 1.5V Rail Steady State Ripple at 3A with ±75mV Compliance Window

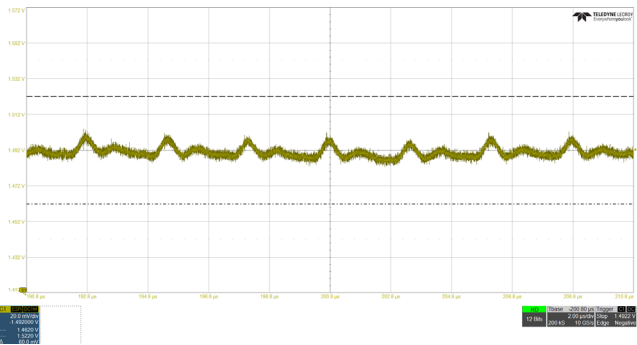


Figure 43. ISL73007_VCCAUX 1.5V Rail Steady State Ripple at 3A with ±30mV Compliance Window

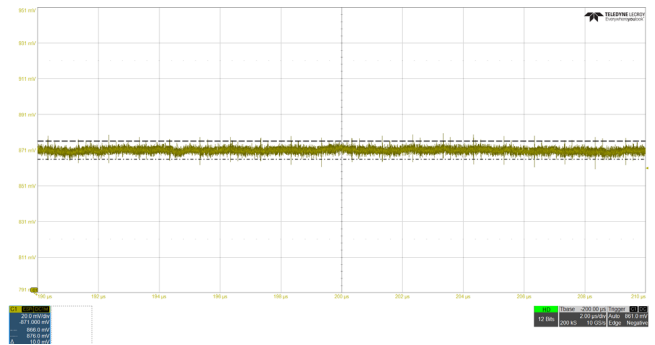


Figure 44. ISL75054_MGTY_AVCC 0.88V Rail Steady State Noise at 0.7A with +10mV_{p-p} Compliance Window

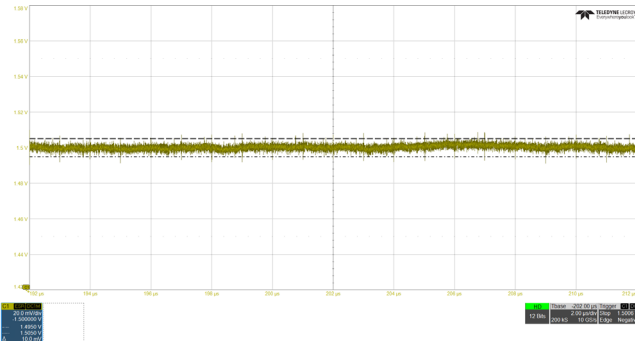


Figure 45. ISL75054 1.5V Rail Steady State Noise at 50mA with $\pm 10V_{p-p}$ Compliance Window

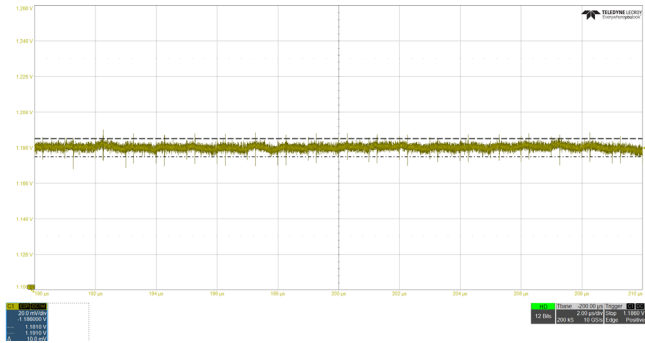


Figure 46. ISL71001A_MGTY_AVTT 1.2V Rail Steady State Ripple at 6A with $+10mV_{p-p}$ Compliance Window

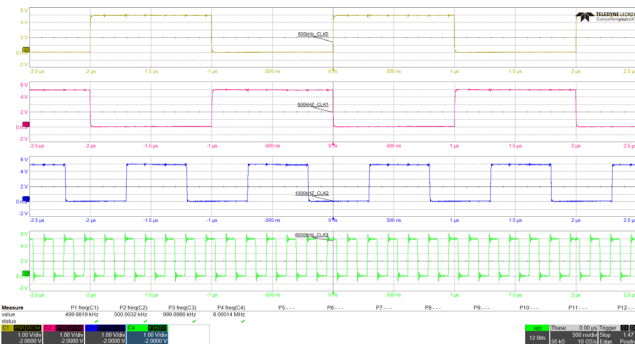


Figure 47. ISL74420 Clock Controller Synchronization Clocks

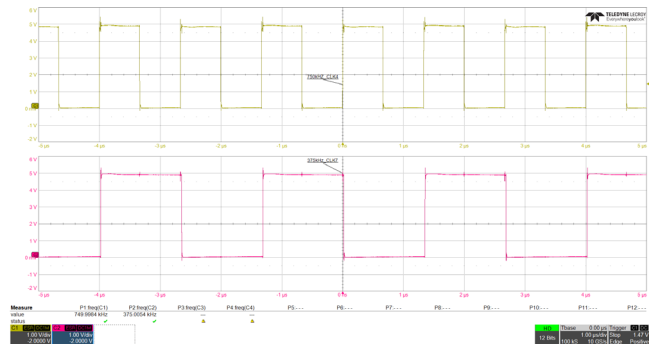


Figure 48. ISL74420 Clock Target Synchronization Clocks

4. Ordering Information

Part Number	Description
ISLVERSALDEMO3Z	Rad Tolerant Power Management Demonstration Board

5. Revision History

Revision	Date	Description
1.00	Jul 24, 2024	Initial release

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