Hardware Manual

V3M Starter Kit

HW Manual

RENESAS ADAS
R-CAR / V3M
Y-ASK-RCAR-V3M-WS10
Y-ASK-RCAR-V3M-WS20

Renesas Electronics
www.renesas.com

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(Rev.3.0-1 November 2016)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the SoC. It is intended for users designing application systems incorporating the SoC. A basic knowledge of electric circuits, logical circuits, and SoCs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	xxx/xx Group User's Manual: Hardware	This User's manual
Renesas Technical Update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The symbol “#” suffixed to the pin (or signal) name means that the pins (or signals) are active “L”.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
CPLD	Complex Programmable Logic Device
GPIO	General Purpose Input Output
SoC	System on a Chip
JTAG	Joint Test Action Group
SPI	Serial Peripheral Interface
QSPI	Quad Serial Peripheral Interface
CoM-Express	Computer on Module - Express
HSSTP	High Speed Serial Trace Probe (for High Speed Debugging)
LVDS	Low-voltage differential signaling (for video output and High Speed Debugging)
HDMI	High-Definition Multimedia Interface
USB	Universal Serial Bus
GUI	Graphical User Interface
PMIC	Power Management Integrated Circuit
RGMII	Reduced gigabit media-independent interface
DIPSW	Dual In-line Package Switch
IPL	Initial Program Loader

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Tables

1. Introduction

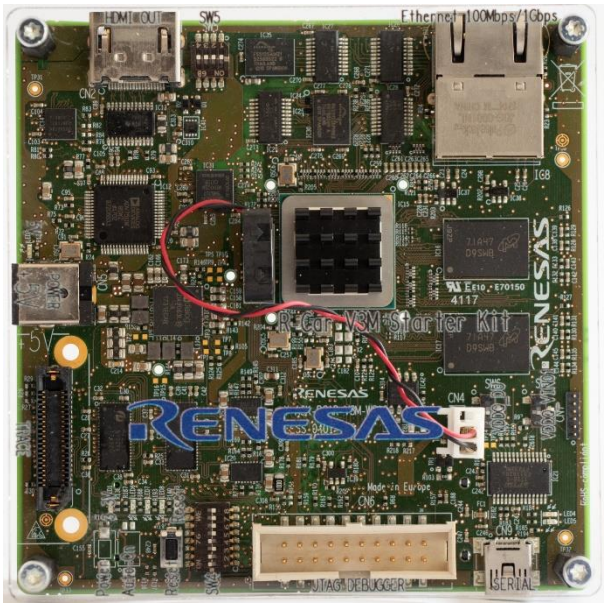

Figure 1. ASK-RCAR-V3M-WS10 Starter Kit top view.

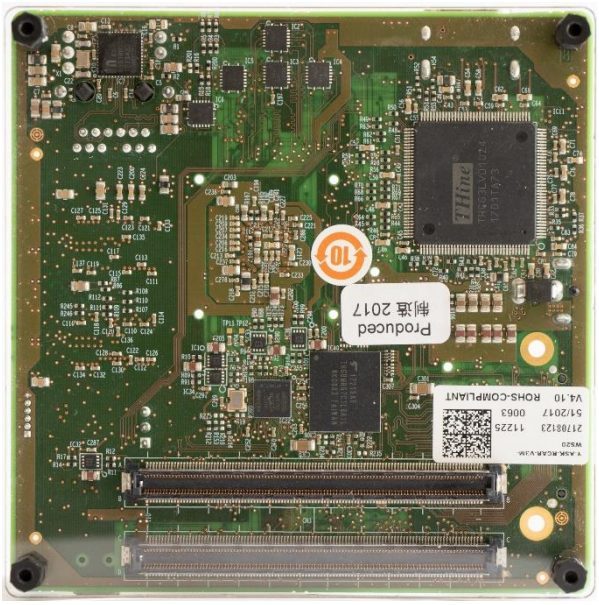

Figure 2. ASK-RCAR-V3M-WS10 Starter Kit bottom view.

1.1 General Function

The ADAS R-CAR V3M Starter Kit is designed to support development of automotive applications based on the SoC R-CAR V3M from Renesas Electronics.

Table 1. Board functions

Board Function	Item	Description	Note
CPU	ARM CA53 (ARMv8)	800 MHz dual core, with NEON/VFPv4, L1$ I/D 32K/32K, L2$ 512K	
	ARM CR7 (ARMv7)	800 MHz, with VFPv3, L1$ I/D 32K/32K, I/D-TCM 32K/32K, lock-step	
Memory	SoC Internal	448KBytes System RAM	
	DDR	2 GBytes (6.4 GBytes/s) DDR3L-1600, 32-bit wide	
	Hyper-Flash (Bootable)	64 MiBytes Hyper-Flash (RPC, reduced pin-count) (512 Mbits, 160 MHz, 320 MBytes/s)	Alternatively to on-board Hyper/QSPI flash memory: 2ch QSPI (max. 80 MHz, 80 MBytes/s)
	QSPI Flash (Bootable)	64MiBytes QSPI (512 Mbits, 80 MHz, 80 MBytes/s)	

	eMMC	16 to 32GiBytes eMMC (HS200) [available only for PCB V3.00 and later]	Available
	Parallel SRAM/ROM (Bootable)	-	Available (shared with many other functions)
Video out	HDMI	No native HDMI; derived from LVDS by converter HDMI connector (type A, 19 pins) HDMI 1.4, up to 1080p60, 148.5 MHz, (no audio)	Alternatively to on-board connector (shared with trace and LVDS)
	RGB (Parallel)	-	RGB888 (Shared with many other functions)
	LVDS	-	1 channel (4+1CLK differential pairs) TIA/EIA-644, max 148.5 MHz, (shared with trace and HDMI)
Video in	Serial	-	MIPI-CSI2, 1 channel (4-lanes) VC/DT supported, up to 1.5Gbps/lane
	Parallel	-	2 channels, RGB/YCbCr/Raw, max 100 MHz (shared with many other functions)
Interfaces	EthAVB	PHY + RJ45 connector (100/1000)	Alternatively to on-board PHY: RGMII V1.3 interface (2.5V)
	SCIF	1 channel via Mini-USB-B (via FT232 USB-to-UART bridge)	Up to 3 additional channels (shared) (on-board channel optionally)
	HSCIF	-	Up to 4 channels (shared)
	MSIOF (SPI)	-	Up to 4 channels (SPI/IIS, master/slave, 66 MHz) (shared)
	CAN-FD	-	Up to 2 channels, 8Mbps (shared)
	I2C	For on-board peripherals	Up to 5 channels, 400kHz, master/slave (shared)
	DigRF	-	Available
Timer	PWM	-	Up to 5 channels (shared)
HMI	output	3 LEDs at GPIOs	-
	input	4 DIP-switches at GPIOs	-
ADC		-	8 channels, 12-bit
GPIOs		-	14 GPIOs by default, up to 105 GPIOs (shared)
Reset		Reset button (and LED)	Input and output
Power		5V/3A input PMIC for all required voltages (OTP)	Power-up/down signals Power-good status
Boot Source		Hyper-Flash, QSPI, SCIF, JTAG debugger	QSPI Flash, SCIF, JTAG debugger, parallel ROM
Debug IF	JTAG debug	20-pin (2.54mm) ARM_EML (“Lauterbach”)	Available
	JTAG trace	EMT-A53-16K/R7-4K	Available

	Parallel trace	On-board connector for HSSTP probe (shared with LVDS)	Available (shared with LVDS and HDMI)
Clocks		All necessary clocks on-board	-
Mode		Can be configured by CPLD, DIPSW, USB or software	-
Cooling		Heat-sink and fan	-
Expansion		-	CoM Express connector (440-pin) backwards-compatible to H3 Starter Kit
Interrupts		-	NMI, IRQ on GPIOs
Size		95 x 95 mm (equivalent to CoM Express type 6)	-
SoC		Soldered	-

1.2 Power requirement

Special attention must be paid when using the power supply. Use only the 5V/3A power supply provided on the Starter Kit. Higher voltages may damage permanently the R-CAR V3M Starter Kit.

Power connector counterpart type: diameter 5.5mm, center pin 2.0mm, insertion depth 8.85mm.

Note that the V3M Starter Kit powers-up directly, there is no power switch.

The SW1 and SW2 have no function.

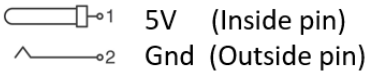

Figure 3. Power connector definition.

1.3 Order codes

Table 2. Order codes.

Boards	Order Codes
V3M Starter Kit. SoC silicon version 1.0	Y-ASK-RCAR-V3M-WS10
V3M Starter Kit. SoC silicon version 2.0	Y-ASK-RCAR-V3M-WS20

1.4 Operating conditions

This board is intended to operate within the temperature range of 0 °C – 40 °C.

1.5 V3M Starter Kit block diagram

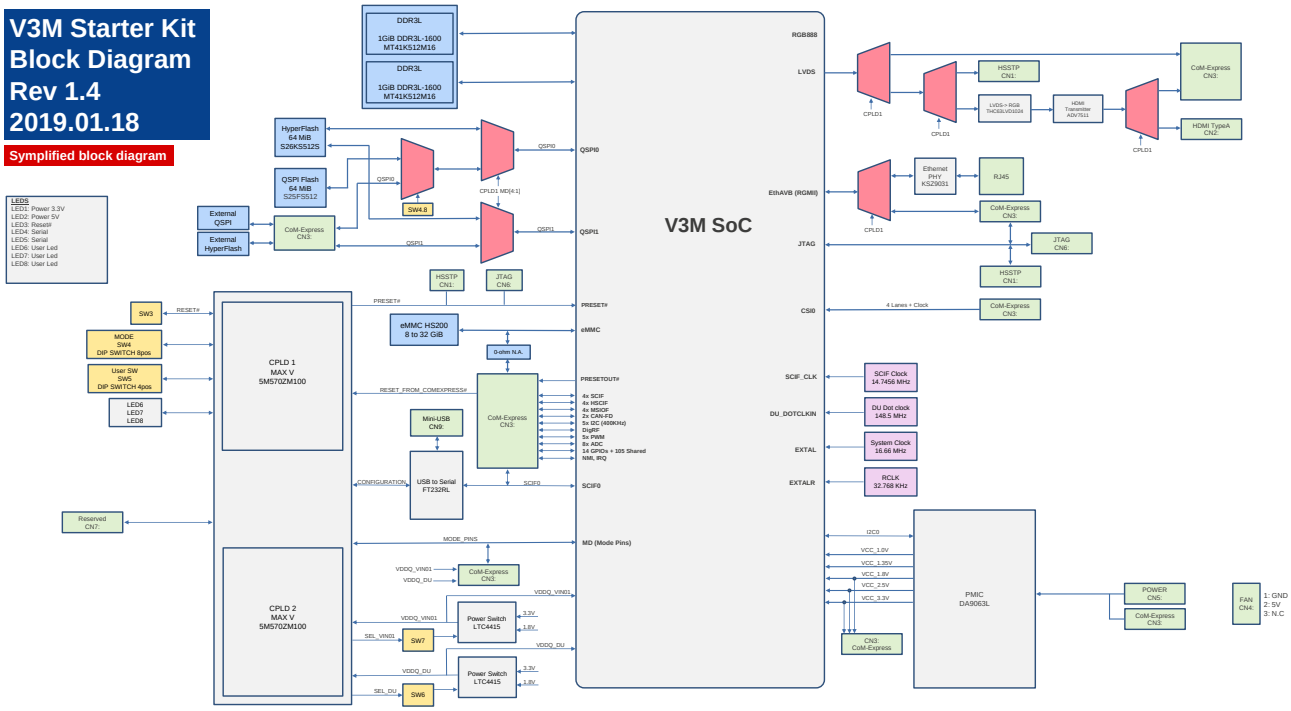

Figure 4. V3M Starter Kit block diagram

1.6 Board releases

[DS] Design Sample: main test coverage

[ES] Engineering Sample: Function test coverage 80%

[CS] Customer sample: Functional test coverage 100% pass

[MP] Mass Production: CE and temperature test pass

1.7 Fan connector pinout

Table 3. Fan connector pinout

Pin Number	Description
1	PWM#
2	5V
3	N.C.

2. SoC Mode

The SoC mode is configured by using dedicated GPIO pins on the SoC. These pins are driven by a CPLD which is the responsible to set up the GPIOs during reset.

The CPLD contains a register where the SoC mode configuration is stored. Some of the configuration bits of the SoC register are accessible through the DIP switch 4 (SW4) available on the board. The rest of the bits have a default value. The preset values are shown in the Table 4. It is possible to write the CPLD register via proprietary CPLD interface or from PC with the GUI provided by Renesas. The SoC is also connected to the CPLD interface and can modify the SoC mode register if it is necessary.

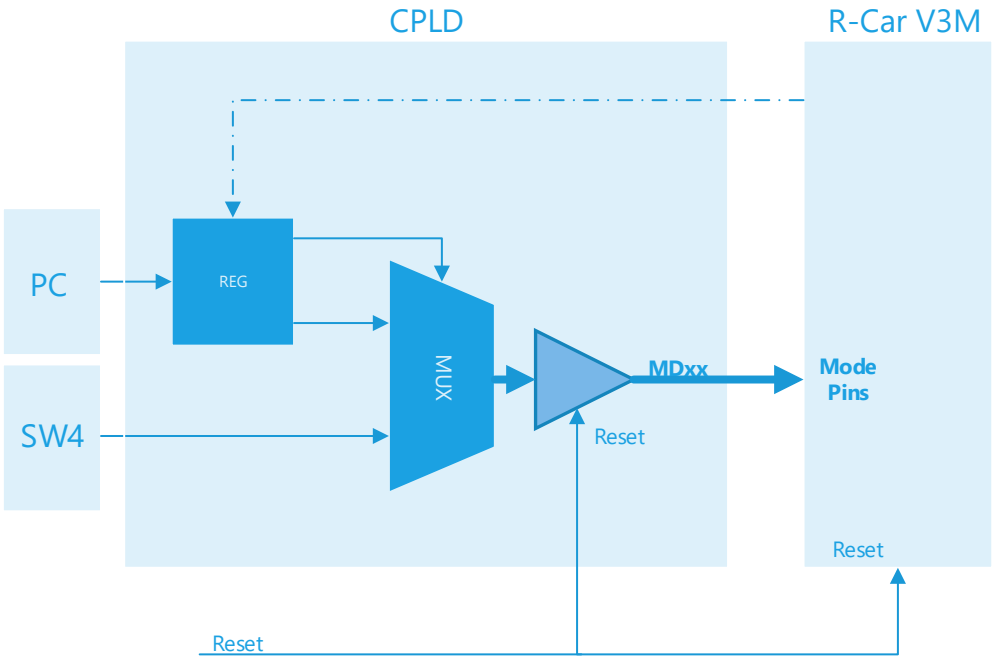

Figure 5. CPLD and SW4 multiplexing diagram.

The CPLD contains a multiplexer to select the Boot Mode configuration source either from the SW4 or from the internal register. This should be defined with the GUI under the tab “SOC mode configuration” and then selecting the desired option on the “MODE setting” checkbox as shown in the figure 4.

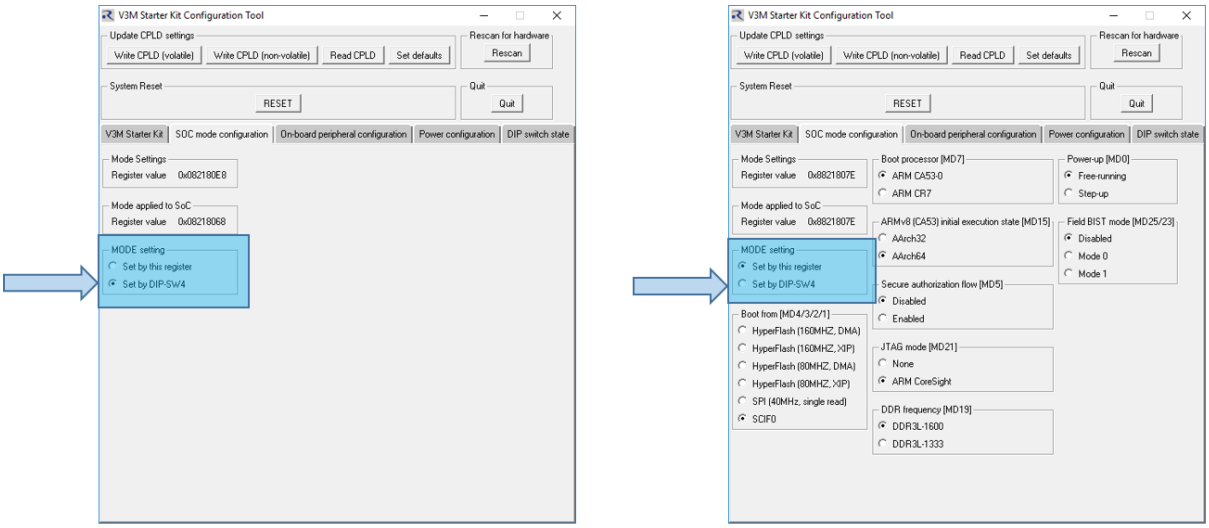

Figure 6. SW4 or CPLD selection.

Table 4. SoC mode.

Mode	Switch	Description	L / ON	H / OFF	Default
MD0			Free running	Prohibited	LOW
MD1	SW4.1	Boot device selection [0]	L	H	ON
MD2	SW4.2	Boot device selection [1]	L	H	ON
MD3	SW4.3	Boot device selection [2]	L	H	OFF
MD4	SW4.4	Boot device selection [3]	L	H	ON
MD5	SW4.5	Secure authorization	Enabled	Disabled	OFF
MD7	SW4.6	Master boot processor	A53 (CPU0)	CR7	OFF
MD8		Databus width of Area 0 space	8 bit	16 bit	LOW
MD9		EXTAL/XTAL	Clock	Crystal	LOW
MD13		EXTAL input frequency [0]			LOW
MD14		EXTAL input frequency [1]			LOW
MD15	SW4.7	Architecture Selection	AArch32	AArch64	OFF
MD16		Reserved. Fix to H			HIGH
MD18		CLKOUT frequency setting	66.67 MHz	44.44 MHz	LOW
MD19		DDR clock frequency	DDR 1600 (800 MHz)	DDR 1333 (666.67 MHz)	LOW
MD21		Debugging mode	Disabled	Coresight	HIGH
MD23		Field BIST mode	Mode 0	Mode 1	LOW
MD25		Field BIST mode	Disabled	Enabled	LOW
MD26		Reserved. Fix to L			LOW

3. Connectors / LEDs / Components

3.1 Connectors

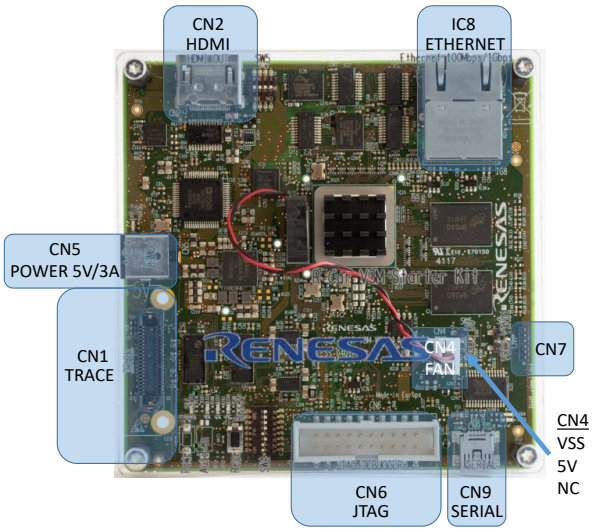

Figure 7. Connectors placement top view.

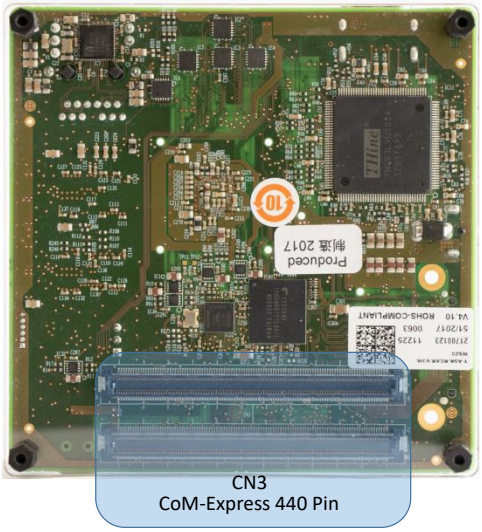

Figure 8. Connectors placement bottom view.

Table 5. Connectors.

Connector	Type	Function
CN1	ERF8-020-05.0-L-DV-L-K-TR	HSSTP Connector
CN2	HMDI Type-A	HDMI Output
CN3	TYCO ELECTRONICS 3-5353652-6 (*)	COM Express Interface
CN4	Header 3 way	Fan Connector
CN5	PJ-063AH	Power Input (5V/3A)
CN6	Header 20 way shrouded SMD	JTAG / TRACE
CN7	-	Internal Use
IC8	J0G-0001NL	Ethernet Connector 100Mbps/1Gpbs
CN9	Mini-B USB	Serial SCIF0

(*) Mating type on top side of an application board: TYCO ELECTRONICS 3-1827231-6

3.2 JTAG Connector

Table 6. JTAG Connector pinout.

Pin Number	Function	I/O	Level	Remark	Pin Number	Function	I/O	Level	Remark
1	VTREF	O	1.8V	-	2	VSUPPLY	I	1.8V	Not connected
3	TRST#	I	1.8V	-	4	GND	-	0V	-
5	TDI	I	1.8V	-	6	GND	-	0V	-
7	TMS	I	1.8V	-	8	GND	-	0V	-
9	TCK	I	1.8V	-	10	GND	-	0V	-
11	N.C.	O	1.8V	-	12	GND	-	0V	-
13	TDO	O	1.8V	-	14	GND	-	0V	-
15	PRESET#	I/O	1.8V	Open Drain	16	GND	-	0V	-
17	N.C.	-	-	-	18	GND	-	0V	-
19	N.U.	-	-	Not used	20	GND	-	0V	-

3.3 Switches

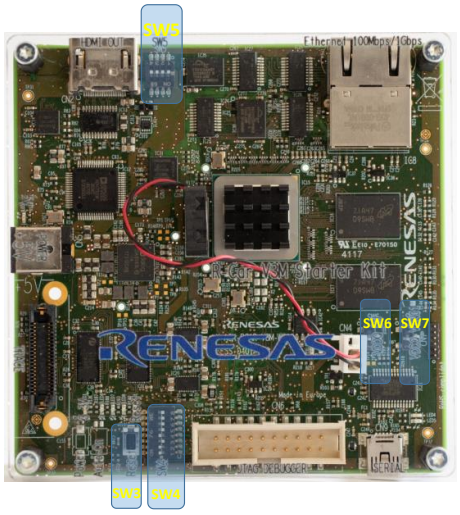

Figure 9. Switches placement top view

Table 7. Switch description

Switch	Function
SW3	Reset
SW4	Mode configuration
SW5	GPIO input and user LEDs
SW6	VCC_VDDQ_DU Select 3.3V or set by CPLD
SW7	VCC_VDDQ_VIN01 Select 3.3V or set by CPLD

3.4 LEDs

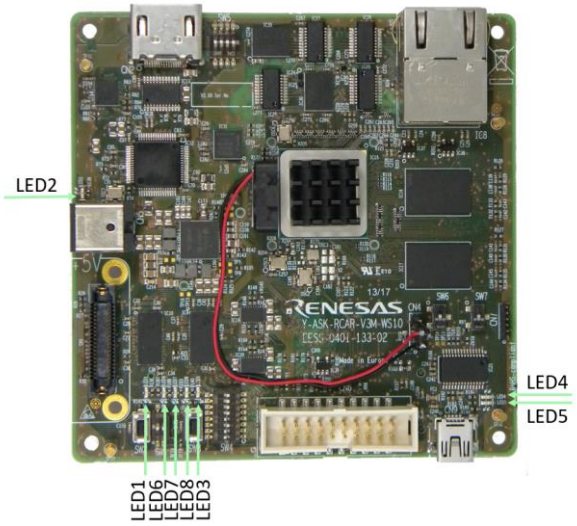

Figure 10. Top view of the board. LEDs position.

Table 8. LEDs description.

LED	Color	Function
LED1	Red	Power LED 3.3V
LED2	Red	Power LED 5.0V
LED3	Yellow	System Reset LED
LED4	Yellow	USB (FT232)
LED5	Green	USB (FT232)
LED6	Green	User LED I01
LED7	Green	User LED I02
LED8	Green	User LED I03

3.5 Components

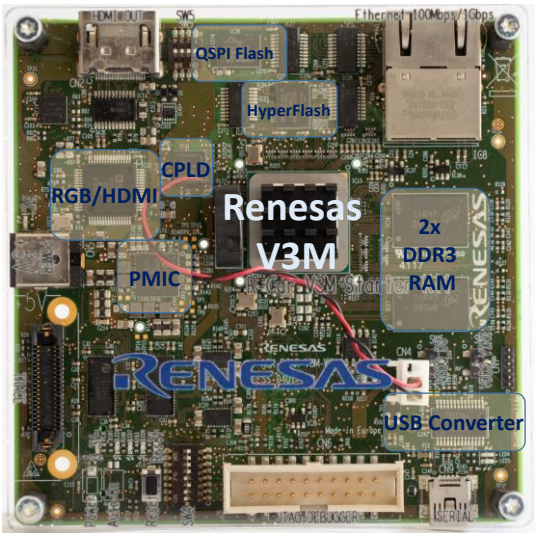

Figure 11. Component position on top side.

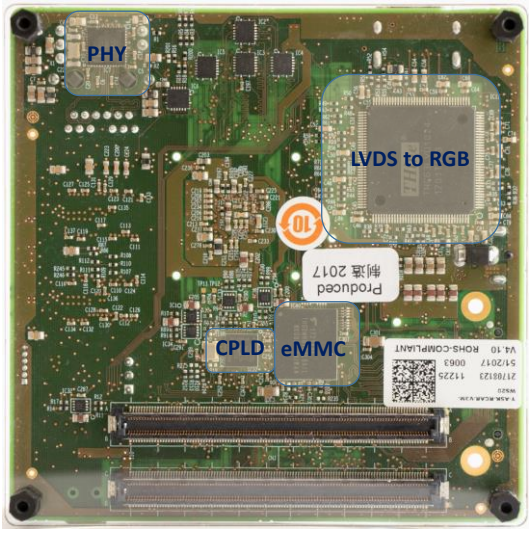

Figure 12. Component position on bottom side.

Note 1: The eMMC memory shown in Figure 12 is only available from board revision REV 3.0 onwards.

Note 2: The size of the eMMC memory depend on the batch. Minimum size is 8 GiB and maximum 32 GiB.

Table 9. List of components.

Name	Function	Reference
IC35	QSPI flash (64MiB)	S25FS512SAGBHI213
IC30	Hyper-Flash (64MiB)	S26KS512SDPBHI020
IC40	eMMC (32GiB) or eMMC (16GiB)	KLMBG4GESD-B03P THGBMHG7C1LBAIL
OSC2	Oscillator, EXTAL 16.667 MHz	
OSC3	Oscillator, EXTALR 32.768 kHz	
OSC5	Oscillator, DU_DOTCLKIN 148.5 MHz	
OSC6	Oscillator, SCIF_CLK 14.7456 MHz	
IC7	Ethernet PHY	KSZ9031RNXCA
IC11	LVDS to RGB converter	THC63LVD1024
IC12	HDMI	ADV7511WBSWZ

4. V3M Starter Kit Configuration Tool

Renesas provides a configuration tool to simplify the set-up of the R-CAR V3M Starter Kit. The tool allows the user to read and modify the internal configuration register of the CPLD.

4.1 First use

Execute the V3M Starter Kit Configuration Tool. Note that before starting the tool, the PCB must be powered and the USB cable has to be connected to the Mini-USB connector (CN9).

The V3M Starter Kit contains a FT232 chip from the vendor FTDI to convert from USB interface to UART.

In case the V3M Starter Kit is not detected, an error message will be shown. In that case check on the Windows Device Manager (Figure 13) if the corresponding USB Serial Port (COMx) is recognized. Otherwise install the driver available on the FTDI web page and try again.

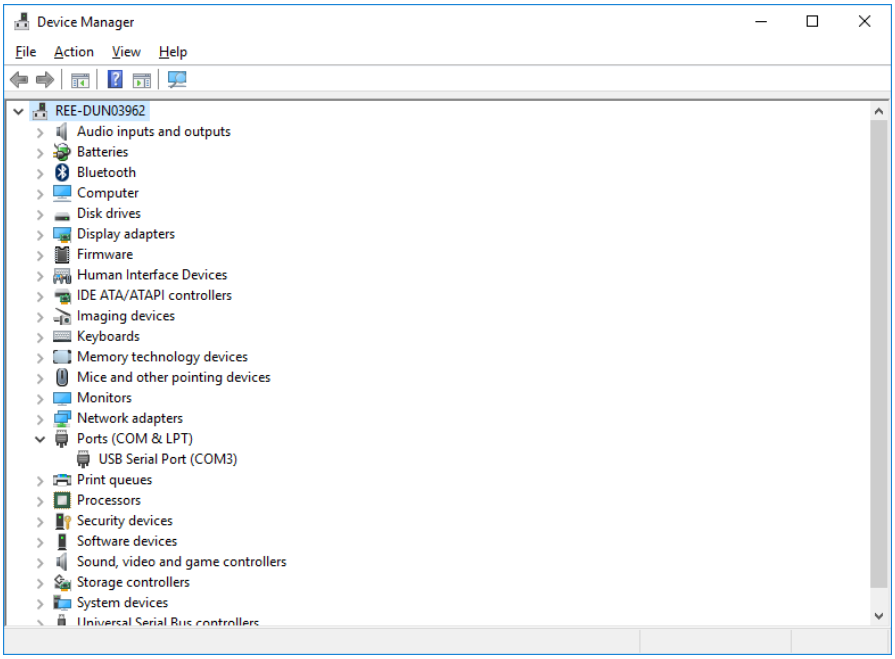

Figure 13. Device manager view. Check for COMx ports.

You can find the drivers on the FTDI web page by clicking the following link. Check for the last version and install the FTDI driver according to your system.

https://www.ftdichip.com/Drivers/VCP.htm

4.2 Configuration tool overview

The user interface shown in Figure 14 appears when the connection with the CPLD is successfully. Note that it is possible to be ask to upgrade the CPLD into a new version. This process is automatically performed by the V3M configuration tool.

The configuration tool allows to communicate easily with the CPLD for changing the settings and modify its registers with a simply user interface. Please take a couple of minutes to familiarize with the interface.

Some of the functions are:

- Write volatile and non-volatile the CPLD
- Read CPLD
- Set defaults
- Generate a system reset
- V3M Starter Kit information

- SoC mode configuration
- On-board peripheral configuration
- Power configuration
- DIP switch state viewer

These functions will be introduced and explained in the following chapters.

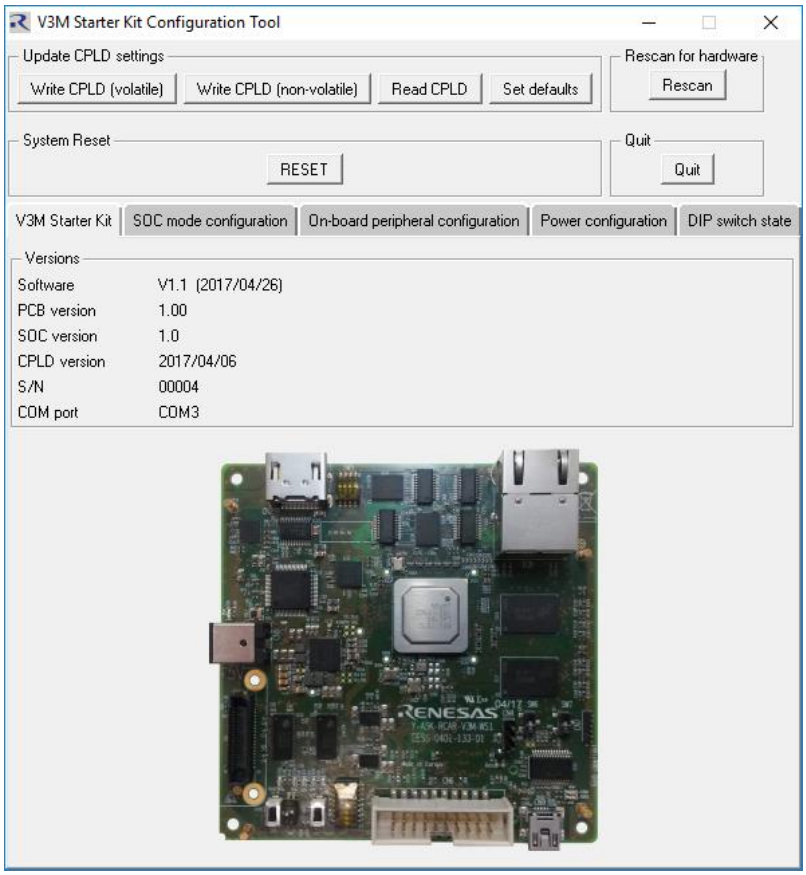

Figure 14. V3M Starter Kit configuration tool.

4.3 Volatile/Non-volatile

V3M Starter Kit CPLD settings can be saved as volatile or non-volatile.

When the settings are set as volatile, these are written in the CPLD registers and are only effective until new power cycle.

When the settings are set as non-volatile, these are written in the internal Flash memory of the CPLD and are effective even after power cycle.

4.4 Terminal blocking virtual COM ports

GUI can only be accessed when no terminal is connected and vice-versa. Make sure you don't have open any terminal software when initiating the GUI.

4.5 SCIF disabled by hardware

When the SCIF0 is routed to the CoM-Express connector be aware that is not possible to stablish communication with the GUI any more. To temporally enable communications with the GUI, (i.e. open GUI, write, read, reset etc) press continuously reset button.

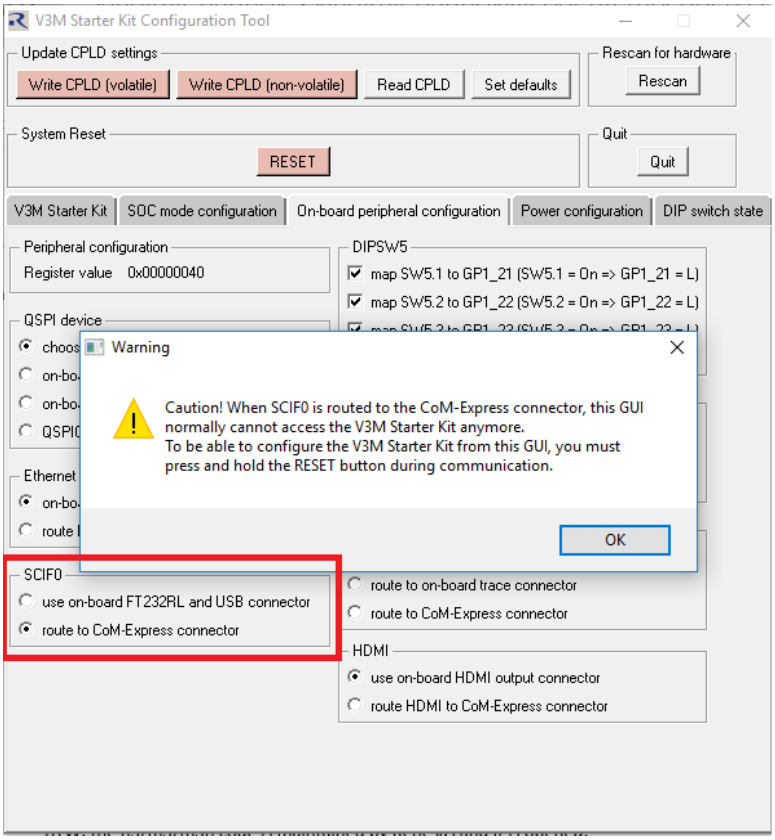

Figure 15. Routing SCIF0 to CoM-Express connector

.

5. Flash Memory Selection

The system booting can be done from three different sources. The first one is a Hyper-Flash memory, the second is a standard on-board QSPI memory and the last option is through the CoM-Express connector. The last method offers the possibility to boot from an external QSPI memory placed on a daughter board.

The multiplexers are driven by the CPLD. The CPLD contains a register where the SoC Mode is configured. This register can be modified either with the GUI or with the switch SW4.

5.1 Multiplexing drawing

The Figure 16 illustrates the flash memories multiplexing schema. The V3M SoC has two different QSPI interfaces which are connected to the three different sources. The CPLD determinates which QSPI path is connected to the SoC. Note that just one or two QSPI customer memories may be installed in a daughter board if the CoM-Express connector is used.

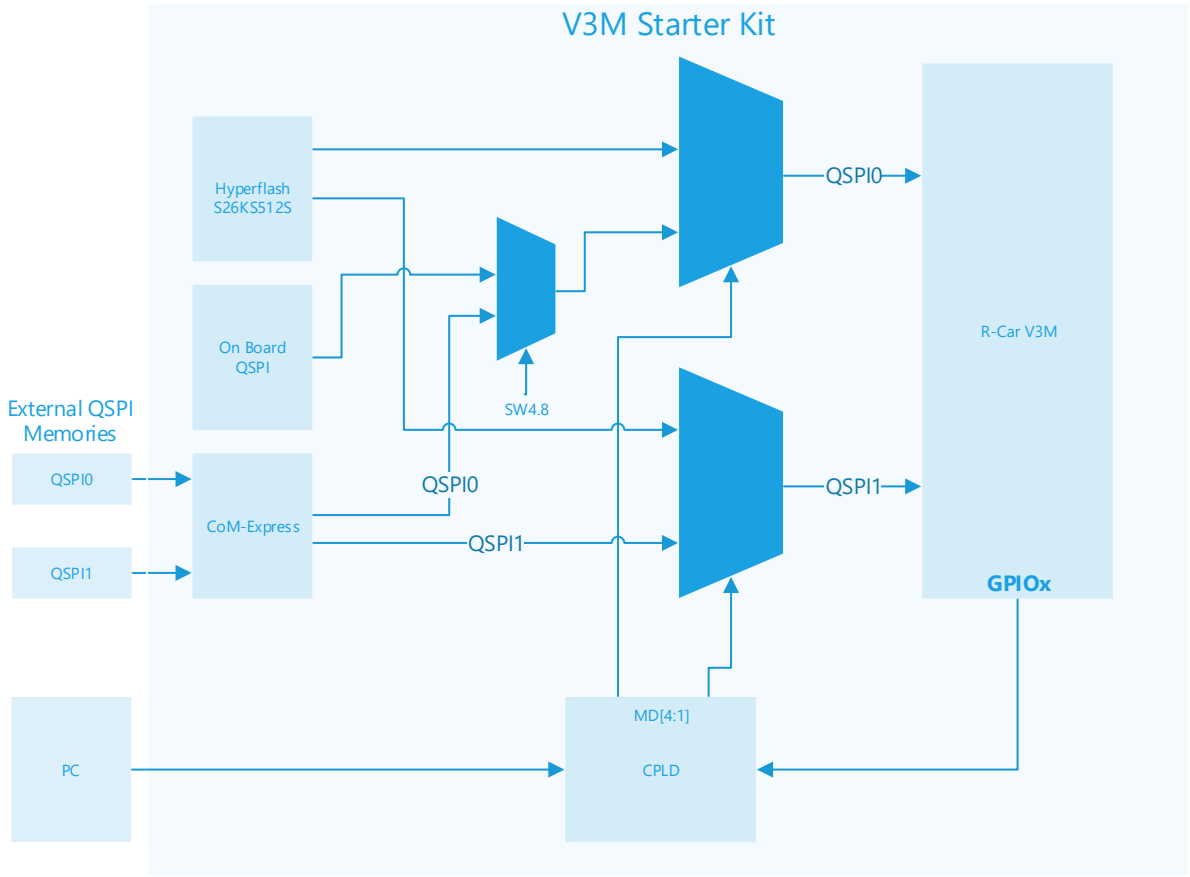

Figure 16. Flash memories multiplexing drawing.

5.2 Flash Memory Selection (via CPLD/GUI)

The user can select which QSPI device will be selected by clicking on the tab “On-board peripheral configuration”. Then select one option on the “QSPI device” checkbox as shown in the Figure 17.

When the desired configuration is chosen, click on Write CPLD (volatile) or Write CPLD (non-volatile). If the Write (volatile) button is pressed, the changes will remain active until the board is powered off. If permanent changes must be applied then click on Write CPLD (non-volatile) button.

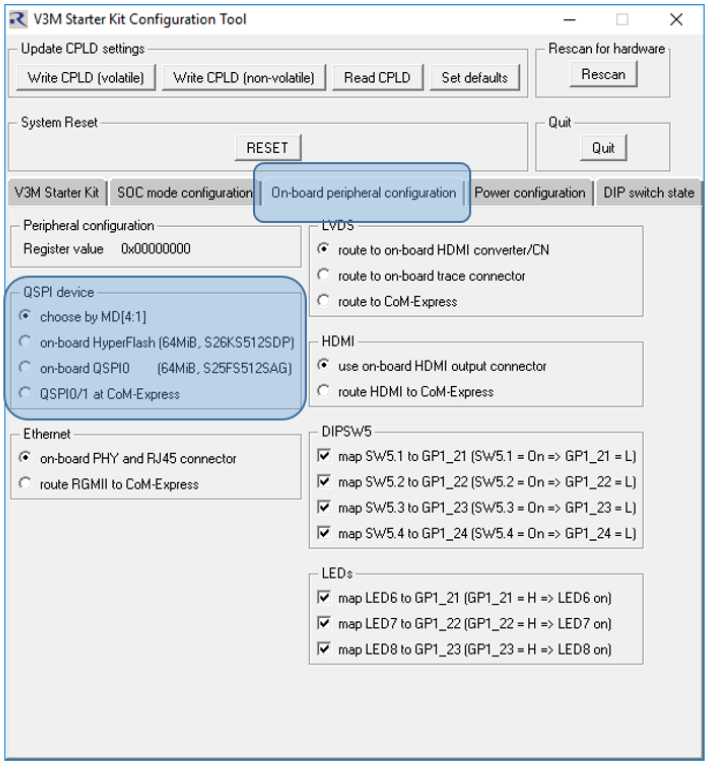

Figure 17. Flash memory selection.

5.3 Boot Memory Selection

To select the booting memory, click on the tab “SOC mode configuration”.

The MODE setting checkbox allows to select between the SW4 or CPLD register as a configuration source as shown in the Figure 18.

Click on “set by this register” and note that additional configuration options are shown (Figure 19).

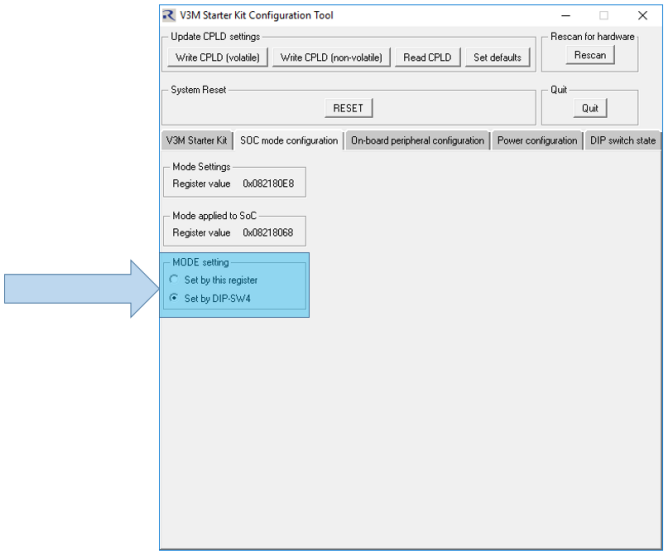

Figure 18. Mode settings by register or by DIP SW4 selection.

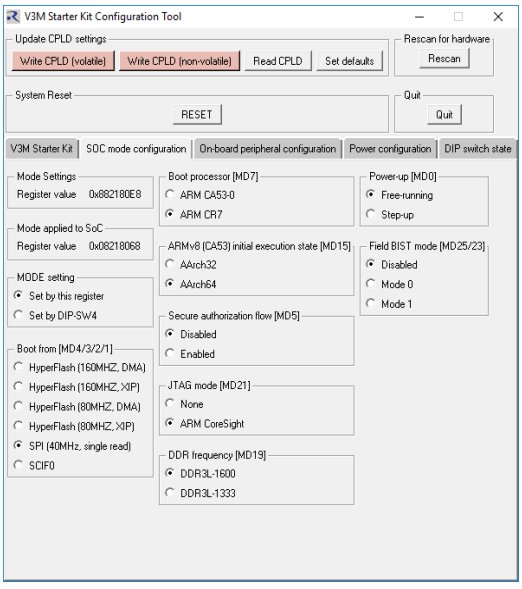

Figure 19. SoC Mode interface.

The boot mode option can be selected by clicking on the desired option available in the “Boot from [MD4/3/2/1] checkbox”.

Now click on Write CPLD (volatile or non-volatile) to apply the changes and write the CPLD.

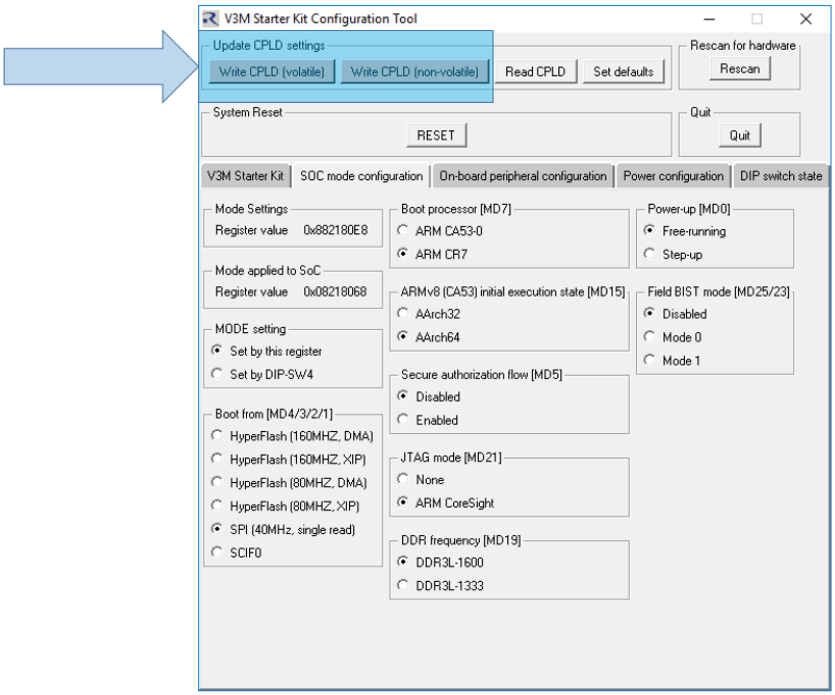

Figure 20. Write CPLD.

5.4 Selection via SW4 switch

As mentioned in the previous section, the boot mode can be also configured either with the switch SW4 or with the CPLD. The SW4 switch is directly connected to the CPLD and modify the SoC mode register bits MD[1..4].

Table 10. Boot source selection.

Boot Source	SW4.1 / MD1	SW4.2 / MD2	SW4.3 / MD3	SW4.4 / MD4	SW4.8
Hyper-Flash (160 MHz, DMA)	ON / ‘0’	OFF / ‘1’	ON / ‘0’	ON / ‘0’	X
Hyper-Flash (160 MHz, XIP)	ON / ‘0’	OFF / ‘1’	ON / ‘0’	OFF / ‘1’	X
Hyper-Flash (80 MHz, DMA)	OFF / ‘1’	OFF / ‘1’	ON / ‘0’	ON / ‘0’	X
Hyper-Flash (80 MHz, XIP)	OFF / ‘1’	OFF / ‘1’	ON / ‘0’	OFF / ‘1’	X
QSPI on-board	ON / ‘0’	ON / ‘0’	OFF / ‘1’	ON / ‘0’	OFF
CoM-Express QSPI	ON / ‘0’	ON / ‘0’	OFF / ‘1’	ON / ‘0’	ON

5.5 eMMC memory

The V3M Starter Kit includes an on board eMMC memory for mass storage.

Additionally, is possible to place an eMMC memory in a Daughter board. Figure 21 shows the eMMC routing diagram.

GPIOs used for the eMMC are not available on the CoM-Express connector.

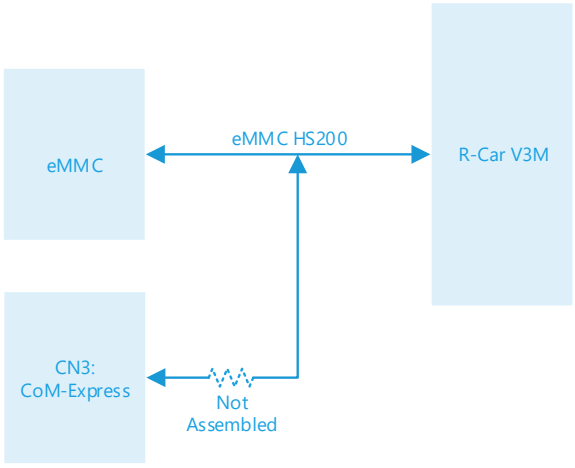

Figure 21. eMMC block diagram

6. LVDS

6.1 Multiplexing drawing

The Figure 22 shows the LVDS multiplexing schema. multiplexing. The V3M SoC contains a LVDS interface that can be used as video output or high speed trace. The multiplexing is done with three multiplexers. The first one multiplex the LVDS signals to the CoM-Express connector or to a second multiplexer. The second multiplex to the HSSTP connector or to a LVDS/RGB and RGB/HDMI converter. The HDMI interface is then multiplexed into the HDMI connector or again into the CoM-Express connector for using in a daughter board.

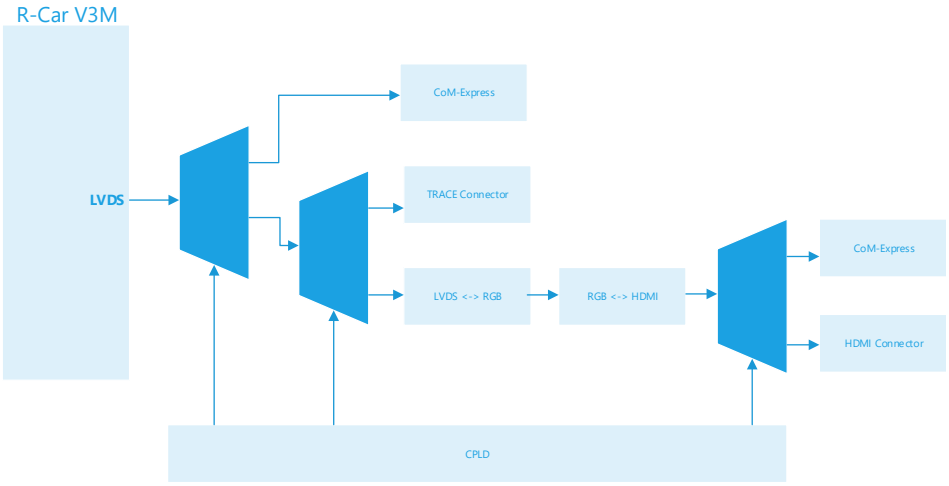

Figure 22. LVDS path multiplexing.

6.2 Selection (via CPLD/GUI)

Click on the “On-board peripheral configuration” tab and select the desired option on the HDMI and LVDS checkbox as shown in the Figure 23.

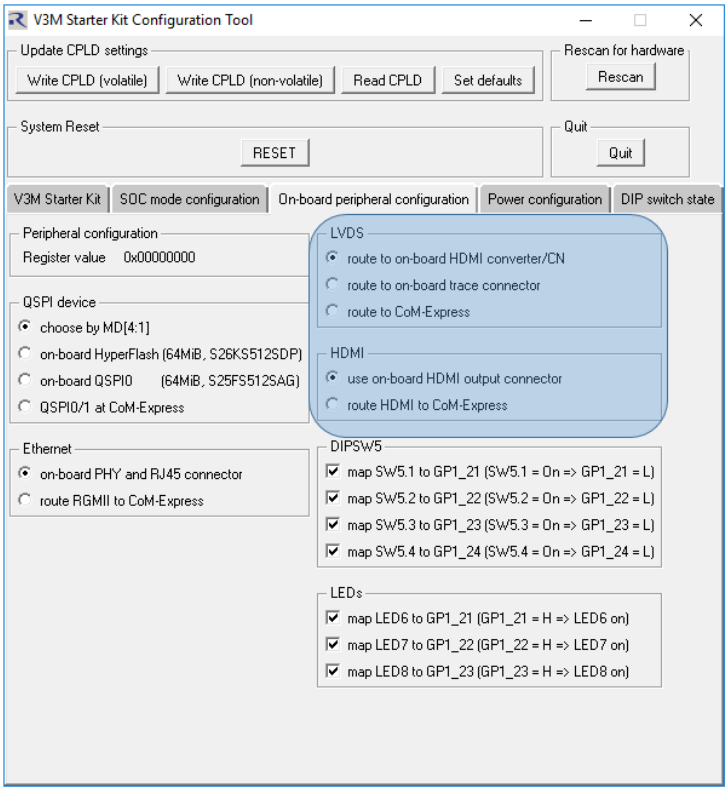

Figure 23. LVDS and HDMI selection using the configuration tool.

7. Trace Connector

7.1 Pinout

Table 11. HSSTP connector pinout.

Pin Number	Function	I/O	Level	Pin Number	Function	I/O	Level
1	GND	Power	0V	2	VCC_1.8V	Power	1.8V
3	GND	Power	0V	4	TCK	I	1.8V
5	GND	Power	0V	6	GND	Power	0V
7	HSSTP_CH2_P	O	HSSTP	8	TMS	I	1.8V
9	HSSTP_CH2_N	O	HSSTP	10	TRST#	I	1.8V
11	GND	Power	0V	12	GND	Power	0V
13	HSSTP_CH0_P	O	HSSTP	14	TDI	I	1.8V
15	HSSTP_CH0_N	O	HSSTP	16	TDO	O	1.8V
17	GND	Power	0V	18	GND	Power	0V
19	HSSTP_CLK_P	O	HSSTP	20	PRESET#	I/O Open Drain	1.8V
21	HSSTP_CLK_N	O	HSSTP	22	NC	-	-
23	GND	Power	0V	24	GND	Power	0V
25	HSSTP_CH1_P	O	HSSTP	26	GND	Power	0V
27	HSSTP_CH1_N	O	HSSTP	28	GND	Power	0V
29	GND	Power	0V	30	GND	Power	0V
31	HSSTP_CH3_P	O	HSSTP	32	NC	-	-
33	HSSTP_CH3_N	O	HSSTP	34	GND	Power	0V
35	GND	Power	0V	36	GND	Power	0V
37	GND	Power	0V	38	GND	Power	0V
39	GND	Power	0V	40	GND	Power	0V
41	GND	power	0V	42	GND	power	0V

7.2 HSSTP over LVDS pins

The HSSTP interface is used as a trace debug. When using the trace debug interface the video output is not available.

The HSSTP trace connector and the video output are connected to the same LVDS buffer.

8. Ethernet

8.1 Multiplexing drawing

As shown in Figure 24, the RGMII interface can be multiplexed to the PHY and RJ45 connector or to a daughter board via CoM-Express connector.

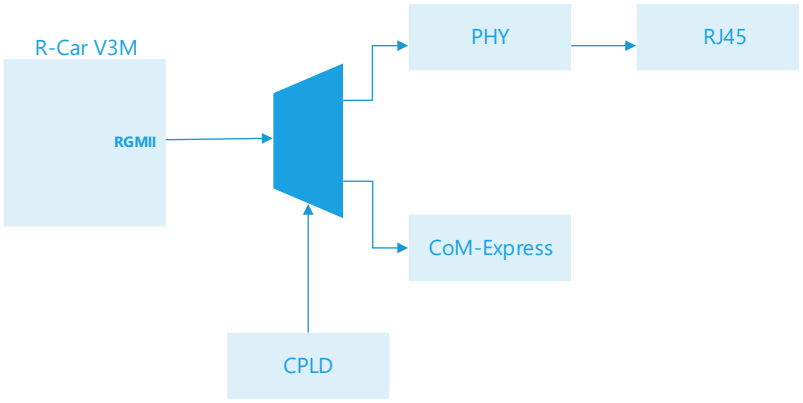

Figure 24. Ethernet RGMII interface multiplexing.

8.2 Selection (via CPLD/GUI)

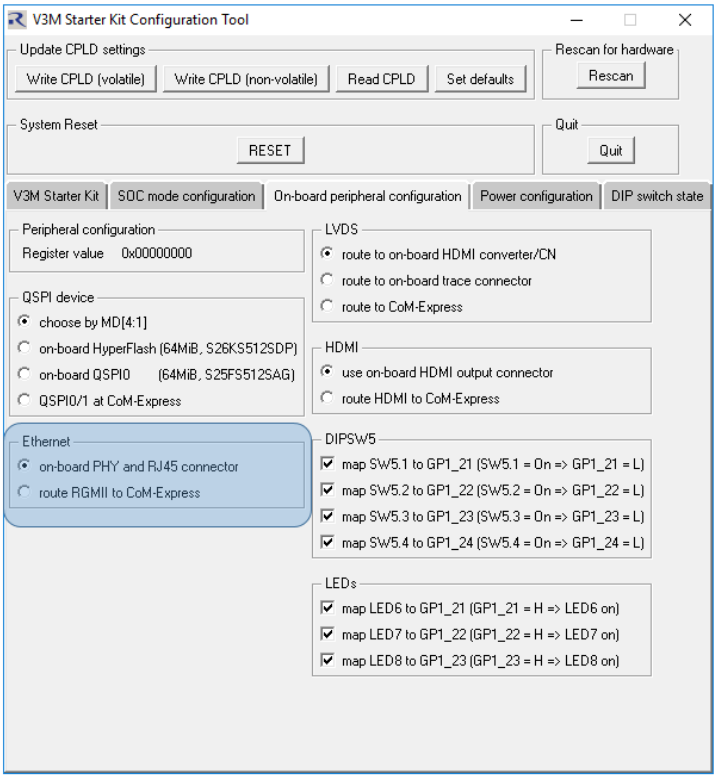

Figure 25. Ethernet selection.

9. Software LEDs

9.1 LED 6 / LED 7 / LED 8 switching (via CPLD)

The Starter Kit contains three user LEDs: LED 6, LED 7 and LED 8. These can be mapped to the SoC GPIOs GP1_21, GP1_22 and GP1_23. This feature can be configured by the LEDs checkbox available under the On-board peripheral configuration tab of the V3M Starter Kit configuration tool. Refer to the diagram shown in Figure 26.

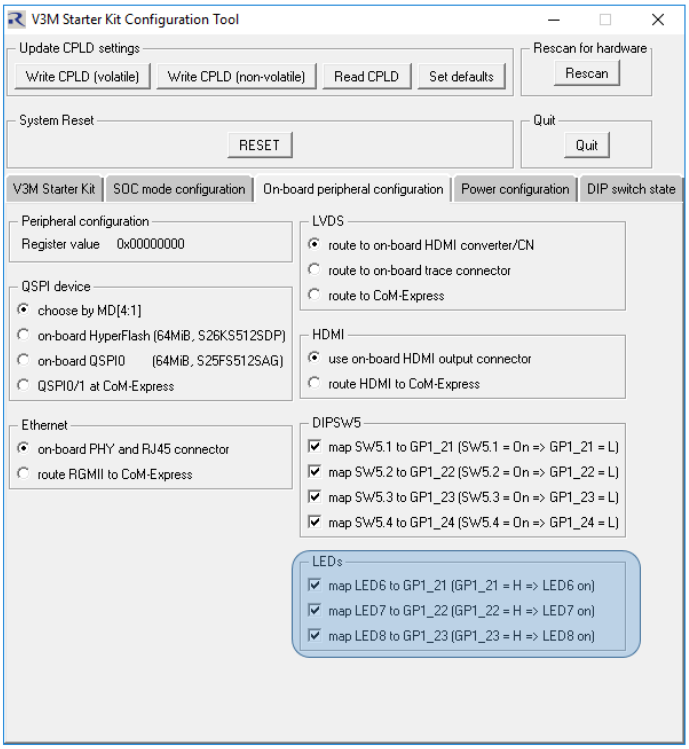

Figure 26. LED switching.

10. Software DIPSW

10.1 Drawing of configuration

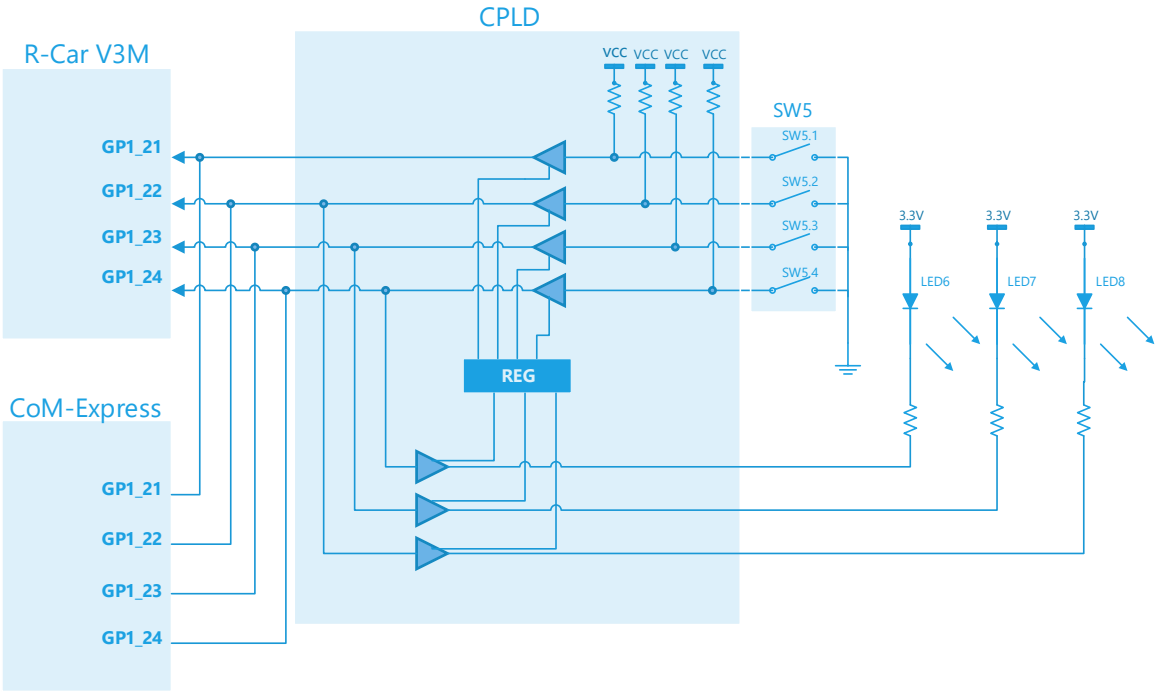

Figure 27. SW5 drawing of configuration.

The DIPSW5 is connected to the GP1_21, GP1_22, GP1_23 and GP1_24 through a tristate buffer. When the buffer is enabled the GPIOs can read the value of the of DIPSW5.

10.2 SW5 available depending on CPLD

The SW5 can be also mapped to the corresponding SoC GPIOs. This can be do with the DIPW5 checkbox available under the On-board peripheral configuration tab on the V3M Starter Kit Configuration Tool.

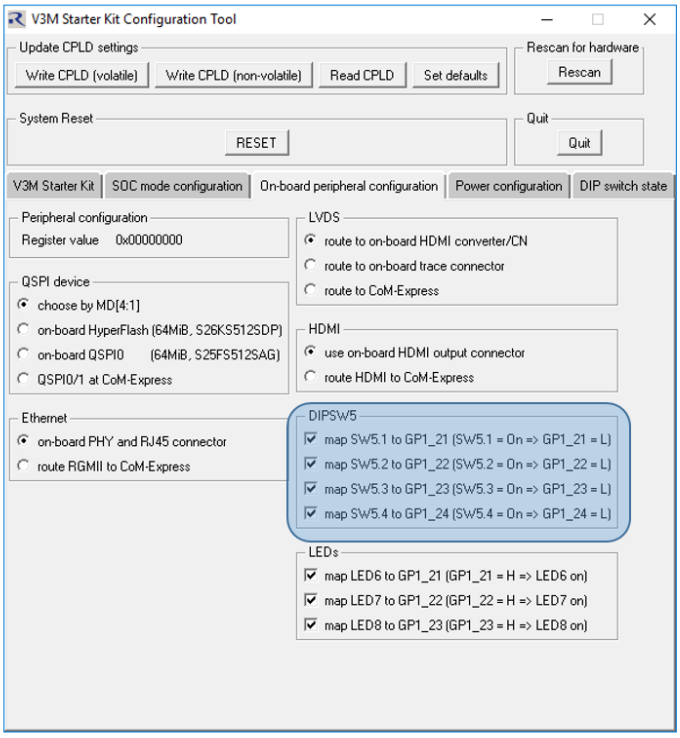

Figure 28. SW5 switching by CPLD.

11. Power switching for domains VDDQ_DU and VDDQ_VIN01

11.1 Overview

The power domains VDDQ_DU and VDDQ_VIN01 can be set to work at 3.3V or 1.8V. By default, is set to 3.3V. This should be considered when using the V3M Starter Kit to provide proper operation and avoid possible device damages on daughter boards connected to the CoM-Express connector.

11.2 Drawing of configuration

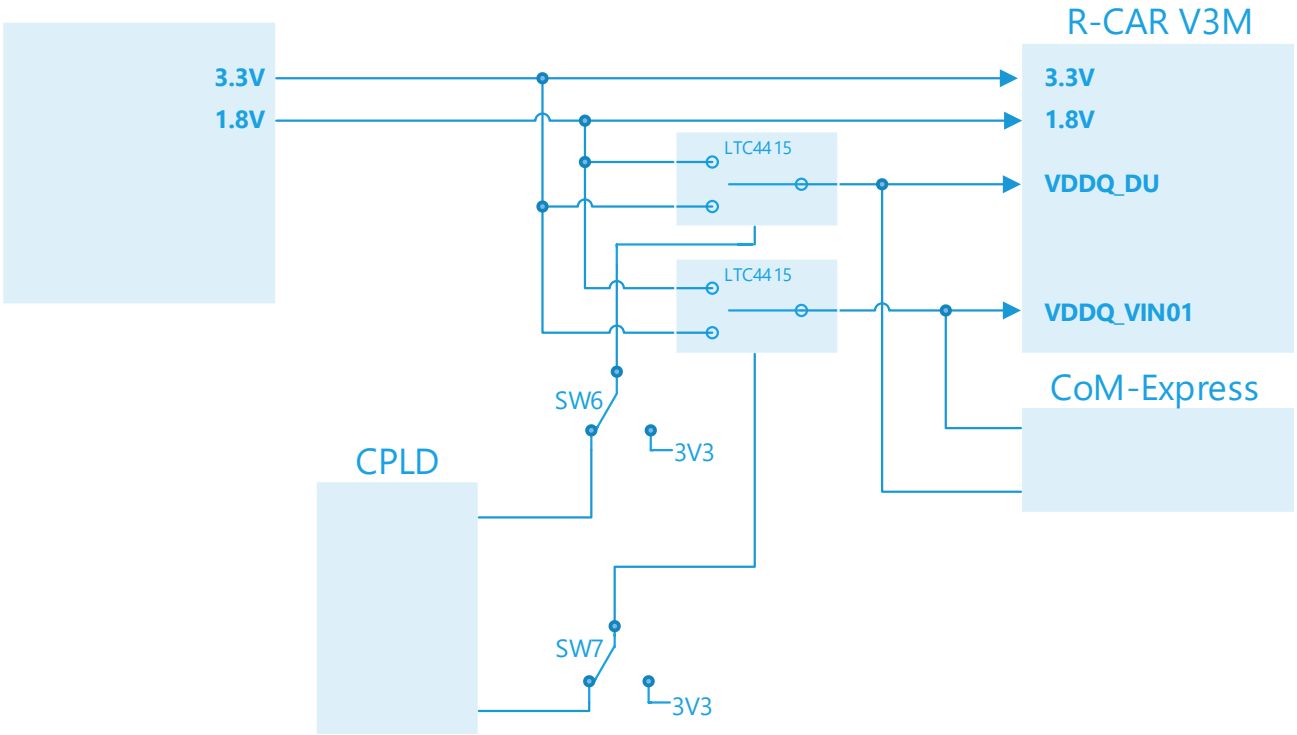

Figure 29. Power switching.

11.3 Power up sequence for 3.3V

During power up sequence the PMIC provides first 1.8V and then 3.3V as shown in Figure 30.

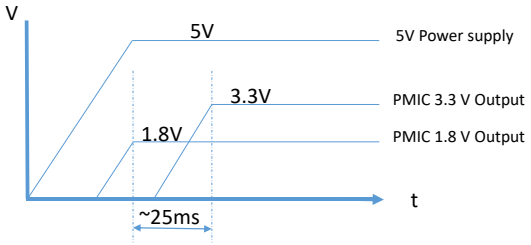

Figure 30. Power-up sequence.

Note: Special attention must be paid when using daughter boards connected to the CoM-Express connector and the settings of VDDQ_VIN01 and VDDQ_DU are set to 3.3V. Both domains are available on the CoM-Express connector. An incorrect voltage level on these domains may damage the daughter board.

The power-up sequence may also cause a wrong operation in such devices connected to the due to the 3.3V power deliver delay between 1.8V and 3.3V.

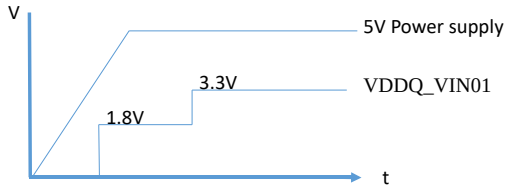

Figure 31. VDDQ_VIN01 voltage at start-up when set to 3.3V.

11.4 Power settings configuration

The VDDQ_DU and VDDQ_VIN01 settings can be configured with the V3M Starter Kit Configuration tool under the tab “Power configuration”.

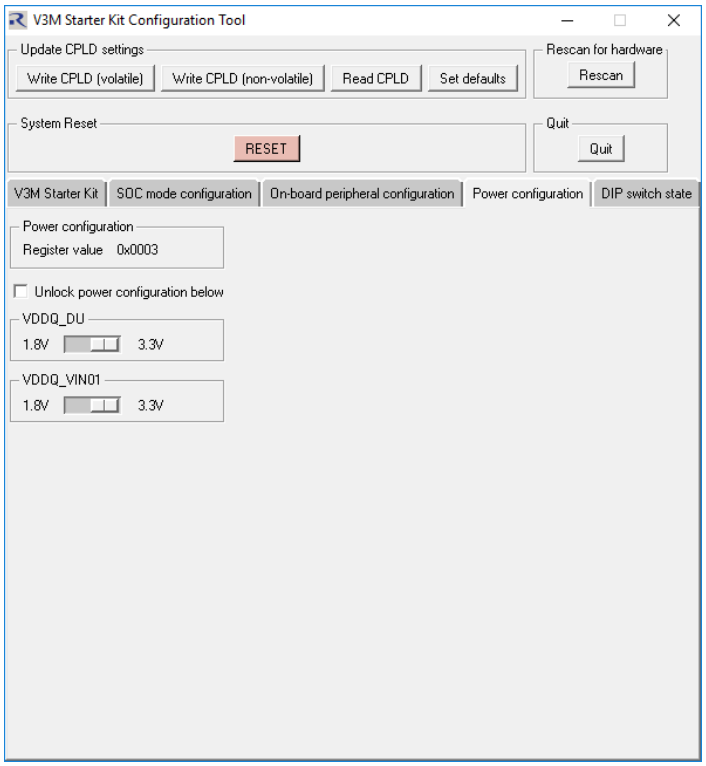

Figure 32. Power settings configuration

If the user needs to apply a custom setting, then is required to check box “Unlock power configuration below”.

Be aware that an incorrect power setting may damage a daughter board connected to the CoM-Express connector.

SW6/SW7 need to be in the “CPLD” position, i.e.
CPLD Position: Slider at the physical switch marking (white bar).
3.3V Position: Slider at the opposite side of the physical switch marking (white bar).

12. Reset

12.1 Drawing of configuration

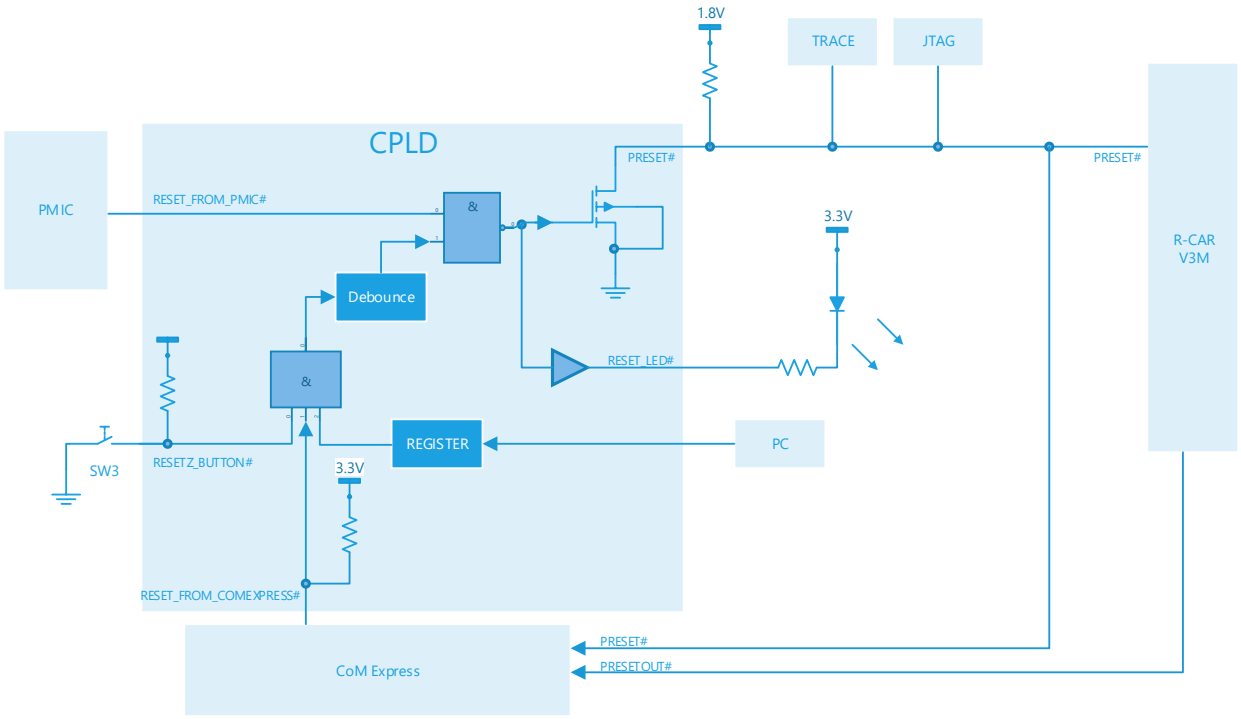

Figure 33. Reset drawing of configuration.

The system reset is controlled by the CPLD.

The CPLD receives different reset sources and generates a controlled reset output which is applied to the SoC. Note that the reset coming from SW3, PC and CoM-Express connector is debounced. The mode pins are latched during reset. The CPLD drive the mode pins during this state. Refer to chapter 2 for further details.

The different reset sources are shown in Figure 33.

- PMIC
- JTAG
- TRACE
- SW3
- PC
- CoM-Express Connector

13. Serial communications

13.1 Overview

SCIF0 is routed to the FT232 USB to UART converter and CN3 CoM-Express connector in parallel.

When the SCIF0 is used on CoM-Express connector, the CPLD held the FT232 in reset state a release the lines so that it can be used by some external device placed in a daughter board.

13.2 SCIF0 block diagram

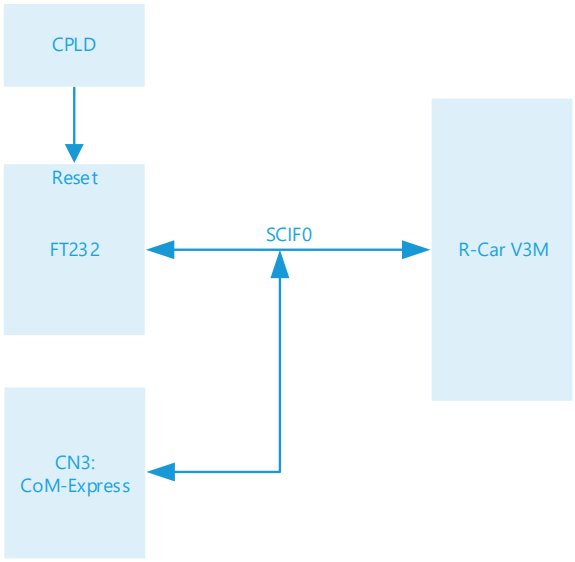

Figure 34. SCIF0 block diagram

14. Booting by SCIF0 (Serial Interface)

14.1 Booting procedure

The V3M Starter Kit needs to be configured to “boot from” SCIF0 interface

- Connect the Mini-USB cable from CN9 to a PC. (Be aware that the installation of the FT232R driver may take several seconds.)
- Execute the V3M Starter Kit Configuration Tool
- In “MODE setting” select “Set by this register”
- In “Boot from [MD4/3/2/1]” select “SCIF0
- Press “Write CPLD (volatile)” or “Write CPLD (non-volatile)”. When CPLD is written as volatile this setting will be reset anytime the board is power-cycled.
- Close the GUI window

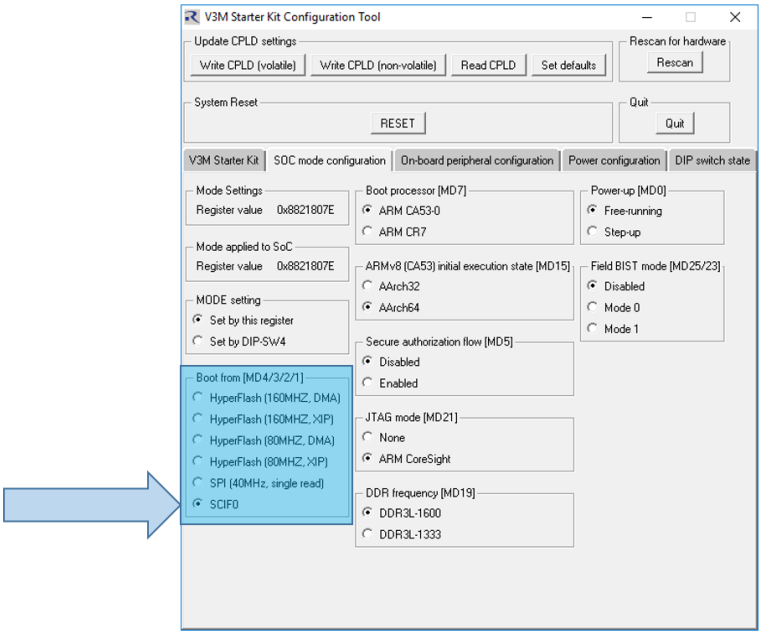

Figure 35. Boot source selection.

14.2 Terminal

Open a terminal program like Tera-Term and configure a new serial communication to the corresponding COM port.

- Configure a new session with: 115200bd, 8N1
- Reset the V3M SoC by pressing on the SW3

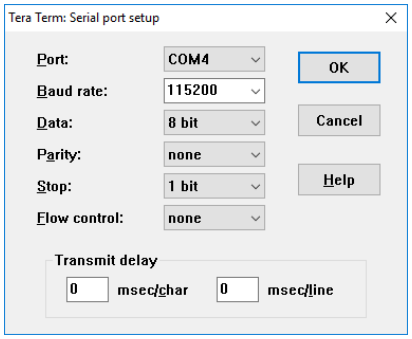

Figure 36. Terminal configuration.

The following message is shown in the terminal console:

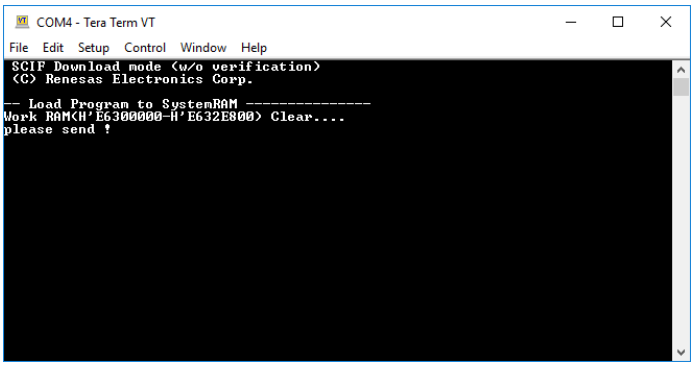

Figure 37. Ready to receive code.

The next step is to send the code to be executed e.g. the Mini-Monitor terminal program to the System-RAM.

14.3 Uploading Mini-Monitor

To copy the Mini-Monitor program into the System-RAM we need to send the corresponding Motorola (.mot) binary file:

Go to: File -> Send file.

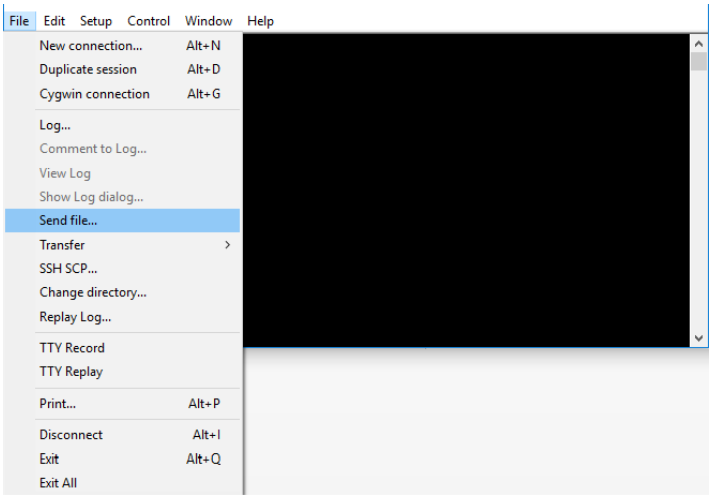

Figure 38. Tera-Term. Send Mini-Monitor to the System RAM.

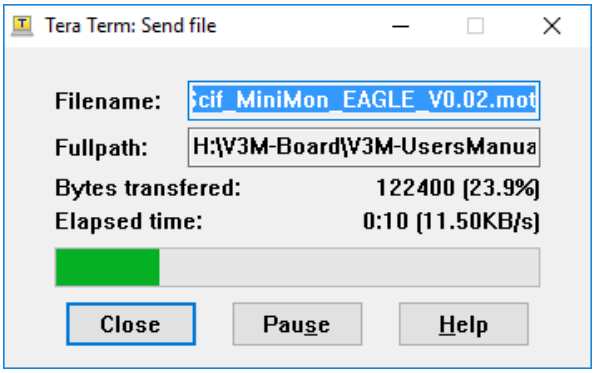

Figure 39. Upload process.

The upload will take approx. 1 minute. Once is finished the program remain waiting for a new command line. This will be explained in the following chapter.

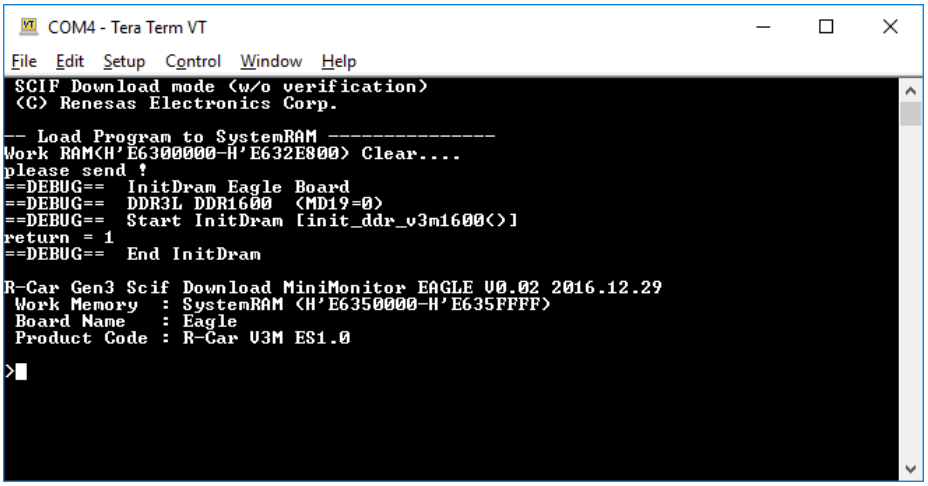

Figure 40. Command terminal.

15. Procedure for flashing on-board QSPI and Hyper-Flash memories

15.1 Hardware set-up

On the previous chapter we have written on the SoC System-RAM the Mini-Monitor program. Now we are going to use this terminal program for flashing the on-board QSPI and Hyper-Flash memory.

First of all we have to reconfigure the hardware settings by using the V3M configuration tool. If you have open a terminal session, please close it now. Otherwise the communication with the CPLD would not be possible.

Now start the V3M configuration tool and select the corresponding device. In this case we are going to select the "on-board QSPI0" option under the "QSPI device" checkbox.

Now update the CPLD by clicking on Write CPLD (Volatile or non-volatile)

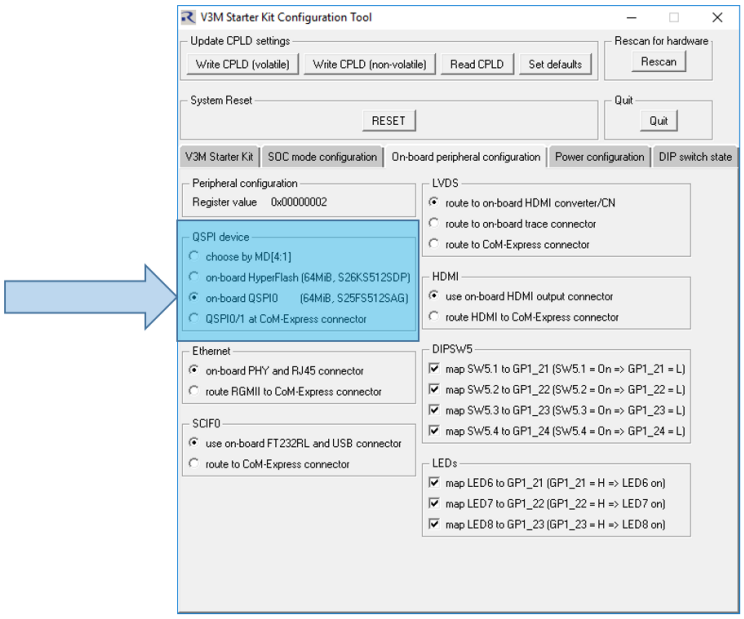

Figure 41. QSPI device selection.

15.2 QSPI Flash Erasing

- Open a TeraTerm session
- Write: xcs
- You will be asked: **ALL ERASE SpiFlash or Hyper-Flash memory?**
- Type Y to accept.
- Type 1 to select the QSPI Flash Option
- You will be asked to check the position of the switch4.
- Check it and push Y Key
- You will be asked to check the position of the switch4.8

Check it and push Y Key

Figure 42. Mini-Mon memory erase.

This process will takes some time (3-4min). Wait until the process is finished.

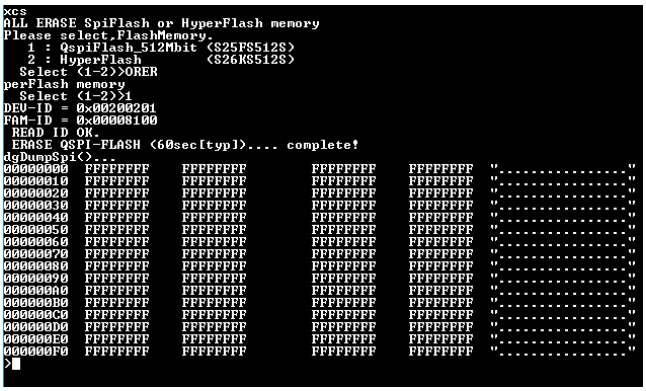

Figure 43. Memory erase.

15.3 Writing the boot loader (IPL) to the QSPI (sector 1)

Once the Mini-monitor is running. Type:

>xls

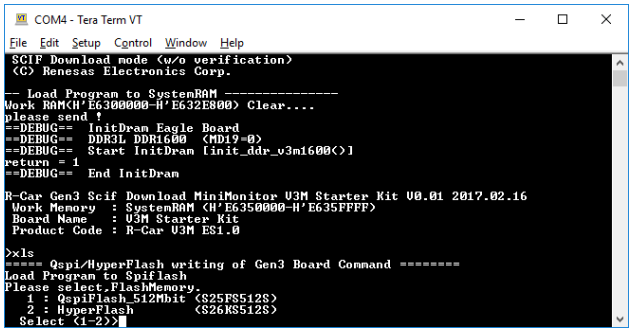

Figure 44. Mini-Mon load program to QSPI flash.

Select the option 1: QspiFlash_512Mbit

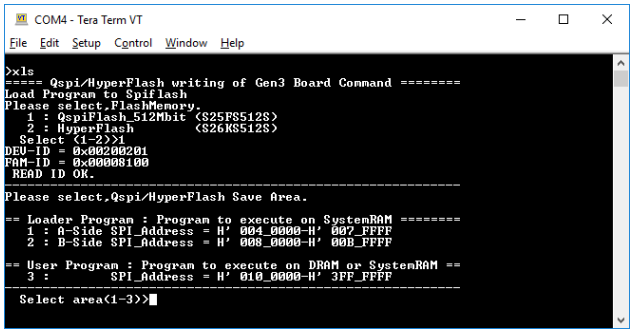

Figure 45. Program area selection.

You will be asked to indicate in which area the program should be saved.

Select the save area and then send the corresponding .mot file.

15.4 Hyper-Flash Erasing

Follow the procedure indicated on the section 15.2 but now selecting the on-board Hyper-Flash as shown in Figure 46.

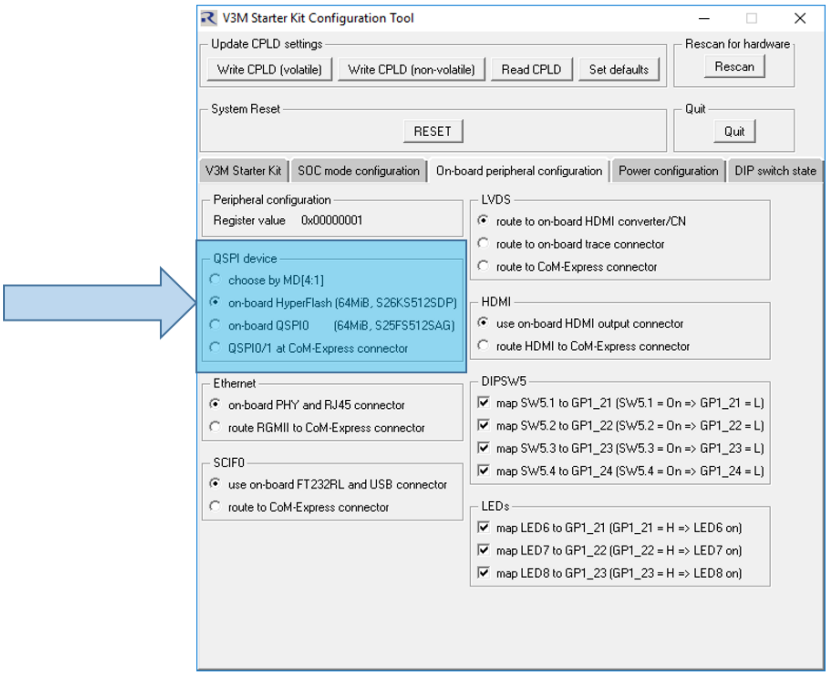

Figure 46. QSPI device selection.

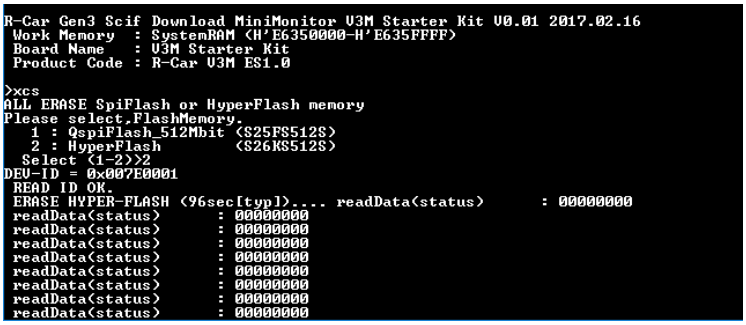

Figure 47. Memory erase process.

15.5 Writing the boot loader (IPL) to the Hyper-Flash (sector 1)

Follow the same procedure as in section 15.3. Make sure to select the Hyper-Flash memory option in the GUI.

16. V3M device hardware pin allocation

16.1 GPIO table

Table 12. GPIO table.

GPIO	Function	Peripheral	Connector
GP1_21	DIPSW5.1 / LED6		
GP1_22	DIPSW5.2 / LED7		
GP1_23	DIPSW5.3 / LED8		
GP1_24	DIPSW5.4		
GP1_25	SCIF_CLK_B	SCIF0 (Uart)	OSC6
GP4_5	TX0	SCIF0 (Uart)	CN9
GP4_4	RX0	SCIF0 (Uart)	CN9
GP4_0	SCL0	I2C0	PMIC, HDMI transmitter
GP4_1	SDA0	I2C0	PMIC, HDMI transmitter
GP1_0	INT# from PMIC	Interrupt	
GP1_20	INT# from HDMI	Interrupt	
GP5_0	QSPI0_SPCLK	QSPI0	
GP5_5	QSPI0_SSL	QSPI0	
GP5_1	QSPI0_MOSI_IO1	QSPI0	
GP5_2	QSPI0_MISO_IO1	QSPI0	
GP5_3	QSPI0_IO2	QSPI0	
GP5_4	QSPI0_IO3	QSPI0	
GP5_6	QSPI1_SPCLK	QSPI1	
GP5_11	QSPI1_SSL	QSPI1	
GP5_7	QSPI1_MOSI_IO0	QSPI1	
GP5_8	QSPI1_MISO_IO1	QSPI1	
GP5_9	QSPI1_IO2	QSPI1	
GP5_10	QSPI1_IO3	QSPI1	
GP5_12	RPC_RESET#		
GP5_14	RPC_INT#		
GP1_16	PHY_RESET	Ethernet (Gbit/AVB)	
GP1_13	AVB0_TXCREFCLK	Ethernet (Gbit/AVB)	
GP1_8	AVB0_TXC	Ethernet (Gbit/AVB)	
GP1_7	AVB0_TX_CTL	Ethernet (Gbit/AVB)	
GP1_9	AVB0_TD0	Ethernet (Gbit/AVB)	
GP1_10	AVB0_TD1	Ethernet (Gbit/AVB)	

GPIO	Function	Peripheral	Connector
GP1_11	AVB0_TD2	Ethernet (Gbit/AVB)	
GP1_12	AVB0_TD3	Ethernet (Gbit/AVB)	
GP1_2	AVB0_RXC	Ethernet (Gbit/AVB)	
GP1_1	AVB0_RX_CTL	Ethernet (Gbit/AVB)	
GP1_3	AVB0_RD0	Ethernet (Gbit/AVB)	
GP1_4	AVB0_RD1	Ethernet (Gbit/AVB)	
GP1_5	AVB0_RD2	Ethernet (Gbit/AVB)	
GP1_6	AVB0_RD3	Ethernet (Gbit/AVB)	
GP1_18	AVB0_LINK	Ethernet (Gbit/AVB)	
GP1_15	AVB0_MDC	Ethernet (Gbit/AVB)	
GP1_14	AVB0_MDIO	Ethernet (Gbit/AVB)	
GP1_17	AVB0_PHY_INT	Ethernet (Gbit/AVB)	
GP0_0	MD00	MD function	CoM-Express & CPLD
GP0_1	MD01	MD function	CoM-Express & CPLD
GP0_2	MD02	MD function	CoM-Express & CPLD
GP0_3	MD03	MD function	CoM-Express & CPLD
GP0_4	MD04	MD function	CoM-Express & CPLD
GP0_5	MD05	MD function	CoM-Express & CPLD
GP0_6	MD07	MD function	CoM-Express & CPLD
GP0_7	MD08	MD function	CoM-Express & CPLD
GP0_20	MD09	MD function	CoM-Express & CPLD
GP0_21	MD13	MD function	CoM-Express & CPLD
GP2_1	MD14	MD function	CoM-Express & CPLD
GP2_2	MD15	MD function	CoM-Express & CPLD
GP2_3	MD16	MD function	CoM-Express & CPLD
GP2_4	MD18	MD function	CoM-Express, CPLD, eMMC Reset
GP2_5	MD19	MD function	CoM-Express & CPLD
GP2_9	MD21	MD function	CoM-Express & CPLD
GP2_10	MD23	MD function	CoM-Express & CPLD
GP2_11	MD25	MD function	CoM-Express & CPLD
GP2_12	MD26	MD function	CoM-Express & CPLD
GP1_19	Used for CPLD	CPLD	CoM-Express & CPLD
GP0_19			CoM-Express
GP2_8			CoM-Express
GP2_0			CoM-Express
GP3_2			CoM-Express
GP3_3			CoM-Express
GP3_4			CoM-Express
GP3_0			CoM-Express
GP3_1			CoM-Express
GP2_13			CoM-Express
GP2_14			CoM-Express
GP2_15			CoM-Express
GP2_16			CoM-Express

GPIO	Function	Peripheral	Connector
GP1_26			CoM-Express
GP1_27			CoM-Express
GP3_15			CoM-Express
GP3_16			CoM-Express
GP0_8			CoM-Express
GP0_9			CoM-Express
GP0_10			CoM-Express
GP0_11			CoM-Express
GP0_12			CoM-Express
GP0_13			CoM-Express
GP0_14			CoM-Express
GP0_15			CoM-Express
GP0_16			CoM-Express
GP0_17			CoM-Express
GP0_18			CoM-Express
GP5_13			CoM-Express
GP3_10	MMC_CLK	eMMC	
GP3_5	MMC_CMD	eMMC	
GP3_6	MMC_D0	eMMC	
GP3_7	MMC_D1	eMMC	
GP3_8	MMC_D2	eMMC	
GP3_9	MMC_D3	eMMC	
GP3_11	MMC_D4	eMMC	
GP3_12	MMC_D5	eMMC	
GP3_13	MMC_D6	eMMC	
GP3_14	MMC_D7	eMMC	

17. Daughter boards

An optional daughter board may be connected to the V3M Starter Kit board to extend its functionalities.

The customer can use the V3M Starter Kit as a mother board and implement its own products.

For this reason, the V3M Starter Kit has been designed following the standard form factor CoM-Express. Note that only the form factor has been considered. No the electrical interface. Please refer to the CoM-Express pin out attached on this manual.

The V3M Starter Kit may be supplied through the CoM-Express connector.

Figure 48 shows an example of daughter board attached to the V3M Starter Kit.

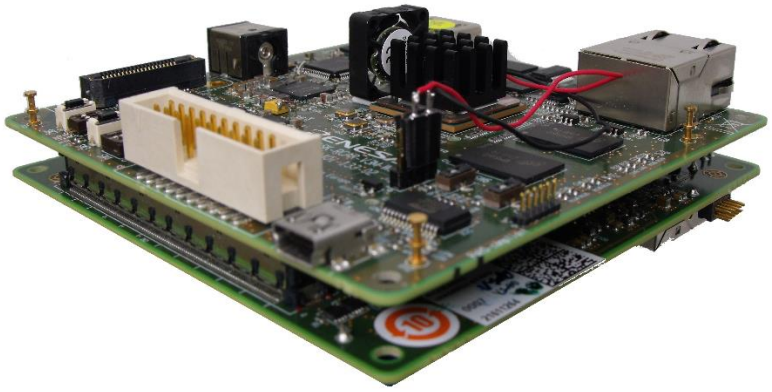

Figure 48. Daughter board example.

18. List of known limitations

18.1 QSPI speed limitation

- Using the V3M Starter Kit, you cannot access the QSPI flash at 80 MHz when using DDR mode. This only affects DDR (double data rate) at 80 MHz, e.g. when using the flash commands 4DDRQIOR (0xEE) or DDRQIOR (0xED). Any other commands running at SDR (single-data-rate) will work without issues. Also, using DDR commands at 33 MHz will work without issues. The reason for this limitation is that this product allows to switch between three options: on-board Hyper-Flash, on-board QSPI or external QSPI. This switching option affects the signal quality. This is a design limitation and will remain on all revisions of this product.

18.2 eMMC availability

- Early versions of V3M Starter Kit previous to V3.00 does not support eMMC. V3M Starter Kits V3.00 and later have an eMMC flash assembled.

18.3 Initial power-up

- Early versions of the V3M Starter Kit sometimes do not power-up correctly or delayed. When the power supply is plugged into the board main power input (CN5), or if the power supply is turned on, the board should power up directly. This is indicated by the LED for 3.3V lighting up (LED1). Please do not confuse this with the input power LED2. However, sometimes this LED1 remains off. In that case, as a work-around, please un-plug and re-plug the board in short sequence until LED1 lights up. This issue only affects the boards with S/N 0001 through 0025. Newer versions of the board do not show this behavior. The affected boards may be updated to overcome this issue.

18.4 HDMI EDID read errors

- When reading the EDID information from an HDMI monitor, you may experience read errors. This issue can be identified by evaluating the EDID embedded checksum. This issue only affects the boards with S/N 0001 through 0025. Newer versions of the board do not show this behavior. The affected boards may be updated to overcome this issue.

18.5 Multiplexors and Switches

- The use of multiplexors and switches effects on the signal integrity and time delays on the CoM-Express interface compared to a real R-CAR design. Please observe that by connecting a daughter board.

18.6 CPLD updates

- **2018/10/05**
  a) If the on-board serial port (Mini-USB connector CN9) is not supplied (ie. connected to a PC), it will interfere with the SCIF0 of the add-on board. After this update the add-on SCIF0 will work as expected.
  b) when the reset button is pressed, the USB connection is shortly lost. This may cause the PC to close a terminal. After this update the USB connection is unaffected during reset.
- **2018/08/29** If the on-board serial port (Mini-USB connector CN9) is not supplied (ie. connected to a PC), it will interfere with the SCIF0 of the add-on board. After this update the add-on SCIF0 will work as expected.
- **2018/03/21** After power-up, the reset button had to be pressed, before the code stored in QSPI or HyperFlash is executed. After this update the system will boot correctly directly after power-up; no need to press the reset button anymore.
- **2018/03/10** When using Win10, downloading of the CPLD sometimes caused the CPLD to become corrupt. After this update it is possible to successfully program the CPLD.
- **2017/10/04** The signal QSPI1_SPCLK was not output to the CoM-Express connector when "QSPI device: at CoM-Express connector" was selected in the configuration GUI. After this update it is possible to use QSPI CH1.
- **2017/05/09** After power-up, the HDMI output previously may have remained in an inoperable state until the hardware was power-cycled. After this update the HDMI output will operate correctly after every power-up.
- **2017/04/28** After power-up, the reset button had to be pressed, before the code stored in QSPI or HyperFlash is executed. After this update the system will boot correctly directly after power-up; no need to press the reset button anymore.

19. Attachments

19.1 Schematic

19.2 Mechanical drawing

19.3 CoM-Express pin out

Please find these documents embedded in this pdf file.

Revision History	V3M Starter Kit Hardware Manual

Rev.	Date	Description	
		Page	Summary
1.00	May 29, 2017	—	First Edition issued
1.01	June 12, 2017		- Document name corrected - Word “Overview” deleted on header
2.00	Dec 21, 2017		- Table 6. Boot source selection. Errata corrected on switch setting for QSPI. - Some drawings have been newly formatted. - Changes on text. - Product order number
2.20	Jan 21, 2019		- Figure 24 contains an error on version 2.00. Has been corrected. - Updated - 1.5 V3M Starter Kit block diagram. New. - 1.6 Board releases. New - Table 4. SoC mode.Updated. - 3.2 JTAG Connector. New - 3.3 Switches. New - 4.3 Volatile/Non-volatile. New - 5.5 eMMC memory. New - 13 Serial communications. New - 18.1 QSPI speed limitation. Updated. - Table 5. Typo in eMMC size - Table 12 Updated - Figure 29. Updated - Figure 33 Updated - General typos and document improvement
2.30	Jan 24, 2019		- New R-Car logo

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