User's Manual

32

RH850 Evaluation Platform

RH850/F1x 100-pin
RH850/R1x 100-pin

User's Manual: Piggyback Board V3

Y-RH850-F1X-100PIN-PB-T1-V3

The latest version of this document can be obtained from the following web location:
Y-RH850-F1X-100PIN-PB-T1-V3 Documents

All information contained in these materials, including products and product specifications, represents information on the product at the time of publication and is subject to change by Renesas Electronics Corp. without notice. Please review the latest information published by Renesas Electronics Corp. through various means, including the Renesas Electronics Corp. website (https://www.renesas.com)

Renesas Electronics
www.renesas.com

Rev. 1.04 August 2021

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

1. Handling of Unused Pins
   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.
   – The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   – The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   – The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable.
   When switching the clock signal during program execution, wait until the target clock signal has **s**tabilized.
   – When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.
   – The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

TABLE OF CONTENTS

CHAPTER 1 INTRODUCTION 6

1.1 PACKAGE COMPONENTS 7

CHAPTER 2 OVERVIEW 8

2.1 BOARD EESS-0401-139-01 8
2.2 BOARD D015312-06-V02 9
2.3 MOUNTING OF THE DEVICE 9

CHAPTER 3 JUMPER CONFIGURATION 10

CHAPTER 4 POWER SUPPLY 12

4.1 BOARD POWER CONNECTION 12
4.2 VOLTAGE DISTRIBUTION 13

CHAPTER 5 CLOCK SOURCES 14

CHAPTER 6 DEBUG AND PROGRAMMING INTERFACE 15

CHAPTER 7 CONNECTORS FOR DEVICE PORTS 16

7.1 CONNECTORS TO MAINBOARD 16
7.1.1 Connector CN1 16
7.1.2 Connector CN2 (EESS0401-139-01) 17
7.1.3 Connector CN2 (D015312-06-V02) 19
7.1.4 Connector CN3 20
7.2 CONNECTORS FOR USER ACCESS 22

CHAPTER 8 OTHER CIRCUITRY 23

8.1 PUSH BUTTON FOR RESET 23
8.2 MODE SELECTION 23
8.3 SIGNALLING LEDS 23

CHAPTER 9 PRECAUTIONS 24

9.1 USAGE OF LIN15 24
9.1.1 Adjustments on RH850/X1x Network Mainboard 24
9.1.2 Adjustments on RH850/X2x Mainboard 25

CHAPTER 10 MECHANICAL DIMENSIONS 26

CHAPTER 11 SCHEMATIC OF PCB MARKED "EESS-0401-139-01" 27

CHAPTER 12 SCHEMATIC OF PCB MARKED "D015312-06-V02" 30

CHAPTER 13 REVISION HISTORY 33

Chapter 1 Introduction

The RH850/F1x Application Board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics 32-bit RH850/F1x microcontrollers. The piggyback board (Y-RH850-F1X-100PIN-PB-T1-V3) can be used as a standalone board or it can be connected to a main board (Y-RH850-X1X-MB-Tx-Vx) for extended functionality.

Main features:

- Socket for mounting of device
- Standalone operation of the board
- Direct supply of device voltage (typ. 3.3V-5.0V)
- Device programming capability
- Device debugging capability
- Pin headers for direct access to each device pin
- Reset switch
- MainOSC circuitry
- Signal LEDs
- Jumpers for device mode selection
- Connectors to a main board

This document describes the functionality provided by the piggyback board and guides the user through its operation.

For details regarding the operation of the microcontroller, refer to the refer to the related User's Manual and Datasheet.

This manual describes the following board revisions:

- RH850-F1X-100PIN-PB-T1-V3 Revision_1 (marked "EESS-0401-139-01")
- RH850-F1X-100PIN-PB-T1-V3 Revision_2 (marked "D015312-06-V02")

For differences to the RH850-F1X-100PIN-PB-T1-V2 see the Revision History.

1.1 Package Components

The Y-RH850-F1X-100PIN-PB-T1-V3 product package consists of the items included in below table. After you have unpacked the box, check if your Y-RH850-F1X-100PIN-PB-T1-V3 package contains all these items.

Item	Description	Quantity
D015311#01	RH850/F1x 100pin piggyback board	1
D015383	Documentation CD	1
D010816-24	China RoHS document	1
D015380-24	Product contents List	1
Jumpers (2-way, 0.1”)	In the bag	29
Red Hirschmann 4 mm power lab sockets	In the bag	2
Black Hirschmann 4 mm power lab sockets	In the bag	1
Crystal, HC49, 8 MHz	In the bag	1
Crystal, HC49, 20 MHz	In the bag	1
Crystal, HC49, 24 MHz	In the bag	1

Note: Please keep the Y-RH850-F1X-100PIN-PB-T1-V3 packing box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original packing box when transporting the Y-RH850-F1X-100PIN-PB-T1-V3. If packing of your product is not complete, it may be damaged during transportation.

Chapter 2 Overview

There are 2 different production versions of the piggyback board.

Boards of the first generation have the marking “EESS-0401-139-01”. The boards have an issue in the connection of pin 34 and pin 36 on connector CN2. This is described in *Chapter 9 Precautions.*

Boards of the second generation have the marking “D015312-06-V02”. With these boards the connection on CN2 has been corrected and the precautions described in chapter 9 do NOT apply.

2.1 Board EESS-0401-139-01

Figures 1 and 2 provide the views of the RH850-F1X-100PIN-PB-T1-V3 piggyback board.

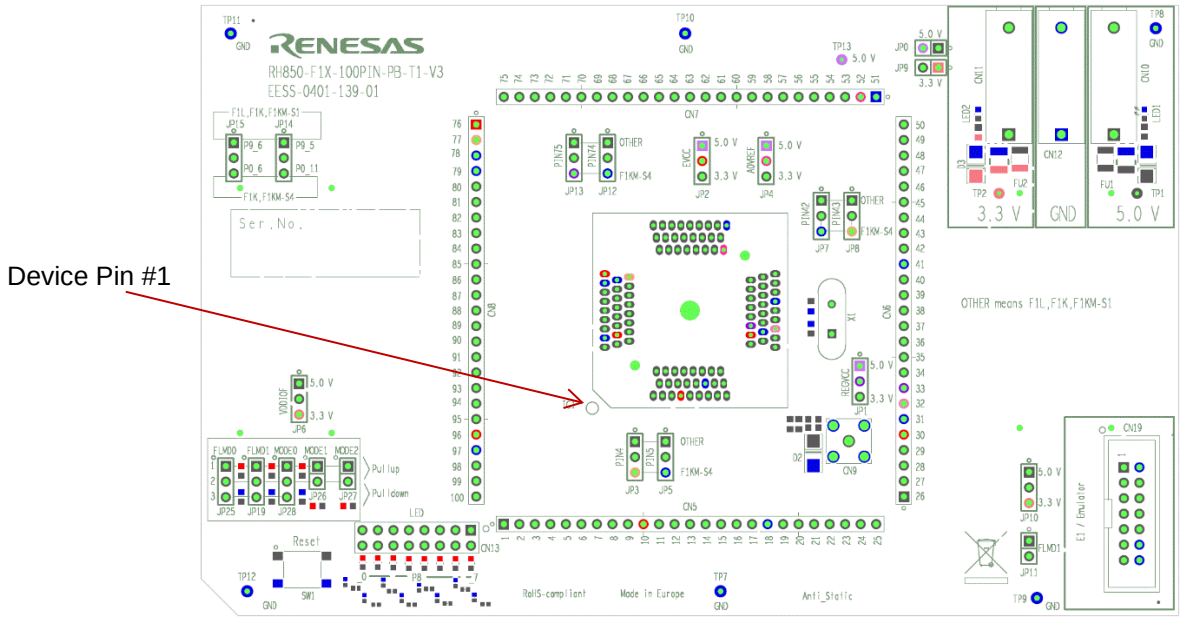


Figure 1 - RH850-F1X-100PIN-PB-T1-V3 top view

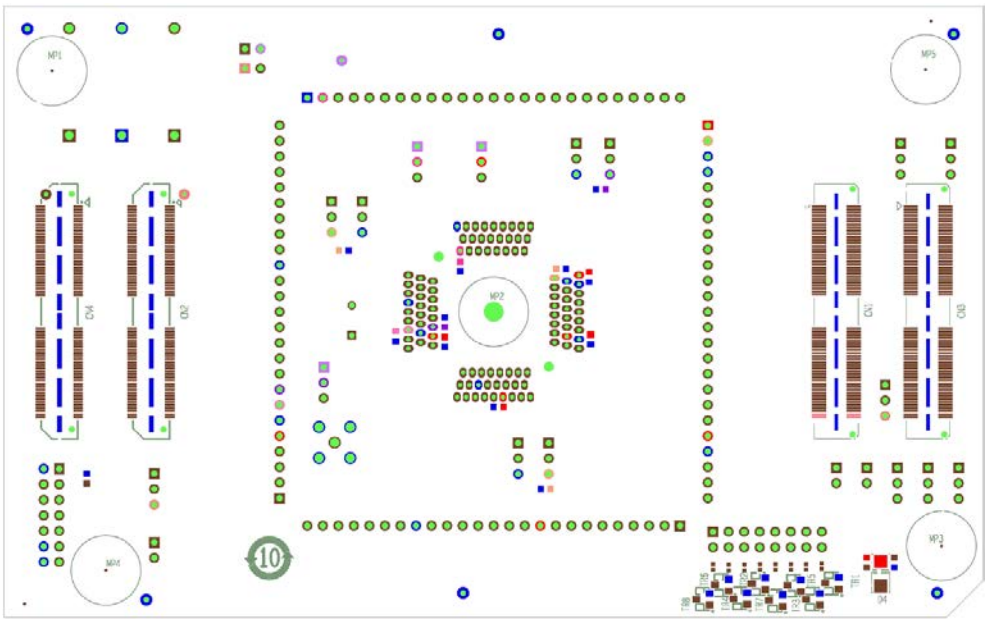


Figure 2 - RH850-F1X-100PIN-PB-T1-V3 bottom view

2.2 Board D015312-06-V02

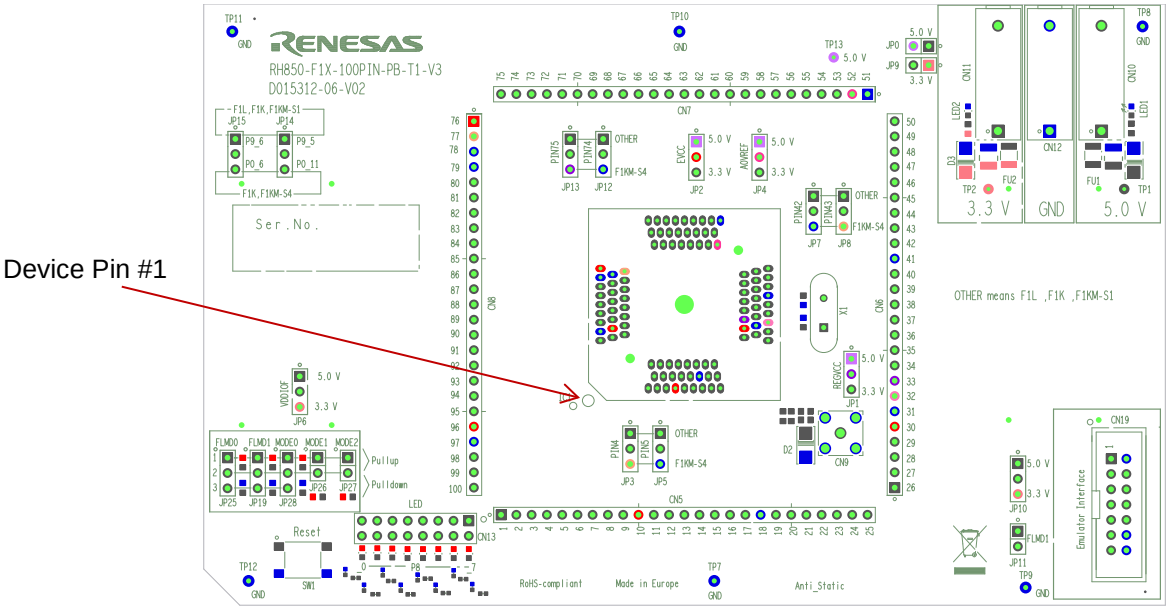


Figure 3 - RH850-F1X-100PIN-PB-T1-V3 top view

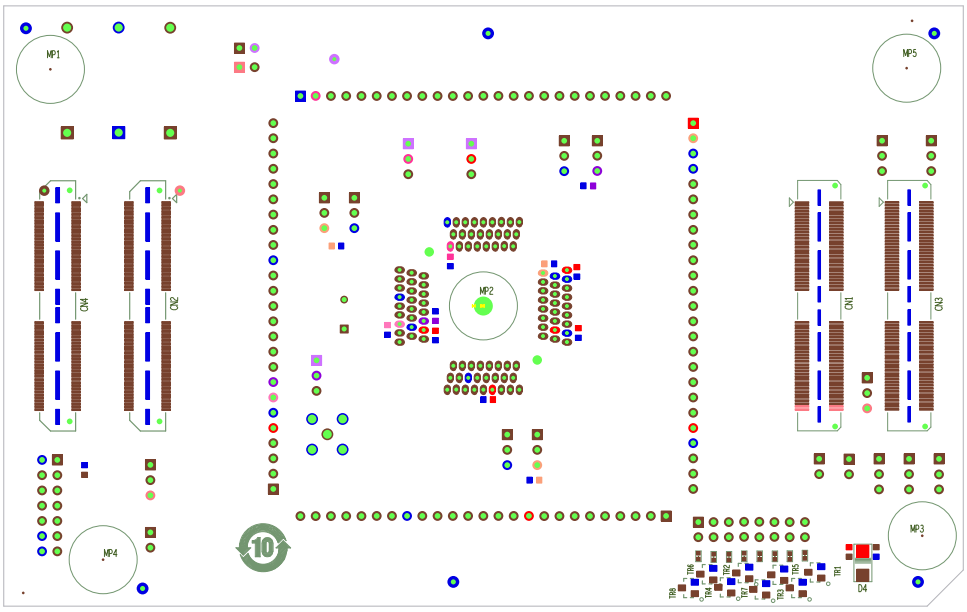


Figure 4 - RH850-F1X-100PIN-PB-T1-V3 bottom view

2.3 Mounting of the Device

The board is designed for use with the following devices, all in 100pin package:

- RH850/F1L
- RH850/R1L
- RH850/F1K
- RH850/F1KM-S1
- RH850/F1KM-S2
- RH850/F1KM-S4

The device must be placed inside the socket IC1. To insert the device, press down the lid, align the #1 pin of the device to the #1pin of the socket, insert the device inside the socket and release the lid.

Chapter 3 Jumper Configuration

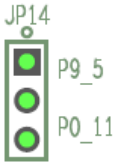
The function of the board can be configured via jumpers. This chapter describes the standard configuration, i.e. jumper setting for the intended devices. For the supported function of the used device, please refer to the corresponding HW user's manual.

Jumper settings are valid for both generations of Y-RH850-F1X-100PIN-PB-T1-V3, even if the picture in *Figure 5 - Example for jumper settings* shows the generation 1 board.

The table has the following meaning:

- x-y: Connect the pins x and y; valid for 3-pin jumpers (e.g. JP14)

Pin #1 can be identified by a small circle in the vicinity of the jumper.



Depending on the used device a configuration of several jumpers is required. The detailed configuration is shown below:

Jumper	F1L	R1L	F1K	F1KM-S1	F1KM-S2 F1KM-S4	Function
JP3	1-2	1-2	1-2	1-2	2-3	Selection pin #4: Either P10_15 or ISOVCL
JP5	1-2	1-2	1-2	1-2	2-3	Selection pin #5: Either P11_0 or VSS
JP7	1-2	1-2	1-2	1-2	2-3	Selection pin #42: Either P8_0 or VSS
JP8	1-2	1-2	1-2	1-2	2-3	Selection pin #43: Either P8_1 or ISOVCL
JP12	1-2	1-2	1-2	1-2	2-3	Selection pin #74: Either P9_5 or VSS
JP13	1-2	1-2	1-2	1-2	2-3	Selection pin #75: Either P9_6 or REGVCC
JP14 [1-2]	Close	-	Either	Close	-	Selection of PWM34
JP14 [2-3]	-	-	- or	-	Close	Either from P9_5 or P0_11
JP15 [1-2]	Close	-	Either	Close	-	Selection of PWM35
JP15 [2-3]	-	-	- or	-	Close	Either from P9_6 or P0_6

The jumper settings also are shown in the picture on the next page.

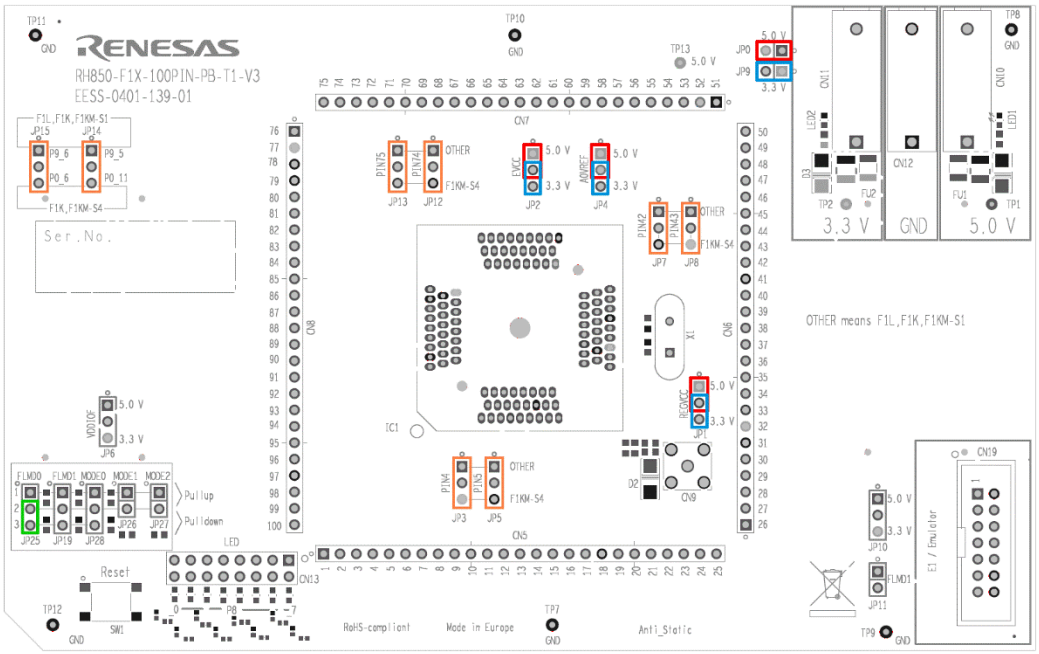


Figure 5 - Example for jumper settings

- The green jumper JP25 for FLMDO0 always must be closed (at the position 2-3) for a ‘normal’ (user mode and debug) operation of the device.
- The red jumpers must be set for a single “Voltage 1” (typ +5.0V) operation of the device.
- The blue jumper must be set for a single “Voltage 2” (typ +3.3V) operation of the device.
- The orange jumpers must be selected depending on the used device. See the printing on the board for the applicable setting.

For jumper settings related to the device operation mode, refer to chapter *8.2 Mode Selection*

Chapter 4 Power Supply

4.1 Board Power Connection

For operation of the device, a supply voltage must be connected to the board. Though a single supply voltage is sufficient to operate the device, it is possible to power the board with two different voltages.

Within this document the following voltages are considered as ‘typical’ connections:

Voltage1 = 5.0V

Voltage2 = 3.3V

The following connectors are available to supply those voltages:

- Three 4mm ‘banana-type’ connectors:
  - Two red connectors for voltages *Voltage1* (CN10) and *Voltage2* (CN11)
  - A black connector for VSS connection on CN12

  Note: The three connectors are supplied with the board but are not assembled.
- The E2 emulator, that is used for debugging or flash programming, can also supply a single operating voltage (“DBG_Voltage”).
  The voltage is programmable via the E2 configuration as 3.3 or 5.0V (typ).
  See the documentation of E2 and *Chapter 5 Clock Sources* for details.
- In case the piggyback board is mounted on a main board, the voltages *Voltage1* and *Voltage2* are supplied by the on-board regulators of the main board.

NOTE: *Do not supply any voltage directly to the piggyback board in case it is mounted on the main board.*

For each of the two voltages, ‘Voltage 1 ‘ and ‘Voltage 2’, a green LED (LED1 and LED2) is available to signal that the related voltage is available on the piggyback board.

4.2 Voltage Distribution

The table shows the required device power supply pins and their function:

Device supply pin	Function
REGVCC	Supply for the device internal regulators for the digital logic.
EVCC	Supply for ports of AWO area.
A0VREF	Supply for ports and analog functions of ADC0.
VDDIOF	IO supply voltage for components located on a connected mainboard.

For each of the above voltages, the power supply can be selected from *Voltage1* (typ. 5.0V) or *Voltage2* (typ. 3.3V) by the jumpers JP0, JP1, JP2, JP4, JP9 and JP6. See the picture below for details.

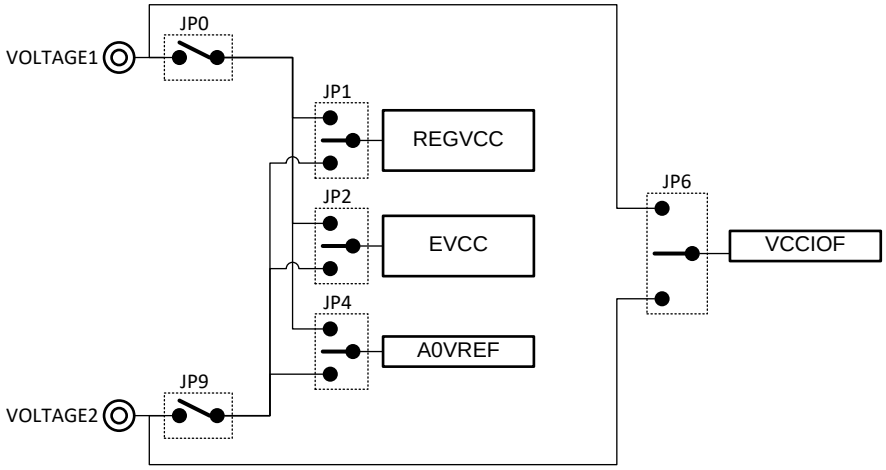


Figure 6 - Jumper settings to select supply voltage

Chapter 5 Clock Sources

For mounting of the external crystal oscillator, a socket is available.

A crystal or ceramic resonator in the range of 8MHz to 24MHz can be mounted on socket X1.

The package with generation 1 of Y-RH850-F1X-100PIN-PB-T1-V3 included 2 crystals of 8MHz and 16MHz.

The package with generation 2 of Y-RH850-F1X-100PIN-PB-T1-V3 includes 4 crystals with 8MHz, 16Mhz, 20MHz and 24MHz.

Chapter 6 Debug and Programming Interface

Connector 19 is provided as interface for debug and flash programming tools to the microcontroller.

The signal connection of connector CN19 is shown in the table below:

CN19	Device Port	Device signal
1	JP0_2	DCUTCK / LPDCLK
2	GND	GND
3	JP0_4	DCUTRST
4	FLMD0	FLMD0
5	JP0_1	DCUTDO / LPDO
6	P10_8*	FLMD1
7	JP0_0	DCUTDI / LPDI
8	DBG_Voltage	-
9	JP0_3	DCUTMS
10	-	-
11	JP0_5	DCURDY / LPDCLKOUT
12	GND	-
13	RESET	-
14	GND	-

* In case the FLMD1 signal must be controlled by the debug/programming tool, the pin header JP11 must be closed.

The DBG_Voltage (on CN19 pin 8) can be monitored by debug and flash programming tools. It is possible to select either Voltage1 or the Voltage2 by pin header JP10 for this monitoring:

JP10	Selection for DBG_Voltage
1-2	Voltage1 (5.0V) is selected
2-3	Voltage2 (3.3V) is selected

Chapter 7 Connectors for Device Ports

The piggyback board has 2 groups of connectors.

One group (CN1-CN3) provides the connection of the device pins to a mainboard.

The second group (CN5-CN8) provides access to each device pin to the user.

7.1 Connectors to Mainboard

Three connectors (CN1 to CN3) are available to connect the piggyback board to a mainboard.

The signal connection of each connector is described in the following tables:

7.1.1 Connector CN1

Pin	Function	Device Port	Pin	Function	Device Port
1	VOLTAGE1	-	2	VOLTAGE1	-
3	VOLTAGE1	-	4	VOLTAGE1	-
5	RESET	_RESET	6	NMI	P9_0
7	WAKE	-	8	-	-
9	INT0	P9_1	10	INT1	P0_6
11	INT2	P9_2	12	INT3	P9_3
13	-	-	14	-	-
15	UART0TX	P10_10	16	UART1TX	P0_5
17	UART0RX	P10_9	18	UART1RX	P0_4
19	LIN0TX	P10_10	20	LIN1TX	P0_8
21	LIN0RX	P10_9	22	LIN1RX	P0_7
23	IIC0SDL	P10_3	24	IIC1SDL	-
25	IIC0SDA	P10_2	26	IIC1SDA	-
27	CAN0TX	P10_1	28	CAN1TX	P0_3
29	CAN0RX	P10_0	30	CAN1RX	P0_2
31	SENTIN0	P8_0	32	SENTIN1	P9_0
33	SENTOUT0	P8_1	34	SENTOUT1	P9_1
35	PSI50Rx	-	36	PSI51Rx	-
37	PSI50Tx	-	38	PSI51Tx	-
39	PSI50Snyc	-	40	PSI51Sync	-
41	FLX0TX	P11_1	42	FLX0EN	P10_11
43	FLX0RX	P10_14	44	FLXSTPWT	P10_12
45	FLX1TX	P10_8	46	FX1EN	P10_13
47	FLX1RX	P10_9	48	FLXCLK	P10_10
49	-	-	50	-	-
51	ETH0MDIO	-	52	ETH0MDC	-
53	ETH0RXD0	-	54	EH0TXD0	-
55	ETH0RXD1	-	56	EH0TXD1	-
57	ETH0RXD2	-	58	EH0TXD2	-
59	ETH0RXD3	-	60	EH0TXD3	-
61	ETH0RXDCLK	-	62	ETH0TXCLK	-

Pin	Function	Device Port	Pin	Function	Device Port
63	ETH0RXER	-	64	ETH0TXER	-
65	ETH0CRSDV	-	66	ETH0TXEN	-
67	ETH0RXDV	-	68	ETH0COL	-
69	ETH0RESET	-	70	-	-
71	-	-	72	-	-
73	USB0UDMF	-	74	USB0UDMH	-
75	USB0UDPF	-	76	USB0UDPH	-
77	-	-	78	-	-
79	-	-	80	-	-
81	-	-	82	-	-
83	-	-	84	-	-
85	DIGIO_0	P8_0	86	DIGIO_1	P8_1
87	DIGIO_2	P8_2	88	DIGIO_3	P8_3
89	DIGIO_4	P8_4	90	DIGIO_5	P8_5
91	DIGIO_6	P8_6	92	DIGIO_7	P11_0
93	DIGIO_8	P10_0	94	DIGIO_9	P10_7
95	DIGIO_10	P10_8	96	DIGIO_11	P10_15
97	DIGIO_12	P0_9	98	DIGIO_13	P0_10
99	DIGIO_14	P0_11	100	DIGIO_15	P0_12
101	-	-	102	-	-
103	MUX0	P10_4	104	MUX1	P10_5
105	MUX2	P10_6	106	-	-
107	ADC0	AP0_0	108	ADC1	AP0_1
109	ADC2	AP0_2	110	ADC3	AP0_3
111	ADC4	AP0_4	112	ADC5	AP0_5
113	ADC6	AP0_6	114	ADC7	AP0_7
115	VDDIOF	-	116	VDDIOF	-
117	VOLTAGE2	-	118	VOLTAGE2	-
119	VOLTAGE2	-	120	VOLTAGE2	-

7.1.2 Connector CN2 (EESS0401-139-01)

Pin	Function	Device Port	Pin	Function	Device Port
1	CAN2Tx	P0_4	2	CAN3Tx	P11_4
3	CAN2Rx	P0_5	4	CAN3Rx	P11_3
5	CAN4Tx	P0_10	6	CAN5Tx	P11_6
7	CAN4Rx	P0_9	8	CAN5Rx	P11_5
9	LIN2Tx	P0_10	10	LIN3Tx	-
11	LIN2Rx	P0_9	12	LIN3Rx	-
13	LIN4Tx	P11_2	14	LIN5Tx	-
15	LIN4Rx	P11_1	16	LIN5Rx	-
17	LIN6Tx	-	18	LIN7Tx	-
Q	LIN6Rx	-	20	LIN7Rx	-
21	LIN8Tx	-	22	LIN9Tx	-
23	LIN8Rx	-	24	LIN9Rx	-

Pin	Function	Device Port	Pin	Function	Device Port
25	LIN10Tx	P10_10	26	LIN11Tx	P0_5
27	LIN10Rx	P10_9	28	LIN11Rx	P0_4
29	LIN12Tx	P10_14	30	LIN13Tx	P11_5
31	LIN12Rx	P10_13	32	LIN13Rx	P11_6
33	LIN14Tx	-	34	LIN15Rx	P10_11
35	LIN14Rx	-	36	LIN15Tx	P10_12
37	-	-	38	-	-
39	-	-	40	-	-
41	MLBCLK	-	42	MLBRESET	-
43	MLBSIG	-	44	MLBDAT	-
45	-	-	46	-	-
47	CAN6Tx	P10_4	48	CAN7Tx	P10_13
49	CAN6Rx	P10_5	50	CAN7Rx	P10_14
51	-	-	52	-	-
53	-	-	54	-	-
55	-	-	56	-	-
57	-	-	58	-	-
59	-	-	60	-	-
61	-	-	62	-	-
63	-	-	64	-	-
65	-	-	66	-	-
67	-	-	68	-	-
69	-	-	70	-	-
71	-	-	72	-	-
73	-	-	74	-	-
75	-	-	76	-	-
77	-	-	78	-	-
79	-	-	80	-	-
81	-	-	82	-	-
83	-	-	84	-	-
85	-	-	86	-	-
87	-	-	88	-	-
89	-	-	90	-	-
91	-	-	92	-	-
93	-	-	94	-	-
95	-	-	96	-	-
97	-	-	98	-	-
99	-	-	100	-	-
101	-	-	102	-	-
103	-	-	104	-	-
105	-	-	106	-	-
107	-	-	108	-	-
109	-	-	110	-	-
111	-	-	112	-	-

Pin	Function	Device Port	Pin	Function	Device Port
113	-	-	114	-	-
115	-	-	116	-	-
117	-	-	118	-	-
119	-	-	120	-	-

7.1.3 Connector CN2 (D015312-06-V02)

Pin	Function	Device Port	Pin	Function	Device Port
1	CAN2Tx	P0_4	2	CAN3Tx	P11_4
3	CAN2Rx	P0_5	4	CAN3Rx	P11_3
5	CAN4Tx	P0_10	6	CAN5Tx	P11_6
7	CAN4Rx	P0_9	8	CAN5Rx	P11_5
9	LIN2Tx	P0_10	10	LIN3Tx	-
11	LIN2Rx	P0_9	12	LIN3Rx	-
13	LIN4Tx	P11_2	14	LIN5Tx	-
15	LIN4Rx	P11_1	16	LIN5Rx	-
17	LIN6Tx	-	18	LIN7Tx	-
Q	LIN6Rx	-	20	LIN7Rx	-
21	LIN8Tx	-	22	LIN9Tx	-
23	LIN8Rx	-	24	LIN9Rx	-
25	LIN10Tx	P10_10	26	LIN11Tx	P0_5
27	LIN10Rx	P10_9	28	LIN11Rx	P0_4
29	LIN12Tx	P10_14	30	LIN13Tx	P11_5
31	LIN12Rx	P10_13	32	LIN13Rx	P11_6
33	LIN14Tx	-	34	LIN15Rx	P10_12
35	LIN14Rx	-	36	LIN15Tx	P10_11
37	-	-	38	-	-
39	-	-	40	-	-
41	MLBCLK	-	42	MLBRESET	-
43	MLBSIG	-	44	MLBDAT	-
45	-	-	46	-	-
47	CAN6Tx	P10_4	48	CAN7Tx	P10_13
49	CAN6Rx	P10_5	50	CAN7Rx	P10_14
51	-	-	52	-	-
53	-	-	54	-	-
55	-	-	56	-	-
57	-	-	58	-	-
59	-	-	60	-	-
61	-	-	62	-	-
63	-	-	64	-	-
65	-	-	66	-	-
67	-	-	68	-	-
69	-	-	70	-	-
71	-	-	72	-	-
73	-	-	74	-	-

Pin	Function	Device Port	Pin	Function	Device Port
75	-	-	76	-	-
77	-	-	78	-	-
79	-	-	80	-	-
81	-	-	82	-	-
83	-	-	84	-	-
85	-	-	86	-	-
87	-	-	88	-	-
89	-	-	90	-	-
91	-	-	92	-	-
93	-	-	94	-	-
95	-	-	96	-	-
97	-	-	98	-	-
99	-	-	100	-	-
101	-	-	102	-	-
103	-	-	104	-	-
105	-	-	106	-	-
107	-	-	108	-	-
109	-	-	110	-	-
111	-	-	112	-	-
113	-	-	114	-	-
115	-	-	116	-	-
117	-	-	118	-	-
119	-	-	120	-	-

7.1.4 Connector CN3

Pin	Function	Device Port	Pin	Function	Device Port
1	PWM00	P10_0	2	PWM01	P10_1
3	PWM02	P10_2	4	PWM03	P10_3
5	PWM04	P10_7	6	PWM05	P10_8
7	PWM06	P10_9	8	PWM07	P10_10
9	PWM08	P9_0	10	PWM09	P9_1
11	PWM10	P0_4	12	PWM11	P0_1
13	PWM12	P0_2	14	PWM13	P0_3
15	PWM14	P8_0	16	PWM15	P8_1
17	PWM16	P10_11	18	PWM17	P10_12
19	PWM18	P10_13	20	PWM19	P10_14
21	PWM20	P9_2	22	PWM21	P9_3
23	PWM22	P8_2	24	PWM23	P8_3
25	PWM24	P10_14	26	PWM25	P11_0
27	PWM26	P11_1	28	PWM27	P11_2
29	PWM28	P11_3	30	PWM29	P11_4
31	PWM30	P11_5	32	PWM31	P11_6
33	PWM32	P11_7	34	PWM33	P9_4

Pin	Function	Device Port	Pin	Function	Device Port
35	PWM34	P9_5 or P0_11	36	PWM35	P9_6 or P0_6
37	PWM36	P8_4	38	PWM37	P8_5
39	PWM38	P8_6	40	PWM39	P8_7
41	PWM40	P8_8	42	PWM41	P8_9
43	PWM42	P8_10	44	PWM43	P8_11
45	PWM44	P8_12	46	PWM45	P0_12
47	PWM46	P0_13	48	PWM47	P0_14
49	PWM48	-	50	PWM49	-
51	PWM50	-	52	PWM51	-
53	PWM52	-	54	PWM53	-
55	PWM54	-	56	PWM55	-
57	PWM56	-	58	PWM57	-
59	PWM58	-	60	PWM59	-
61	PWM60	-	62	PWM61	-
63	PWM62	-	64	PWM63	-
65	PWM64	-	66	PWM65	-
67	PWM66	-	68	PWM67	-
69	PWM68	-	70	PWM69	-
71	PWM70	-	72	PWM71	-
73	PWM72	-	74	PWM73	-
75	PWM74	-	76	PWM75	-
77	PWM76	-	78	PWM77	-
79	PWM78	-	80	PWM79	-
81	PWMADC00	AP0_8	82	PWMADC01	AP0_9
83	PWMADC02	AP0_10	84	PWMADC03	AP0_11
85	PWMADC04	AP0_12	86	PWMADC05	AP0_13
87	PWMADC06	AP0_14	88	PWMADC07	AP0_15
89	PWMADC08	-	90	PWMADC09	-
91	PWMADC10	-	92	PWMADC11	-
93	PWMADC12	-	94	PWMADC13	-
95	PWMADC14	-	96	PWMADC15	-
97	-	-	98	-	-
99	-	-	100	-	-
101	-	-	102	-	-
103	-	-	104	-	-
105	-	-	106	-	-
107	-	-	108	-	-
109	-	-	110	-	-
111	-	-	112	-	-
113	-	-	114	-	-
115	-	-	116	-	-
117	-	-	118	-	-
119	-	-	120	-	-

7.2 Connectors for User Access

Connection to each pin of the device is possible via the connectors CN5 to CN8.

Note :The pin headers are directly connected to the pins of the device, therefore special care must be taken to avoid any electrostatic or other damage to the device.

Pin	Device Function			
	CN5	CN6	CN7	CN8
1	P10_3	JP0_2	A0VSS	EVCC
2	P10_4	JP0_1	A0VREF	ISOVCL
3	P10_5	JP0_0	AP0_15	ISOVSS
4	P10_15	RESET	AP0_14	EVSS
5	P11_0	EVCC	AP0_13	P10_6
6	P0_0	AWOVSS	AP0_12	P10_7
7	P0_1	AWOVCL	AP0_11	P10_8
8	P0_2	REGVCC	AP0_10	P10_9
9	P0_3	X2	AP0_9	P10_10
10	EVCC	X1	AP0_8	P10_11
11	P0_4	FLMD0	AP0_7	P10_12
12	P0_5	P0_10	AP0_6	P10_13
13	P0_6	P0_9	AP0_5	P10_14
14	P0_11	P0_8	AP0_4	P11_1
15	P0_12	P0_7	AP0_3	P11_2
16	P0_13	EVSS	AP0_2	P11_3
17	P0_14	P8_0	AP0_1	P11_4
18	EVSS	P8_1	AP0_0	P11_5
19	P8_2	P8_3	P9_0	P11_6
20	P8_10	P8_4	P9_1	P11_7
21	P8_11	P8_5	P9_2	EVCC
22	P8_12	P8_6	P9_3	EVSS
23	JP0_5	P8_7	P9_4	P10_0
24	JP0_4	P8_8	P9_5	P10_1
25	JP0_3	P8_9	P9_6	P10_2

Chapter 8 Other Circuitry

8.1 Push Button for RESET

In order to issue a RESET to the device, the push-button SW1 is available.

8.2 Mode Selection

The piggyback board gives the possibility to configure the following mode pins

- FLMD0 via jumper JP25
- FLMD1 via jumper JP19
- MODE0 via jumper JP28
- MODE1 via jumper JP26
- MODE2 via jumper JP27

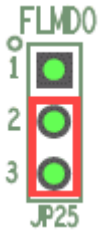
To apply “High” or “Low” to the mode pins, the pins 1 and 2, or the pins 2 and 3 (if available) of the corresponding jumper must be closed, respectively.

Note: Pin 1 of all jumpers is marked by a small circle.

CAUTION: *Be careful in configuration of mode related pins. Wrong configuration and operation of the device outside of its specification can cause irregular behaviour of the device and long term damage cannot be ruled out completely. Be sure to check the corresponding User’s Manual for details, which modes are specified for the used device.*

Note: In most cases the ‘Normal operating mode’ of the device will be used. This mode is for execution of the user program. The on-chip debug functions also use this mode.

To select the ‘Normal operating mode’ of the device, the FLMD0 pin must be pulled low. To do so, close the pins 2-3 on the jumper JP25:



All other jumper related to the mode selection can be left open.

8.3 Signalling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins. Device pins P8_0 to P8_7 are connected to the odd pins 1 to 15 of the pin header CN13, while the LEDs 1 to 8 are connected to the even pins 2 to 16, respectively.

The LEDs can be either connected to

- the device port pins P8_0 to P8_7 by closing the connection on CN13 using a jumper, or
- any device port pin by using wire connections provided with the mainboard.

Chapter 9 Precautions

9.1 Usage of LIN15

On piggyback board V3 the LIN15 Rx/Tx signals on CN2 have been crossed.

This applies only to the pcb with the marking “EESS-0401-139-01”.

Port P10_11 is LIN15RX, but it is connected to LIN15TX.

Port P10_12 is LIN15TX, but it is connected to LIN15RX.

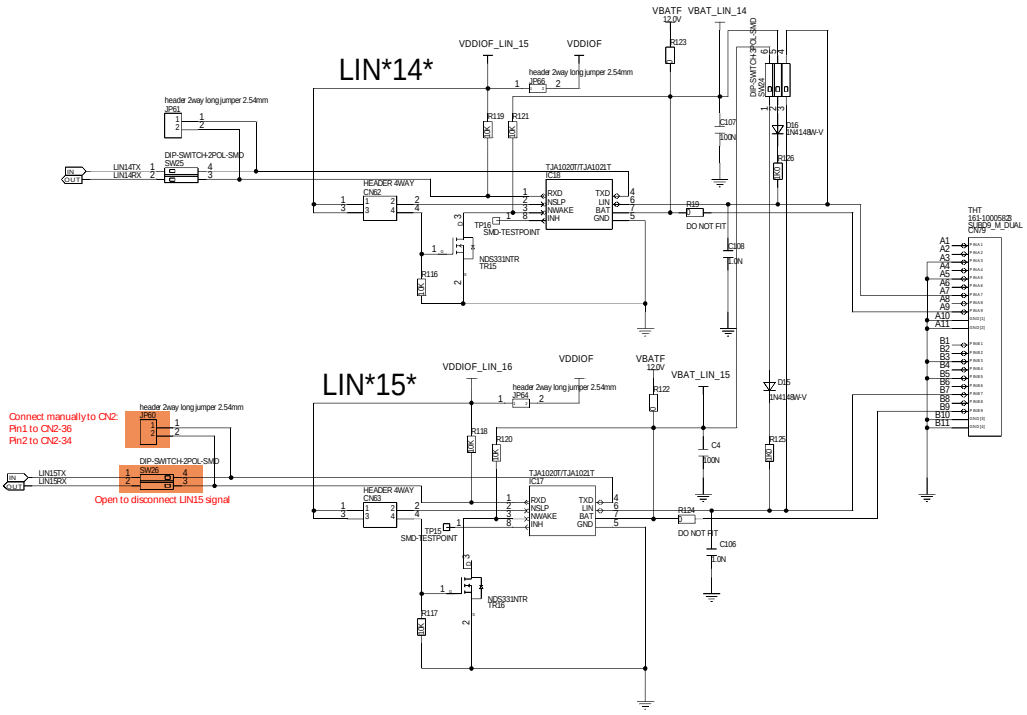
In order to fix this it is best to make the appropriate modifications on the RH850/X1x Network Mainboard (Y-RH850-X1X-MB-T2-V1 or Y-RH850-X1X-MB-T2-V2) or on the RH850/X2x Mainboard (Y-RH850-X2X-MB-T1-V1).

9.1.1 Adjustments on RH850/X1x Network Mainboard

In order to use LIN15 on the RH850/X1x Network Mainboard following modifications on the mainboard are needed:

1. Disconnect LIN15Tx and LIN15Rx from connector CN2 by setting switch SW26-1 and SW26-2 to “OFF”.
2. Connect LIN15Tx manually from jumper JP60-1 to connector CN2-36.
3. Connect LIN15Rx manually from jumper JP60-2 to connector CN2-34.

Please see below picture for the necessary changes.



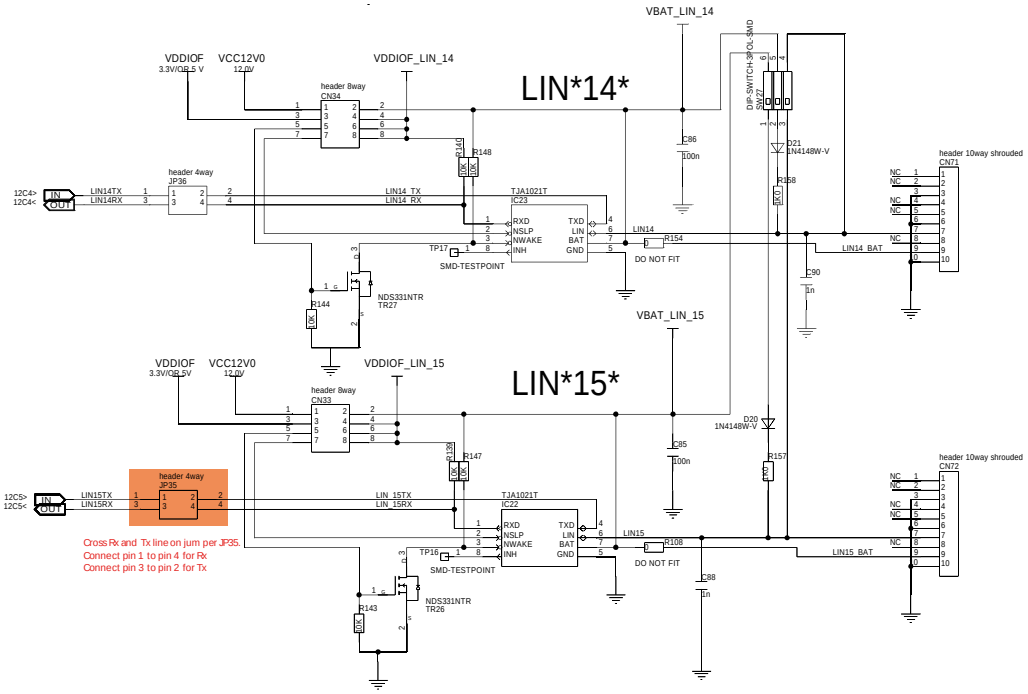
9.1.2 Adjustments on RH850/X2x Mainboard

To be able to use LIN15 with the RH850/X2x Mainboard changes are very simple.

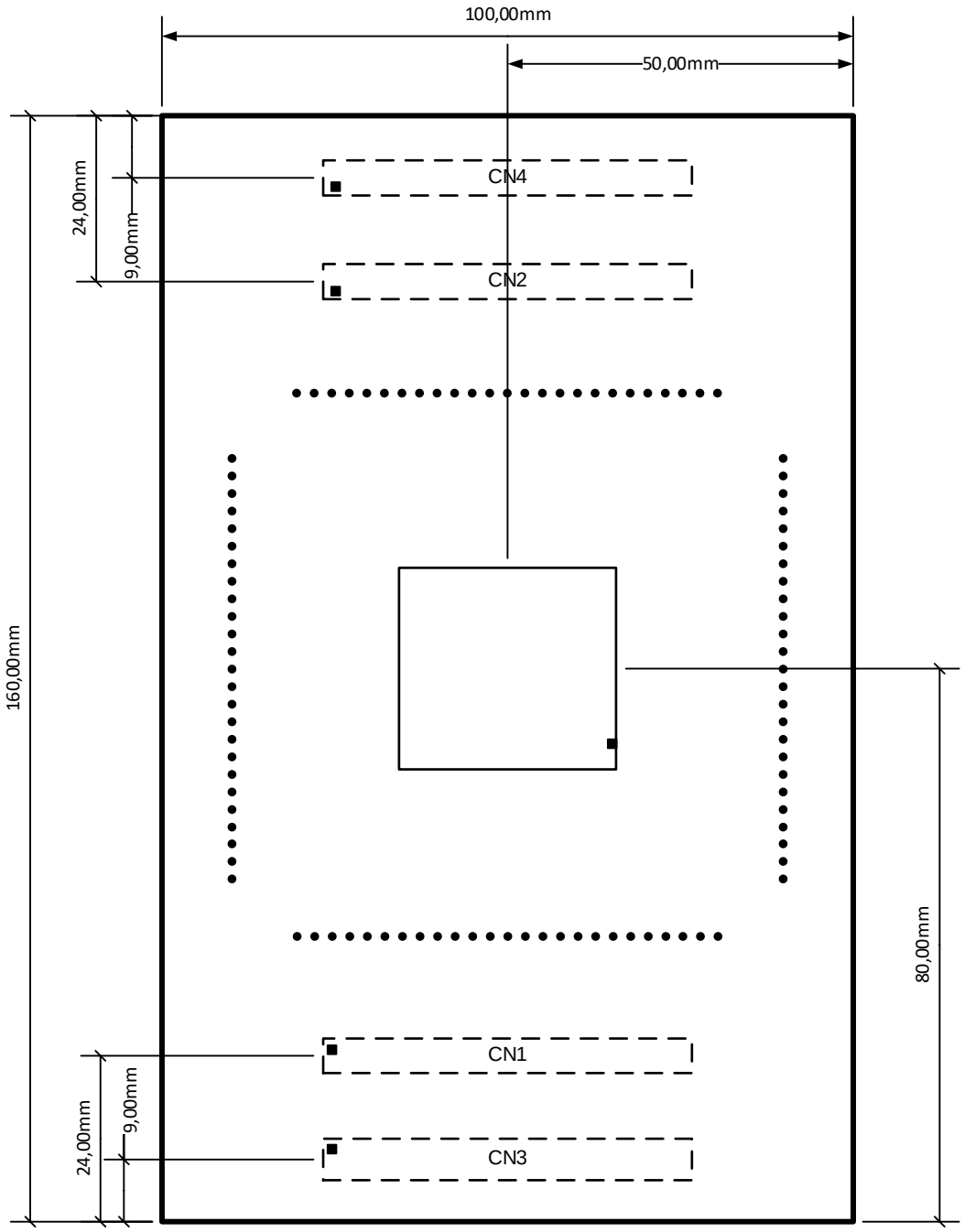
On RH850/X2x Mainboard the connection of LIN15Tx and LIN15Rx to connector CN2 is by jumper JP35. This can be modified easily to accommodate the pin swap on CN2:

1. Remove the jumpers on JP35.
2. On JP35 connect JP35-1 with JP35-4 for LIN15Rx.
3. On JP35 connect JP35-2 with JP35-3 for LIN15Tx

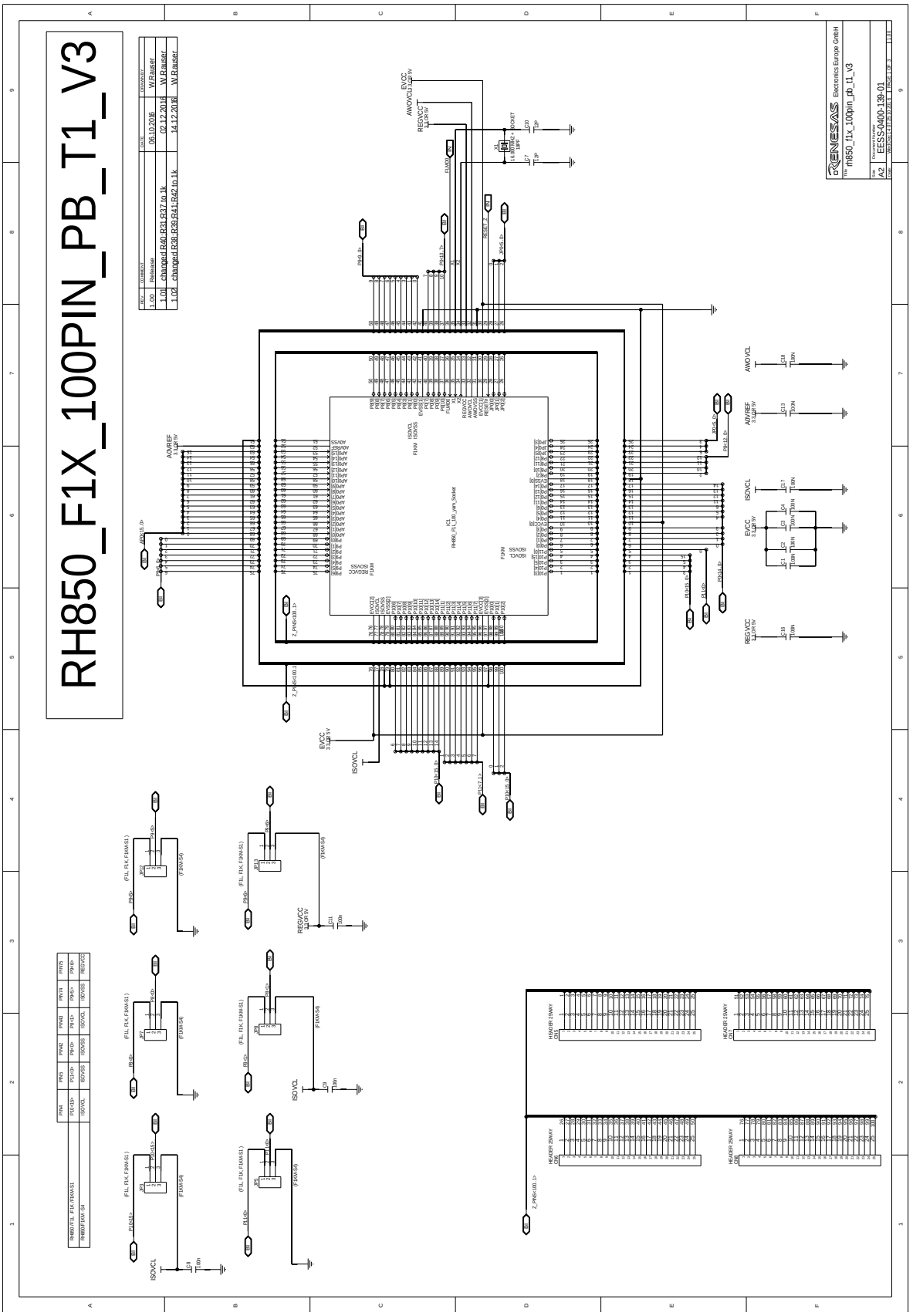
Please see below picture for the necessary changes.

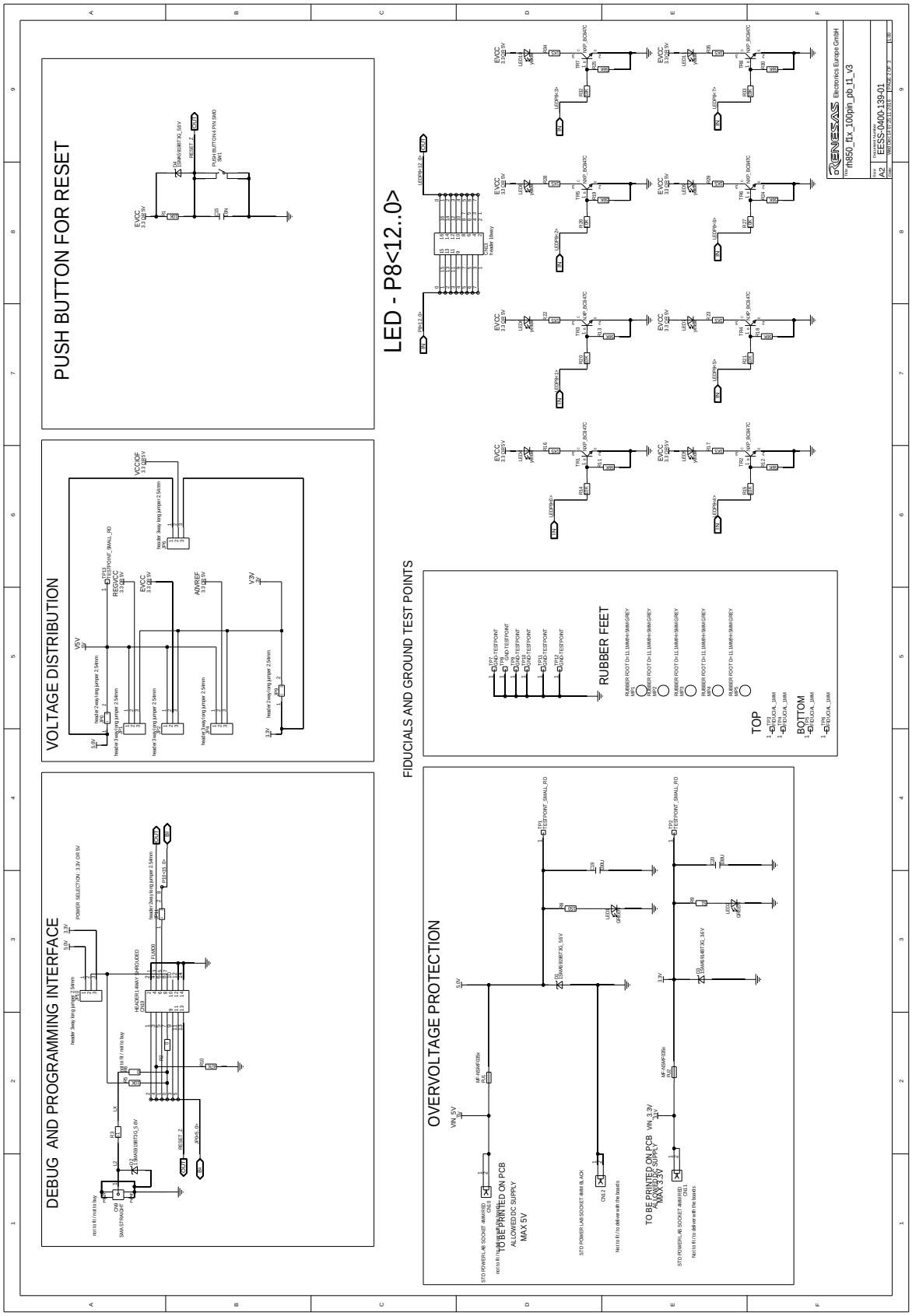


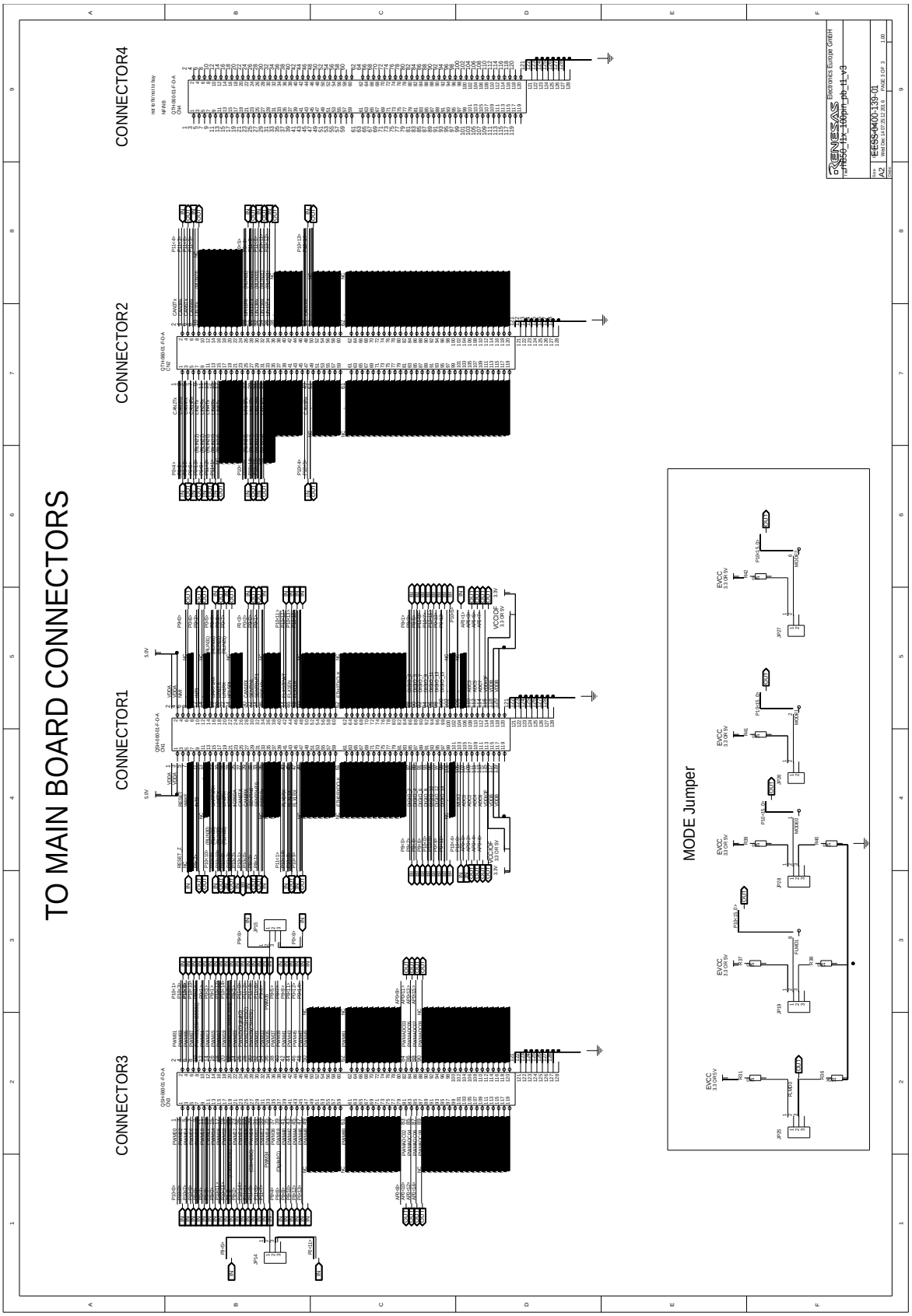
Chapter 10 Mechanical dimensions



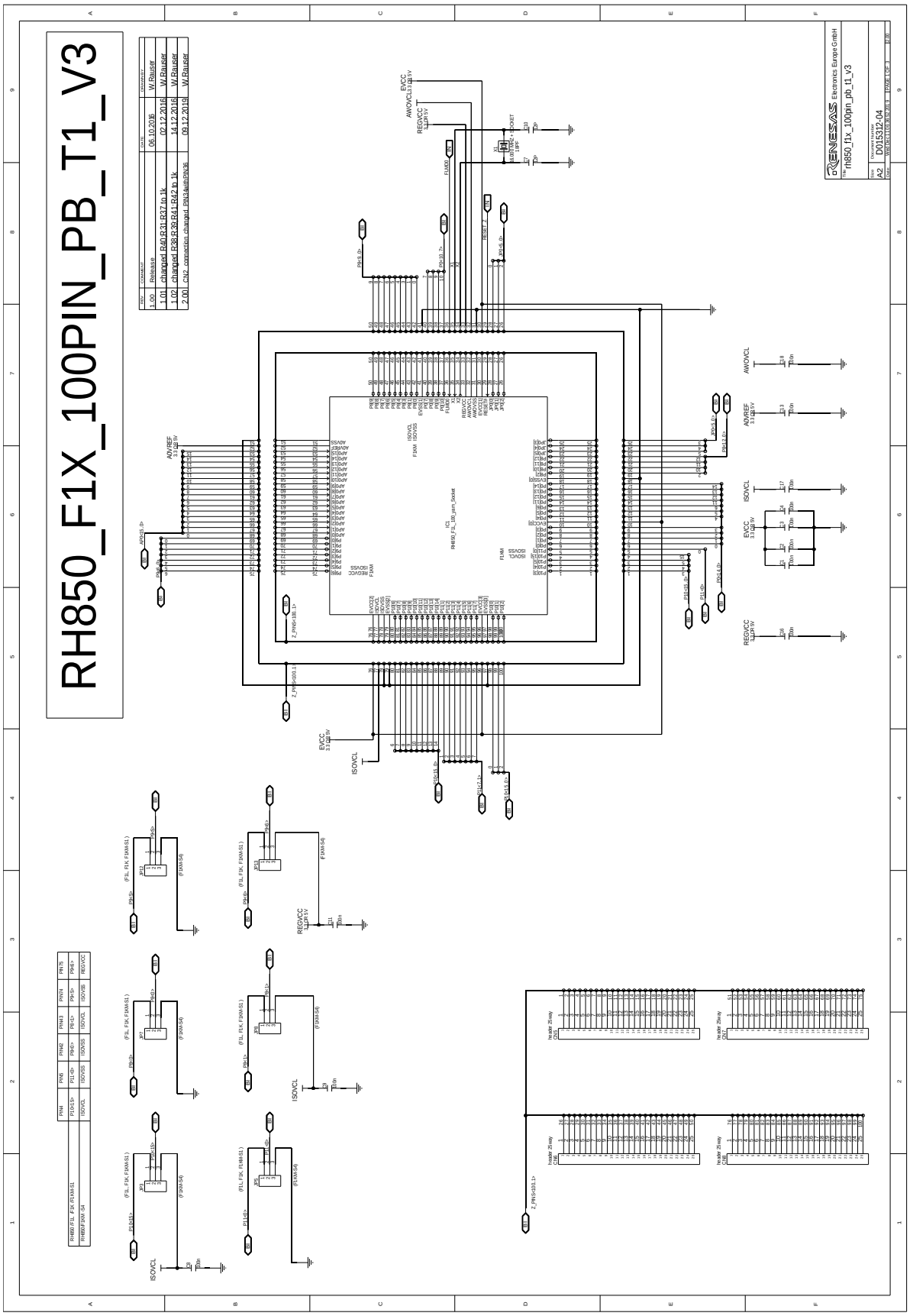
Chapter 11 Schematic of PCB marked “EESS-0401-139-01”



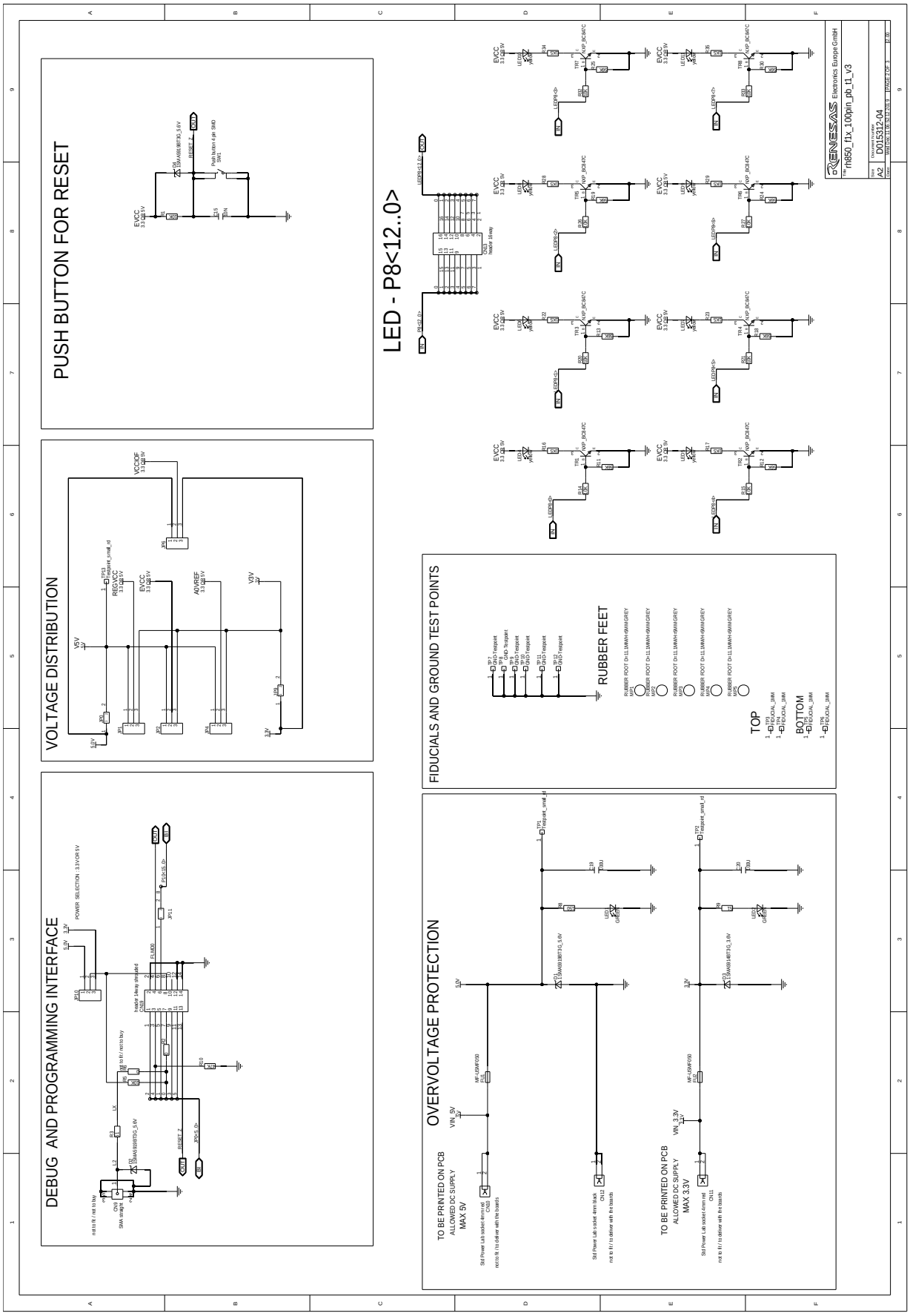

PUSH BUTTON FOR RESET
VOLTAGE DISTRIBUTION
DEBUG AND PROGRAMMING INTERFACE
LED - P8<12..0>
FIDUCIALS AND GROUND TEST POINTS
RUBBER FEET
TOP
BOTTOM
OVERVOLTAGE PROTECTION
TO BE PRINTED ON PCB
ALLOWED DC SUPPLY
MAX 5V
TO BE PRINTED ON PCB
ALLOWED DC SUPPLY
MAX 3.3V
RENESAS Electronics Europe GmbH
rh850_f1x_100pin_pb_11_v3
EESS-0400-139-01
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.

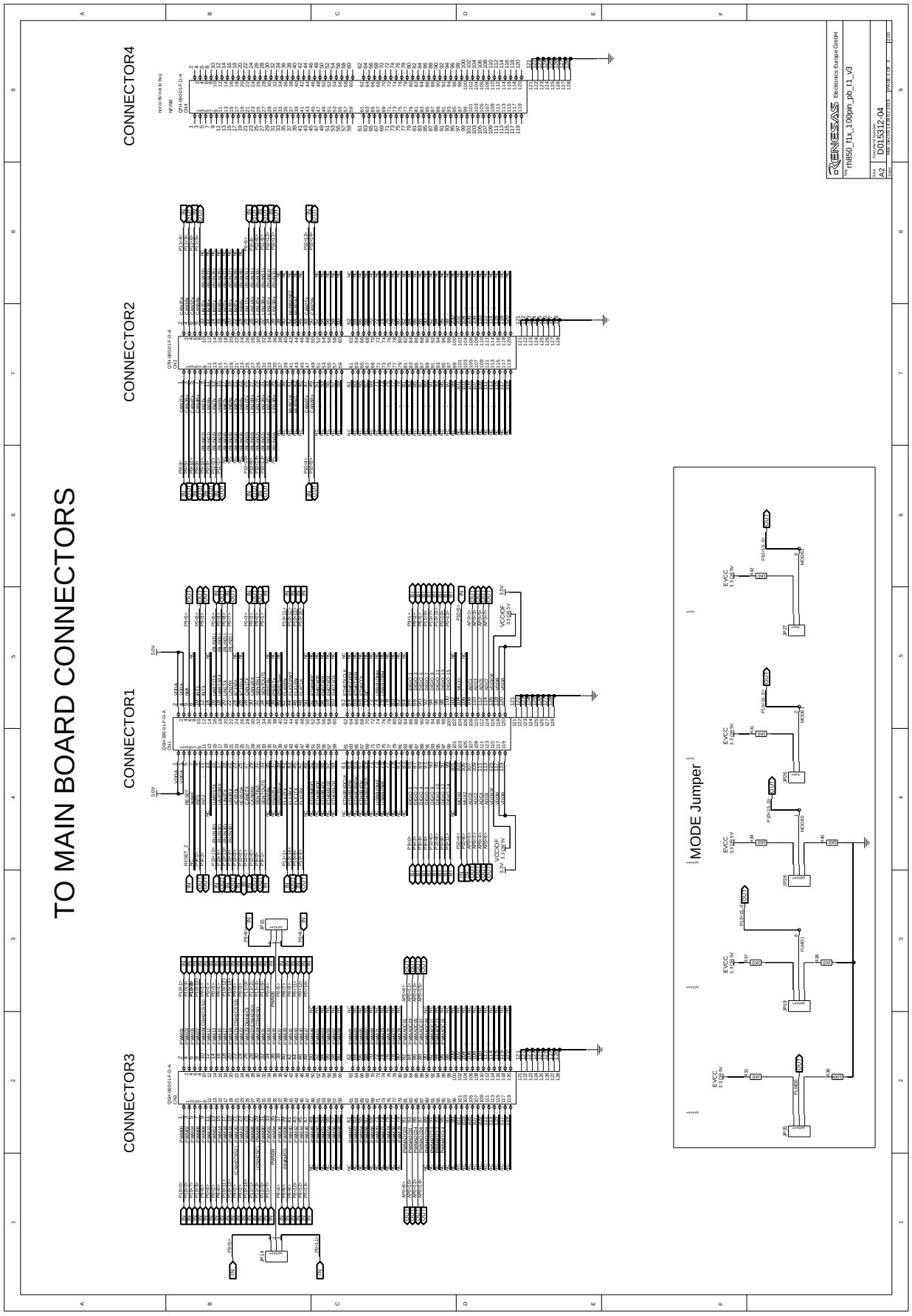

TO MAIN BOARD CONNECTORS
CONNECTOR4
CONNECTOR2
CONNECTOR1
CONNECTOR3
MODE Jumper
RENESAS Electronics Europe GmbH
EESS-0401-139-01
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version

Chapter 12 Schematic of PCB marked “D015312-06-V02”



These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.


PUSH BUTTON FOR RESET
VOLTAGE DISTRIBUTION
DEBUG AND PROGRAMMING INTERFACE
LED - P8<12..0>
FIDUCIALS AND GROUND TEST POINTS
RUBBER FEET
TOP
BOTTOM
OVERVOLTAGE PROTECTION
TO BE PRINTED ON PCB
ALLOWED DC SUPPLY
MAX 5V
TO BE PRINTED ON PCB
ALLOWED DC SUPPLY
MAX 3.3V
RENESAS Electronics Europe GmbH
rh850_f1x_100pin_pb_f1_v3
D015312-04
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.


TO MAIN BOARD CONNECTORS
CONNECTOR4
CONNECTOR2
CONNECTOR1
CONNECTOR3
MODE Jumper
RENESAS Electronics Europe GmbH
rh850_f1x_100pin_pb_i1_v3
D015312-04
These intangible goods are not subject to Annex I of common Dual-Use list (428/2009) in its current version.

Chapter 13 Revision History

The table provides information about the major changes of the document versions.

		Description	
Rev.	**Date**	**Page**	**Summary**
V1.00	2016-11-25	–	Initial release
V1.01	2019-11-27	16	Changed “Function” for pin 34 and pin 36 on CN2
		20	Added precaution for LIN15 signal on connector CN2
V1.02	2020-01-17	–	Released an updated pcb with modified signals on CN2.
V1.03	2020-09-09	9	Corrected jumper setting for F1KM-S1 in table in chapter3. JP14 and JP15 setting was changed.
V1.04	2021-08-12	8	Add RH850/F1KM-S2 to supported devices

Main differences to the RH850-F1X-100PIN-PB-T1-**V2**:

- Added support for the RH850/F1KM-S1, F1KM-S2 and RH850/F1KM-S4 device.
  This mainly relates to the added jumpers on page 1 of the schematic for the device pin selection.
- Modified signals on CN1, CN2 and CN3.
- Added functionality for the mode selection of the device.
- Added signalling LEDs.

RH850/F1x, R1x 100pin Piggyback Board T1-V3 User's Manual: Piggyback Board T1-V3

Publication Date: Rev.1.04 August 12, 2021

Published by: Renesas Electronics Corporation

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics Corporation
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 101-T01, Floor 1, Building 7, Yard No. 7, 8th Street, Shangdi, Haidian District, Beijing 100085, China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai 200333, China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit No 3A-1 Level 3A Tower 8 UOA Business Park, No 1 Jalan Pengaturcara U1/51A, Seksyen U1, 40150 Shah Alam, Selangor, Malaysia
Tel: +60-3-5022-1288, Fax: +60-3-5022-1290

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

© 2019 Renesas Electronics Corporation. All rights reserved.

Colophon 6.0

RH850/F1x, R1x 100PIN

Renesas Electronics Corporation

R20UT3959ED0104