RTKA215300E00000BU

Evaluation Board with Socket Mounted RAA215300 PMIC

The RTKA215300E00000BU socket evaluation board (EVB) is a platform for demonstrating functionality of the RAA215300 PMIC. There is access to regulator switching voltages, inductor currents, input currents, control loops, and more.The user can change many operating characteristics using an I^2C interface.

The socket EVB can be used to program the EEPROM and set the registers, and to debug the configuration.

Important: The socket EVB is not electrically or thermally capable of delivering significant power and should only be used at normal room temperature.

Features

- A complete power supply system but with limited power capability
- EEPROM programming
- Access to all RAA215300 features
- Facility to adjust RAA215300 settings
- Connectivity to the whole power system
- Access for monitoring and test
- Access for design modification

Specifications

Requiring only the addition of inductors and capacitors, RAA215300 integrates all semiconductors and control circuitry to create a complete power solution for systems that use Renesas RZ/G2L microprocessors. The socket EVB can easily be configured to explore many other applications, but with limited power capability.

Evaluation Board Contents

- Socket EVB PCB assembly
- Mini USB I^2C dongle with USB cable (ISLUSBMINIEVAL1Z)

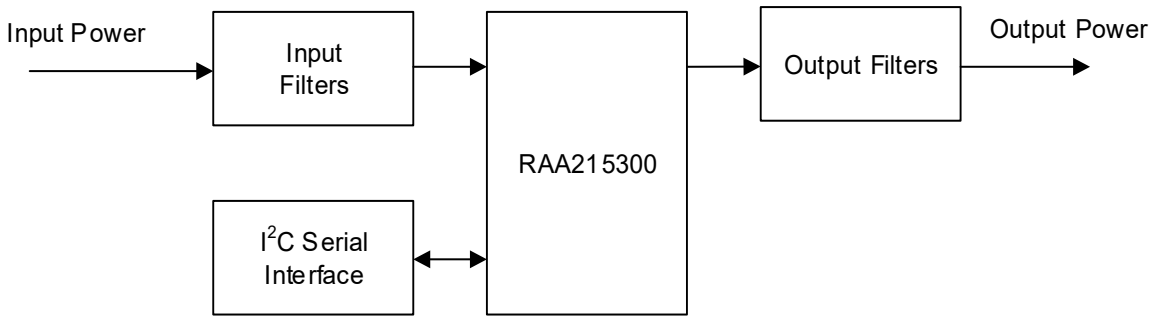

Figure 1. EVB Block Diagram

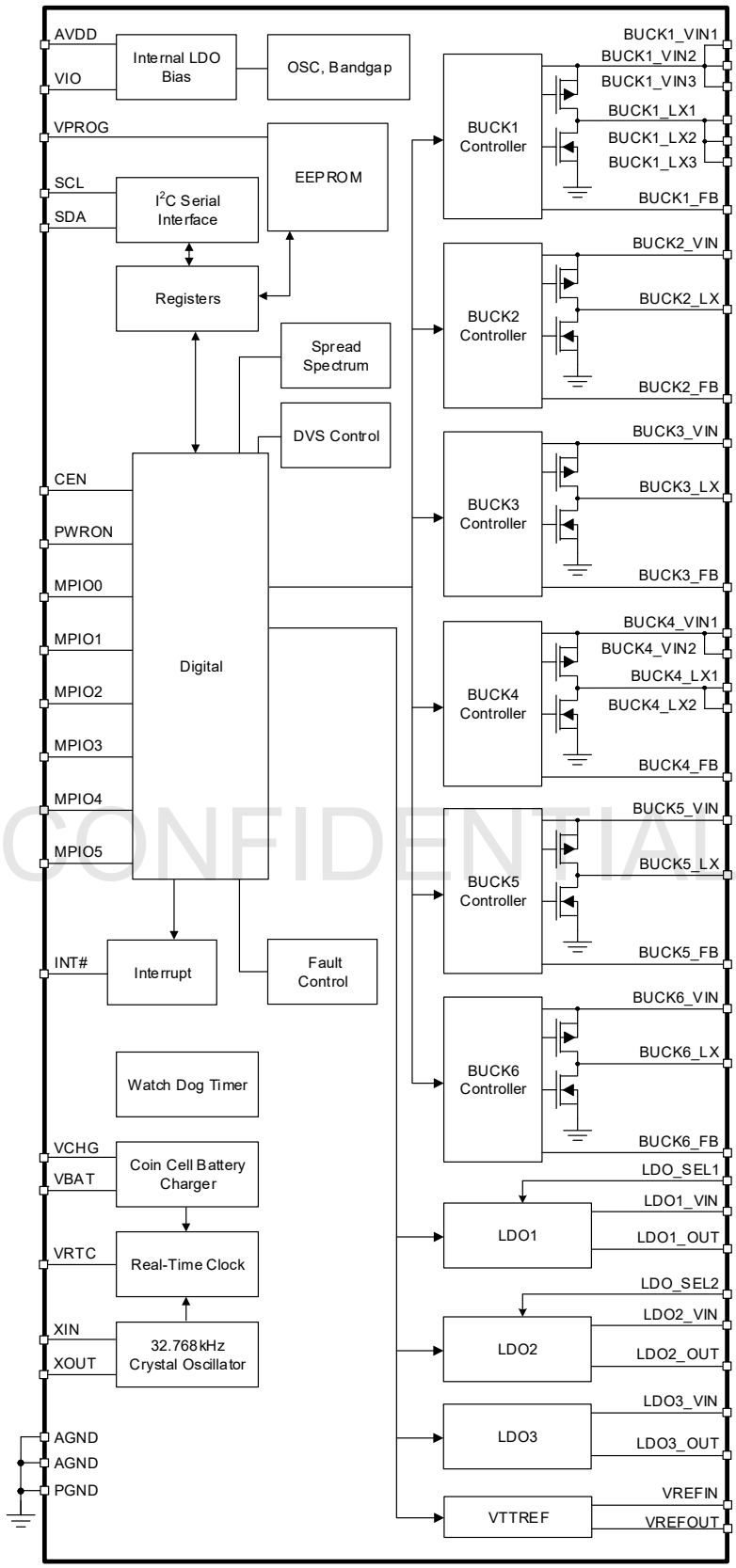

Figure 2. PMIC Block Diagram

Contents

1. Reference Material

For reference material, including the datasheet and evaluation software, visit the RAA215300 product page.

2. Functional Description

2.1 Overview

- Operating input voltage range: 2.7V to 5.5V
- Six synchronous buck regulators, with settable output voltage, but limited power capability
- Three LDOs, with bypass mode and settable output voltage
- Integral EEPROM for system settings
- Programmable settings and configuration using an I^2C interface
- I^2C serial interface (up to 1MHz, with SCL and SDA pull-up resistors on dongle changed to 1kohm)
- Internal MOSFETs
- Internally compensated control loops
- Power sequencing control
- Dedicated VTTREF for DDR memory
- Auto PFM/PWM, Forced PWM (FPWM)
- Selectable switching frequency
- Ultrasonic switching mode
- Spread spectrum switching mode
- Phase synchronization
- Sleep Mode
- Dynamic voltage scaling
- 32kHz crystal oscillator, RTC, battery / supercapacitor charger

The EVB has a dongle to facilitate an I^2C interface, which is used to adjust PMIC settings and communicate status. The I^2C interface can be controlled by a dedicated Renesas proprietary Graphical User Interface (GUI), which requires a host computer.

The EVB includes switches and jumpers to emulate the signal interface (some of which are configurable MPIO) with a microprocessor-based system.

The PMIC can be connected to the onboard I^2C interface dongle or to onboard pull-up and pull-down switches. For each signal, there is a straight 3-way header on the PCB. The middle pin is connected to the PMIC; one outer pin is connected to the dongle; the other outer pin is connected to a switch. A jumper connects the middle pin to either of the two outer pins and thereby selects the source of the signal. The switch position selects pull-up or pull-down.

2.2 Handling Instructions

Take precautions to avoid electrostatic discharge (ESD) to the PMIC. These include keeping PMICs in protective packaging when possible, and connecting yourself and tools to earth/ground when handling PMICs.

Renesas recommends using a vacuum suction tool to lift and place the PMIC. If using tweezers, use only light force. There are slots in the socket for tweezer access. See the red boxes in Figure 3.

Important: Do not apply power to the board when the socket is open. Do not open the socket when power is applied to the board.

1. Unlatch and lift the lid of the socket slowly, without allowing its spring to flip the lid open.
2. Ensure correct orientation of the PMIC in the socket. The socket is marked with a circular recess. The PMIC is marked with an etched circle at pin 1. See the green box in Figure 3.
3. Before closing the socket lid, ensure the PMIC is square and level in the socket. Failure to do so can result in damage to the PMIC and/or socket.
4. Do not loosen the socket fixings or remove the socket from the PCB.

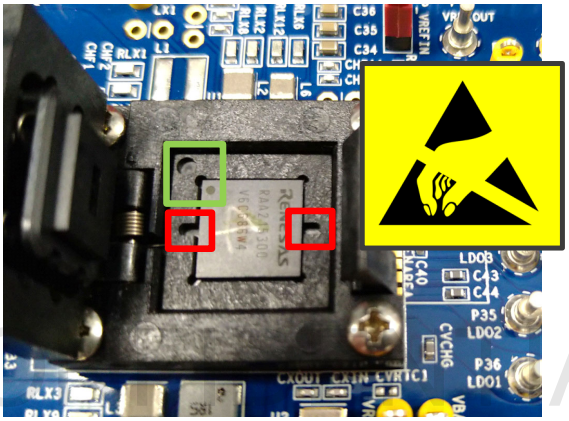

Figure 3. PMIC Orientation and Tweezer Access

2.3 Operating Characteristics

2.3.1 Operating Limits

The socket EVB can be operated across the full ranges of voltage described in the datasheet.

Important: The socket electrical and thermal capabilities cannot support full load current on the regulators. The resistance of socket connections can cause voltage drops that compromise signals. Large load currents and/or high power dissipation can damage the socket and/or the PMIC. The thermal limits of operation depend on ambient temperature and PMIC power dissipation, which depends on load currents, voltage settings, and regulator efficiencies.

- Only operate the socket EVB in normal room conditions
- Do not allow PMIC power dissipation to exceed 100mW
- Do not allow PMIC case temperature to exceed 100°C
- Do not exceed 100mA load on a single regulator
- Do not simultaneously load multiple regulators with 100mA. It is okay to apply multiple low current loads if power dissipation does not exceed 100mW.

2.3.2 Operation

As delivered, the capacitors, inductors, and PMIC settings of the socket EVB are consistent with a design that meet the requirements of an RZ/G2L microprocessor system with a 5V input. However, as stated in Operating Limits, the socket cannot support the currents to meet those requirements.

The output voltage settings for the RZ/G2L microprocessor system are shown in Table 1. All settings described in the Register Map Detail section of the datasheet can be changed using the I^2C interface, so many other power systems can be created and operated within the limits described in Operating Limits. The input voltage must be greater than each output voltage.

No damage is caused by experimenting with settings but it would require significant knowledge of the PMIC to optimize a power system.

Table 1. Socket EVB Default Output Voltage Settings

Regulator	Output voltage (V)
BUCK1	1.1
BUCK2	1.2
BUCK3	1.8
BUCK4	3.3
BUCK5	1.2
BUCK6	0.6
LDO1	3.3
LDO2	3.3
LDO3	2.5

2.4 Setup and Configuration

2.4.1 Signal List and Access

The signal list, switch identification, and jumper identification are shown in Table 2

Table 2. Signal Interface List

Signal Name	Switch Identifier	Jumper Identifier	Description
CEN	SW_CEN	JP_CEN	Chip enable.
PWRON	SW_PWRON	JP_PWRON	Regulator output enable.
VPULLUP	N/A	JP_VPULLUP	Select pull-up voltage for digital signals.
VPROG	SW_VPROG	N/A	⚠ See warning in Power Supplies. 21V to 23V power supply, only required when programming the EEPROM.
LDO_SEL1	SW_LDOSEL1	JP_LDOSEL1	Enables LDO1 output voltage to be changed during active state.
LDO_SEL2	SW_LDOSEL2	JP_LDOSEL2	Enables LDO2 output voltage to be changed during active state.
INT#		JP_INT#	Interrupt output, fault alarm.
MPIOx	SW_MPIOx	JP_MPIOx	x represents numbers 0 to 5. See the datasheet for functions.
BUCKx_FB		JP_RFBx	x represents numbers 1 to 6. The jumper can be used to open the feedback loop to enable gain measurement, or to enable remote sensing if the load is some distance from the EVB.
VRTC		JP_VRTC	Connects extra capacitance to RTC power supply.
VREFIN		JP_VREFIN	Connects buck2 output to VREFIN.
VCHG		JP_VCHG	Connects VCHG to VIN.
VBAT		JP_VBAT	Connects VBAT output to optional supercapacitor.
SDA_HV		JP_SDA	Connects I^2C serial data line to the dongle.
SCL_HV		JP_SCL	Connects I^2C serial clock line to the dongle.

2.4.2 Recommended Equipment

- Bench power supply: 0 to 5.5V; 0 to 2A
- Digital storage oscilloscope (DSO): 4 channels; 100MHz bandwidth
- Multiple loads: adjustable electronic loads and/or resistive loads
- Multiple voltmeters and ammeters
- Multiple cables with 4mm banana plugs for connection to the EVB
- Soldering iron

2.4.3 Initial State of Jumpers and Switches

1. See Figure 4. Set all the switch positions as shown by yellow arrows.
2. Set the jumpers as shown by red rectangles. Do not place any jumpers not shown.
3. Connect the interface board to the computer with the USB cable.

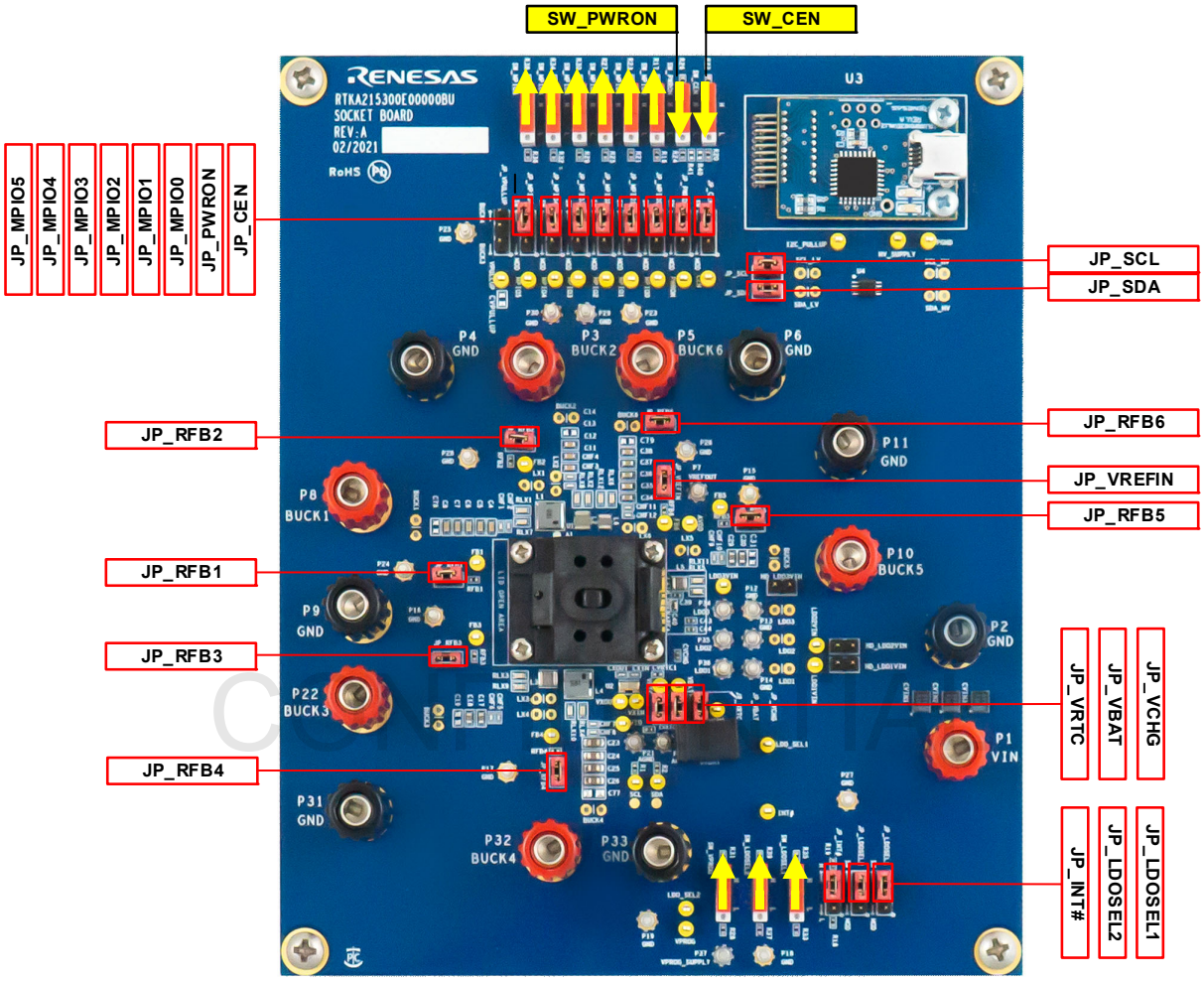

Figure 4. Default State of Switches and Jumpers

2.4.4 Evaluation Software and GUI

The EVB operates without running the RAA215300 evaluation software. For enhanced access and adjustability, the RAA215300 evaluation software and its user guide are available for download from the RAA215300 product page.

4. Save the software file and install the software by double clicking on the file name and following the on-screen instructions.
5. Attach the USB I^2C interface dongle to the computer using the supplied USB cable.
6. Run the RAA215300 evaluation software.

The GUI provides read and write access to the registers. The GUI is organized into sections for each regulator, fault management, MPIO, global configuration, and RTC. Each section provides values and simple descriptions of settings. Drop-down lists show the setting options and facilitate changes to those settings.

2.4.5 Operating Procedure

The following operating procedure does not require the RAA215300 evaluation software.

2.4.5.1 Power Supplies

WARNING! Do not hot-swap: Connecting or disconnecting a device to or from a powered-up circuit can cause damage to the device. All power supplies used for operating the device must be powered down and their outputs discharged before adding or removing a device to or from a circuit, including but not limited to: a test socket, a test harness, or a test jig.

Fast connection or fast disconnection of the power supply to VPROG_SUPPLY can damage the EVB.

The external, current limited power supply must be increased from 0V to between 21V and 23V in no less than 1ms.

The external, current limited power supply must be decreased from between 21V and 23V to 0V in no less than 1ms.

The VPROG switch on the EVB must not be closed while the external power supply is connected and at a voltage greater than 0V.

See Figure 5.

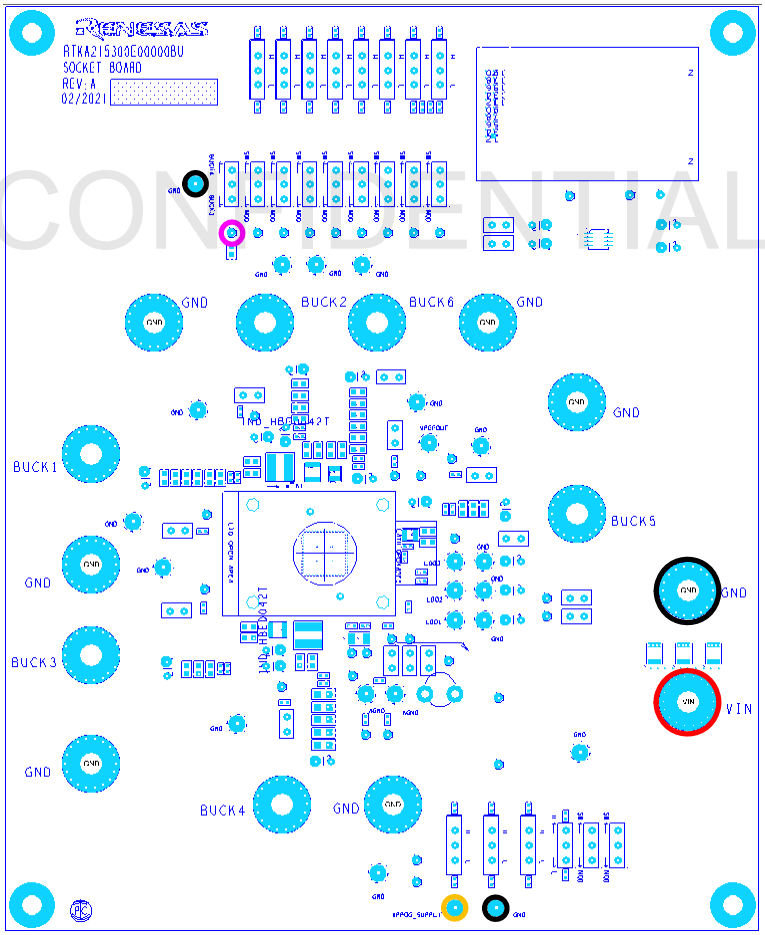

Figure 5. Power Supply Connections

1. Connect a power supply to VIN (red) and GND (black) banana sockets, with the voltage set to 5.0V (OFF).
2. Connect a power supply to VPULLUP_SUPPLY post (magenta), and GND post (black), with the voltage set to 1.8V (OFF).
3. Only if writing to EEPROM, apply a power supply to VPROG_SUPPLY post (circled in orange) and GND post (black), with the power supply off or set to 0V. Leave open if not used.
4. As a precaution, set current limits on the power supplies. For example:
   - VIN: 500mA
   - VPULLUP: 100mA
   - VPROG_SUPPLY: 100mA
5. Apply power supplies in any sequence.

2.4.5.2 Power Up Procedure

1. Switch CEN on (see green arrow in Figure 6).

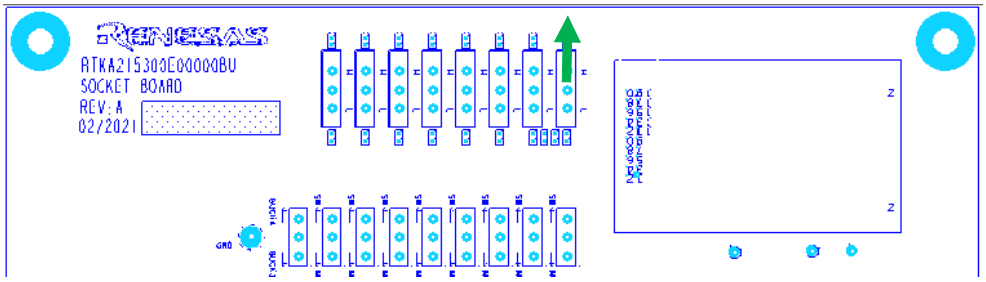

Figure 6. CEN Switch

2. Switch PWRON on (see the orange arrow in Figure 7) to enable the regulators. Regulator output voltages are established in the sequence set in the relevant registers.

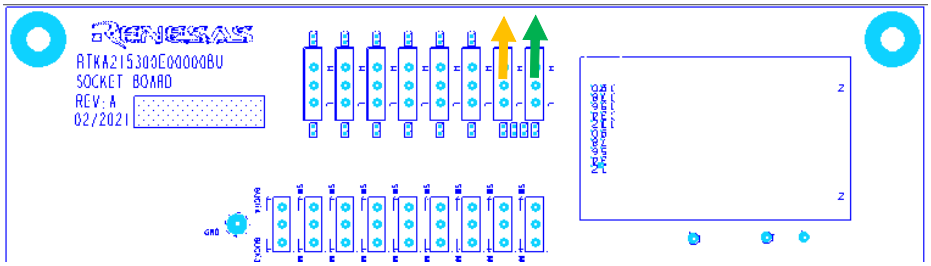

Figure 7. PWRON Switch

2.4.5.3 Loading the Regulators

1. Before applying load to the regulator outputs, check that the current limit on the input supply (VIN) is high enough to support the load.
2. Connect loads to the buck regulator outputs at the 4mm banana sockets shown in Figure 8. The ground of each output is the black socket adjacent to its respective red socket. The sockets include screw-down connections that can be used for connecting electronic load remote sensing.

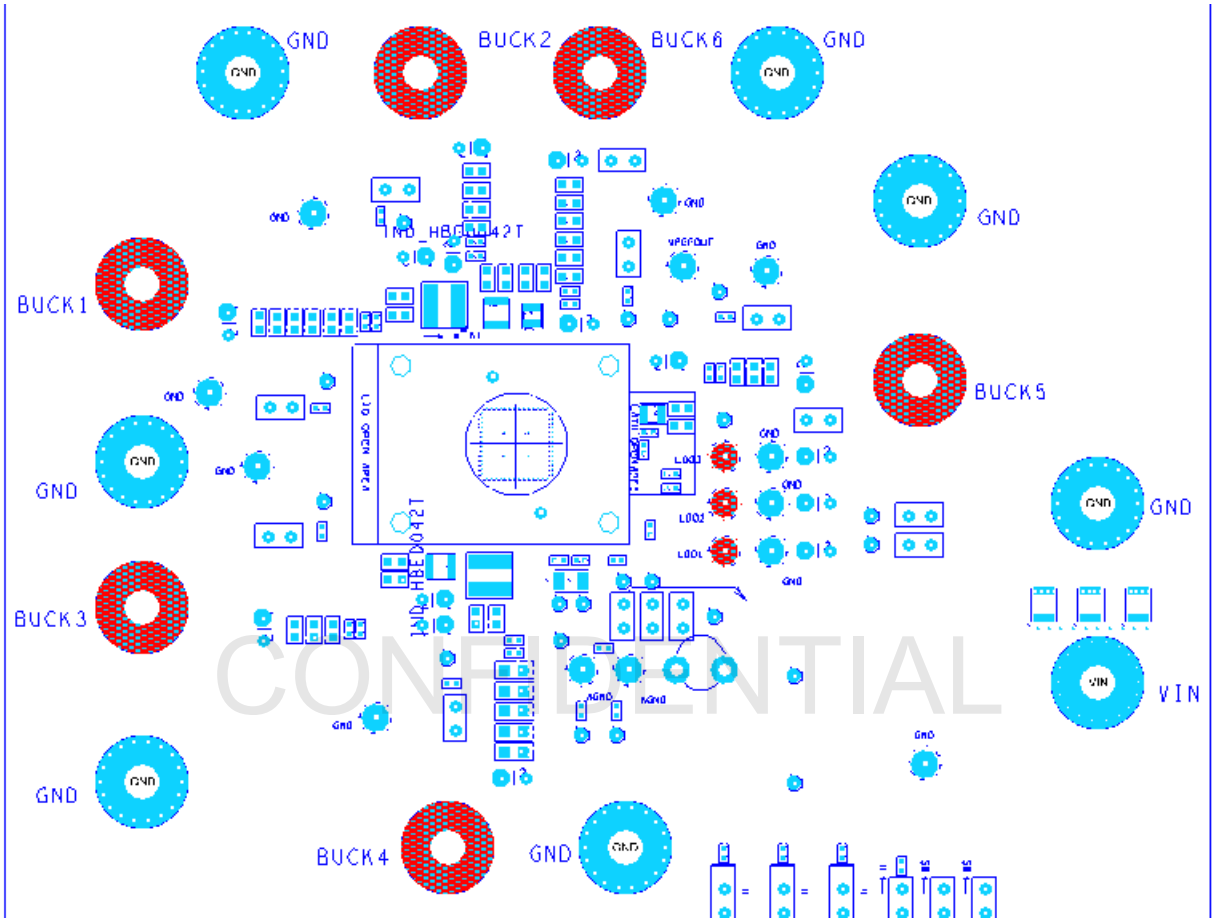

Figure 8. Regulator Load Connection Points

3. Connect loads to the LDO regulator outputs at the pins shown in Figure 9.

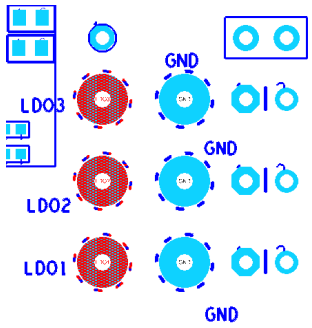

Figure 9. LDO Regulator Load Connection Points

2.4.5.4 Monitoring Regulator Output Voltages

4. Figure 10 shows locations on the PCB where the buck regulator output voltages can be measured accurately. For each buck regulator, there is a pair of pads with holes to which wires, pins, or connectors can be soldered, or an oscilloscope probe can be connected. The larger of each pair of pads is the positive; the smaller pad is ground.

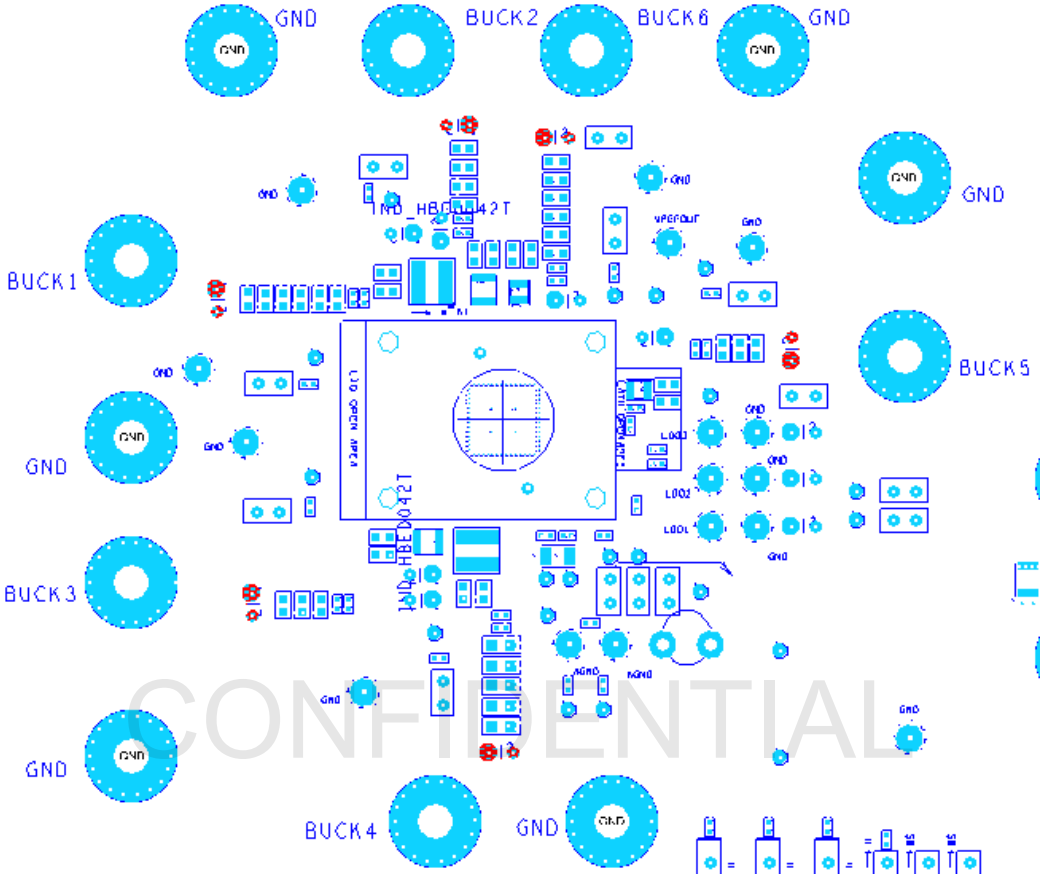

Figure 10. Locations for Measurement of Buck Regulator Output Voltages

5. Figure 11 shows locations on the PCB where the LDO regulator output voltages can be measured accurately. For each LDO regulator, there is a pair of pads with holes to which wires, pins, or connectors can be soldered, or an oscilloscope probe can be connected. The larger of each pair of pads is the positive; the smaller pad is ground.

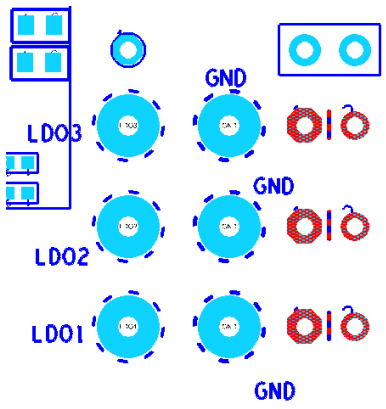

Figure 11. Locations for Measurement of LDO Regulator Output Voltages

3. Board Design

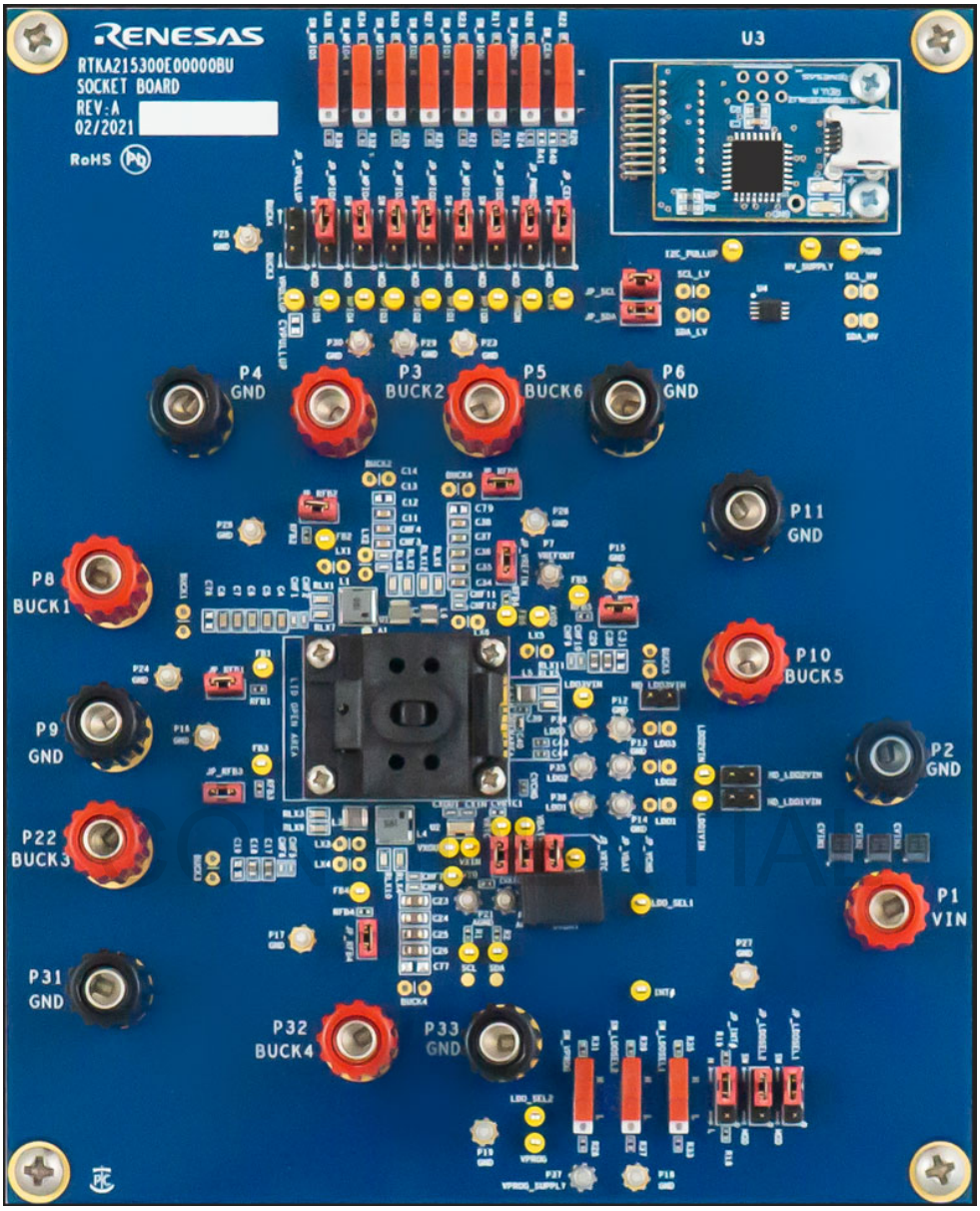

Figure 12. RTKA215300E00000BU Evaluation Board (Top)

3.1 Schematic Diagrams

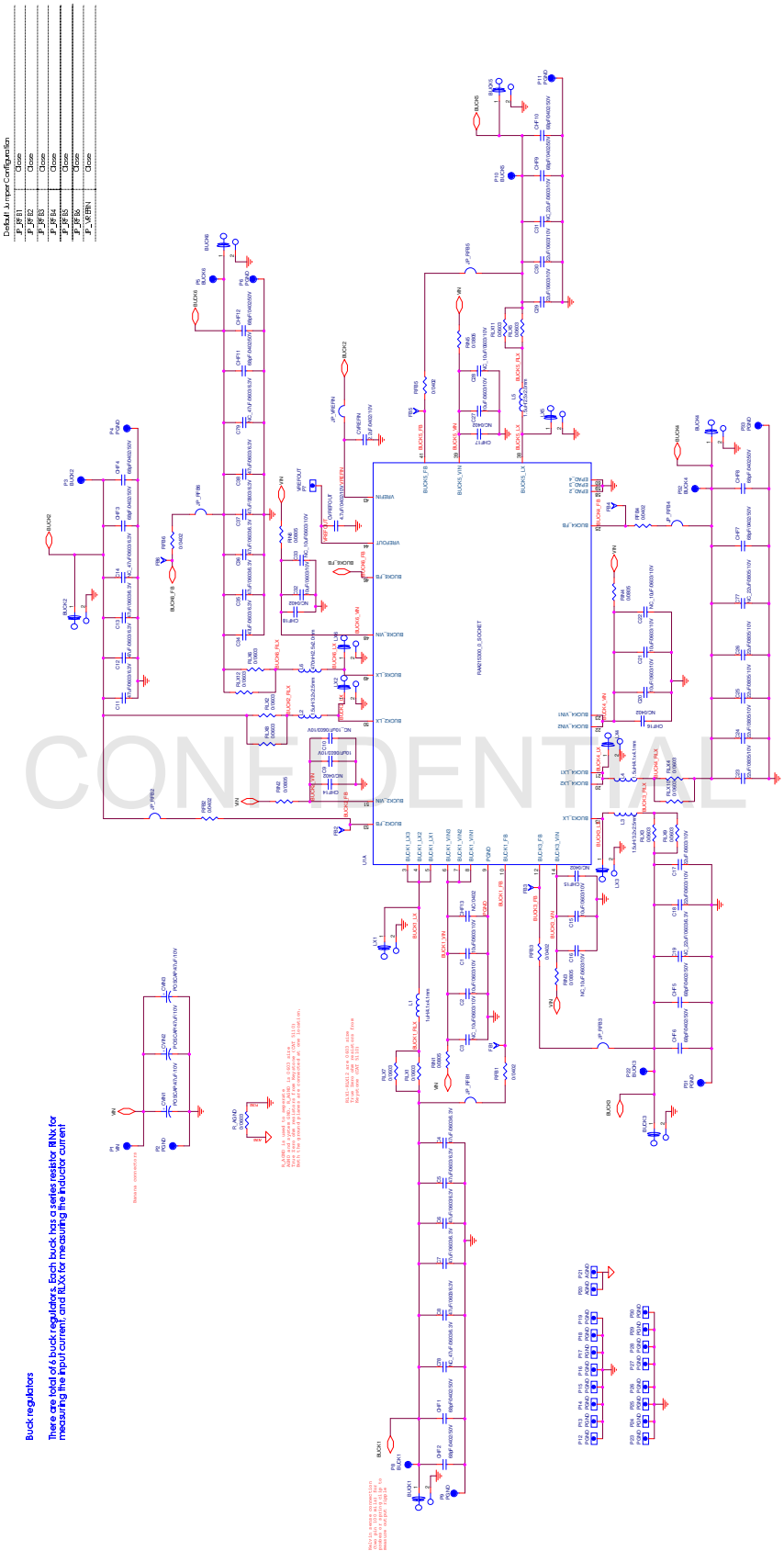

Figure 13. RTKA215300E00000BU EVB Schematic Sheet 1

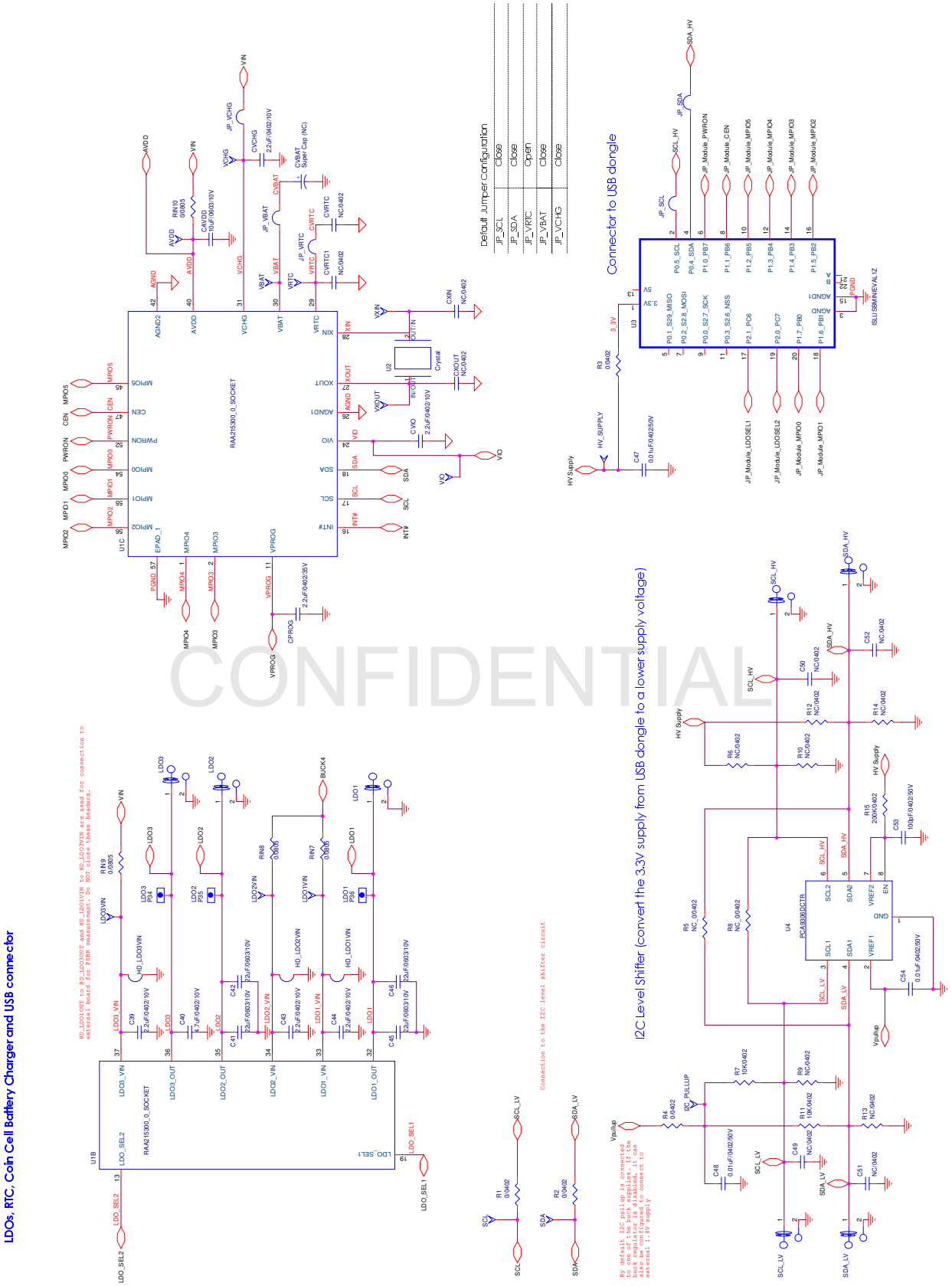

Figure 14. RTKA215300E00000BU EVB Schematic Sheet 2

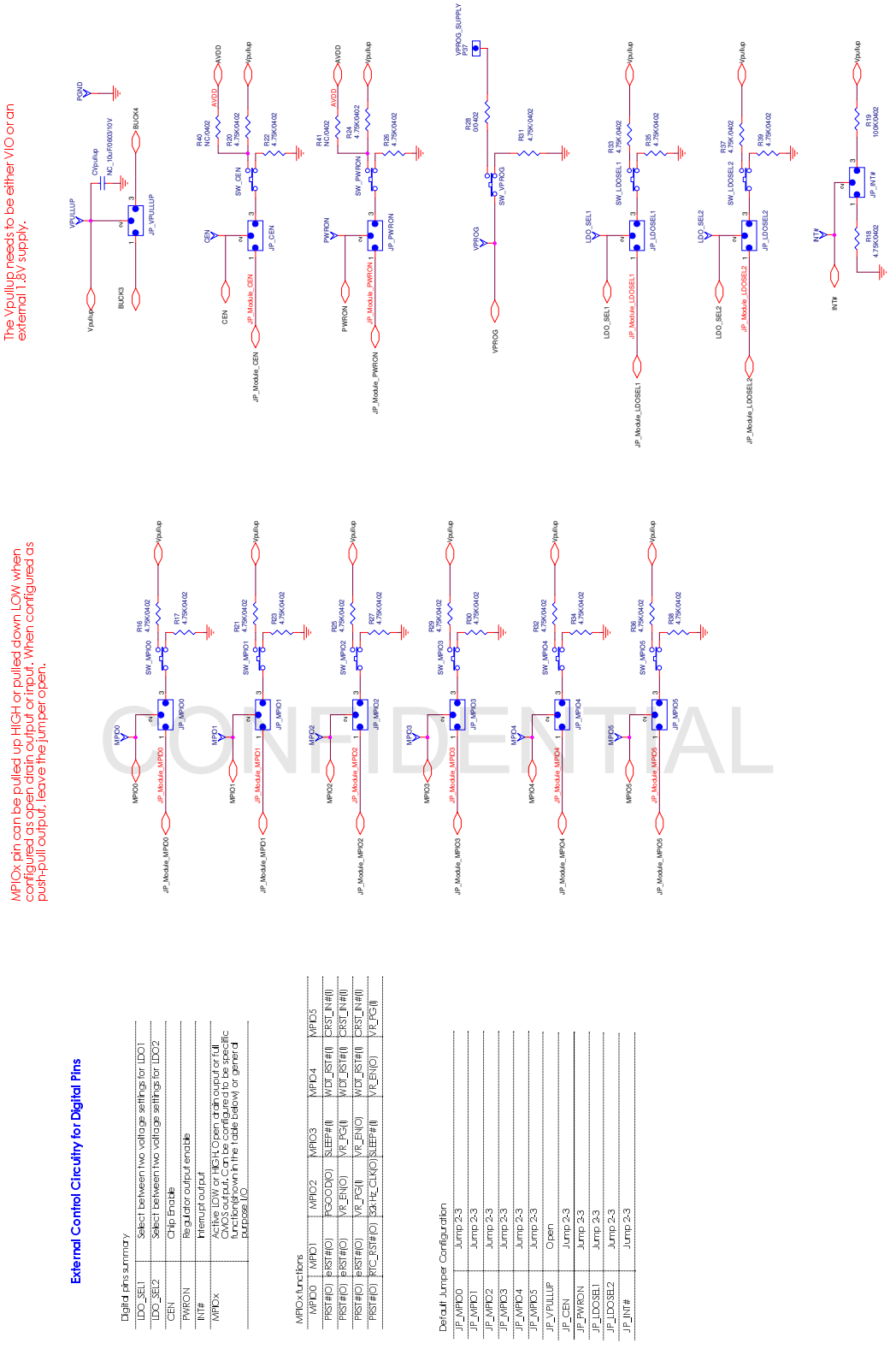

Figure 15. RTKA215300E00000BU EVB Schematic Sheet 3

3.2 Bill of Materials

The EVB BOM is available in the design files on the RTKA215300E00000BU page.

3.3 Board Layout

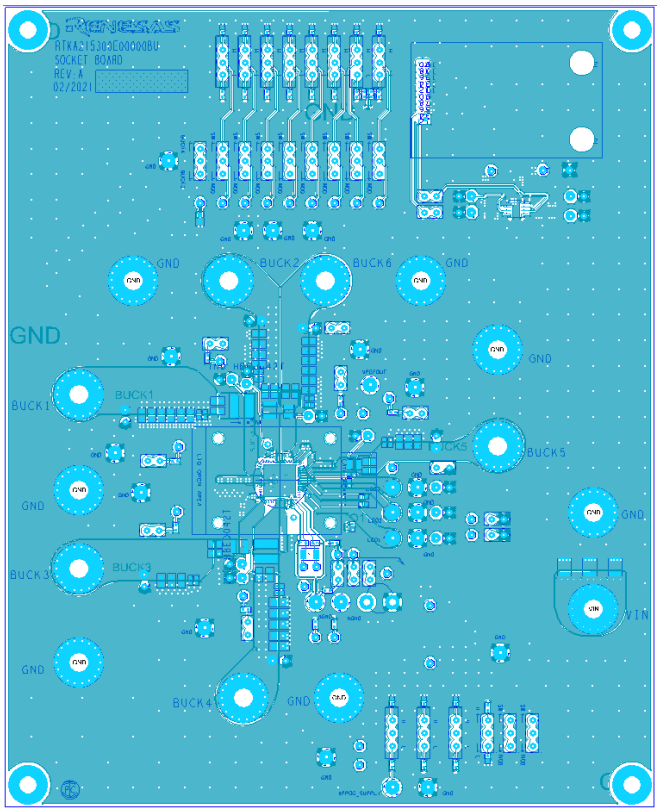

Figure 16. Top Layer Copper

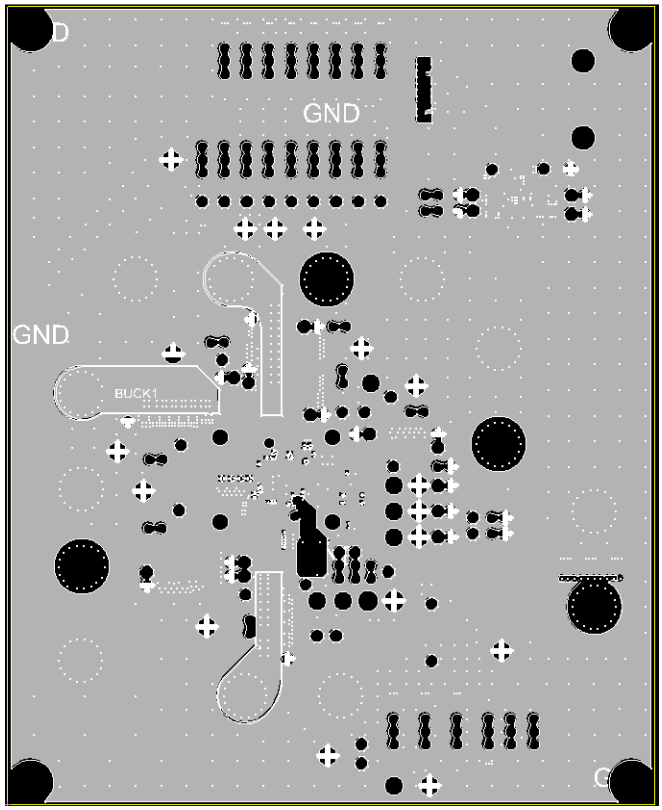

Figure 17. Layer 2 Copper

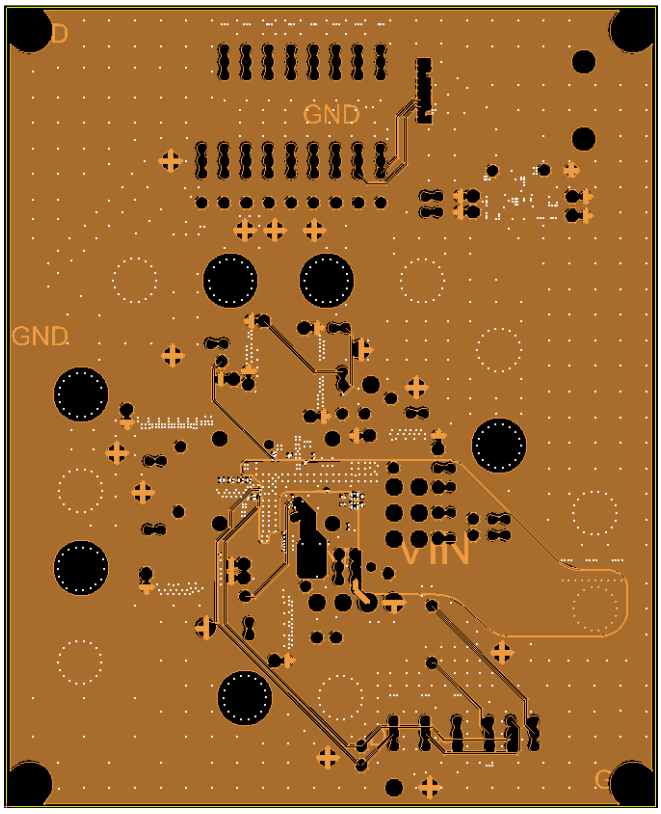

Figure 18. Layer 3 Copper

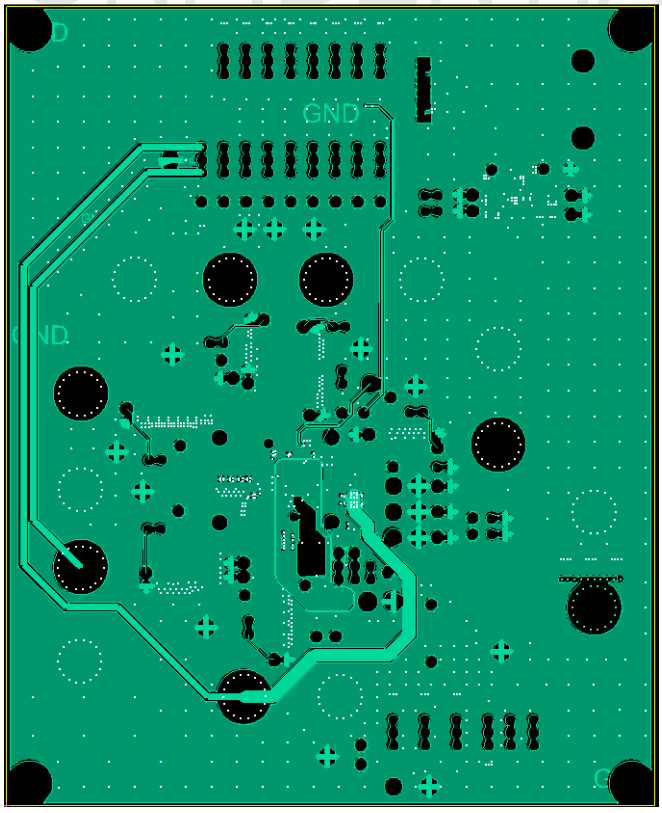

Figure 19. Layer 4 Copper

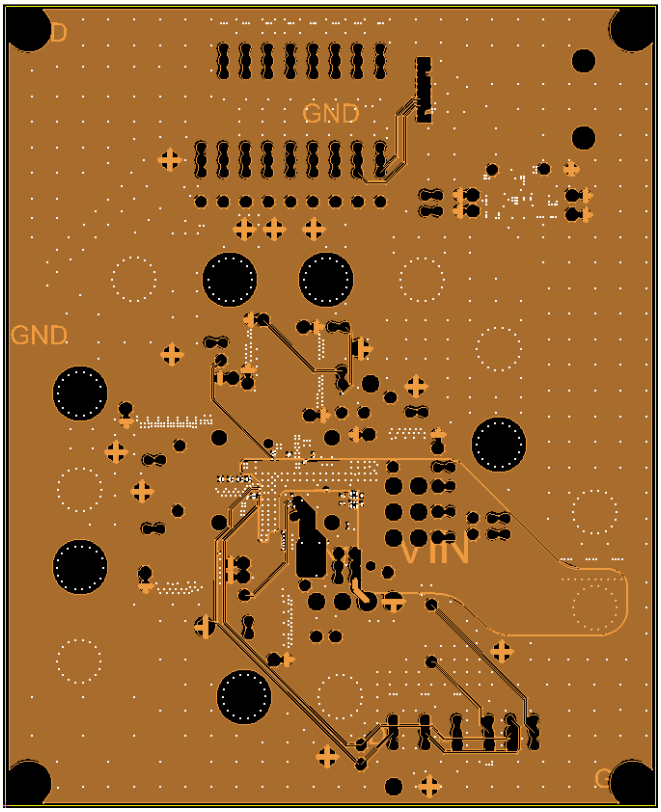

Figure 20. Layer 5 Copper

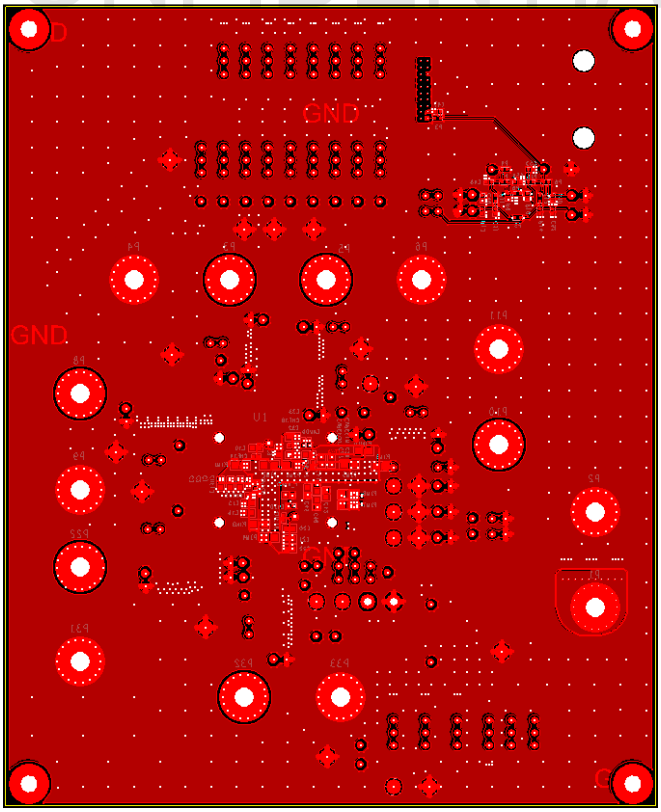

Figure 21. Bottom Layer Copper

4. Ordering Information

Part Number	Description
RTKA215300E00000BU	Socket Evaluation board for RAA215300A2GNP#HA0

5. Revision History

Revision	Date	Description
1.02	Dec 19, 2022	Updated Table 2. Updated Power Supplies section. Updated Schematics.
1.01	Aug 10, 2022	Updated Schematics.
1.00	Jun 30, 2022	Initial release

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